

PMIC Solution for RZ/V2H

Power Tree

This document describes the power system required for RZ/V2H, including register settings of RAA215300 and DA9141.

The RAA215300 is a high-performance, low-cost, 9-channel PMIC designed for 32-bit and 64-bit MCU and MPU applications. It supports DDR3, DDR3L, DDR4, and LPDDR4 memory power interfaces. The internally compensated regulators, built-in Real-Time Clock (RTC), 32kHz crystal oscillator, and coin cell battery charger provide a highly integrated, small footprint power solution ideal for System-On-Module (SOM) applications.

The DA9141 is a high-efficiency, high current, quad-phase, step-down DC/DC (buck) converter with integrated switching FETs and can drive loads up to 40A.

Target Device

- RZ/V2H

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1. Terms and Definitions

- CH<x> – Channel <x>, where x = 1 to 4
- LDO – Low Dropout linear regulator
- OTP – One-Time Programmable
- QFN – Quad Flat-pack No-lead (package)

2. References

- [RAA215300](#) Datasheet
- [RZ/V2H-EVK](#) - RZ/V2H Quad-core Vision AI MPU Evaluation Kit
- [DA9141](#) Datasheet
- [ISL6185](#) Datasheet
- [SLG59M1603V](#) Datasheet
- [SLG59M1717V](#) Datasheet

3. Power Tree

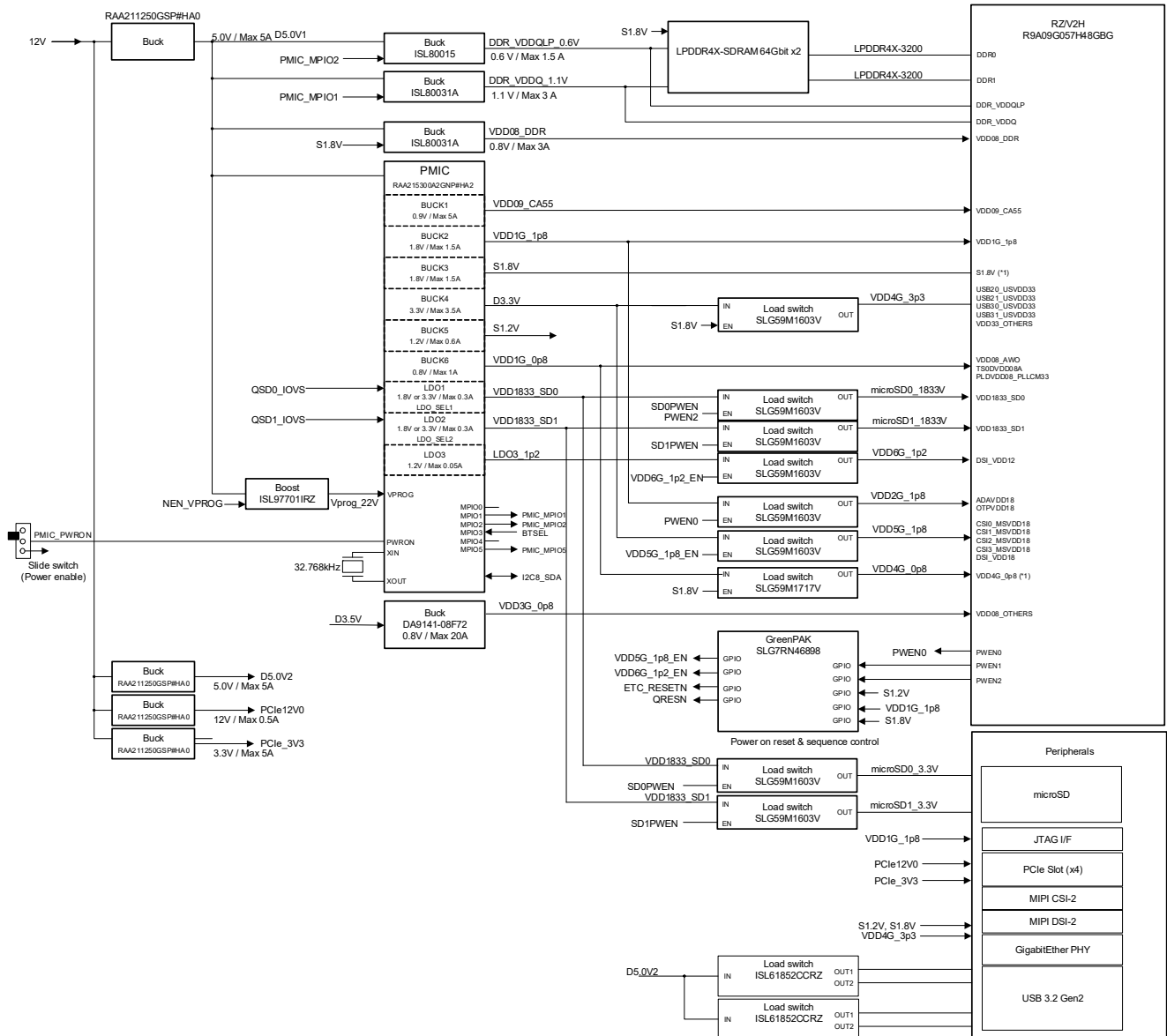


Figure 1. RZ/V2H Power Tree

3.1 Renesas Components in Power Tree

Table 1. Renesas Components in Power Tree

Part Number	Description
RAA215300A2GNP#HA2	PMIC
DA9141-08F72	High-Performance, 25A/40A Peak, DC/DC Converter
ISL61852CCRZ	Dual USB Port Power Supply Controller
ISL80031A	3A Synchronous Buck Converter in 2x2 DFN Package
ISL80015	Compact Synchronous Buck Converter
ISL97701IRZ-T7	Boost Regulator with Integrated Schottky and Input Disconnect Switch
RAA211250GSP#HA0	Integrated FET 30V, 5A Synchronous Buck Regulator with Internal Compensation and Programmable Frequency
SLG7RN46898	GreenPAK - Power-On reset & sequence control
SLG59M1603V	GreenFET Dual N-Channel Load Switch
SLG59M1717V	GreenFET Single N-Channel Load Switch

4. Power Requirements

4.1 Power-On Sequence – CA55 Boot Mode

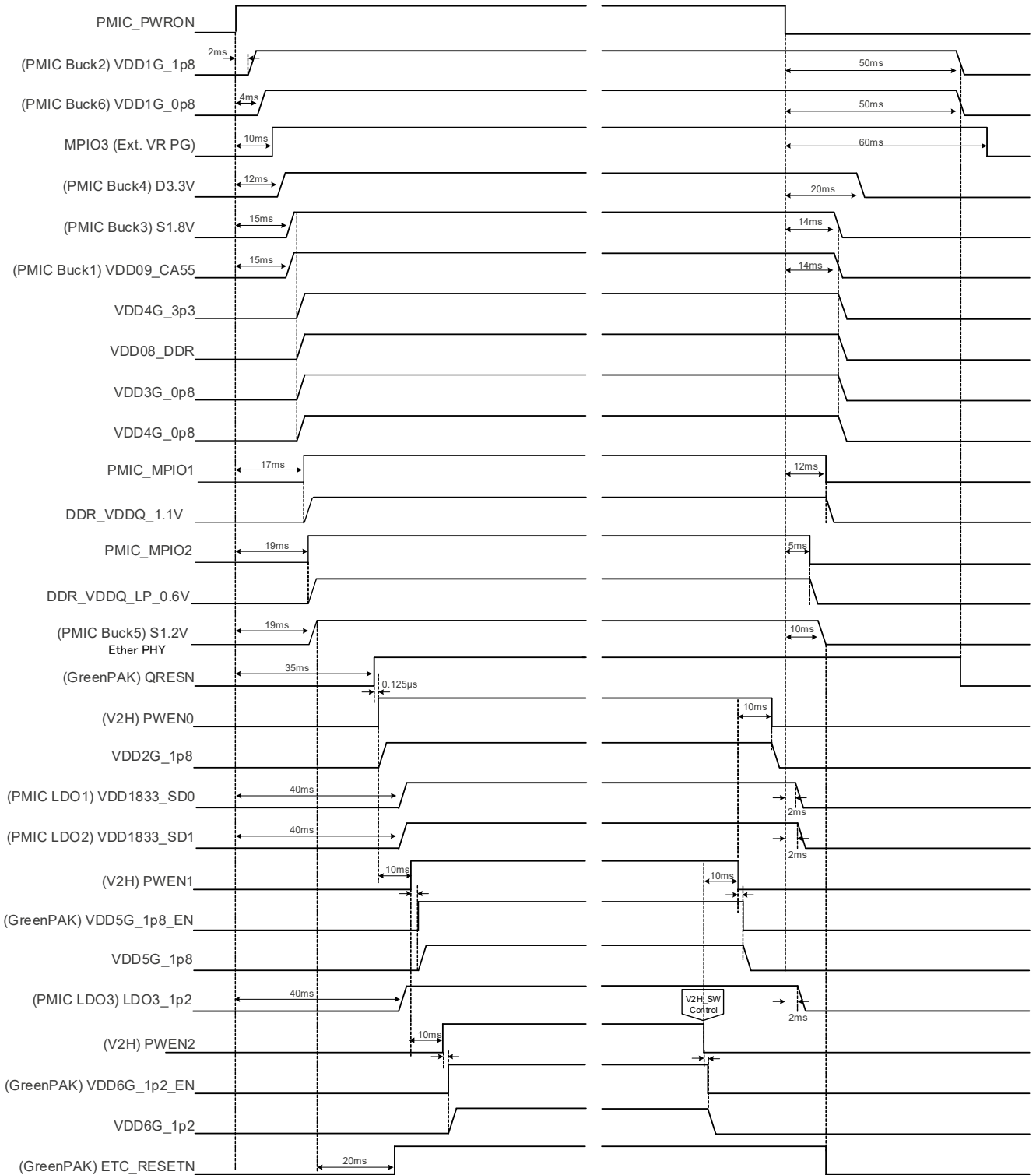


Figure 2. Power-On/Off Sequence CA55

5. Variant Table and Ordering Information

Table 2. Variant Table

Part Number	Package	Size	Shipment Form	Pack Quantity
RAA215300AGNP#HA2	QFN56	5mm×5mm Exposed Paddle	Reel	1000
DA9141-08F72	60 FCBGA	4.5mm×7mm 0.65 mm pitch	Reel	-
ISL61852CCRZ	8 Lead DFN	3mm×3mm	Tray	-
ISL80031FRZ-T	8 Ld DFN	2mm×2mm	Reel	1000
ISL80015FRZ-T	8 Ld TDFN	2mm×2mm	Reel	1000
ISL80015IRZ-T	8 Ld TDFN	2mm×2mm	Reel	250
ISL97701IRZ-T7	10 Ld 3x3 DFN	3mm×3mm	Reel	1000
RAA211250GSP#HA0	16 Ld HTSSOP	5mm×4.4mm	Reel	2500
SLG59M1603V	STDFN 14L	1mm×3mm	Reel	3000
SLG59M1717V	STQFN 16L	1.6mm×2.5mm	Reel	3000
SLG7RN46898	-	-	-	-

6. Register Settings

Table 3. Register Setting RAA215300AGNP#HA2

Register Address	Register Name	Default Value	Description
0x1E	Main Slave Address	0x00	Main Slave address = 0x12
0x1F	RTC Slave Address	0x00	RTC Slave Address
0x20	Buck1 Enable	0x05	Buck1 Enabled in Active state and Disabled in Sleep state. ABS enabled. Phase Sync and Spread Spectrum disabled
0x21	Buck1 ACTIVE	0x02	Buck1 Output in Active state = 0.9V (Auto)
0x22	Buck1 SLEEP	0x02	Buck1 Output in Sleep state = 0.9V (Disabled)
0x23	Buck1 Power On	0x0F	Buck1 Power-on Delay = 15ms
0x24	Buck1 Power Off	0x0E	Buck1 Power-off Delay = 14ms
0x25	Buck1 SR	0x5A	Buck1 Startup and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x26	Buck1 Config	0x0B	Buck1 Switching frequency = 0.833MHz Output discharge = Fast
0x27	Buck2 Enable	0x07	Buck2 Enabled in Active and Sleep states. ABS enabled. Phase Sync and Spread Spectrum disabled
0x28	Buck2 ACTIVE	0x0E	Buck2 Output in Active state = 1.8V (Auto)
0x29	Buck2 SLEEP	0x0E	Buck2 Output in Sleep state = 1.8V (Auto)
0x2A	Buck2 Power On	0x02	Buck2 Power-on Delay = 2ms
0x2B	Buck2 Power Off	0x32	Buck2 Power-off Delay = 50ms
0x2C	Buck2 SR	0x5A	Buck2 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs

Table 3. Register Setting RAA215300AGNP#HA2 (Cont.)

Register Address	Register Name	Default Value	Description
0x2D	Buck2 Config	0x07	Buck2 Switching Frequency = 0.769MHz Output discharge = Fast
0x2E	Buck3 Enable	0x05	Buck3 Enabled in Active state and Disabled in Sleep state. ABS enabled. Phase Sync and Spread Spectrum disabled
0x2F	Buck3 ACTIVE	0x00	Buck3 Output in Active state = 1.8V (Auto)
0x30	Buck3 SLEEP	0x00	Buck3 Output in Sleep state = 1.8V (Disabled)
0x31	Buck3 Power On	0x0F	Buck3 Power-on Delay = 15ms
0x32	Buck3 Power Off	0x0E	Buck3 Power-off Delay = 14ms
0x33	Buck3 SR	0x5A	Buck3 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x34	Buck3 Config	0x1B	Buck3 Switching Frequency = 1.54MHz Output discharge = Fast
0x35	Buck4 Enable	0x07	Buck4 Enabled in Active and Sleep states. ABS enabled. Phase Sync and Spread Spectrum disabled
0x36	Buck4 ACTIVE	0x0F	Buck4 Output in Active state 3.3V
0x37	Buck4 SLEEP	0x0F	Buck4 Output in Sleep state = 3.3V
0x38	Buck4 Power On	0x0C	Buck4 Power-on Delay = 12ms
0x39	Buck4 Power Off	0x14	Buck4 Power-off Delay = 20ms
0x3A	Buck4 SR	0x5A	Buck4 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x3B	Buck4 Config	0x1B	Buck4 Switching Frequency = 1.54MHz Output discharge = Fast
0x3C	Buck5 Enable	0x07	Buck5 Enabled in Active and Sleep states. ABS enabled. Phase Sync and Spread Spectrum disabled
0x3D	Buck5 ACTIVE	0x00	Buck5 Output in Active state = 1.2V
0x3E	Buck5 SLEEP	0x00	Buck5 Output in Sleep state = 1.2V
0x3F	Buck5 Power On	0x13	Buck5 Power-on Delay = 19ms
0x40	Buck5 Power Off	0x0A	Buck5 Power-off Delay = 10ms
0x41	Buck5 SR	0x5A	Buck5 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x42	Buck5 Config	0x1B	Buck5 Switching Frequency = 1.54MHz Output discharge = Fast
0x43	Buck6 Enable	0x07	Buck6 Enabled in Active and Sleep states. ABS enabled. Phase Sync and Spread Spectrum disabled
0x44	Buck6 ACTIVE	0x50	Buck6 Output set to 1.1V in Active state, but VTTREF is enabled so output = VREFIN/2 FPWM Independent soft-start, not linked to buck2

Table 3. Register Setting RAA215300AGNP#HA2 (Cont.)

Register Address	Register Name	Default Value	Description
0x45	Buck6 SLEEP	0xD0	Buck6 Output set to 1.1V in Sleep state, but VTTREF is enabled so output = VREFIN/2 FPWM Independent soft-start, not linked to buck2
0x46	Buck6 Power On	0x04	Buck6 Power-on Delay = 4ms
0x47	Buck6 Power Off	0x32	Buck6 Power-off Delay = 50ms
0x48	Buck6 SR	0x5A	Buck6 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x49	Buck6 Config	0x03	Buck6 Switching Frequency = 0.667MHz Output discharge = Fast
0x4A	LDO1 ACTIVE	0x67	LDO1 Enabled in Active state Active 0 setting = 3.3V Active 1 setting = 1.8V Bypass operation disabled
0x4B	LDO1 SLEEP	0x04	LDO1 disabled in Sleep state
0x4C	LDO1 Power On	0x28	LDO1 Power-on Delay 40ms
0x4D	LDO1 Power Off	0x02	LDO1 Power-off Delay = 2ms
0x4E	LDO1 SR	0x5A	LDO1 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x4F	LDO2 ACTIVE	0x67	LDO2 Enabled in Active state Active 0 setting = 3.3V Active 1 setting = 1.8V Bypass operation disabled
0x50	LDO2 SLEEP	0x04	LDO2 disabled in Sleep state.
0x51	LDO2 Power On	0x28	LDO2 Power-on Delay = 40ms
0x52	LDO2 Power Off	0x02	LDO2 Power-off Delay = 2ms
0x53	LDO2 SR	0x5A	LDO2 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x54	LDO3 ACTIVE SLEEP	0xD2	LDO3 Enabled in Active and Sleep states Active setting = 1.2V Sleep setting = 1.2V
0x55	LDO3 Power On	0x28	LDO3 Power-on Delay = 40ms
0x56	LDO3 Power Off	0x02	LDO3 Power-off Delay = 2ms
0x57	LDO3 SR	0x5A	DVS ramp-up and ramp-down slew rate = 8mV/μs
0x58	LDOs Config	0x3F	LDO1, LDO2, LDO3 discharge = Fast
0x64	nINT Mask 1	0x00	Undervoltage fault on each buck regulator is not masked from INT#.
0x65	nINT Mask 2	0x00	VIO PGOOD fault is not masked from INT#. Undervoltage fault on each LDO is not masked from INT#.
0x66	nINT Mask 3	0x00	Overvoltage fault on each buck regulator is not masked from INT#.

Table 3. Register Setting RAA215300AGNP#HA2 (Cont.)

Register Address	Register Name	Default Value	Description
0x67	nINT Mask 4	0x00	Buck1 high current fault is not masked from INT#.
0x68	nINT Mask 6	0x00	The following faults are not masked from INT#. <ul style="list-style-type: none"> PGOODCCBAT. VREFIN UVLO. AVDD UVPD. NVM. CRST Triggered. WDT Error. Over-temperature warning.
0x69	Fault Config 1	0x3F	Shut down all regulators if any buck regulator is undervoltage.
0x6A	Fault Config 2	0x07	Shut down all regulators if any LDO is undervoltage.
0x6B	Fault Config 3	0x7F	Shut down all regulators if VREFIN is undervoltage. Shut down all regulators if any buck regulator is overvoltage.
0x6C	Block EN	0x00	VBAT comparator enabled. Watchdog timer enabled. Power down when watchdog timer expires. Reset when watchdog timer expires. Power down when CRST_IN# is asserted.
0x6F	Config 1	0xFA	Battery charge current = 60μA. Temperature warning = 120°C. Buck1 high current warning = 6A. AVDD UVPD threshold = 2.7V. PWRON = on/off switch.
0x70	Config 2	0xF8	VCCBAT = 3.3V.
0x71	Config 3	0x17	VIO Timeout = 1ms. Cold reset delay = 255ms.
0x74	MPIO1 Power On	0x11	MPIO1 Power-on delay = 17ms
0x75	MPIO1 Power Off	0x0C	MPIO1 Power-off delay = 12ms
0x76	MPIO2 Power On	0x13	MPIO2 Power-on delay = 19ms
0x77	MPIO2 Power Off	0x05	MPIO2 Power-off delay = 5ms
0x78	MPIO3 Power On	0x0A	MPIO3 Power-on delay = 10ms
0x79	MPIO3 Power Off	0x3C	MPIO3 Power-off delay = 60ms
0x80	MPIO Assertion	0x38	External VR enable signals will be de-asserted in Sleep state.
0x89	Shutdown Config	0x02	Shut down all regulators, applying discharge resistors and respective shutdown time settings.
0x8A	MPIO0 Config	0x00	Disabled.
0x8B	MPIO1 Config	0x2E	External VR EN output, Open drain NMOS, Active High.
0x8C	MPIO2 Config	0x2E	External VR EN output, Open drain NMOS, Active High.
0x8D	MPIO3 Config	0x22	External VR PGOOD input, high impedance, Active High.
0x8E	MPIO4 Config	0x00	Disabled.

Table 3. Register Setting RAA215300AGNP#HA2 (Cont.)

Register Address	Register Name	Default Value	Description
0x8F	MPIO5 Config	0x00	Disabled.
0x90	PWRON Polarity Config	0x01	Active high.

Table 4. Register Settings DA9141-08F72

Register Address	Register Name	Default Value	Description
0x07	SYS_MASK_0	0x07	nIRQ interrupt, all masked
0x08	SYS_MASK_1	0x0F	nIRQ interrupt, all masked
0x09	SYS_MASK_2	0x07	nIRQ interrupt, all masked
0x0A	SYS_MASK_3	0x0D	nIRQ interrupt, all masked
0x0B	SYS_CONFIG_0	0x00	Delay for CH1 disabled.
0x0D	SYS_CONFIG_2	0x18	Overcurrent latch-off function disabled. OC event is masked during DVC. PG is masked during DVC.
0x0E	SYS_CONFIG_3	0x00	Oscillator tuning (OSC_TUNE) is off. I2C_TIMEOUT is disabled.
0x10	SYS_GPIO0_0	0x02	GPIO0 set to EN1 input.
0x11	SYS_GPIO0_1	0x00	GPIO0 Pull-down disabled, Active High, Dual-edge triggered.
0x12	SYS_GPIO1_0	0x08	GPIO1 set to DVC1 input.
0x13	SYS_GPIO1_1	0x08	GPIO1 Pull-down enabled, Active High, Dual-edge triggered.
0x14	SYS_GPIO2_0	0x10	GPIO2 set to PG1 output, Open Drain.
0x15	SYS_GPIO2_1	0x08	GPIO2 Pull-up to AVDD enabled, Dual-edge triggered
0x16	SYS_GPIO3_0	0x00	GPIO3 disabled.
0x17	SYS_GPIO3_1	0x00	Not applicable
0x18	SYS_GPIO4_0	0x00	GPIO4 disabled.
0x19	SYS_GPIO4_1	0x00	Not applicable
0x20	BUCK_BUCK1_0	0x36	DVC ramp-down slew rate = 10mV/μs DVC ramp-up slew rate = 10mV/μs
0x21	BUCK_BUCK1_1	0x36	Shutdown slew rate = 10mV/μs Start-up slew rate = 10mV/μs
0x22	BUCK_BUCK1_2	0x09	CH1 current limit = 14.5A
0x23	BUCK_BUCK1_3	0x82	CH1 Vmax = 1.3V
0x24	BUCK_BUCK1_4	0x0A	CH1 output A selected. CH1 B mode set to FPWM with phase shedding. CH1 A mode set to FPWM with phase shedding.
0x25	BUCK_BUCK1_5	0x50	CH1 output voltage A = 0.8V
0x26	BUCK_BUCK1_6	0x55	CH1 output voltage B = 0.85V
0x48	OTP_DEVICE_ID	0x00	Device ID
0x49	OTP_VARIANT_ID	0x01	Mark revision Code = 0, Chip Variant Code = 1

Table 4. Register Settings DA9141-08F72 (Cont.)

Register Address	Register Name	Default Value	Description
0x4A	OTP_CUSTOMER_ID	0x02	Customer ID
0x4B	OTP_CONFIG_ID	0x08	OTP Variant 08

7. Revision History

Revision	Date	Description
1.01	Feb 10, 2025	Removed ISL28022 part information throughout. Updated Figure 1. Updated Tables 1, 2, and 4.
1.00	Jul 2, 2024	Initial release.

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