RAA225019 I²C Sequence and Timing Guidelines

1. Introduction

The following are recommended guidelines that customers must follow to ensure the RAA225019 operates robustly and without issues:

2. I²C Ready Sequence

The I²C interface goes through a preparation stage after VIN rises above the Power-On Reset (POR) rising threshold. On the LNL-MX platform, multiple units support various rails, and each unit requires a different configuration before it can support full operation. For these rails, it is crucial to ensure that I²C write operations are accessible and that all write commands are acknowledged before the VR_EN signal is asserted. I²C communication becomes available after the I2C_ready time (V_{IN}POR to I²C Timing) as in the datasheet EC table. Figure 2 shows the timing diagram. When PIN and AVIN are above the POR rising threshold, the internal bandgap and LDO are activated. The startup state machine runs, and the settings on each of the three PROG pins are read sequentially. The RAA225019 cannot guarantee package recognition until the I²C addresses are configured by the PROGx pins. To ensure that the proper configuration is loaded into each rail, the I²C ready enable timing must be adhered to for all rails. After the I²C enable timing is completed (V_{IN}POR to I²C Timing), the I²C bus is ready for communication.

V_{IN} POR to I²C Timing[4]	-	PIN > POR rising to I2C Communication start	-	-	3.785	ms
		PIN > POR rising to SDA release	-	-	700	µs
V_{IN} POR to EN Ready[4]	-	PIN > POR rising to VR_EN1/VR_EN2/EN3/EN_LDO going high	-	-	3.865	ms

Figure 1. Datasheet Electrical Specification Table Snapshot

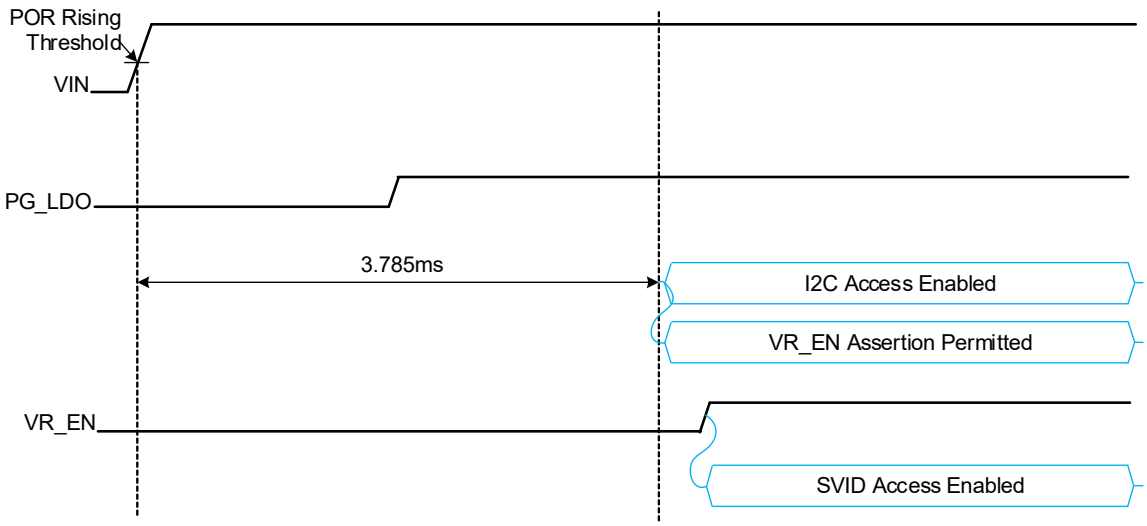

Figure 2. Startup Timing Diagram

The I2C_Data line (SDA) is pulled low before the RAA225019 VIN POR. Typically, the Embedded Controller (EC) begins sending configuration commands only after all PRIM rails to the SoC have been supplied. Since the RAA225019 is a system Power Management Integrated Circuit (PMIC), it supplies some of these PRIM rails. As a result, a few of the ROP rails are enabled with default One-Time Programmable (OTP) settings. If the customer follows this architecture, I2C communication for the register configuration commences only after the RAA225019 POR sequence is completed and some rails have been enabled. To confirm this, either gate EC programming until the Power-Good signal of VnnAON is asserted or verify the sequence in the actual system.

Other system implementation recommendations include:

- Characterize PMIC_VIN discharge at pre-regulator disable, and/or implement a discharging circuit.
- Use a separate I2C bus line for the PMIC compared to other devices (such as charger, pre-regulator).
- Configure the charger before enabling the pre-regulator or after the PMIC_VIN POR is reached if the I2C bus of the charger is shared with the PMIC.
- Align EC configuration for the PMIC's V_{IN}POR to I2C Timing after the PMIC reaches Vin_POR.

3. Revision History

Revision	Date	Description
1.00	Nov 7, 2024	Initial release.

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