

# PMIC Solution for RZ/V2H SOM

## Power Tree

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### Introduction

This document describes the power systems required for RZ/V2H SOM core and includes register settings for RAA215300 and DA9215.

The RAA215300 is a high-performance, low-cost, 9-channel PMIC designed for 32-bit and 64-bit MCU and MPU applications. It supports DDR3, DDR3L, DDR4, and LPDDR4 memory power interfaces. The internally compensated regulators, built-in Real-Time Clock (RTC), 32kHz crystal oscillator, and coin cell battery charger provide a highly integrated, small footprint power solution ideal for System-On-Module (SOM) applications.

The DA9215 is a PMU optimized for the supply of CPUs, GPUs, and DDR memory rails. It integrates a 3-phase buck converter capable of delivering 15A and a single-phase buck converter delivering 5A.

### Target Device

- RZ/V2H

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## 1. Terms and Definitions

- CH<x> – Channel <x>, where x = 1 to 4
- LDO – Low Dropout linear regulator
- OTP – One-Time Programmable
- QFN – Quad Flat-pack No-lead (package)

## 2. References

- [RAA215300](#) Datasheet
- [RZ/V2H-EVK](#) - RZ/V2H Quad-core Vision AI MPU Evaluation Kit
- [DA9215](#) Datasheet
- [SLG59M1603V](#) Datasheet
- [SLG59M1717V](#) Datasheet

### 3. Power Tree

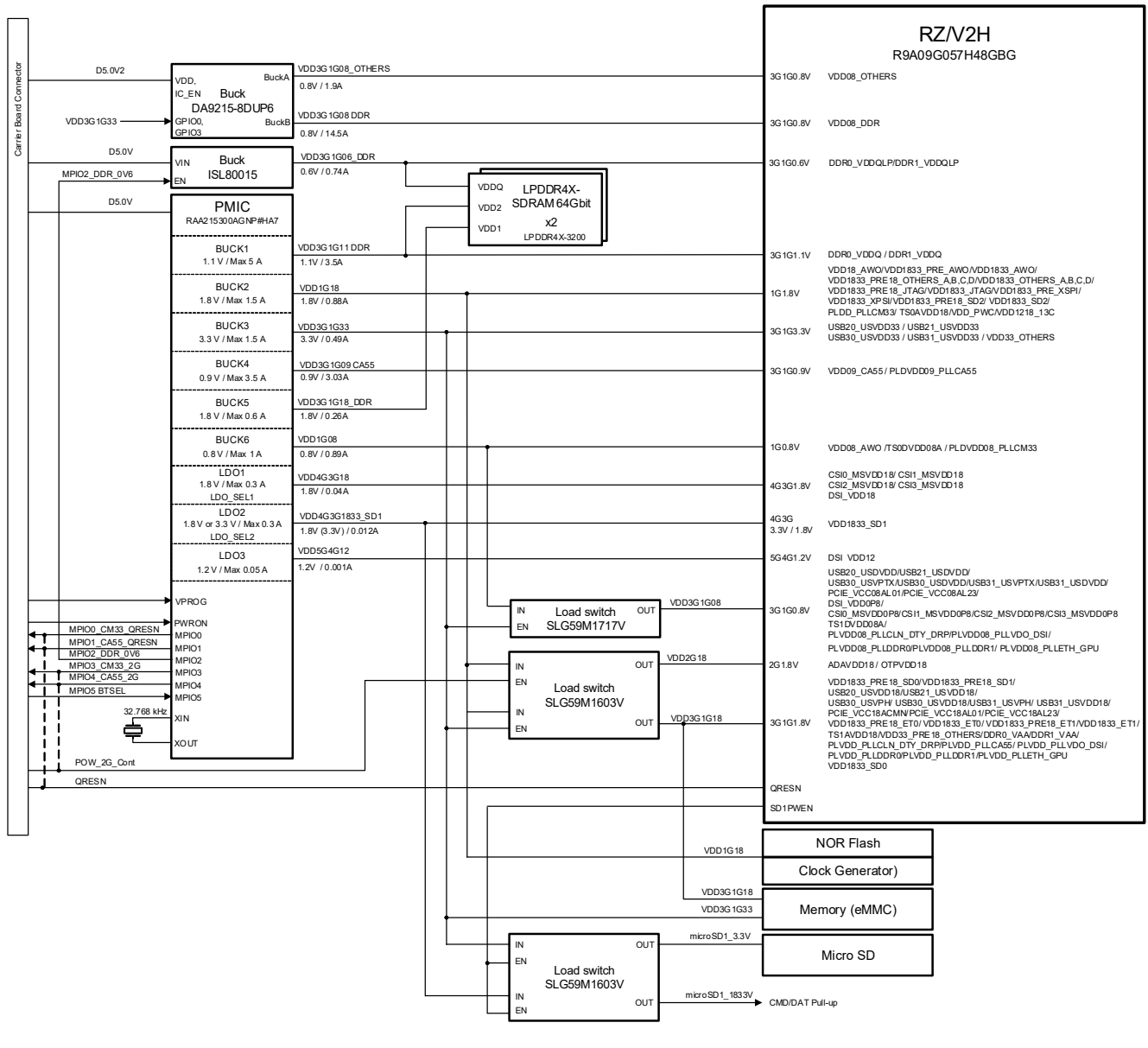


Figure 1. Power Tree for RZ/V2H

#### 3.1 Renesas Components in Power Tree

Table 1. Renesas Components in Power Trees

Part Number	Description
RAA215300A2GNP#HA7	PMIC
ISL80015	Compact Synchronous Buck Converter
DA9215-8DUP6	Synchronous dual Step-Down Converter
SLG59M1603V	GreenFET Dual N-Channel Load Switch
SLG59M1717V	GreenFET Single N-Channel Load Switch

## 4. Power Requirements

### 4.1 Power Sequence – CA55 Boot Mode

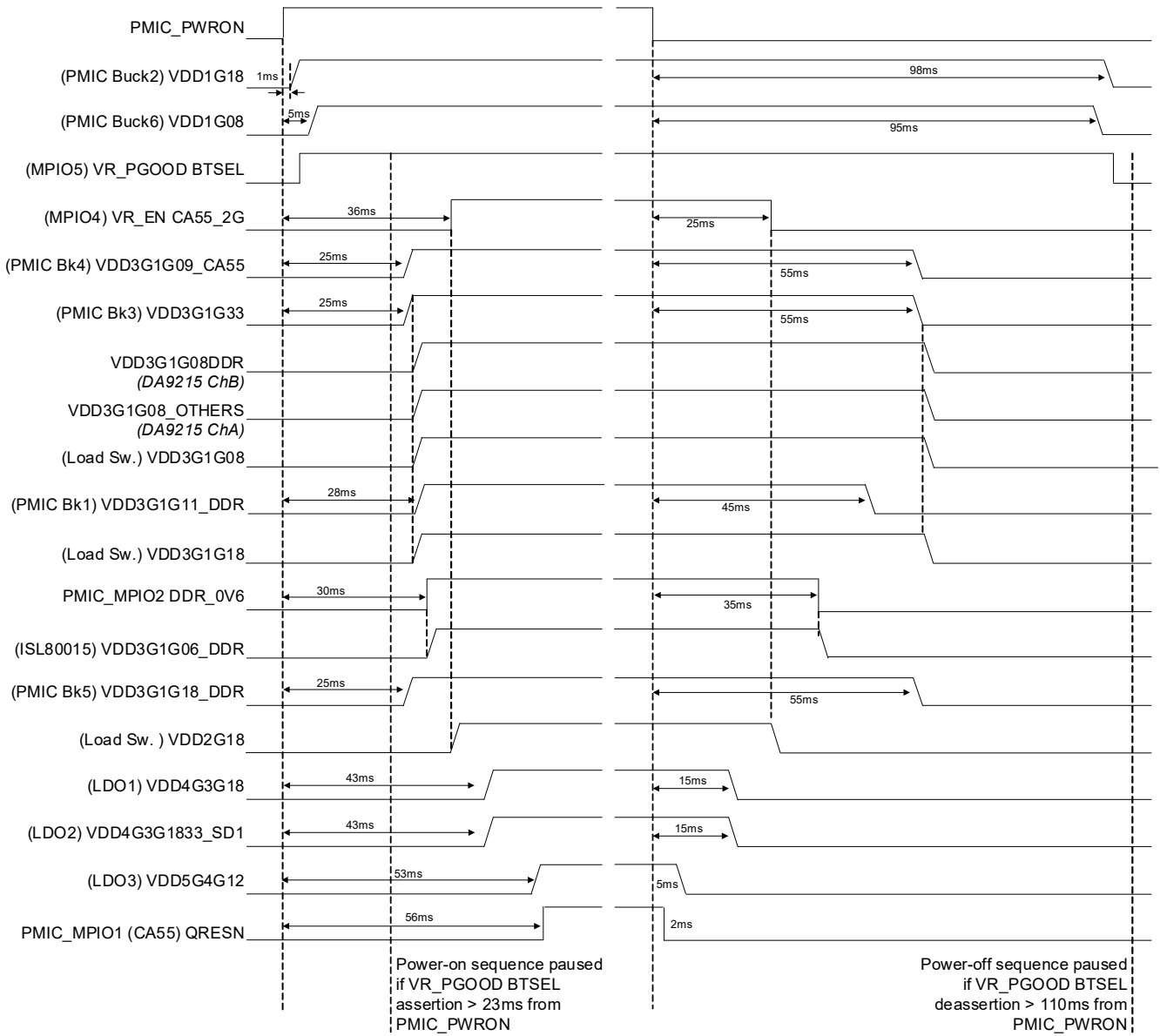


Figure 2. Power Sequence - CA55 Boot Mode

## 4.2 Power Sequence – CM33 Boot Mode

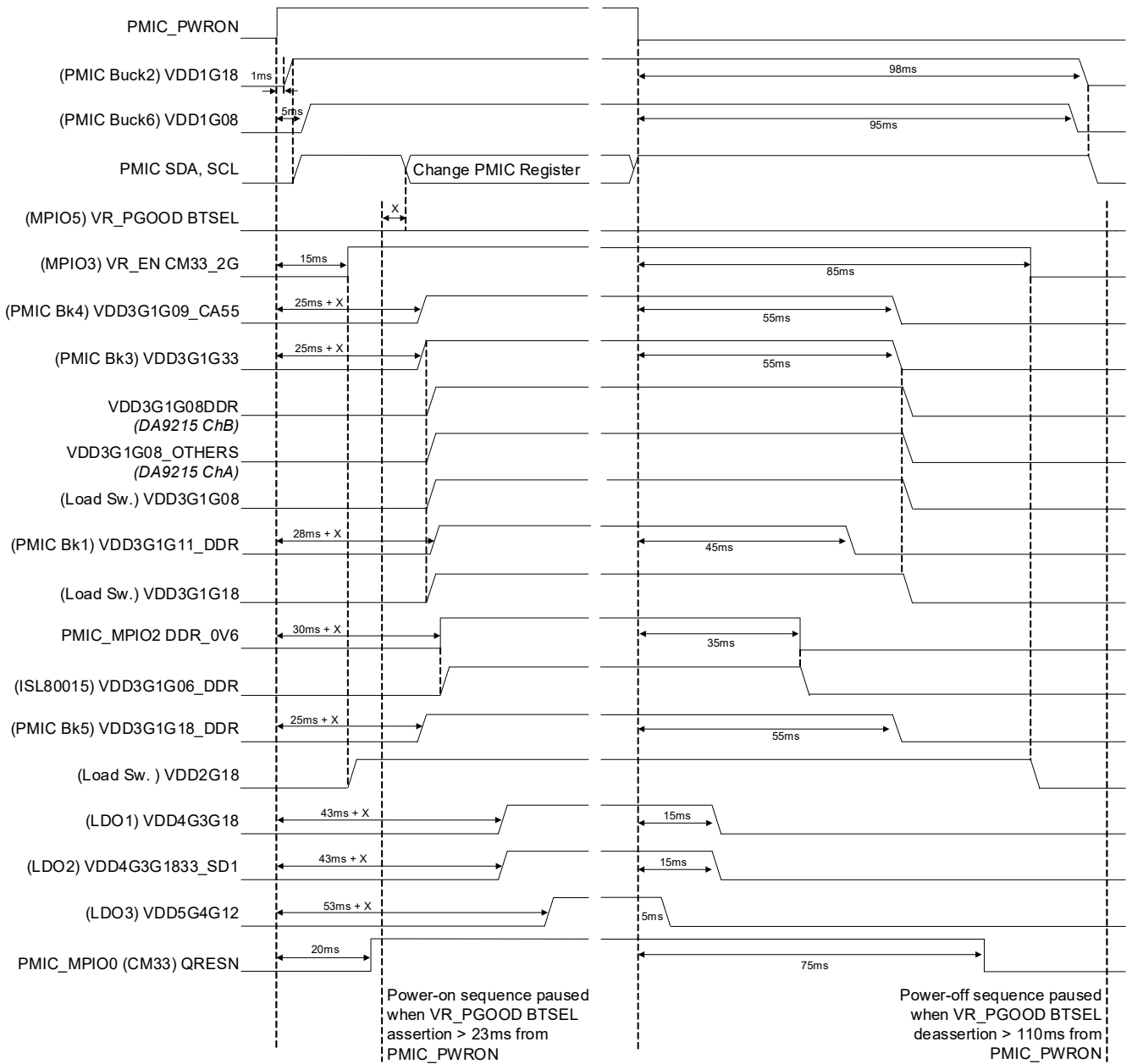


Figure 3. Power Sequence - CM33 Boot Mode

## 5. Variant Table and Ordering Information

Table 2. Variant Table

Part Number	Package	Size	Shipment Form	Pack Quantity
RAA215300AGNP#HA7	QFN56	8mm×8mm Exposed Paddle	Reel	260
DA9215-8DUP6	66 ball WL-CSP	4.5mm×2.5mm	Waffle	2600
ISL80015FRZ-T	8 Ld TDFN	2mm×2mm	Reel	1000
ISL80015IRZ-T	8 Ld TDFN	2mm×2mm	Reel	250
SLG59M1603V	STDFN 14L	1mm×3mm	Reel	3000
SLG59M1717V	STQFN 16L	1.6mm×2.5mm	Reel	3000

## 6. Register Settings

Table 3. Register Setting RAA215300AGNP#HA7

Register Address	Register Name	Default Value	Description
0x1E	Main Slave Address	0x00	Main Slave address = 0x12
0x1F	RTC Slave Address	0x00	RTC Slave Address = 0x6F
0x20	Buck1 Enable	0x07	Buck1 Enabled in Active and Sleep states. ABS enabled. Phase Sync and Spread Spectrum disabled
0x21	Buck1 ACTIVE	0x06	Buck1 Output in Active state = 1.1V (Auto)
0x22	Buck1 SLEEP	0x06	Buck1 Output in Sleep state = 1.1V (Auto)
0x23	Buck1 Power On	0x1C	Buck1 Power-On Delay = 28ms
0x24	Buck1 Power Off	0x2D	Buck1 Power-Off Delay = 45ms
0x25	Buck1 SR	0xAA	Buck1 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x26	Buck1 Config	0x13	Buck1 Switching frequency = 1.11MHz Output discharge = Fast
0x27	Buck2 Enable	0x07	Buck2 Enabled in Active and Sleep states. ABS enabled. Phase Sync and Spread Spectrum disabled
0x28	Buck2 ACTIVE	0x0E	Buck2 Output in Active state = 1.8V (Auto)
0x29	Buck2 SLEEP	0x0E	Buck2 Output in Sleep state = 1.8V (Auto)
0x2A	Buck2 Power On	0x01	Buck2 Power-On Delay = 1ms
0x2B	Buck2 Power Off	0x62	Buck2 Power-Off Delay = 98ms
0x2C	Buck2 SR	0x9A	Buck2 Start Up time = 1ms and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x2D	Buck2 Config	0x1B	Buck2 Switching Frequency = 1.54MHz Output discharge = Fast
0x2E	Buck3 Enable	0x05	Buck3 Enabled in Active state and Disabled in Sleep state. ABS enabled. Phase Sync and Spread Spectrum disabled
0x2F	Buck3 ACTIVE	0x0F	Buck3 Output in Active state = 3.3V (Auto)
0x30	Buck3 SLEEP	0x0F	Buck3 Output in Sleep state = 3.3V (Disabled)
0x31	Buck3 Power On	0x19	Buck3 Power-On Delay = 25ms
0x32	Buck3 Power Off	0x37	Buck3 Power-Off Delay = 55ms
0x33	Buck3 SR	0xAA	Buck3 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x34	Buck3 Config	0x0F	Buck3 Switching Frequency = 1MHz Output discharge = Fast

Table 3. Register Setting RAA215300AGNP#HA7 (Cont.)

Register Address	Register Name	Default Value	Description
0x35	Buck4 Enable	0x05	Buck4 Enabled in Active state and Disabled in Sleep state. ABS enabled. Phase Sync and Spread Spectrum disabled
0x36	Buck4 ACTIVE	0x02	Buck4 Output in Active state 0.9V
0x37	Buck4 SLEEP	0x02	Buck4 Output in Sleep state = 0.9V
0x38	Buck4 Power On	0x19	Buck4 Power-On Delay = 25ms
0x39	Buck4 Power Off	0x37	Buck4 Power-Off Delay = 55ms
0x3A	Buck4 SR	0x5A	Buck4 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x3B	Buck4 Config	0x07	Buck4 Switching Frequency = 0.769MHz Output discharge = Fast
0x3C	Buck5 Enable	0x07	Buck5 Enabled in Active and Sleep states. ABS enabled. Phase Sync and Spread Spectrum disabled
0x3D	Buck5 ACTIVE	0x03	Buck5 Output in Active state = 1.8V
0x3E	Buck5 SLEEP	0x03	Buck5 Output in Sleep state = 1.8V
0x3F	Buck5 Power On	0x19	Buck5 Power-On Delay = 25ms
0x40	Buck5 Power Off	0x37	Buck5 Power-Off Delay = 55ms
0x41	Buck5 SR	0xAA	Buck5 Start Up and Shutdown time = 1ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x42	Buck5 Config	0x1B	Buck5 Switching Frequency = 1.54MHz Output discharge = Fast
0x43	Buck6 Enable	0x07	Buck6 Enabled in Active and Sleep states. ABS enabled. Phase Sync and Spread Spectrum disabled
0x44	Buck6 ACTIVE	0x40	Buck6 Output set to 1.1V in Active state, but VTTREF is enabled so output = VREFIN/2 Auto Independent soft-start, not linked to buck2
0x45	Buck6 SLEEP	0x00	Buck6 Output set to 1.1V in Sleep state, but VTTREF is enabled so output = VREFIN/2 Auto EnPD VTTREF Disabled
0x46	Buck6 Power On	0x05	Buck6 Power-On Delay = 5ms
0x47	Buck6 Power Off	0x5F	Buck6 Power-Off Delay = 95ms
0x48	Buck6 SR	0x5A	Buck6 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x49	Buck6 Config	0x03	Buck6 Switching Frequency = 0.667MHz Output discharge = Fast
0x4A	LDO1 ACTIVE	0x64	LDO1 Enabled in Active state Active 0 setting = 1.8V Active 1 setting = 1.8V Bypass operation disabled
0x4B	LDO1 SLEEP	0x04	LDO1 disabled in Sleep state
0x4C	LDO1 Power On	0x2B	LDO1 Power-On Delay 43ms
0x4D	LDO1 Power Off	0x0F	LDO1 Power-Off Delay = 15ms
0x4E	LDO1 SR	0x5A	LDO1 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x4F	LDO2 ACTIVE	0x67	LDO2 Enabled in Active state Active 0 setting = 3.3V Active 1 setting = 1.8V Bypass operation disabled

Table 3. Register Setting RAA215300AGNP#HA7 (Cont.)

Register Address	Register Name	Default Value	Description
0x50	LDO2 SLEEP	0x07	LDO2 disabled in Sleep state.
0x51	LDO2 Power On	0x2B	LDO2 Power-On Delay = 43ms
0x52	LDO2 Power Off	0x0F	LDO2 Power-Off Delay = 15ms
0x53	LDO2 SR	0x5A	LDO2 Start Up and Shutdown time = 2ms DVS ramp-up and ramp-down slew rate = 8mV/μs
0x54	LDO3 ACTIVE SLEEP	0x52	LDO3 Enabled in Active and Sleep states Active setting = 1.2V Sleep setting = 1.2V (Disabled)
0x55	LDO3 Power On	0x35	LDO3 Power-On Delay = 53ms
0x56	LDO3 Power Off	0x05	LDO3 Power-Off Delay = 5ms
0x57	LDO3 SR	0x5A	DVS ramp-up and ramp-down slew rate = 8mV/μs
0x58	LDOs Config	0x3F	LDO1, LDO2, LDO3 discharge = Fast
0x64	nINT Mask 1	0x00	Undervoltage fault on each buck regulator is not masked from INT#.
0x65	nINT Mask 2	0x00	VIO PGOOD fault is not masked from INT#. Undervoltage fault on each LDO is not masked from INT#.
0x66	nINT Mask 3	0x00	Overvoltage fault on each buck regulator is not masked from INT#.
0x67	nINT Mask 4	0x00	Buck1 high current fault is not masked from INT#.
0x68	nINT Mask 6	0x00	The following faults are not masked from INT#. <ul style="list-style-type: none"> <li>▪ PGOODCCBAT</li> <li>▪ VREFIN UVLO</li> <li>▪ AVDD UVPD</li> <li>▪ NVM</li> <li>▪ CRST Triggered</li> <li>▪ WDT Error</li> <li>▪ Over-temperature warning</li> </ul>
0x69	Fault Config 1	0x3F	Shut down all regulators if any buck regulator is undervoltage.
0x6A	Fault Config 2	0x07	Shut down all regulators if any LDO is undervoltage.
0x6B	Fault Config 3	0x7F	Shut down all regulators if VREFIN is undervoltage. Shut down all regulators if any buck regulator is overvoltage.
0x6C	Block EN	0x00	VBAT comparator enabled. Watchdog timer enabled. Power down when watchdog timer expires. Reset when watchdog timer expires. Power down when CRST_IN# is asserted.
0x6F	Config 1	0xFA	Battery charge current = 60μA. Temperature warning = 120°C. Buck1 high current warning = 6A. AVDD UVPD threshold = 2.7V. PWRON = on/off switch.
0x70	Config 2	0xF8	VCCBAT = 3.3V.
0x71	Config 3	0x17	VIO Timeout = 1ms. Cold reset delay = 255ms.
0x72	MPIO0 Power On	0x14	MPIO0 Power-On delay = 20ms
0x73	MPIO0 Power Off	0x4B	MPIO0 Power-Off delay = 75ms
0x74	MPIO1 Power On	0x38	MPIO1 Power-On delay = 56ms
0x75	MPIO1 Power Off	0x02	MPIO1 Power-Off delay = 2ms
0x76	MPIO2 Power On	0x1E	MPIO2 Power-On delay = 30ms
0x77	MPIO2 Power Off	0x23	MPIO2 Power-Off delay = 35ms



Table 3. Register Setting RAA215300AGNP#HA7 (Cont.)

Register Address	Register Name	Default Value	Description
0x78	MPIO3 Power On	0x0F	MPIO3 Power-On delay = 15ms
0x79	MPIO3 Power Off	0x55	MPIO3 Power-Off delay = 85ms
0x7A	MPIO4 Power On	0x24	MPIO4 Power-On delay = 36ms
0x7B	MPIO4 Power Off	0x19	MPIO4 Power-Off delay = 25ms
0x7C	MPIO5 Power On	0x17	MPIO5 Power-On delay = 23ms
0x7D	MPIO5 Power Off	0x6E	MPIO5 Power-Off delay = 110ms
0x80	MPIO Assertion	0x32	MPIOs 0,1 and 2 External VR enable signals will NOT be de-asserted in Sleep state. MPIOs 3,4 and 5 External VR enable signals will be de-asserted in Sleep state.
0x89	Shutdown Config	0x02	Shut down all regulators, applying discharge resistors and respective shutdown time settings.
0x8A	MPIO0 Config	0x0D	Reset Output, Open drain NMOS, Active Low
0x8B	MPIO1 Config	0x0D	Reset Output, Open drain NMOS, Active Low
0x8C	MPIO2 Config	0x3E	External VR EN output, CMOS Output, Active High.
0x8D	MPIO3 Config	0x3E	External VR EN output, CMOS Output, Active High.
0x8E	MPIO4 Config	0x3E	External VR EN output, CMOS Output, Active High.
0x8F	MPIO5 Config	0x22	External VR PGOOD input, high impedance, Active High.
0x90	PWRON Polarity Config	0x01	Active high.

Table 4. Register Settings DA9215-8DUP6

Register Address	Register Name	Default Value	Description
0x54	MASK A	0x00	nIRQ interrupt, all un-masked
0x55	MASK B	0x00	OV_CURR, TEMP_CRIT, TEMP_WARN and PWRGOOD, all un-masked
0x56	CONTROL_A	0x52	Allow register access (0xD0 to 0x14F) Slew Rate (Both Ch.A and Ch.B) = 10mV/1us. Debounce time = 1ms
0x58	GPIO0-1	0xCC	GPIO0 set to GPI, Active high, debounce Enabled. GPIO1 set to GPI, Active high, debounce Enabled.
0x59	GPIO2-3	0xCC	GPIO2 set to GPI, Active high, debounce Enabled. GPIO3 set to GPI, Active high, debounce Enabled.
0x5A	GPIO4	0x0C	GPIO4 set to GPI, Active high, debounce Enabled.
0x5D	BUCKA_CONT	0x22	Buck A disabled GPIO0 enables Buck A (Passive to Active) Pull down resistor enabled when disabled) Buck A voltage selected from VBUCKA_A GPIO1 specifies the target voltage
0x5E	BUCKB_CONT	0x46	Buck B disabled GPIO3 enables Buck B (Passive to Active) Pull down resistor enabled when disabled) Buck B voltage selected from VBUCKB_A GPIO2 specifies the target voltage
0xD0	BUCK_ILIM	0xE8	Buck B ILIM 6800mA per phase Buck A ILIM 5600mA per phase

Table 4. Register Settings DA9215-8DUP6 (Cont.)

Register Address	Register Name	Default Value	Description
0xD1	BUCKA_CONF	0x93	Buck A: Operates in Automatic mode Shutdown slew rate = 20mV/μs Start-up slew rate = 20mV/μs
0xD2	BUCKB_CONF	0x93	Buck B: Operates in Automatic mode Shutdown slew rate = 20mV/μs Start-up slew rate = 20mV/μs
0xD3	BUCK_CONF	0x1A	Buck A mode set to 3 phases with phase shedding. Buck B mode set to 1 phase with phase shedding.
0xD5	VBUCKA_MAX	0x7C	Buck A Maximum allowable voltage = 1.54V
0xD6	VBUCKB_MAX	0x5B	Buck B Maximum allowable voltage = 1.21V
0xD7	VBUCKA_A	0x32	Buck A Voltage A = 0.8V
0xD8	VBUCKA_B	0x37	Buck A Voltage B = 0.85V
0xD9	VBUCKB_A	0x32	Buck B Voltage A = 0.8V
0xDA	VBUCKB_B	0x3C	Buck B Voltage B = 0.9V
0x143	CONFIG_A	0x1A	nIRQ is Open drain, Active low GPIs are supplied from VDDIO Automatic reset of 2-WIRE interface enabled
0x144	CONFIG_B	0x60	Enabled GPIO0 as OTP reload (if configured as input) Buck A: OC event generation active during DVS Buck B: OC event generation active during DVS Buck A: Power-Good signal masked during DVS Buck B: Power-Good signal masked during DVS
0x145	CONFIG_C	0x16	GPI0 and GPI3: pull down resistor disabled GPI1, GPI2 and GPI4: pull down resistor enabled
0x146	CONFIG_D	0x00	No PG_SEL or READY signals for selected for BuckA or Buck B
0x147	CONFIG_E	0xE0	DA9215 configured as STAND_ALONE
0x148	CONFIG_F	0xC3	-

## 7. Revision History

Revision	Date	Description
1.00	Dec 16, 2024	Initial release

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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