RH4Z2501 Power Consumption and Dissipation

Usage and implementation of internal and external voltage regulators

The RH4Z2501 is a line driver/level shifter IC for IO-Link communication and features a 5V and 3.3V LDO, for example, to supply a sensor circuit with power. External DC-DC converters are required due to the small package and power dissipation is limited especially in high voltage/temperature environments.

This application note is a guideline to the optimal design of the power supply.

Contents

1. Power Supply Architecture and Limitations of the RH4Z2501

Figure 1 shows the block diagram of the RH4Z2501, objects belonging to the power supply are highlighted with red. The chip-internal 3.3V and 5V LDO derive power from L+ (24V nominal, 18V to 30V), generated by IO-Link master.

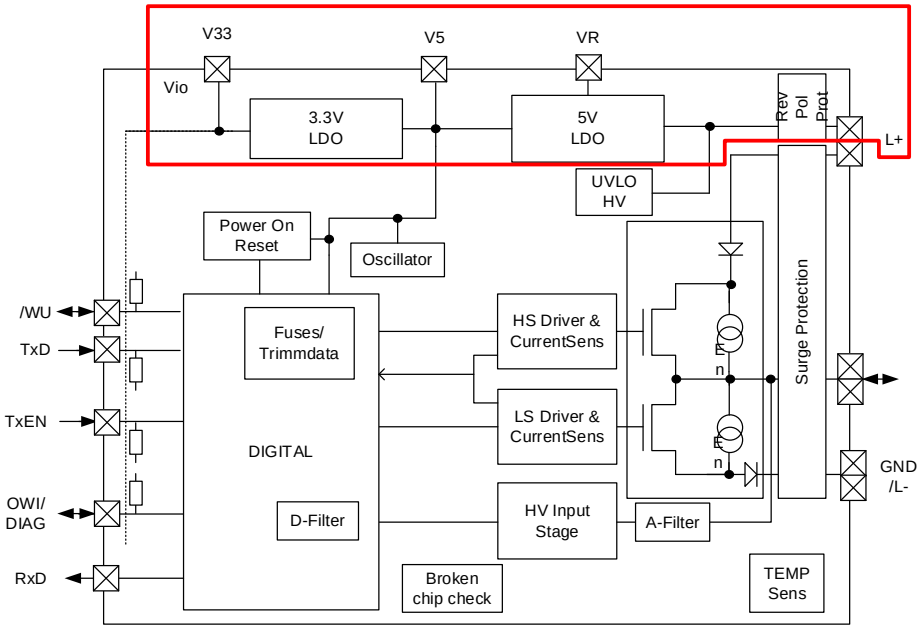

Figure 1. Block Diagram

See Table 1 for functions of the relevant pins.

Table 1. Power Supply Pins

Name	Type	Function
L+	Supply voltage	Power supply via IO-Link (24V nominal, 18V to 30V).
VR	Analog output	5V LDO regulator output.
V5	5V power supply input/output	5V either generated by internal LDO or by external DC-DC regulator.
V33	3.3V power supply output/analog input	3.3V from internal LDO. Defines logic level of the pins, for a 5V logic level, connect this pin to 5V.

The RH4Z2501 offers both internal and external options to generate 5V and 3.3V, see sections 2.1, 2.2, and 2.3 for details. Current draw from internal voltage generation is limited by the maximum power dissipation of the available packages which offer different thermal conductivity. See Equation 1 for calculating the maximum power dissipation ($P_{dis,max}$) with a maximum internal junction temperature ($T_{J,max}$ = 150°C).

$$P_{dis,max} = \frac{T_{J,max} - T_{ambient}}{\theta_{JA}}$$ **Equation 1**

Table 2. $P_{dis,max}$ Calculations for RH4Z2501

Package	Thermal Conductivity θ_{JA} [K/W]	Maximum Power Dissipation $P_{dis,max}$ [W]		
		25°C	80°C	100°C
WLCSP	50	2.5	1.4	1
DFN12	41.5	3	1.7	1.2

For calculations of the generated heat that needs to be dissipated, refer to the *RH5Z2501 Datasheet* document. For high current applications, only P_{CQ} (power generated in the C/Q driver) and the internal LDOs have a major contribution to the total power dissipation.

The significant total power $P_{tot,sig}$ is calculated using the equations displayed in Table 3.

Table 3. $P_{tot,sig}$ Calculations

Variable	Equation	Description
P_{CQ}	$P_{CQ} = I_{CQ(max)} \times R_{on}$	Power loss generated in the C/Q driver.
P_{V5}	$P_{V5} = (V_{L+} - 5V) \times I_{V5}$	Power loss generated by the 5V LDO.
P_{V33}	$P_{V33} = 1.7V \times I_{V33}$	Power loss generated by the 3.3V LDO.
$P_{tot,sig}$	$P_{tot,sig} = P_{CQ} + P_{V5} + P_{V33}$	Sum of the calculated power losses (significant power loss for power dissipation).

2. Implementation of Options for Voltage Generation

2.1 Internal LDOs

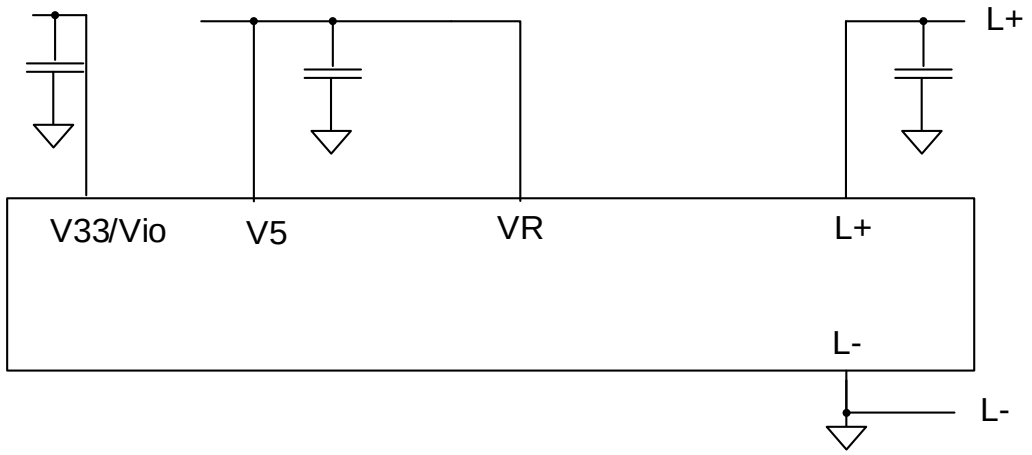

Figure 2. External Circuitry for Using Internal LDOs

See Figure 2 for the simplest solution that only requires passive components and uses the internal LDOs. Offering the smallest footprint, this method is limited to approximately 50mA output current (3.3V and 5V combined) by thermal limitations.

For typical use cases, a C/Q load current of 200mA, a C/Q driver on resistance of 1Ω, and a supply voltage of 24V are assumed. For a worst-case scenario, the C/Q load current is 400mA with an on-resistance of 2.5Ω and a maximum IO-Link supply voltage of 30V.
Regarding the thermal limits and calculations in Table 2 and Table 3, this results in theoretical maximum LDO currents in Table 4 (assuming all current is directly drawn from the 5V LDO).

Note that when current is drawn from the 3.3V LDO, thermal situation is worse due to the additional 1.7V voltage drop from 5V to 3.3V.

Table 4. Maximum Theoretical 5V LDO Current

Package	Normal Use Case [mA]			Worst Case [mA]		
	25°C	80°C	100°C	25°C	80°C	100°C
WLCSP	129[1]	71[1]	50[2]	84[1]	40[3]	24[3]
DFN12	155[1]	87[1]	61[2]	104[1]	52[2]	32[3]

1. The device can be used throughout the entire specified values.
2. The device runs near the limit, values do not offer a margin.
3. Values are outside of the specified normal circumstances. The device must operate below default specification.

While at room temperature or in normal use cases the specified 50mA for the 5V/3.3V LDOs are guaranteed, cases with higher voltage or current need separate considerations. For such cases, outsourcing the voltage regulating components is highly recommended.

2.2 External Transistor

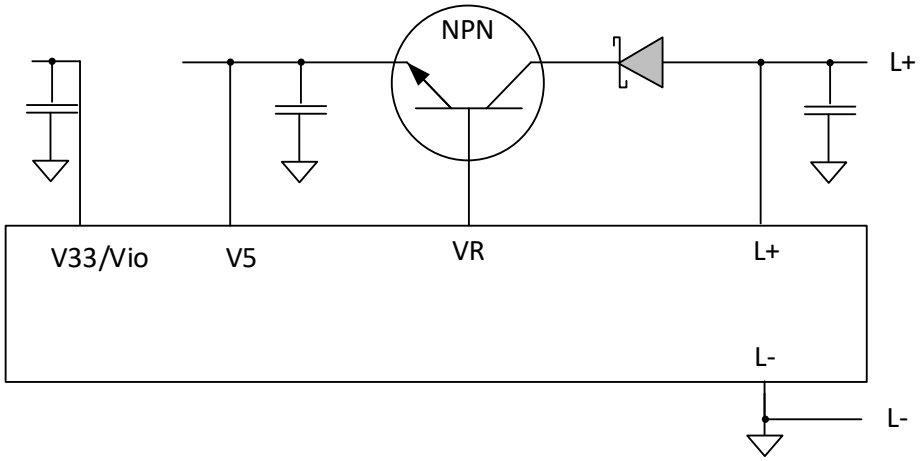

Figure 3. Circuitry for Using an External Transistor

If an external NPN transistor is added, the voltage drop across the internal LDO's power stage is outsourced. The internal LDO functions as a controller for the final control element, the NPN transistor. The heat must be dissipated that comes from the base current of the output VR regulated external transistor. Overall efficiency remains approximately the same, the total power loss can increase when higher currents are drawn than what the internal LDO could supply.

A diode at the collector is necessary to protect the circuit from reverse polarity.

Using a Power MOSFET instead of a bipolar transistor lowers the regulator current to almost 0mA. Methods for heat dissipation must be implemented since the entire voltage drop occurs in the MOSFET. The following Power MOSFETs are suitable for the RH4Z2501:

- RJK0853DPB
- RJF0612JPE

2.3 External DC-DC Converter

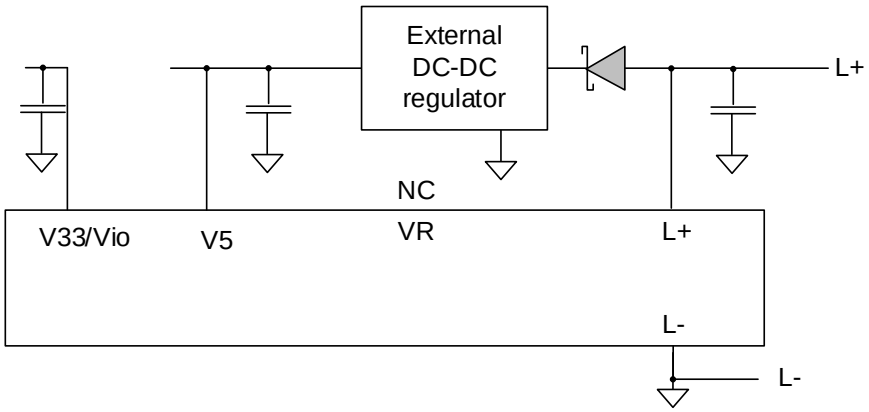

Figure 4. Circuitry for Using an External DC-DC Converter

An external switching regulator allows much higher currents and improves efficiency while adding complexity to the circuit. Note that a protection diode is mandatory. Renesas recommends the RAA211405 and RAA211805 as low power, high efficiency DC-DC converters with an output current of up to 300mA and full IO-Link voltage coverage (18V to 30V).

Using Equation 1, the device packages allow the maximum power dissipation shown in Table 5.

Table 5. $P_{dis,max}$ Calculations for DC-DC Converters

Device	Thermal Conductivity θ_{JA} [K/W]	Maximum Power Dissipation $P_{dis,max}$ [mW]		
		25°C	80°C	100°C
RAA211405/ RAA211403	90	1111	500	277
RAA211805/ RAA211803	85	1176	529	294

The theoretical maximum output current is calculated by Equation 2.

$$I_{out,max} = \frac{\eta}{1-\eta} \cdot \frac{P_{dis,max}}{5V}$$ **Equation 2**

Table 6. Theoretical Output Current

Device	Average Efficiency η	Maximum Theoretical Output Current $I_{out,max}$ [mA]		
		25°C	80°C	100°C
RAA211405	80%	889[1]	400[1]	222[2]
RAA211805	73%	636[1]	286[2]	159[2]

1. The device can be used throughout the entire specified values.
2. The device runs near the limit, values do not offer a margin. The device must operate below default specification.

The internal 3.3V LDO is guaranteed to supply up to 50mA across the entire operating temperature range (no thermal limitation by the 5V LDO is provided). If higher currents are required, generate 3.3V from an external DC-DC converter, but do not connect externally generated 3.3V to pin V33/IO.
Note that if the external voltage is less than the internal voltage, the LDO drives as much current as needed to

reach the voltage, potentially overloading or damaging the device. Small deviations are negligible for logic levels. If the external voltage is ensured to be always higher than the internal voltage, the logic level can be safely adjusted.

To ensure that the calculated limits in Table 5 and Table 6 are implementable, proper design and layout of the components is crucial. The design guides in the respective datasheets of the components must be applied for dimensioning and PCB layout. A possible, recommended schematic and PCB layout for the RH4Z2501 using an external DC-DC solution is shown in Figure 5 and Figure 6. Table 7 lists the components used in the design. For further information on thermal design, refer to *RH4Z2501-KIT EMC Compliance Application Note* document of the evaluation package.

General design guidelines:

- Use at least a two-layer PCB with 1oz copper. Bottom layer shall be GND, especially underneath switching components.
- Place power components on the same side of PCB.
- Place and route power components as short/compact as possible. Avoid large power loops.

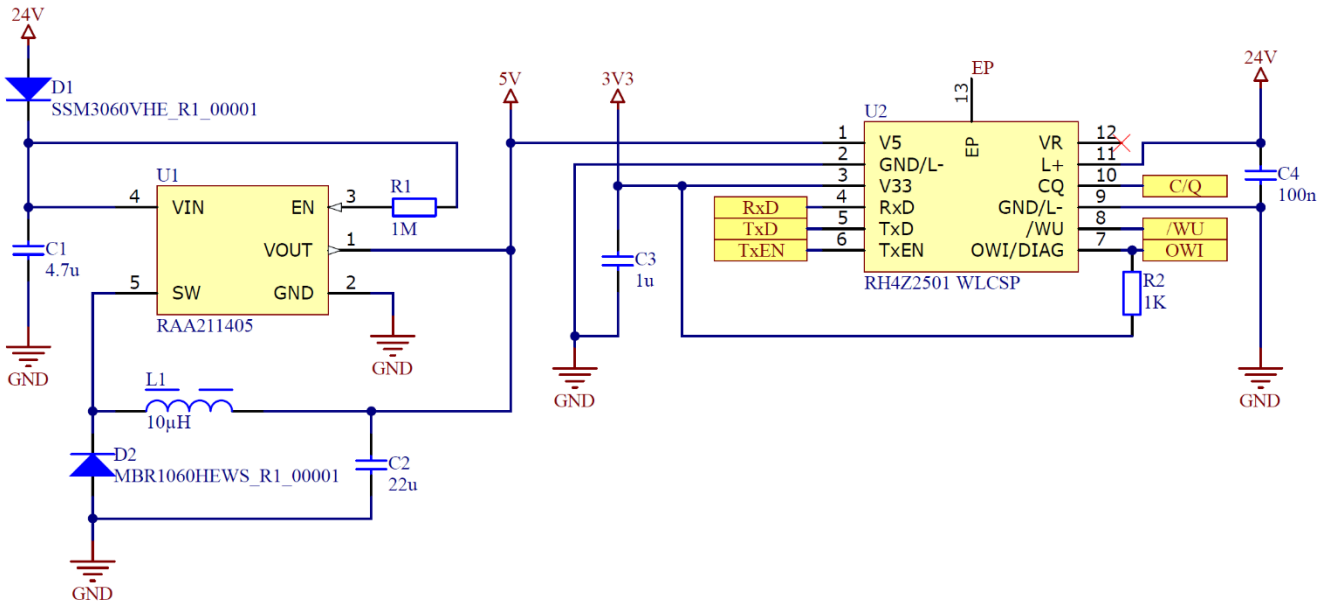

Figure 5. Example Schematic for DC-DC Converter Implementation

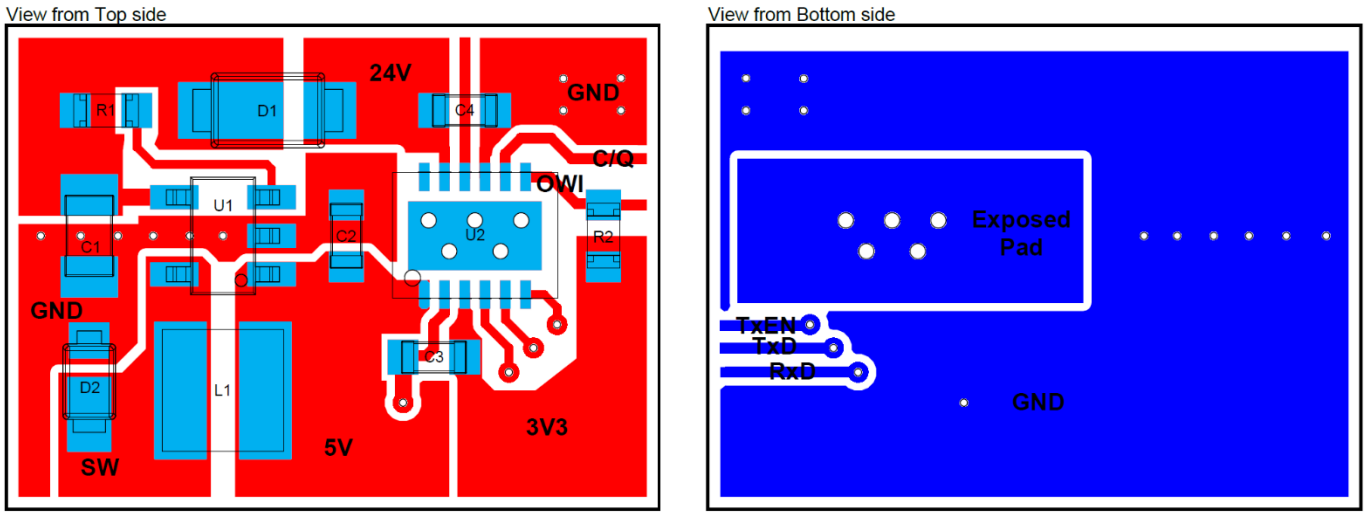

Figure 6. Example Layout for DC-DC Converter Implementation

Table 7. Bill of Materials for Example Schematic

Designator	Description	Manufacturer and Part Number	Application Comment
U1	40V, 300mA, 4µA I_Q DC-DC step-down regulator	Renesas RAA211405	Use thermal vias on GND copper for heat dissipation.
U2	IO-Link transceiver with integrated protection	Renesas RH4Z2501	Use vias on exposed pad and a large copper area on bottom layer for heat dissipation.
C1	4.7µF, 50V, 0805 ceramic capacitor	Various	Input capacitor for U1. Place as close to U1 as possible.
C2	22µF, 16V, 0603 ceramic capacitor	Various	Output capacitor for U1. Place close to L1.
C3	1µF, 10V, 0603 ceramic capacitor	Various	Output capacitor for U2 (3.3V LDO output). Place close to U2.
C4	100nF, 50V, 0603 ceramic capacitor	Various	Input capacitor for U2. Place as close to U2 as possible.
R1	1MΩ metal film resistor	Various	Enable signal for U1.
R2	1kΩ metal film resistor	Various	Pull-Up resistor for OWI.
D1	3A, 60V, SOD-123HE schottky barrier diode	Panjit SSM3060VHE_R1_00001	Reverse polarity protection for U1. Choose diode with low forward voltage.
D2	1A, 60V, SOD-323HE schottky barrier diode	Panjit MBR1060HEWS_R1_00001	Rectifier diode for U1. Place close to L1 to keep the copper area of SW as small as possible.
L1	10µH, 1.25A, 446mΩ DCR Power Coil Inductor	Würth Elektronik 74438335100	Inductor for U1. Place as close to U1 as possible.

3. Glossary

Term	Description
C/Q	C/Q line of IO-Link interface. Connection for communication (C) or switching (Q) signal.
DC-DC	Direct-Current - Direct Current
IO	Input Output
IO-Link	Industrial Communication Standard (IEC 61131-9 Single-drop digital communication interface for small sensors and actuators (SDCI))
LDO	Low Drop Out Regulator
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NPN	Negative Positive Negative
OWI	One Wire Interface
PCB	Printed Circuit Board
VR	Voltage Regulator

4. Revision History

Revision	Date	Description
1.00	Jan 24, 2024	Initial release.

5. Related Documents

Revision	Date	Description
1.00	Jun 08, 2023	RH4Z2501 Datasheet
1.03	Dec 01, 2023	RAA211403, RAA211405 Datasheet
1.00	Oct 02, 2023	RAA211803, RAA211805 Datasheet
1.00	Jun 30, 2023	RH4Z2501-KIT EMC Compliance