RL78 Family

RL78 8-bit PWM Dithering

R01AN3796EU0100
Rev.1.00
Aug 10, 2017

Introduction

Most RL78 MCUs have a 16-bit TAU timer that can be used to implement a PWM output, where that digital output can be RC-filtered to create a DAC-like DC output voltage proportional to the PWM duty cycle. This app note describes a method to utilize the TAU timer in 8-bit PWM mode and use PWM dithering (modulation) method to implement a 12-bit effective DAC function.

Target Device

RL78/G14 MCUs having 16-bit TAU timer and fSUB = 32768HZ oscillator. **Note:** *RL78, S3 core MCUs having 16-bit TAU timer, 10bit ADC, and DTC (Data Transfer Control), such as RL78/G11, G1F, G1H, I1D, I1E, L1C, F13, F14, and F15 may also be used, but should be tested thoroughly to assure compatibility.*

Contents

1. Overview

Most RL78 MCUs have a 16-bit TAU timer that can be used to generate a PWM output with variable duty cycle by using a TAU master channel and slave channel. That PWM output can be filtered by a simple RC low pass filter to create a DC level proportional to the duty cycle percentage. The key is reduce the ripple of the filtered PWM target DC voltage, so the ripple amplitude is less than 1lsb at the desired effective bit resolution. Even though the 16-bit timer can create constant, repetitive PWM waveforms directly, with up to 16-bit resolution, the PWM period for 12-bit to 16-bit PWM resolution can be quite long, requiring an inordinately long RC filter time taking one second or longer to settle. However, an 8-bit resolution PWM with 256 possible duty cycle/factor values provides a short PWM period that can be RC filtered to a proportional DC value much more quickly. Then to achieve higher equivalent bit resolution, a PWM duty cycle dithering method can be utilized, similar to PWM dithering implemented on the 16bit KB timer hardware found in RL78/I1A, L1C and L13 series MCUs.

For example, in LED lighting or analog control systems that need a logarithmic type transfer function, a total of 256 linear levels may not be adequate, since the control needs to have finer resolution steps at lower drive levels. By modulating or dithering the PWM output between 2 consecutive 8-bit code duty cycles and smoothing the output by RC low-pass filter, a variable duty cycle can achieve more than 256 DC output levels from an 8-bit PWM timer output.

This application note provides a framework to implement the PWM dithering method to increase the resolution of effective filtered PWM output DC levels. It is up to the user to perform a full evaluation to measure DC accuracy, and response time versus PWM dithering update frequency and RC low-pass filter characteristics. The DC output accuracy and performance also depends on the user's Hardware implementation, including measures to minimize residual digital noise level in the user's board design.

2. PWM Dithering method

The dithering method is accomplished by modulating the PWM output between 2 adjacent duty cycle percentage values in a periodic manner, automatically, by using DTC (Data Transfer Control) function. For example, the simplest PWM dithering method could be implemented by toggling between a PWM duty cycle value of 128/256 (50% duty cycle) and 129/256 (~50.4% duty cycle), alternating between these 2 duty cycles continuously. This waveform would look almost like a square ware (with a peak-to-peak value of VDD-VSS voltages) alternating between 50% and 50.4% duty cycle. If this (almost 50%/50%) square wave is filtered by a sufficiently designed low pass filter, an equivalent DC value of 128.5 out of full-scale 255 amplitude levels above 0Volts could be obtained, emulating approximately 9 bits of resolution. The low pass filter is used to reduce the dithering pattern ripple to less than 1 LSB at the new effective 9-bit resolution. **Note:** *Figure 1 example shows a 5.6KΩ series resistor and 5.6uF filter capacitor for reducing ripple in a repeating 256uSEC PWM dither pattern, but values could be modified as required if using different PWM dithering timing.*

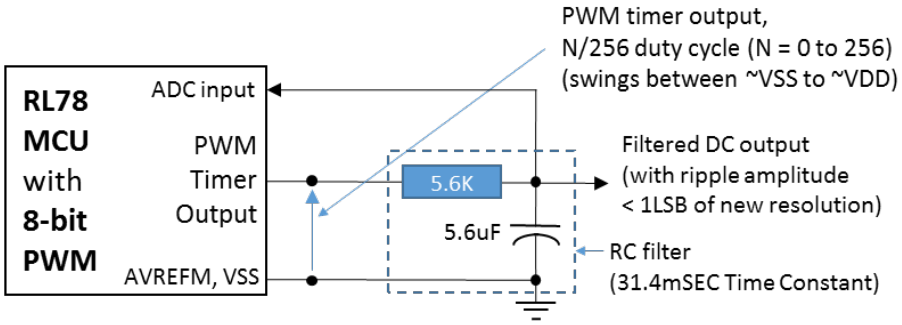


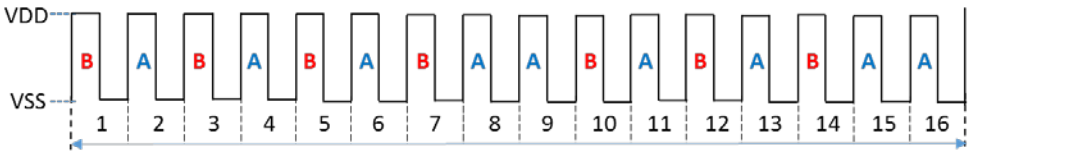
Figure 1: Low Pass RC filtering of dither PWM Output

2.1 8-bit Dithering over 16 PWM output cycles

By modulating or dithering the PWM duty cycle values over a longer repeat period, with different dither patterns, more equivalent DC resolution bits can be obtained. This App note shows a method to create 4 additional bits of resolution, by outputting PWM output patterns that repeat every 16 PWM cycles. With the 16 cycle pattern smoothed out by an RC low pass filter, it is capable of producing one of 15 intermediate DC voltage values between two adjacent 8-bit PWM filtered DC values. Thus, the effective DC output resolution can be almost 12 bits, with some limitations (described later).

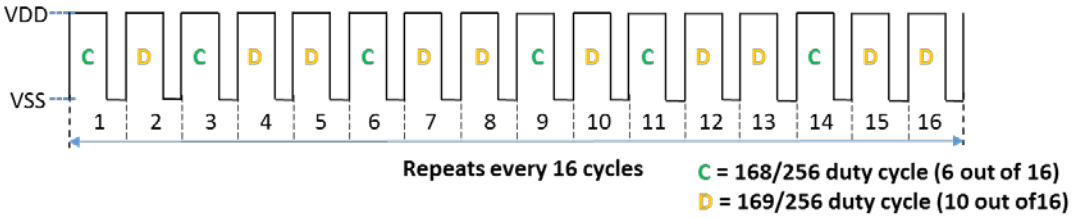
In **Figure 1** above, the RC filter of R = 5.6KΩ and C = 5.6uF (RC time constant = 31.4mSEC) was chosen to reduce the ripple amplitude of a PWM carrier with 16uSEC duration to about ½ lsb at 12-bit effective resolution. A larger series and smaller shunt C could also be used to implement the RC time constant of 31.4mSEC, although DC accuracy could be affected more by test instrument loading. Generally, the RC low-pass Filter time constant should be about 2048 x PWM period to achieve ½ lsb at 12-bit effective DC resolution.

(a) **Example 1: PWM output dithered between codes 0x80 and 0x81 (dither pattern for 0x80 + 7/16)**



$$0x80 + \frac{7}{16} \Rightarrow 0x807 \text{ (12bit representation)}$$

(b) **Example 2: PWM output dithered between codes 0xA7 and 0xA8 (dither pattern for 0xA7 + 10/16)**



$$0xA7 + \frac{10}{16} \Rightarrow 0xA7A \text{ (12bit Representation)}$$

The Data Transfer Control (DTC) function is used to automatically update the changing PWM duty cycle for 16 states of Dithering pattern, without CPU intervention needed until the last of 16 cycles, when the DTC is re-set for next 16-state operation. The RC filter with 31.4mSEC Time constant shown in Figure 1 is used to implement the PWM dithering Application Note Software project. With a PWM duty factor update cycle time of 16uSEC, and the dither pattern repeating every 256uSEC, a single stage RC filter with time constant of 31.4mSEC can reduce the ripple to less than 1 lsb amplitude at the new, higher effective resolution, targeted at 12 bits. The target low-pass filter RC time constant is estimated by RC = 2048 x 16uSEC = 32.768mSEC.

As shown in the **Figure 1** block diagram, the ADC input can be used to monitor the filtered PWM dithering, and apply a correction (closed-loop method) for better DC output accuracy, within the absolute accuracy of the ADC conversion measurements.

2.2 PWM dithering control options:

(a) **Using open-loop PWM dithering WITHOUT ADC monitoring:**

This method will create monotonic DC steps, with almost 12-bit resolution (limitations discussed later). However, the filtered 8-bit PWM duty cycle to DC accuracy will be affected by voltage offsets due to port pin VOL voltage when the PWM output is at low state and by VOH voltage when the PWM output is at high state. In other words, PWM peak-peak output swing will most likely not be between VDD and VSS, where the full-scale analog references are usually AVREFP=VDD, and AVREFM=VSS. The open-loop method may be more useful when an absolute DC voltage level is not required, but DC level feedback is done by a human interacting with pot adjustment or up-down pushbutton control.

Tradeoffs*:* Using the open-loop PWM dither mode will settle to the target DC value more quickly but will have larger absolute offset error compared to using the closed method with ADC monitoring and feedback.

(b) **Using closed-loop PWM dithering WITH ADC monitoring and feedback:**

The RL78 10-bit ADC maximum overall error is +/-3.5 LSB (when using AVREFP and AVREFM full-scale analog voltage reference). By calibrating the individual RL78 MCU ADCs on each board in the factory, even better accuracy might be obtained for the ADC conversion results, and therefore to the filtered PWM dithered DC output. By summing and averaging 16 consecutive 10-bit ADC conversions, it is possible to measure the target 12 bits effective resolution of the filtered PWM dithering DC output.

Due to system digital noise it's inevitable that each averaged/scaled sum of 16 consecutive 10-bit ADC conversion of filtered PWM dithered values will still vary by 1-2 LSB (or possibly more) out of 12-bit effective value. So there will be some random amplitude jitter on the corrected PWM dithered 12-bit effective resolution when using ADC averaged measurements and feedback. The app note Software project takes 256 ADC samples (1638.4HZ sample rate) and updates the Dither factor by +1, or -1 (for correction) or zero (if no offset is detected), every 256 ADC samples which is at a 6.4HZ (156.25mSEC) update rate. This simple correction method is often referred to as "bang-bang" feedback.

Tradeoffs*:* the closed-loop PWM Dithering method provides better DC accuracy, but takes longer (typically 500-600mSEC or more) to settle to a new target 12-bit effective DC value.

3. RL78 MCU resources used

3.1 MCU Hardware

(1) 16bit TAU timer Channels 0 and 1. Ch0 is used to create PWM carrier frequency and constant 16uSEC DTC update rate to PWM duty cycle value, and Ch1 for generating 8bit variable duty cycle PWM output.

(2) DTC (Data Transfer Control) operation to automatically load sequential 16 state dither pattern into the PWM duty cycle register setting. Takes about 8 CPU/System clock cycles per DTC transfer, with no CPU operation needed.

(3) 10bit ADC conversions at 1638.4HZ rate (every 610.4 uSEC), using fSUB = 32768HZ clock with ADC Hardware Trigger Wait mode from 12-bit Interval Timer.

(4) Optional UART1 output to transmit live 12-bit averages of filtered PWM dithering DC value.

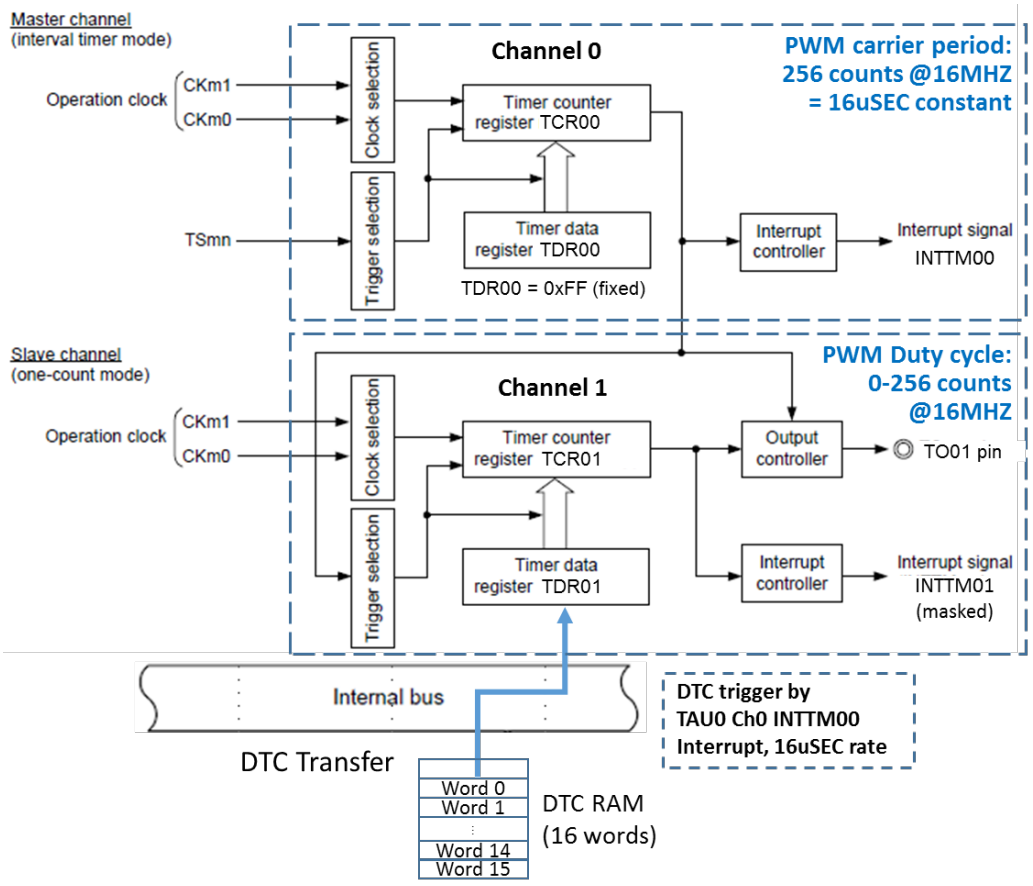


Figure 2: DTC data transfers triggered by TAU Ch0 timer to load next PWM duty cycle value

3.2 MCU CPU processing

Since the PWM output is being dithered, some CPU processing overhead is required:

(1) DTC updates every 16uSEC; DTC uses 8 CPU cycles out of every 512 cycles when using 32MHZ CPU clock rate. The update rate could be adjusted for faster or slower updates if desired, as long as the RC low-pass filter time constant is adjusted accordingly.

(2) DTC state reload interrupts, `r_tau0_channel0_interrupt()`, every 16 DTC cycles, at 256uSEC rate.

(3) 10-bit ADC conversion completion interrupt processing every 610.4 uSEC (1638.4HZ rate). 10-bit ADC conversions occur at 1638.4HZ rate using fSUB = 32768HZ clock in ADC Hardware trigger wait mode. However, the ADC HW triggered conversions themselves can operate in parallel with Software operation. ADC conversions are an optional method to monitor RC low-pass filter output from PWM dithering pattern, and correct the DC value by modifying the dither patter.

(4) Processing sum of 16 consecutive ADC conversion every 9.677mSEC (102.4HZ rate)

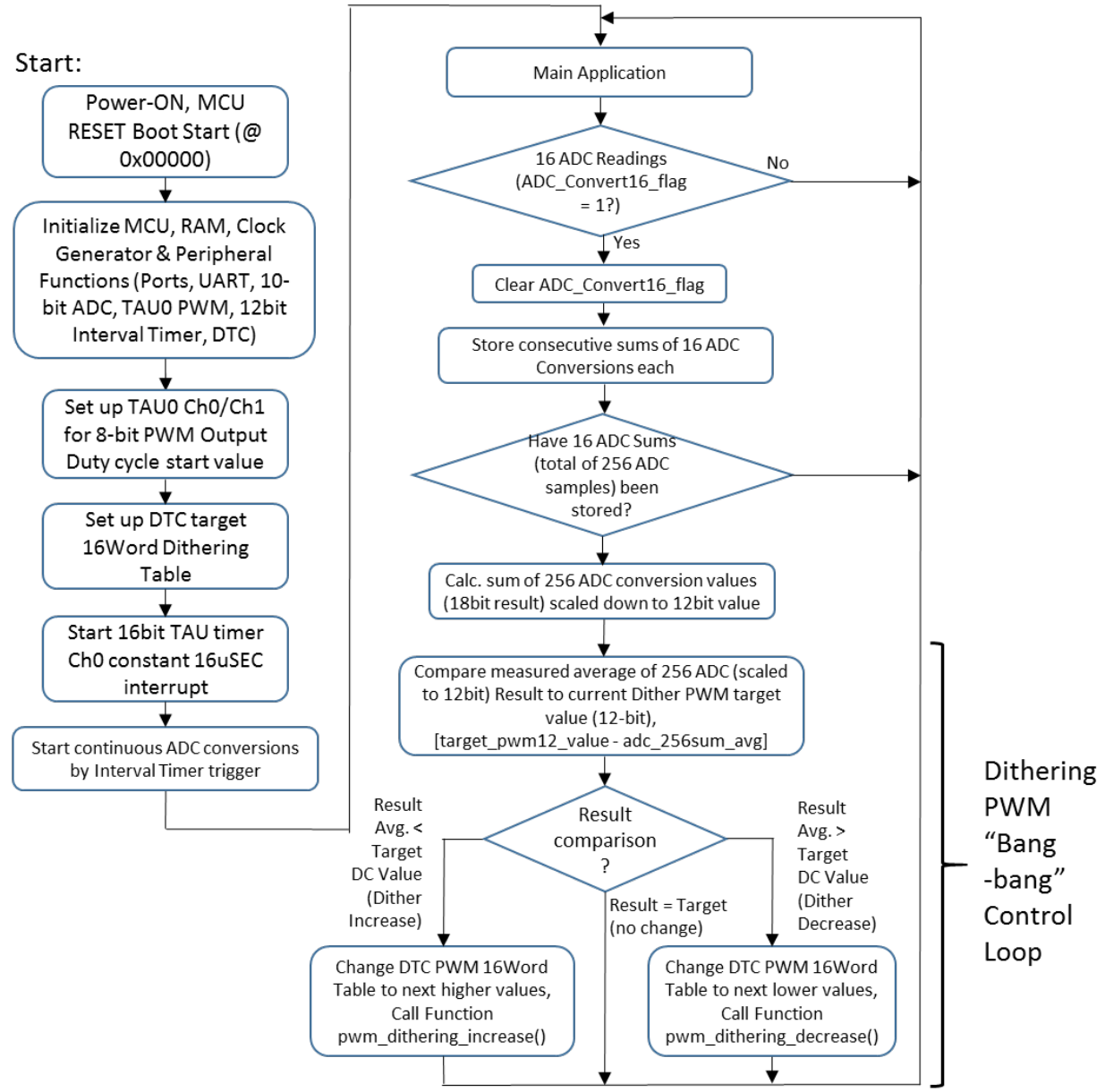
(5) Optional UART1 interrupts, processing at 86.81uSEC per ASCII Character at 115.2Kbaud. This facilitates real-time monitoring of 16 consecutive averaged 10-bit ADC conversions of filter PWM dithered output, in a testing mode.

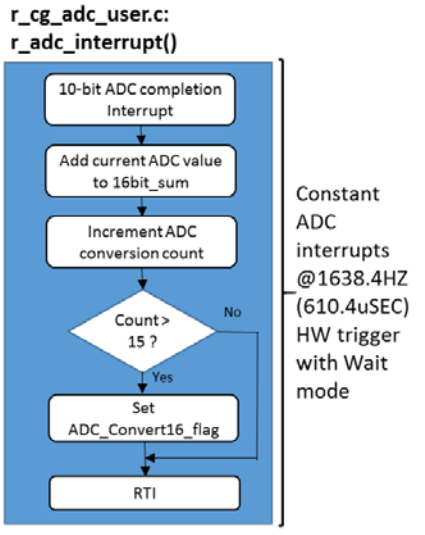
4. Software Environment

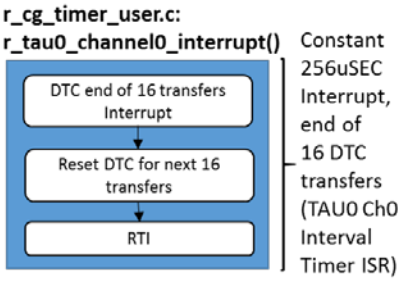
IDE	RL78 Compiler	Compiler Versions
Renesas e2studio v5.4.0.018	CC-RL	v1.05

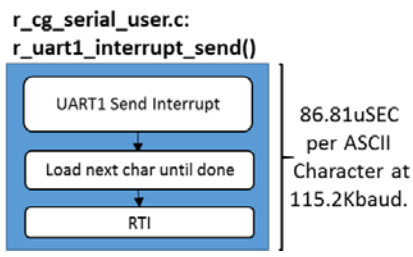
Table 1: Sample Software project environment

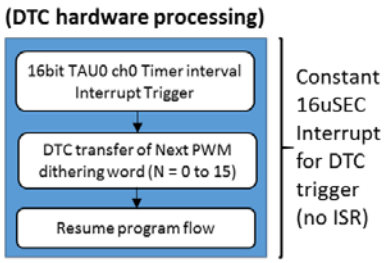
5. PWM Dithering (High-level Flowchart and Interrupt processing)











6. PWM dithering method details

6.1 PWM Dither Adder Sequence table

This PWM dither adder sequence table was designed to distribute the zeroes and ones pattern for highest repetition frequency, although PWM dither pattern is not so critical, since frequency components are similar for adjacent duty cycles (for example 128/256, and 129/256 duty cycles have almost the same harmonic content values). A zero means the base PWM duty cycle value is used and a one means the base PWM duty cycle + 1 value is used. The Dither factor is the total duty cycle of N/16, where N = 0 to 15.

	Dither sequence (Dither factor)															
DTC State	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
3	0	0	0	0	0	0	1	1	1	0	0	1	1	1	1	1
4	0	0	0	0	0	1	0	0	0	1	1	0	1	1	1	1
5	0	0	0	0	1	0	0	1	1	0	1	1	0	1	1	1
6	0	0	0	1	0	0	1	0	0	1	0	1	1	0	1	1
7	0	0	0	0	0	1	0	1	1	0	1	0	1	1	1	1
8	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
9	0	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1
10	0	0	0	0	0	1	0	1	0	0	1	0	1	1	1	1
11	0	0	0	1	0	0	1	0	1	1	0	1	1	0	1	1
12	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1
13	0	0	0	0	1	1	0	0	1	1	1	0	0	1	1	1
14	0	0	0	0	0	0	1	1	0	0	0	1	1	1	1	1
15	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
16	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
DTC Dither sequence	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Base PWM value Base PWM value + 1

Table 2: Dithering adder sequence table

Each vertical set of 16 adder values is for creating a new DTC sequence by adding to the base PWM value.

Examples:

- DTC Adder Sequence 0 has all zeroes (no dithering)
- DTC Adder Sequence 7 has 9 zeroes and 7 ones (7/16 dithering)
- DTC Adder Sequence 15 has one zero and 15 ones (15/16 dithering)

6.2 DTC PWM Dithering adder example

Example to create new DTC Dithering values:
If base PWM value is 0x0080, and adder is for 7/16 dithering, use DTC Adder Table 7

DTC state	PWM Base Value		Dithering Adder Values		New DTC Sequence
1	0x0080	+	1	=	0x0081
2	0x0080	+	0	=	0x0080
3	0x0080	+	1	=	0x0081
4	0x0080	+	0	=	0x0080
5	0x0080	+	1	=	0x0081
6	0x0080	+	0	=	0x0080
7	0x0080	+	1	=	0x0081
8	0x0080	+	0	=	0x0080
9	0x0080	+	0	=	0x0080
10	0x0080	+	1	=	0x0081
11	0x0080	+	0	=	0x0080
12	0x0080	+	1	=	0x0081
13	0x0080	+	0	=	0x0080
14	0x0080	+	1	=	0x0081
15	0x0080	+	0	=	0x0080
16	0x0080	+	0	=	0x0080

Table 3: Dithering adder example for target 12bit value 0x807

6.3 Tradeoffs for PWM dither update rate versus CPU overhead

When implementing the PWM dithering method shown in this app note, it may be desirable to change the dithering rate, which may also require modifying the low-pass filter RC time constant. The tradeoff is that a slow dithering update rate, and longer RC filter time constant, will have a longer response time when changing the target PWM dithered 12-bit effective resolution value, especially when the target DC output value delta change is large. For example, changing from 10% to 90% of the analog full scale reference will take a settling time that is proportional to the RC low pass filter time constant (approximately 2.5 to 3 RC time constants for 10% to 90% slew rate). However, a faster PWM dither rate will require more CPU/System clock cycles for DTC operation and higher CPU processing overhead. Therefore, the user will need to determine a balance between adequate DC Slew rate performance versus System/CPU processing overhead. The sample software project uses 16uSEC DTC update rates based on a 16MHZ TAU timer clock rate, so at 32MHZ system clock the DTC operation uses 8clocks out of every 512 System clocks.

6.4 Measuring PWM dithering ripple at RC low-pass filter output

The app note software project implements a 16uSEC PWM dither update rate that repeats every 16 periods (256uSEC total period) to create close to 12-bit effective resolution. The RC low pass filter should be designed to limit ripple to less than 1LSB at 12-bit effective resolution. This app note sample project uses 5.6K series resistor and 5.6uF capacitor for a 31.4mSEC RC time constant. Using the 31.4mSEC RC time constant achieves about 0.5-0.6 LSB typical ripple amplitude (relative to 12-bit effective resolution) when the duty cycle is 50%, which is worst case.

It is difficult to measure the dithering ripple amplitude after RC filtering for these reasons:

(1) The ripple amplitude for 12-bit effective resolution from RC filtered PWM is typically less than 0.75mV-1.25mV (or lower) depending on VDD value. In Table 2 example below, VDD values of 3.072 Volts and 5.12 Volts (similar to typical 3Volt and 5Volt power supplies) are shown to make the steps easy to represent. At these 0.75-1.25millivolts levels (or less) the System/MCU noise levels may be as high the PWM dithering ripple value.

		Each LSB step, when AVREFP = VDD =	
Using RL78:	**Resolution**	**3.072 Volts**	**5.12 Volts**
ADC	10-bit	3mV	5mV
RC-filtered PWM Dithering	12-bit (effective)	0.75mV	1.25mV

Table 4: ADC/PWM Dithering resolutions

(2) Although an RC filter series resistance of 5.6KΩ was used for app note sample project, almost any instrument loading on the RC filter will still affect the 12-bit effective DC level accuracy somewhat, especially when loaded with a 1MΩ probe. In open-loop mode, the DC value will drop by about 23 LSB (12-bit resolution) if loaded by 1MΩ impedance. In closed-loop mode the PWM dither algorithm will try to compensate and bring the RC-filtered output back to the target 12-bit effective DC value. The compensation will work for most of the 12-bit DC voltage target range unless the unloaded target DC value was at the upper PWM duty cycle range, and no more compensation "head-room" is left.

Scope/meter Probe Loading on RC filter output (5.6Kohm series resistor)	Lowered DC amplitude due to Probe loading	Loading Error, One part in:	Equivalent LSB error @12bit resolution:
1 Megohm	0.99443	179.6	22.8
10 Megohm	0.99944	1788	2.3

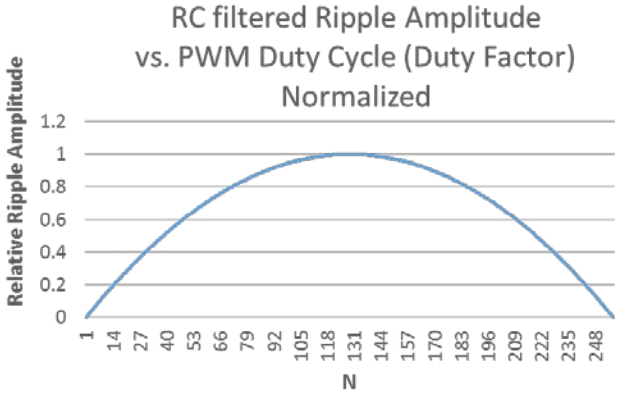
Figure 3: Measurement errors due to instrument loading

6.5 Typical PWM dithering ripple amplitude from RC low filter

For a variable duty cycle PWM waveform filtered by RC filter, the maximum ripple is at 50% duty cycle (duty factor). If the maximum ripple at 50% duty factor is normalized to 1.0, the relative RC-filter PWM ripple is shown by equation:

$$\text{RC-Filtered PWM ripple} = 4*(DF - (DF)^2);$$

where DF *= Duty Factor = N/256 for N = 0 to 256*



N	Duty Factor	Relative Ripple Amplitude
0, 256	0	0
1, 255	0.0039	0.0156
2, 254	0.0078	0.0310
4, 252	0.0156	0.0615
8, 248	0.0313	0.1211
16, 240	0.0625	0.2344
32, 224	0.1250	0.4375
64, 192	0.2500	0.7500
128	0.5000	1.0000

Figure 4. Relative PWM ripple amplitude after simple Low Pass RC Filtering

The RC-filtered PWM ripple amplitude is symmetrical around 50% duty cycle. For example the filtered ripple amplitude for duty factor = 64/256 is the same as for duty factor 192/256, just inverted. As the Duty factor approaches 0% and 100%, the PWM output harmonic content increases and is more highly attenuated by the RC filter. Since dithering is performed by alternating between 2 adjacent PWM duty cycles (for example, 128/256 versus 129/256 duty cycle), there is almost no difference in ripple amplitude between different dither factors using the same base PWM duty cycle value.

6.6 Understanding PWM DC offset errors due to VOL and VOH offsets

When the PWM dithering is in open-loop mode the main DC errors are from DC offsets in the port pin P16/TO01 output due to VOL (when PWM output is at low state) and VOH (when PWM output is at high state). Most often the P-channel transistor driving the port pin high is weaker than the N-channel transistor, so that the VDD-VOH difference offset is typically larger than the VOL-VSS difference offset. That means the range of RC filtered DC value over PWM values of duty cycle of 0x00 to 0xFF will be less than VDD-VSS (AVREFP-AVREFM) full scale analog voltage reference. It could also mean in some PWM value cases there can also be a lowered skew of DC value. For example, if

VDD – VOH = 50mV and VOL – VSS = 20mV, then a 50% PWM duty cycle will generate a DC value that is about 37.5mV lower than (VDD-VSS)/2, the DC value halfway between VDD-VSS (AVREFP-AVREFM) full scale analog voltage. Typically, the DC offset error won't be this large though.

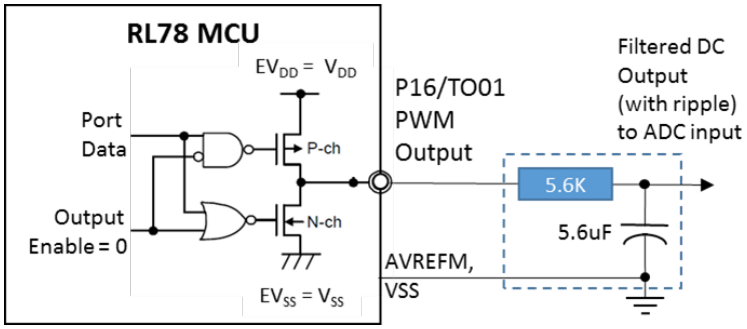


Figure 5. Internal Structure of P16/TO01 PWM output pin

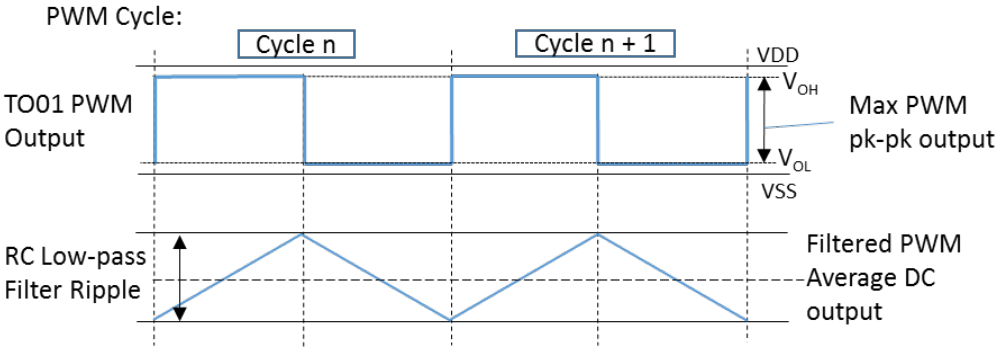


Figure 6. Actual PWM output on P16/TO01 pin

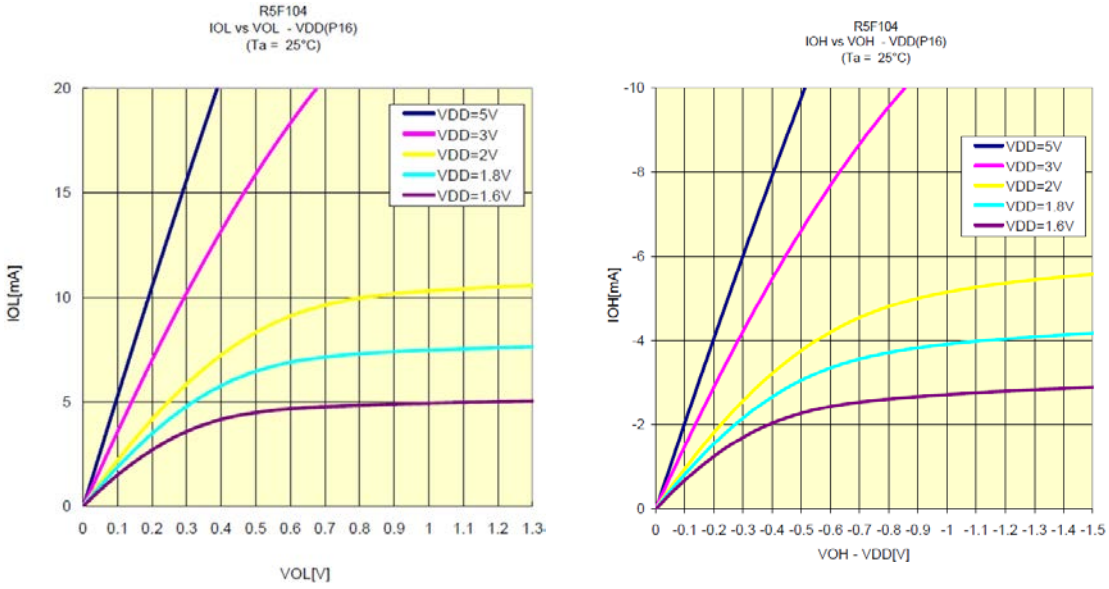


Figure 7: RL78/G14 (R5F104) VOL versus IOL, VOH versus IOH typical curves

In Figure 7, the PWM pin VOL vs IOL and VOH vs IOH curves can be used to evaluate typical PWM DC offsets.
Note: *these curves are typical, not guaranteed specifications.*

For PWM Dithering in closed loop mode, the feedback loop will attempt to compensate for DC offset errors if possible. However, due to DC offset issues at low and high PWM values, it is recommend to operate the PWM dithering in a narrower range than full 100% of 0x000 to 0xFF0 dithered, 12-bit effective DC values. For example, a 5%-95% range or 10%-90% operation range is more likely to achieve accurate results.

7. Limitation of Dynamic range using PWM Dithering method

There are 256 possible output values of the 8-bit PWM, but the dithering requires toggling between 2 adjacent PWM output values. Using a 16 state dithering sequence there are only 15 different dithering sequences between any 2 PWM output states. As can be seen, the Dither adder sequence 0 (in Table 2.) is all zeroes which means no dithering is done.

Otherwise, dithering can only be applied on 255 combinations of 2 adjacent PWM codes, so there are only 4081 possible values:

Maximum range of Dithered "12-bit" output values =

256 (PWM codes 0x00 to 0xFF, no dithering) + 255 x 15 dithering sequences

= 4081 values,

0-4080 decimal (0x000 to 0xFF0)

So when using the PWM Dithering method, the effective 12-bit resolution target setting the max value is limited to the 12-bit code of 0xFF0, which is the same maximum of the 8-bit PWM output codes. Note: Although the PWM dithering output setting is limited to a max target value of 0x0FF0, it is possible that ADC conversion values of 0xFF1 to 0xFFF may still occur, due to DC offsets/errors from ADC conversions.

It would be possible to dither between a duty cycle of 255/256 and constant output state = 1, but the app note SW project limits the max PWM duty cycle to 255/256 (0x00FF), to avoid any PWM timer start/stop issues.

8. Typical monitoring results of PWM dithering Output

The app note Software Project includes an optional UART1 output (provided on RSKRL78G14 board DB-9 connector) to provide real-time monitoring of the PWM dithering output, both before and after RC filtering. UART1 is set for 115.2Kbps, and each 10bit character takes about 86.8uSEC. Each hex value of 3 ASCII characters (plus comma or LF character) in section 8.1 and 8.2 is output at 102.4HZ (9.77mSEC) rate and takes about 347uSEC for 4characters. The UART1 print function was intended for troubleshooting and accuracy measurement, but is not needed to implement the PWM dithering open-loop or closed-loop functions.

8.1 UART output for RC filtered PWM dithering, open-loop mode

When variables `enable_print = 1` and `g_closed_loop = 0` in r_main.c, UART1 will output the sum of 16 consecutive ADC conversion, scaled down to a 12bit Hex value, with no correction on the PWM dithering. The first (single) hex value is the target 12-bit effective dithered PWM DC value. Each line thereafter represents 16 averaged/scaled RC filtered output values (each value is sum of 16 ADC 10-bit conversions). So each line occurs at 64HZ rate (16384HZ sample rate/256 total samples). In this example output, `target_pwm12_value = 0xD1B`. After about 16mSEC startup time, the dithered PWM RC filtered output settles to 0xD19, which is an offset of about -2 steps below the target 0xD1B value in 12bit effective PWM resolution.

```
D1B
D1B,F75,F75,F75,F75,F75,F75,F75,F74,F74,F74,F74,F74,F74,F74,F74
F73,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19
D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19
 (…continues indefinitely)
```

Figure 8.: UART1 print monitoring in Open-loop mode

8.2 UART output for RC filtered PWM dithering, closed-loop mode

When variables `enable_print = 1` and `g_closed_loop` = 1 in r_main.c, UART1 will output the sum of 16 consecutive ADC conversion, scaled down to a 12bit Hex value, with the PWM Dithering value corrected once on each line (156.25mSEC correction rate). The data output is the same format as described in section 8.1 above. In this example, again the `target_pwm12_value = 0xD1B`. However due to the closed-loop ADC measurement and correction, the

dithered PWM RC filtered output settles to the target 0xzD1B value in 12bit effective resolution but takes about 3-4 periods of 156.25mSEC correction to achieve stable output. However, due to system noise, the ADC occasionally sees averaged 12-bit DC values at 0xD1A and 0xD1C, even if no dithering correction is applied.

```
D1B
D1B,F75,F75,F75,F75,F75,F75,F75,F75,F74,F74,F74,F74,F74,F74,F74
F74,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19
D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D19,D1A,D1A,D1A,D1A,D1A
D1A,D1A,D1A,D1A,D1A,D1A,D1A,D1A,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B
D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B
D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B
D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B
D1B,D1B,D1B,D1B,D1B,D1B,D1C,D1C,D1C,D1B,D1B,D1C,D1C,D1C,D1C,D1C
D1C,D1C,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1A,D1A,D1A
D1A,D1A,D1A,D1A,D1A,D1A,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B,D1B
```

(…continues indefinitely)

Figure 9.: UART1 print monitoring in Closed-loop mode

8.3 UART output for measuring PWM output offset errors

When `g_pwmout_test_flag = 1` in r_main.c, and function `pwmout_test_to_adc_input()` is run, the 10bit ADC measures each of 8-bit PWM codes 0x00 to 0xFF, without dithering, for 256 consecutive ADC conversions per PWM output code at the RC filter output (ANI10). Each line evaluates a single 8-bit PWM output code, starting with 0x00 and ending with 0xFF. Each 4 character value corresponds to the sum of 16 consecutive 10-bit ADC conversions, so each value can contain up to 14bit results, not scaled down. Possible output range is 0x0000 to 0x3FFC max (0 to 16380 decimal).
From this example below, it is seen the 8-bit PWM code of 0xFF, when measured 256 times has a 14bit average value of 0x3FBB, or about 1019.68 decimal (or 0x3FC) at 10-bit resolution. This Figure 10. Data is representative but will vary from one RL78/G14 MCU device to another.

```
0010,0010,0010,0010,0010,0010,0010,0010,0010,0010,0010,0010,0010,0010,0010,0010
003C,0040,0040,0040,0048,0048,004E,004F,0050,004E,004F,004E,0050,0050,0050,0050
0071,007B,0080,0080,0080,0080,0080,0081,0081,0086,0084,0086,0089,0089,0087,0089
00B4,00C0,00C0,00C0,00C1,00C1,00C0,00C6,00C4,00C9,00CB,00CB,00CA,00CB,00CA,00C7
       ⋮
3EF0,3EF2,3EF4,3EF3,3EF7,3EF7,3EF9,3EFB,3EF7,3EFC,3EF9,3EFB,3EFE,3EFE,3F04,3EFA
3F37,3F32,3F3B,3F38,3F3A,3F3A,3F3F,3F3C,3F3B,3F3A,3F3F,3F3C,3F45,3F43,3F3D,3F3E
3F6F,3F71,3F72,3F72,3F78,3F78,3F7F,3F7C,3F77,3F7D,3F7A,3F7F,3F7A,3F7B,3F79,3F7D
3FB4,3FB2,3FBA,3FB4,3FBC,3FBA,3FB9,3FBC,3FBB,3FBB,3FBF,3FBF,3FBB,3FBD,3FC2,3FC0
```

(completes after 256 total lines)

Figure 10. UART1 print monitoring for all 256 PWM codes out to ADC input

By taking the above data from `pwmout_test_to_adc_input()` UART1 data output averaging and scaling down to 10-bit results equivalent resolution, the average RC-filtered PWM DC output error can be visualized. The errors tend to be larger toward the middle ranges of PWM duty cycle. This is probably because the RC filter charge and discharge currents are larger in the middle ranges (50%/50%) of PWM, and therefore has larger VOH and VOL offsets.

Note: *Data in Figure 11 is typical, not guaranteed.*

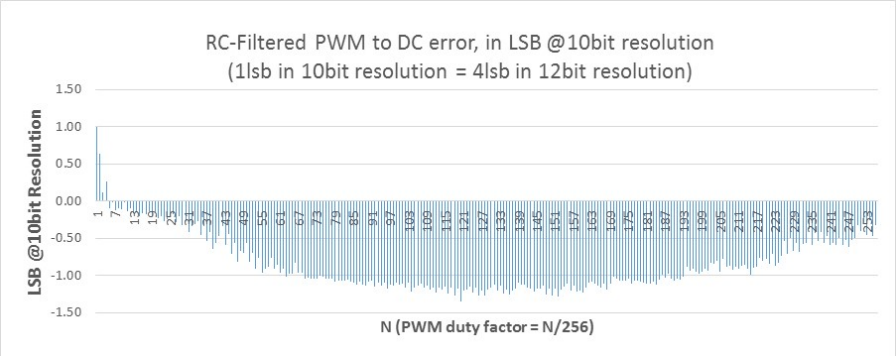


Figure 11. Typical RC-filtered PWM with no dithering

9. PWM Dithering increase/decrease, closed-loop algorithm

In the PWM Dithering close-loop mode, the sum of the last 256 ADC conversions (10bits x 256 = 18bit result) is scaled down and rounded off to a 12bit effective result every 156.25mSEC. Then the 12bit actual (averaged) result is compared to the User settable 12-bit target_pwm12_value. If target and measured values are equal, then no PWM dithering correction is made. If the actual measured value is less than the target value, the dithering factor is increased by one bit value in 12-bit resolution. If the actual measured value is greater than the target value, the dithering factor is decreased by one bit value (12-bit resolution). Care is taken not to produce a Dithering base value and factor that is out of range.

Depending on the previous PWM output Base Value, either the Base Value, the Dithering factor, or both values will need to be updated into the 16word RAM table transferred to TAU timer channel1 (duty cycle compare register (TDR01) by DTC data transfers.

9.1 PWM Dithering Increase

For Dithering increases, a special case occurs when the previous PWM Dithering value is 0xFF0, and no increase is allowed, since Dithering can only occur between PWM output codes 0xFE and 0xFF to produce 12bit PWM effective codes of 0xFE0 to 0xFEF. A constant PWM output code of 0xFF represents 0xFF0 in 12-bit resolution and no further increase is allowed. Of course, there could be some DC offset due to VOH output level being lower than VDD = AVREFP, when PWM output is 0xFF code, resulting in the 12bit effective DC value slightly less than 0xFF0.

9.2 PWM Dithering Decrease

For Dithering decreases, a special case occurs when the previous PWM Dithering value is 0x000, and no decrease is possible, since Dithering can only occur between PWM output codes 0x00 and 0x01 to produce 12bit PWM effective codes of 0x000 to 0x00F. A constant PWM output code of 0x00 represents 0x000 in 12-bit resolution and no further decrease is possible.

10. HW implementation for Sample SW project

The PWM dithering application note Sample SW project was developed on an RSKRL78G14 board, populated with 100pin RL78/G14 (device R5F104PJ). This board layout was designed to maximize access to all the MCU pins, and provide a preliminary prototyping platform for customer RL78/G14 designs. However, the printed circuit board layout may not be optimum for lowest Analog noise riding on the RL78 power supply and ground lines. RSKRL78G14 board wiring for the Sample SW project is shown in Figure 12 and Figure 13.

In a customer-designed board, care should be taken to minimize ground loops and power supply line impedance to the Analog voltage reference pins. For the RSKRL78G14 board, connector J4 is the shortest, most convenient place to wire up the ADC lines and analog reference pins on RL78/G14 MCU ports P2 and P15. ADC analog reference pins AVREFP and AVREFM are connected to VDD and VSS/Ground respectively, by connecting to connector J12.

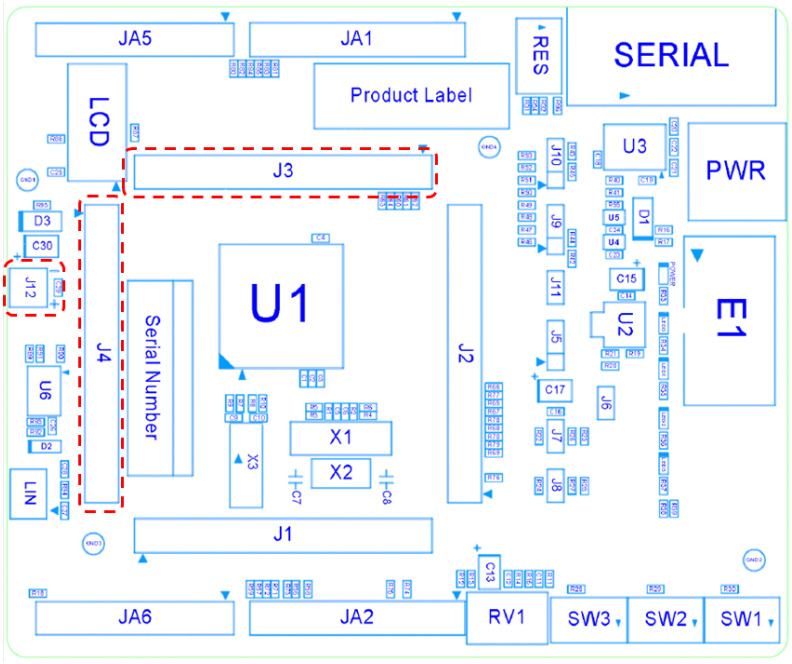
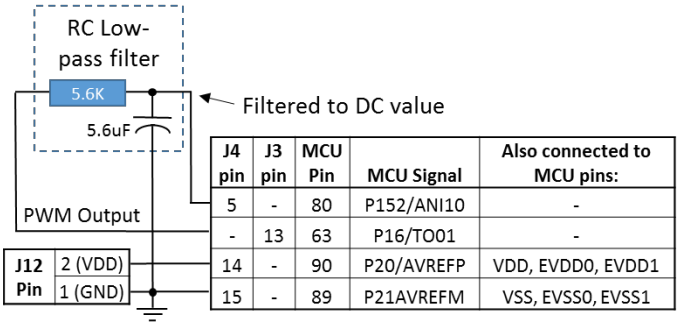


Figure 12: Standard RSKRL78G14 board (part #R0K50104PC000BE)

In wiring diagram Figure 13, ANI10 ADC input is used for checking/correcting the PWM dithering Low-pass filtered output value.



J4 pin	J3 pin	MCU Pin	MCU Signal	Also connected to MCU pins:
5	-	80	P152/ANI10	-
-	13	63	P16/TO01	-
14	-	90	P20/AVREFP	VDD, EVDD0, EVDD1
15	-	89	P21AVREFM	VSS, EVSS0, EVSS1

Figure 13: Recommended wiring for PWM dithering Sample SW project using RSKRL78G14 board

11. Documents for Reference

User's Manual:
RL78/G14 User's Manual: Hardware Rev.3.30 (R01UH0200EJ0330)
RL78 Family User's Manual: Software Rev.2.00 (R01US0015EJ0200)
RL78 Family DAC Dithering Rev. 1.00 (R01AN3795EJ100)

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	16Jun2017		First edition

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   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

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(Rev.3.0-1 November 2016)

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