RZ/V2H, V2N

AWO Example Program Startup Guide

Introduction

This material shows how to set up and invoke AWO Example Program for RZ/V2H and RZ/V2N.

Target Device

RZ/V2H, V2N

Contents

1. Specifications

1.1 Deliverables

Table 1-1. Deliverables of RZ/V AWO Example Project

Deliverables	File name	Description
RZ/V2H Cortex®-M33 AWO example project	freertos_w_awo_rzv2h_evk.zip	AWO example project for RZ/V2H.
RZ/V2N Cortex®-M33 AWO example project	freertos_w_awo_rzv2n_evk.zip	AWO example project for RZ/V2N.
RZ/V AWO Example Program Start-up Guide	r01an7723ej0100-rzv2h-rzv2n-awo-example-program-startup-guide.pdf	This material.

2. Proven Environment

Environments	Contents and versions
Integrated Development Environment	e2 studio 2025-01
JTAG Emulator	Segger J-Link 7.96e
Dependent Software	• RZ/V2H AI SDK v5.00 • RZ/V Flexible Software Package (FSP) v3.1.0

3. AWO Example Program Setup for RZ/V2H

3.1 Setup of Cortex-A55 software related stuff

1. Carry out Step 1, Step 2, and 1-8 of Step 3 stated in **How to build RZ/V2H AI SDK Source Code** showcased at AI Applications and AI SDK of RZ/V series.
2. Download Multi-OS Package (r01an7254ej0300-rzv-multi-os-pkg.zip) to a working directory and run the commands stated below:

```
$ cd ${YOCTO_WORK}
$ unzip <Multi-OS Dir>/r01an7254ej0300-rzv-multi-os-pkg.zip
$ tar zxvf r01an7254ej0300-rzv-multi-os-pkg/meta-rz-features_multi-os_v3.0.0.tar.gz
```

Here, <Multi-OS Dir> indicates the path to the directory where Multi-OS Package is placed.

3. Uncomment the following lines in **meta-rz-features/meta-rz-multi-os/meta-rzv2h/conf/layer.conf**.

```
MACHINE_FEATURES_append = " RZV2H_CM33_BOOT"
#MACHINE_FEATURES_append = " SRAM_REGION_ACCESS"
#MACHINE_FEATURES_append = " CM33_FIRMWARE_LOAD"
#MACHINE_FEATURES_append = " CA55_CPU_CLOCKUP"
```

   Be sure NOT to uncomment the above-mentioned 3rd and 4th line when CM33 cold boot support is enabled.

4. Add the layer for Multi-OS Package.

```
$ cd build
$ bitbake-layers add-layer ../meta-rz-features/meta-rz-multi-os/meta-rzv2h
```

5. Continue to carry out the remaining procedures stated in **Step 3** of **How to build RZ/V2H AI SDK Source Code**.

3.2 Deployment of CA55 Build Artifacts

1. Connect CN12 of RZ/V2H EVK with Host PC and established serial port connection.
2. Configure DSW1-4 and DSW1-5 of RZ/V2H EVK as OFF and ON respectively to specify boot mode as SCIF download mode.
3. Turn on RZ/V2H EVK. Then, the following message is shown on your terminal:

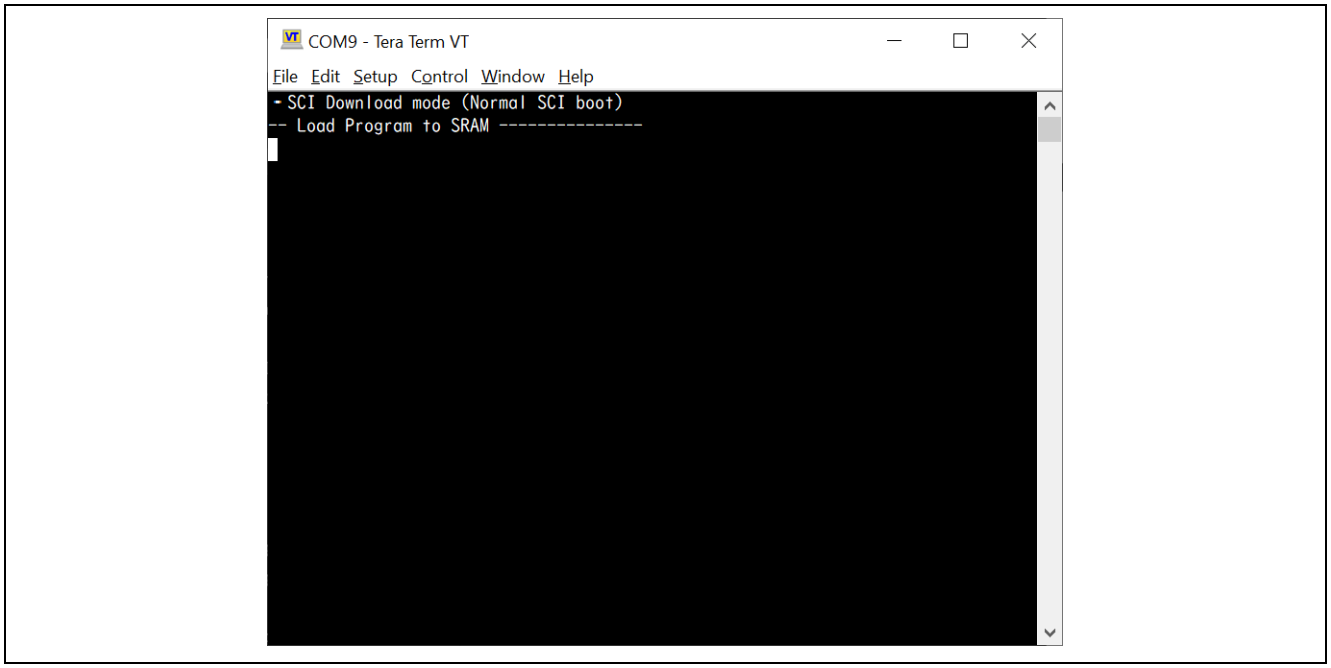

Figure 5-3. SCIF Download mode

4. Send **Flash_Writer_SCIF_RZV2H_DEV_INTERNAL_MEMORY.mot** to RZ/V2H EVK via terminal software. If it's successfully transferred, the following message is shown on your terminal:

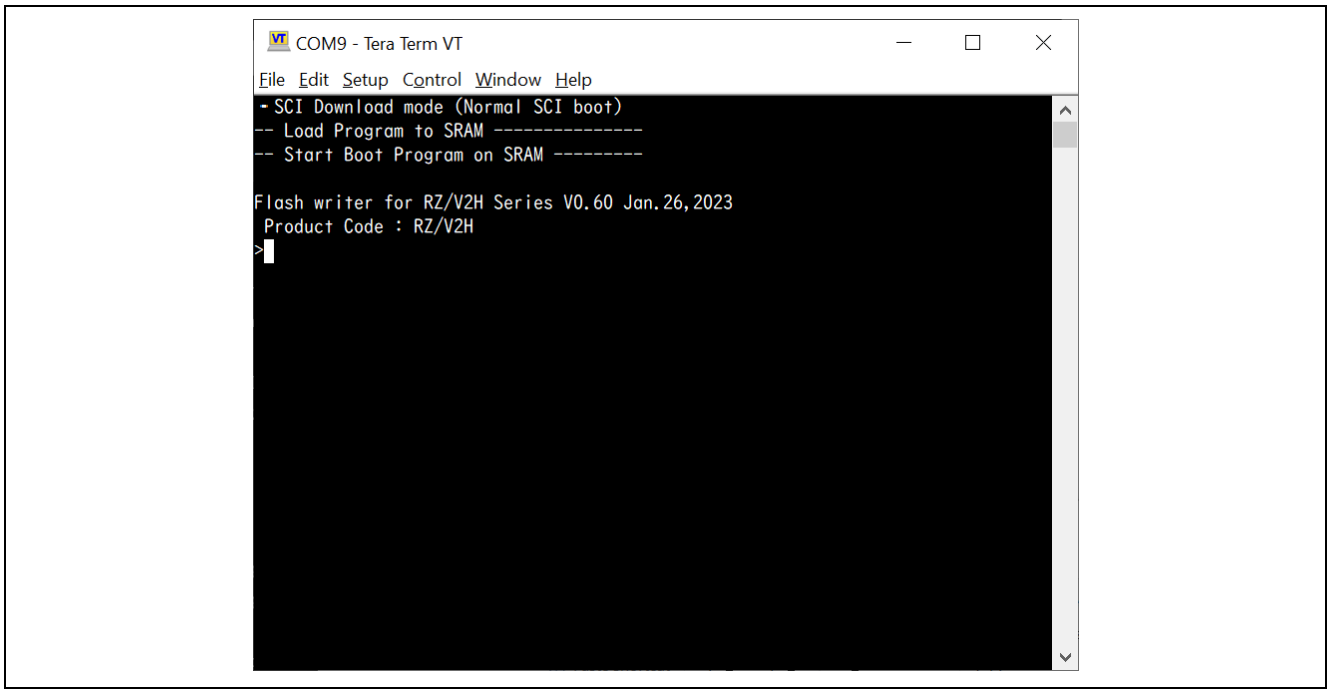

Figure 5-4. Flash Writer invocation

5. Program **bl2_bp_spi-rzv2h-evk-ver1.srec** with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'8101E00

===== Please Input Qspi Save Address ===
  Please Input : H'100000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00100000
SpiFlashMemory End Address  : H'00136D17
============================================================
```

6. Program **fip-rzv2h-evk-ver1.srec** with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'00000

===== Please Input Qspi Save Address ===
  Please Input : H'280000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00280000
SpiFlashMemory End Address  : H'0033C2BE
============================================================
```

4. AWO Example Program Setup for RZ/V2N

4.1 Setup of Cortex-A55 software related stuff

1. Carry out Step 1, Step 2, and 1-8 of Step 3 stated in **How to build RZ/V2N AI SDK Source Code** showcased at AI Applications and AI SDK of RZ/V series.
2. Download Multi-OS Package (r01an7254ej0300-rzv-multi-os-pkg.zip) to a working directory and run the commands stated below:

```
$ cd ${YOCTO_WORK}
$ unzip <Multi-OS Dir>/r01an7254ej0300-rzv-multi-os-pkg.zip
$ tar zxvf r01an7254ej0300-rzv-multi-os-pkg/meta-rz-features_multi-os_v3.0.0.tar.gz
```

Here, <Multi-OS Dir> indicates the path to the directory where Multi-OS Package is placed.

3. Uncomment the following lines in **meta-rz-features/meta-rz-multi-os/meta-rzv2n/conf/layer.conf**.

```
MACHINE_FEATURES_append = " RZV2N_CM33_BOOT"
#MACHINE_FEATURES_append = " SRAM_REGION_ACCESS"
#MACHINE_FEATURES_append = " CM33_FIRMWARE_LOAD"
#MACHINE_FEATURES_append = " CA55_CPU_CLOCKUP"
```

Be sure NOT to uncomment the above-mentioned 3rd and 4th line when CM33 cold boot support is enabled.

4. Add the layer for Multi-OS Package.

```
$ cd build
$ bitbake-layers add-layer ../meta-rz-features/meta-rz-multi-os/meta-rzv2n
```

5. Continue to carry out the remaining procedures stated in **Step 3** of **How to build RZ/V2N AI SDK Source Code**.

4.2 Deployment of CA55 Build Artifacts

1. Connect CN12 of RZ/V2N EVK with Host PC and established serial port connection.
2. Configure DSW1-4 and DSW1-5 of RZ/V2N EVK as OFF and ON respectively to specify boot mode as SCIF download mode.
3. Turn on RZ/V2N EVK. Then, the following message is shown on your terminal:

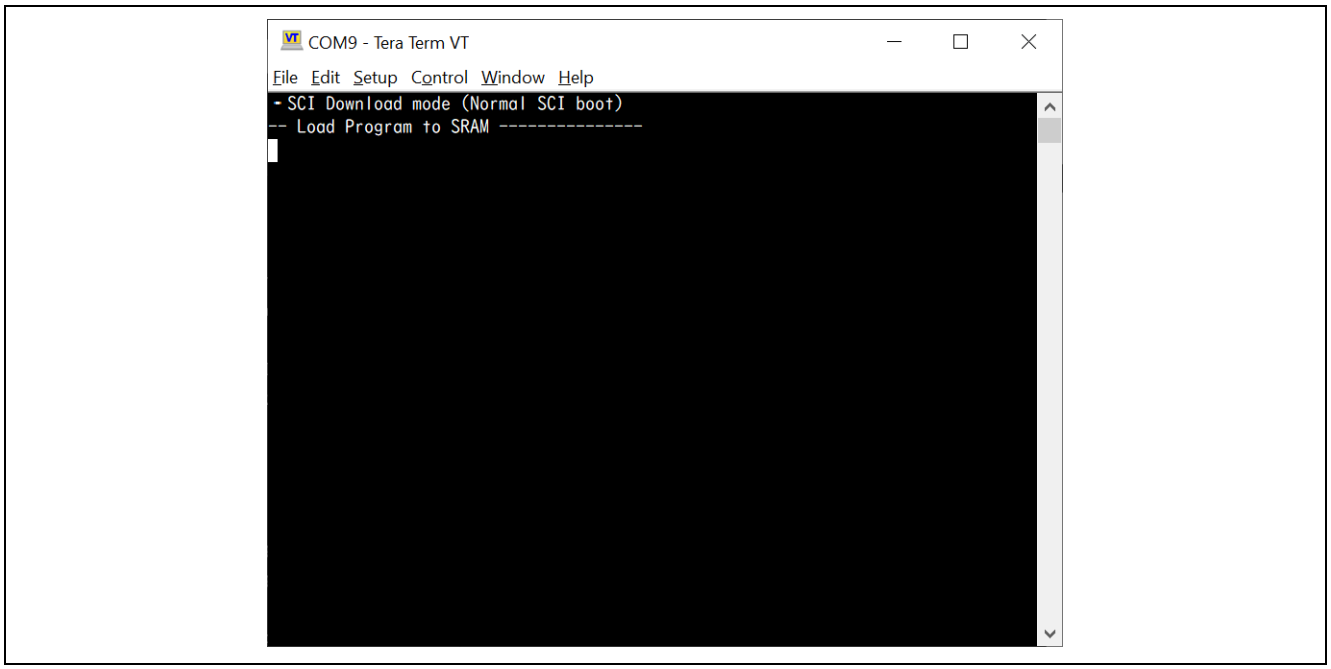

Figure 5-3. SCIF Download mode

4. Send **Flash_Writer_SCIF_RZV2N_DEV_INTERNAL_MEMORY.mot** to RZ/V2N EVK via terminal software. If it's successfully transferred, the following message is shown on your terminal:

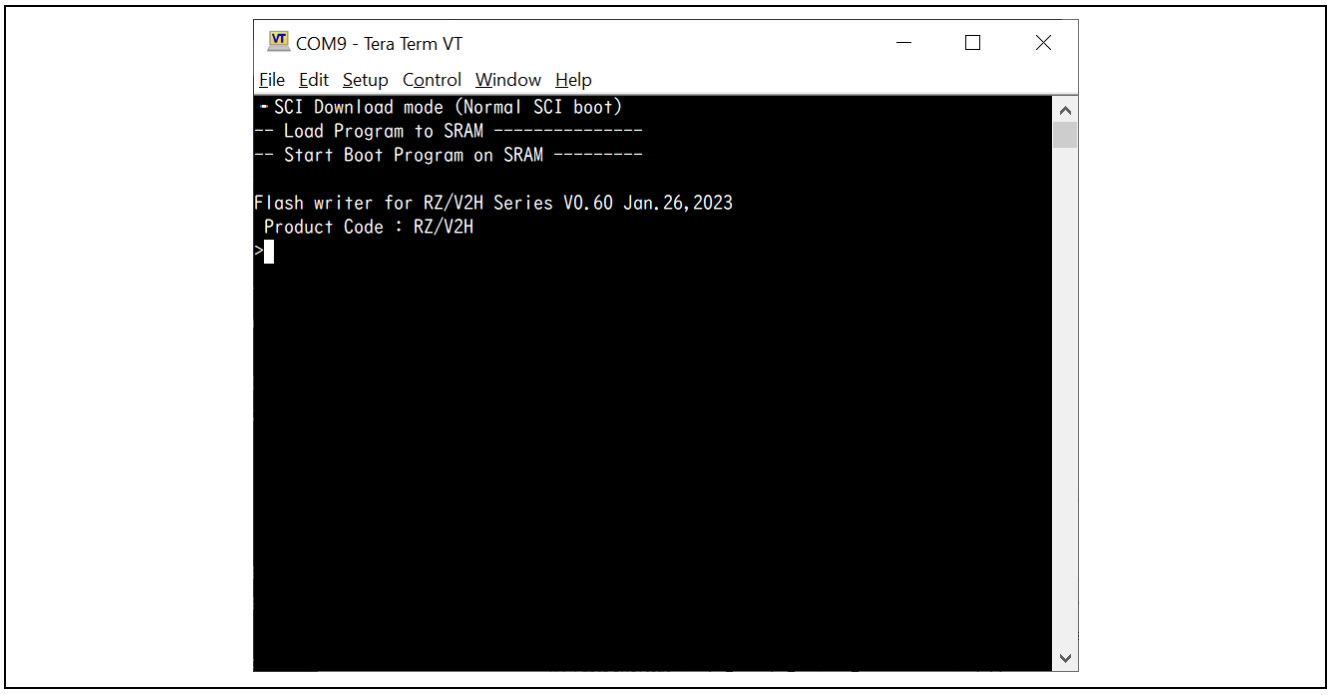

Figure 5-4. Flash Writer invocation

5. Program **bl2_bp_spi-rzv2n-evk.srec** with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'8101E00

===== Please Input Qspi Save Address ===
  Please Input : H'100000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00100000
SpiFlashMemory End Address  : H'00136D17
============================================================
```

6. Program **fip-rzv2n-evk.srec** with Flash Writer as shown below:

```
xls2
===== Qspi writing of RZ/G2 Board Command =============
Load Program to Spiflash
Writes to any of SPI address.
Program size & Qspi Save Address
===== Please Input Program Top Address ============
  Please Input : H'00000

===== Please Input Qspi Save Address ===
  Please Input : H'280000
please send ! ('.' & CR stop load)
Erase SPI Flash memory...
Erase Completed
Write to SPI Flash memory.
======= Qspi  Save Information  =================
SpiFlashMemory Stat Address : H'00280000
SpiFlashMemory End Address  : H'0033C2BE
============================================================
```

4.3 Setup of CM33 software related stuff

1. Extract **r01an7254ej0300-rzv-multi-os-pkg.zip** on your development PC.
2. Extract either of **freertos_w_awo_rzv2h_evk.zip** or **freertos_w_awo_rzv2n_evk.zip** included in **r01an7254ej0300-rzv-multi-os-pkg**.
3. Invoke e^2 studio 2025-01 and click **File** > **Import**.
4. Double-click **General** and select **Existing Projects into Workspace** as shown in Figure 4-1:

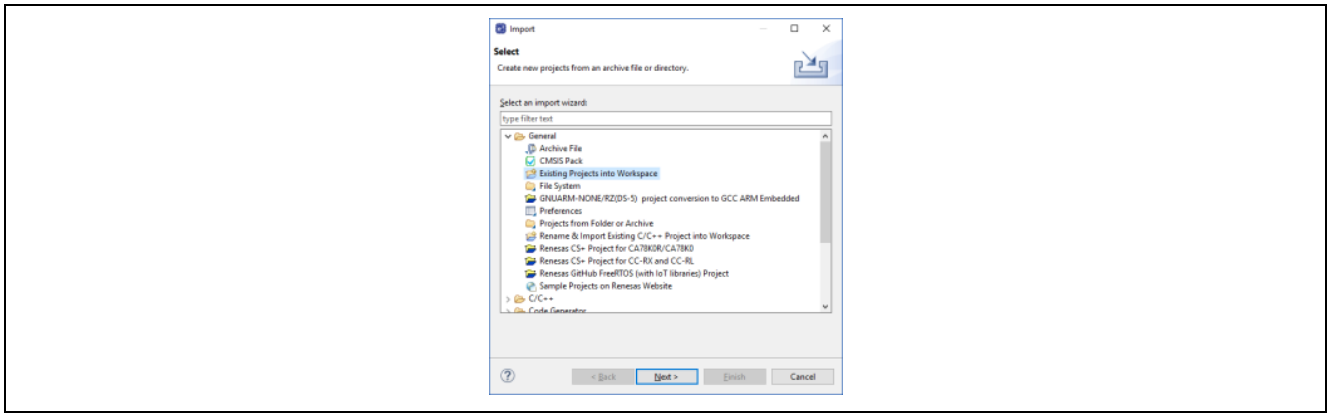

Figure 3-1. Import sample project (1)

5. Input the path to the directory of sample project you would like to import to **Select root directory**, press **Enter** key and click **Finish** button.

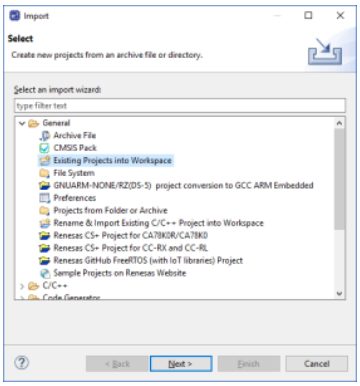

Figure 3-2. Import sample project (2)

6. Open **configurator.xml** in the project and choose **BSP** tab.
7. Configure **Launch CA55(core0)** as Enabled. Also, enabled **Clock up for CA55** if you would like to configure operational frequency of CA55 as 1.8GHz.
8. Click **Generate Project Content** to reflect the changes to your project.

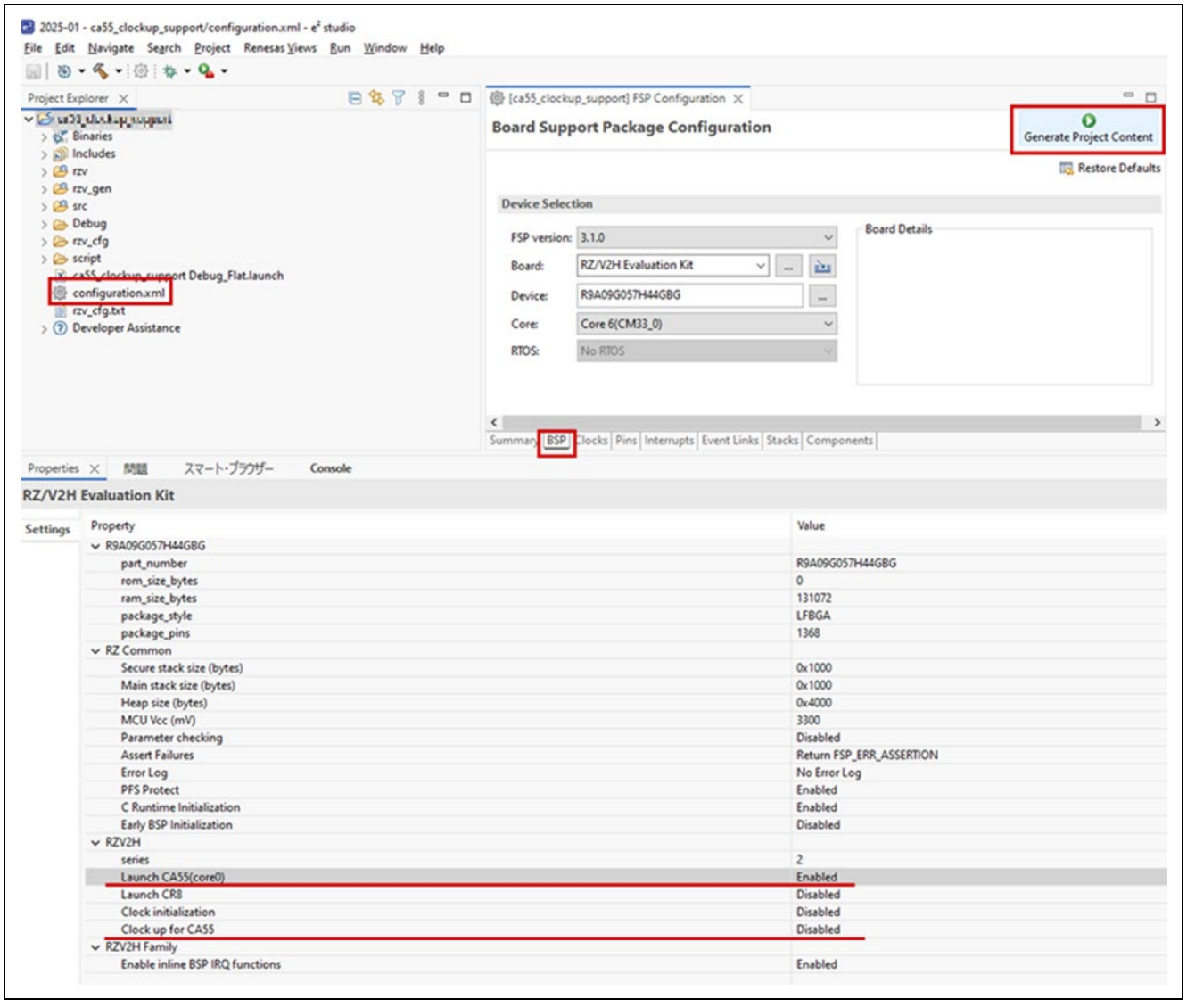

Figure 3-3. CM33 project setting for CM33 cold boot

9. Build the project from **Choose Project** > **Build Project**.
10. If building project is successfully completed, build artifacts as listed below should be generated in **Debug** or **Release** directory of the project you imported in accordance with the active Build Configuration.
    - freertos_w_awo_<cpu>_evk.elf

    Hereafter, <cpu> should be either rzv2h or rzv2n.

4.4 AWO Example Program Invocation

1. Click **Run** > **Debug Configurations...** , expand **Renesas GDB Hardware Debugging** and choose **freertos_w_awo_<cpu>_evk Debug_Flat**.

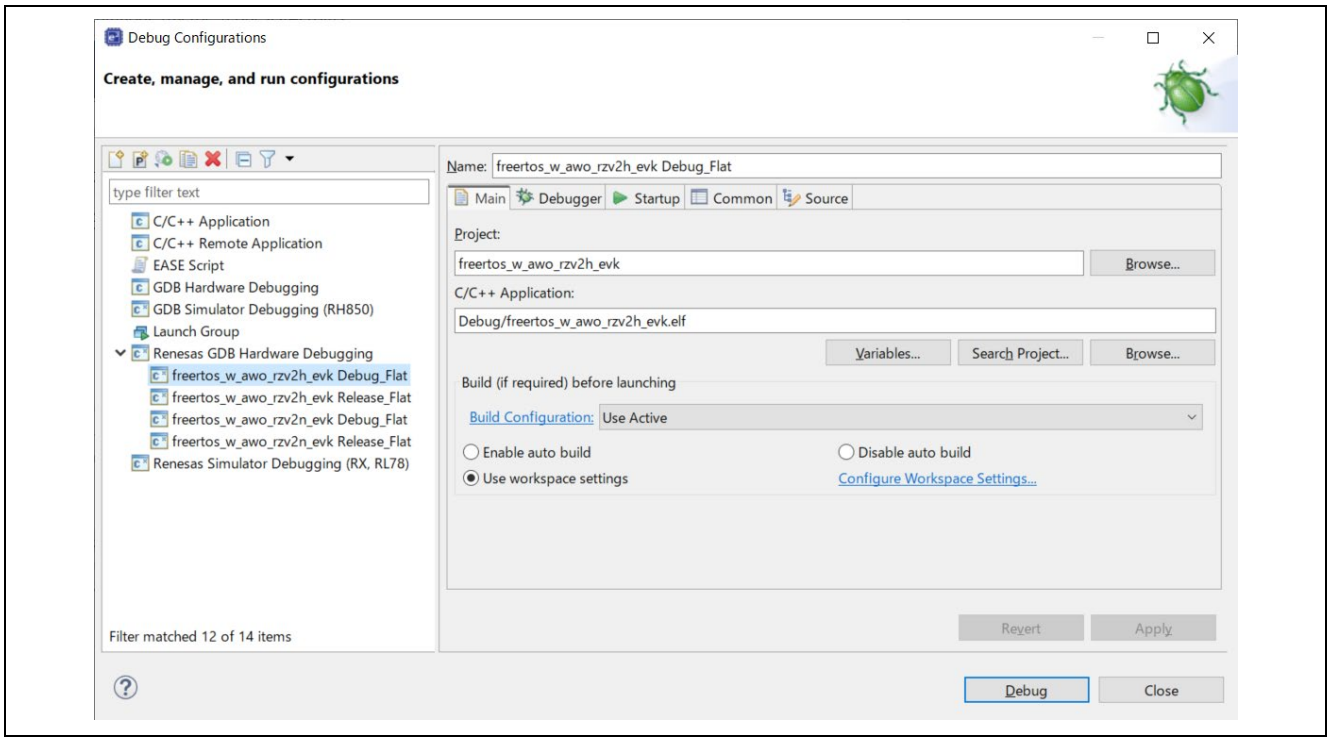

Figure 3-4. Debug Configuration Launch

2. Click **Debug** button as shown below:

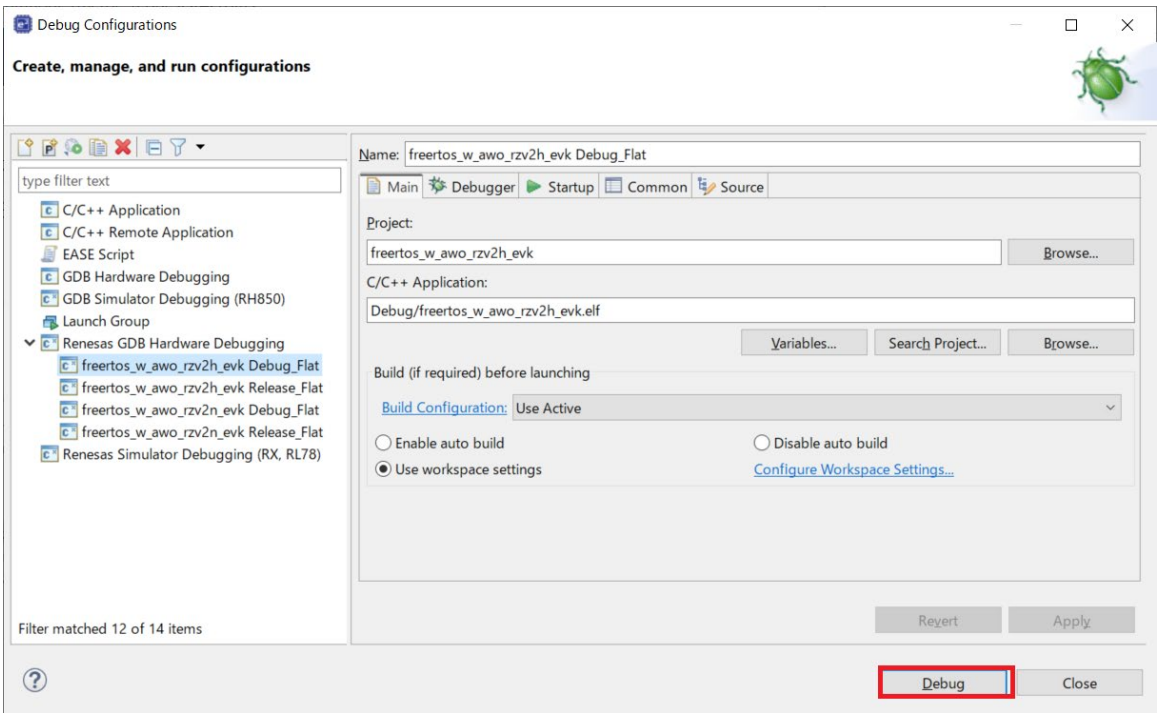

Figure 3-8. Debug Perspective Launch (1)

Note that DSW1-4, 5 and 7 of RZ/V2H EVK or RZ/V2N EVK must be specified as OFF, OFF, ON, respectively beforehand.

If the following **Confirm Perspective Switch** window appears, press **Switch** to go ahead.

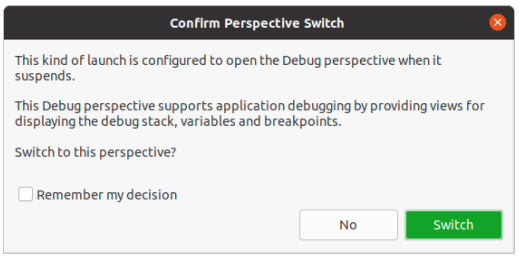

Figure 3-10. Debug Perspective Launch (3)

4. When **Debug Perspective** is opened, Program Counter (PC) should be located as shown in Figure 3-11. Then, continue the program to push the button shown in Figure 3-11.

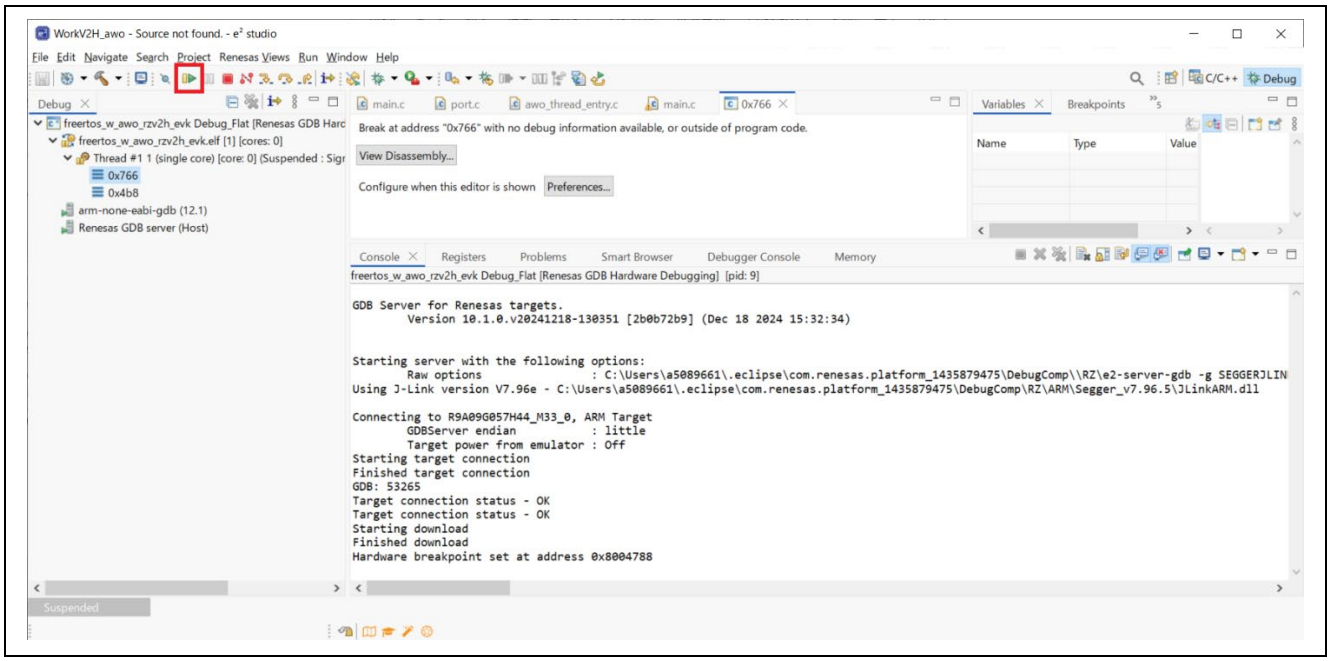

Figure 3-11. How to start to AWO Example Program (1)

5. PC should be stopped at the top of **main** function. Then, click the same button in the previous step to continue.

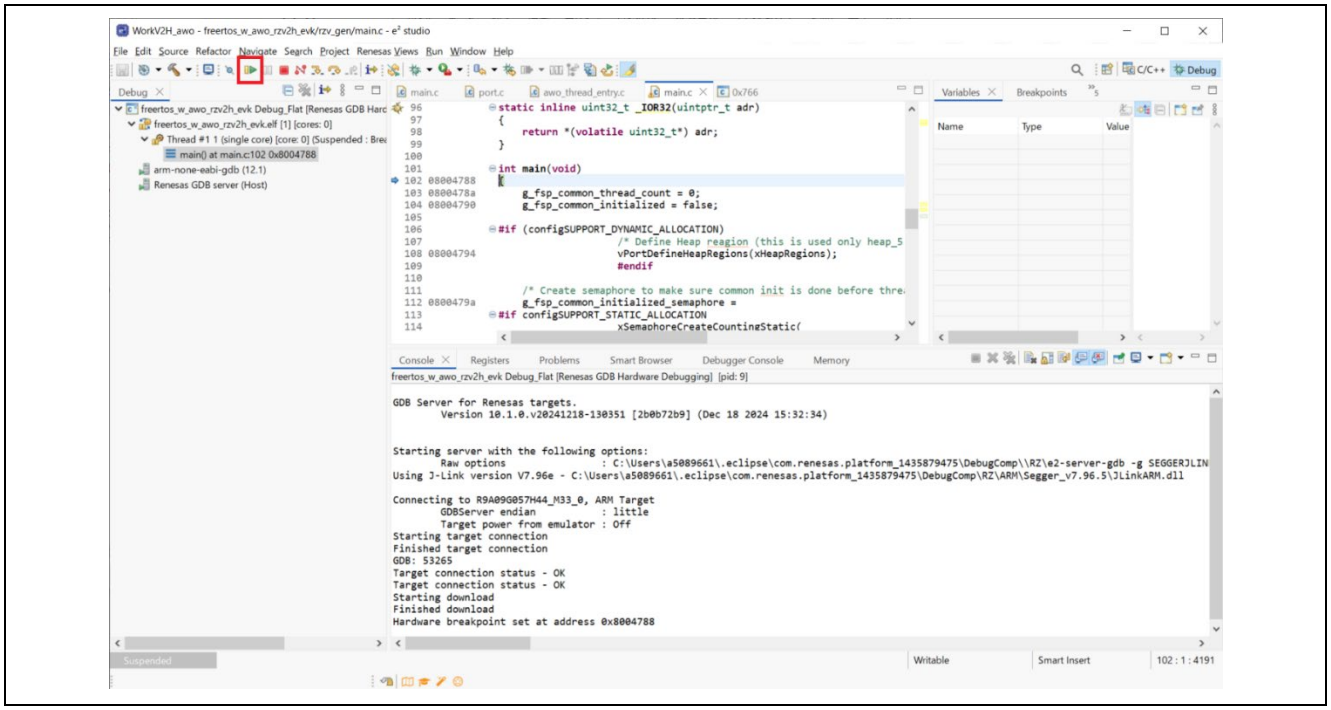

Figure 3-12. How to start to AWO Example Program (2)

CM33 AWO example program now starts, loads CA55 build artifacts and kick CA55.

5. AWO Example Program Invocation

This chapter describes how AWO Example Program works.

1. Boot up Linux kernel.
2. Login as **root**.

```
rzv2h-evk-ver1 login: root
```

3. Load **AWO Notifier** which notifies CM33 that CA55 becomes ready to enter AWO.

```
root@rzv2h-evk-ver1:~# insmod ./awo-notifier.ko
```

4. Issue shutdown command as shown below:

```
root@rzv2h-evk-ver1:~# shutdown -h now
```

   While CA55 is being shut down, AWO Notifier fires an external interrupt.
5. Once CM33 AWO example project detects the external interrupt, RZ/V2H or RZ/V2N is configured as AWO. Then, the following message is shown on your console:

```
CM33: AWO request accept.
Hit any key to go to ALLON mode.
```

6. When hitting any key on your development PC, CM33 AWO example project configures RZ/V2H or RZ/V2N as ALLON, load BL2 of TrustedFirmware-A to internal SRAM and kick CA55 for restart.

```
CM33: Set GreenPAK to ALLON
```

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar 11, 2025	-	First edition.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
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(Rev.5.0-1 October 2020)

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