VersaClock® 7 (VC7) Internal Capacitance Configuration

This document describes how the internal capacitance is configured within a VersaClock® 7 (VC7) device using the Renesas IC Toolbox software (RICBox). For more information about RICBox, download the *Renesas IC Toolbox Software Manual* from the Renesas IC Toolbox (RICBox) page.

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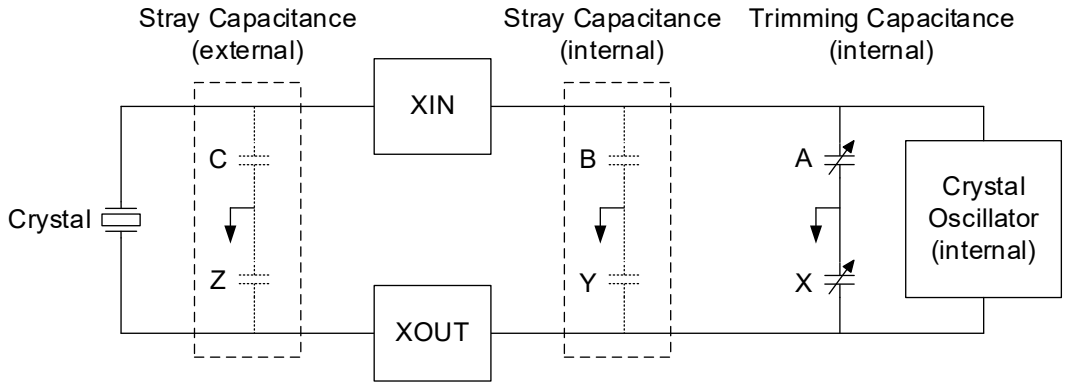
1. Calculating Load Capacitance

The load capacitance (C_L) on the crystal can be modeled as follows:



The external stray capacitance (denoted by C and Z) is made up of the parasitic capacitance from the PCB trace and any installed load capacitors. The internal stray capacitance (denoted by B and Y) consists of the package pins and bond wires. For VC7, this value is fixed at 8.2pF. The trimming capacitance (denoted by A and X) can be set by **en_cap_x1** and **en_cap_x2** register fields. The range is 0pF to 26.46pF in 0.42pF steps.

To calculate the load capacitance, note that the external stray, internal stray, and trimming capacitance are in parallel per leg. Next, the effective capacitance on XIN and XOUT are in series. Therefore, the load capacitance can be approximated with:

$$\frac{1}{C_L} = \frac{1}{A+B+C} + \frac{1}{X+Y+Z}$$

If each respective capacitance is allowed to be equal, or A = X, B = Y, and C = Z then:

$$\frac{1}{C_L} = \frac{2}{A+B+C}$$

Solving for A:

$$C_L = \frac{A+B+C}{2}$$

$$2C_L = A+B+C$$

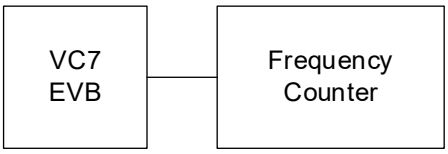
$$A = 2C_L - B - C$$

Knowing the goal C_L capacitance of the crystal, the expected trimming (A and X) capacitance can be calculated. The internal stray (B and Y) capacitance are fixed at 8.2pF. The external stray (C and Z) capacitance can be set in RICBox. The name of the fields are **xin_pcb_capacitance** and **xout_pcb_capacitance**. For the RC21012 EVB, the PCB trace capacitance is about 2.5pF and for the RC21008 EVB, the PCB trace capacitance is about 1.7pF. After these fields are set, the trim value is calculated (as shown below) and the nearest trim setting is chosen by the VC7 plugin.

$$Trim = int\left(\frac{2C_L - 8.2pF - 2.5pF}{0.42pF}\right)$$

2. Bench Setup for Trimming

Use the RC21008A/RC31008A Evaluation Kit (EVK) and Frequency Counter equipment for the trimming measurement. The RC21012A/RC31012A EVK may be used as well.



2.1 Evaluation Board (EVB) Setup

The RC21008 EVB ships with a 50MHz crystal installed. The C_L required for this crystal is 8pF. Ensure that the **XIN_DIF_INA_S** and **DIF_INA#_S** traces are not connected to a VC7 device via R11 and R19. Also, ensure C5 and C6 are not populated. Any extra stubs will add stray capacitance to XIN/XOUT. For more information, refer to the schematics in the RC210xxA/RC310xxA Evaluation Board Manual.

2.2 Frequency Counter Setup

Setup the counter to accept 50MHz. If the VC7 EVB has AC-coupled outputs, adjust the counter to enable 50Ω termination.

2.3 RICBox Installation

For more information on installing RICBox software for VC7, see the Renesas IC Toolbox Software Manual.

2.4 Trimming the Crystal

Use OUT10 to measure the crystal signal as it can be muxed out. Start RICBox and create a new project. Choose the product variant that matches the unit on the EVB. During the wizard phase, just click Finish. Next, view the block diagram. If your crystal is different from the default value, then update the XIN_REFIN frequency (see Figure 1).

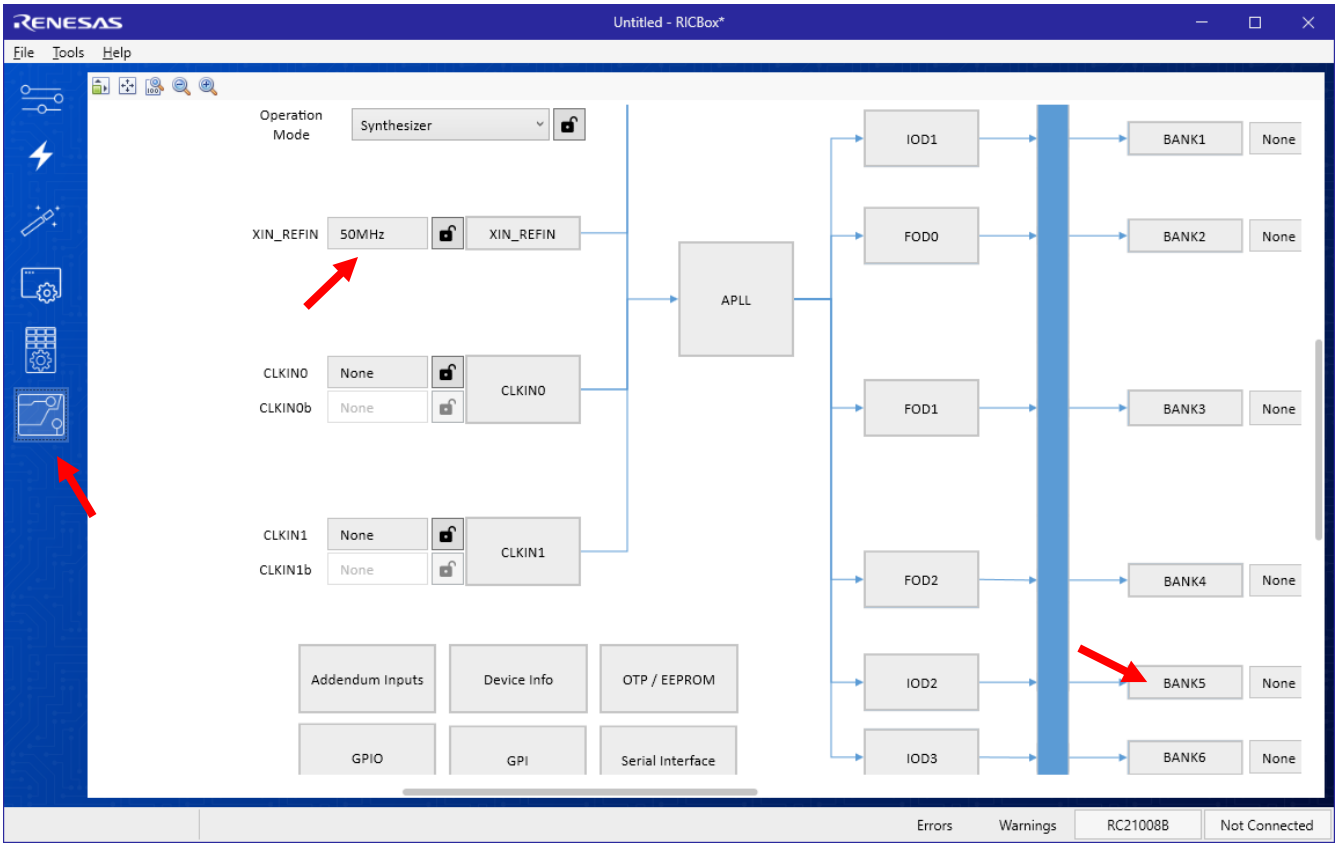


Figure 1. Block Diagram Window

From the window above, click on **Bank5** to bring up the BANK5 sub-diagram window (see Figure 2). For the frequency source, choose **XIN_REFIN.** Set the *Desired Output Frequency* field to match the crystal frequency.

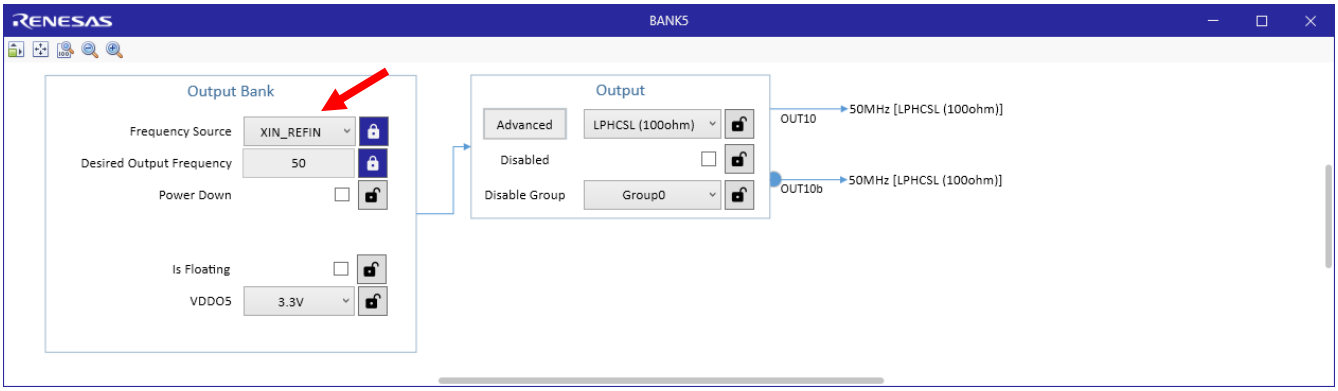


Figure 2. BANK5 Sub-Diagram Window

Connect and program VC7. Use the frequency counter to measure the crystal frequency. Go back to the main block diagram and click on the **XIN_REFIN** block to bring up its configuration window (see Figure 3). Adjust the *Load Capacitance (pf)* until the measured frequency by the counter is closest to your expected crystal frequency. Use increments of 0.1 (pF) for best results. After changing the load capacitance value, the changes are effective immediately.

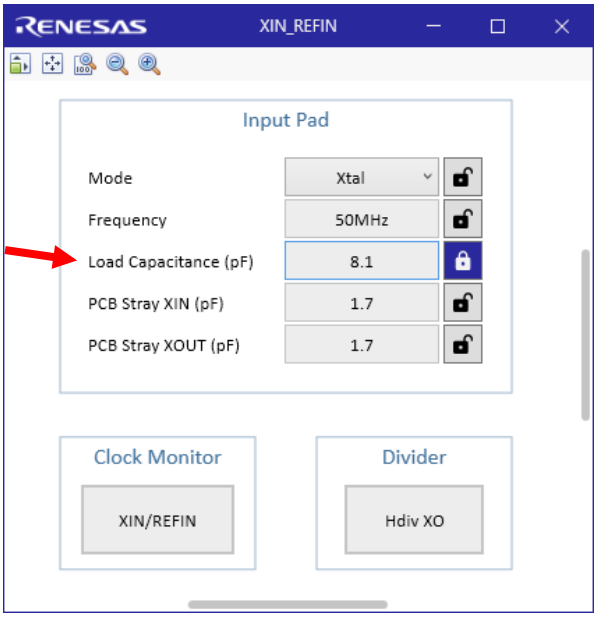


Figure 3. XIN_REFIN Configuration Window

You can also use the RICBox CLI (Command Line Interface). To read/write the **XO_CNFG** register use:

read TOP.XO.XO_CNFG

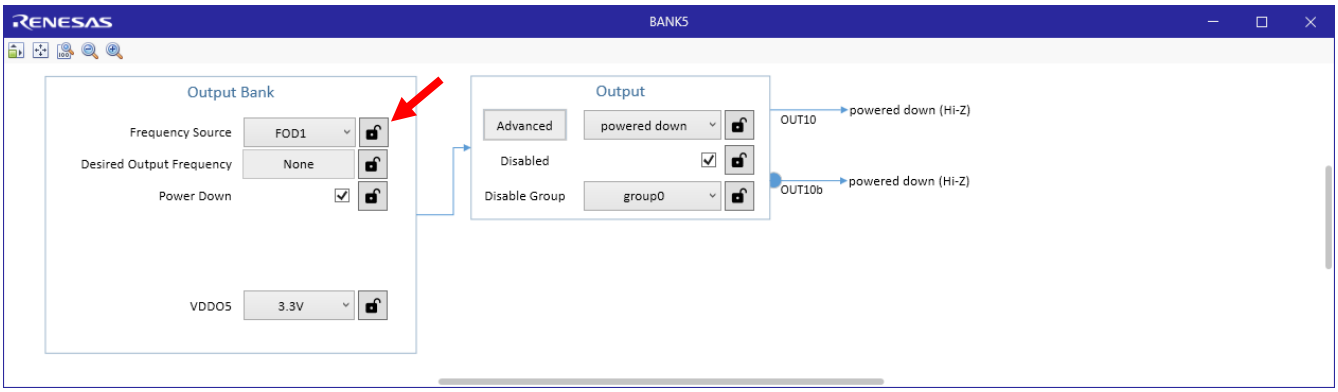
write TOP.XO.XO_CNFG 0x205D1D45

RENESAS RICBox CLI

```
> read TOP.XO.XO_CNFG
TOP.XO.XO_CNFG = 0x20682845
BitSet                Location       Value
--------------------  -------------  ------------------------------------------------------
xo_ib_h_div_setb      0x2C[29]       0x1
xo_ib_h_div           0x2C[28:24]    0x00
en_gain               0x2C[23:22]    0x1 (1 Amplifier)
en_cap_x2             0x2C[21:16]    0x28 (16.80pF)
xo_buff_dis           0x2C[14]       0x0 (XO buffer enable is controlled by the hardware)
en_cap_x1             0x2C[13:8]     0x28 (16.80pF)
xo_res                0x2C[6:4]      0x4
xo_ib_en_dc_bias      0x2C[3]        0x0 (Disable internal DC bias)
sel_ib_xo             0x2C[2]        0x1 (XO)
xo_ib_cmos_sel        0x2C[1]        0x0 (Differential input is selected)
xo_ib_p_n_diff_sel    0x2C[0]        0x1 (Enable NMOS input pair)
> write TOP.XO.XO_CNFG 0x205D1D45
Wrote 4 byte(s) to offset 0x2C
> read TOP.XO.XO_CNFG
TOP.XO.XO_CNFG = 0x205D1D45
BitSet                Location       Value
--------------------  -------------  ------------------------------------------------------
xo_ib_h_div_setb      0x2C[29]       0x1
xo_ib_h_div           0x2C[28:24]    0x00
en_gain               0x2C[23:22]    0x1 (1 Amplifier)
en_cap_x2             0x2C[21:16]    0x1D (12.18pF)
xo_buff_dis           0x2C[14]       0x0 (XO buffer enable is controlled by the hardware)
en_cap_x1             0x2C[13:8]     0x1D (12.18pF)
xo_res                0x2C[6:4]      0x4
xo_ib_en_dc_bias      0x2C[3]        0x0 (Disable internal DC bias)
sel_ib_xo             0x2C[2]        0x1 (XO)
xo_ib_cmos_sel        0x2C[1]        0x0 (Differential input is selected)
xo_ib_p_n_diff_sel    0x2C[0]        0x1 (Enable NMOS input pair)
```

Figure 4. RICBox CLI Window

Close the **XIN_REFIN** configuration window and go back to the BANK5 sub-diagram window (see below). Click on the blue lock icons to reset the fields back to the GUI defaults.



The onboard crystal is now trimmed.

3. Revision History

Revision	Date	Description
1.00	May 31, 2024	Initial release.

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