Wafer-level Chip Scale Package (WLCSP) Implementation Guidelines

This application note generically describes typical Wafer Level Chip Scale Packages (WLCSP) and serves only as a guideline to help develop a workable solution. Device specific information is not provided. Actual experience and development efforts are still required to optimize the process per individual device and application requirements.

Contents

1. Introduction

This application note outlines the basic guidelines to use the Renesas Wafer Level Chip Scale Package (WLCSP) to ensure consistent Printed Circuit Board (PCB) assembly necessary to achieve high yield and reliability. The recommendations are proven to work under the given conditions. However, variances in the manufacturing equipment, processes and PCB designs may lead to a combination where other process parameters yield superior performance. It is also possible that a significant deviation from the recommended guidelines show inferior yield and reliability performance. Reference data is provided for these packages with respect to MSL ratings, board level thermal cycling and drop test performance.

2. Package Description

The process of assembling WLCSP is very similar to direct chip attach method, eliminating the need of individually assembling the units in packages after dicing from a wafer. This process is essentially an extension of the chip fabrication process where the device interconnects and protections are accomplished using the traditional fab processes and equipment. The final solution is a device with an array pattern of bumps or solder balls formed on the chip with a pitch compatible with traditional PCB assembly processes. WLCSP is essentially a true Chip Scale Package (CSP) with the final package the same size as the chip. Figure 1 is an actual image of a Renesas WLCSP package. It differs from other ball-grid array, leaded and laminate-based CSPs because no bond wires, leads or substrate interconnections are required.

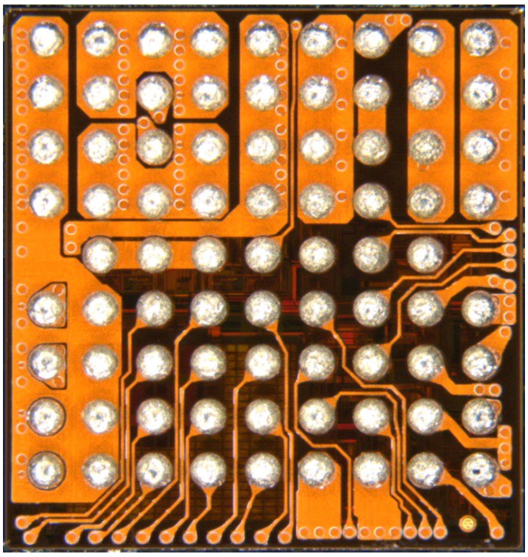

Figure 1. Image of a WLCSP Package

3. WLCSP Configurations and Dimensions

WLCSP packages range from 2 × 2 to 12 × 12 bump array, with a standard pitch of 0.40mm and a standard solder ball diameter of 268µm. The physical outlines (POD) of WLCSP packages are dynamic since those depend on actual die sizes. Therefore, users of devices in these packages must exercise greater care in utilization than those in more standardized packages. For details regarding standard solder ball arrays at 0.40mm pitch, see Table 1. Typical package height is 0.6mm nominal with 0.65mm being the maximum. 0.55mm maximum and 0.4mm maximum package heights are also available.

Renesas ships WLCSP in tape-and-reel (T and R) format. Tape and Reel requirements are based on the EIA-481 standard. Pin 1 identifiers are present on both sides of the WLCSP package to help with the assembly process.

Table 1. WLCSP Package Options

Solder Ball Array	Maximum I/O	Bump Pitch (mm)	Minimum Die Size (mm) [1][2]
2 × 2	4	0.4	0.8 × 0.8
3 × 3	9	0.4	1.2 × 1.2
4 × 4	16	0.4	1.6 × 1.6
5 × 5	25	0.4	2.0 × 2.0
6 × 6	36	0.4	2.4 × 2.4
7 × 7	49	0.4	2.8 × 2.8
8 × 8	64	0.4	3.2 × 3.2
9 × 9	81	0.4	3.6 × 3.6
10 × 10	100	0.4	4.0 × 4.0
11 × 11	121	0.4	4.4 × 4.4
12 × 12	144	0.4	4.8 × 4.8

1. Die size includes saw street.
2. Rectangular array is also available.

3.1 WLCSP Construction

Figure 2 below outlines a typical representation of a WLCSP package with Redistribution Layer (RDL) and Under-Bump Metalization (UBM) structures. The WLCSP die has a first layer of organic dielectric (Polyimide 1), a metal redistribution layer (RDL) to re-route the signal path from the I/O to a new desired location, and a second polyimide layer (Polyimide 2) to cover the RDL metal, which in turn is patterned into the solder ball array. To prevent diffusion and enable solder wetting, an under-bump metalization (UBM) layer is deposited on the RDL. The solder ball is a lead-free alloy. Backside wafer lamination (a protective polymer film) is optional for WLCSP products. This polymer material offers both mechanical contact (SMT assembly pick and place) and UV light protection to the die backside.

Note: A non-UBM WLCSP option is also available.

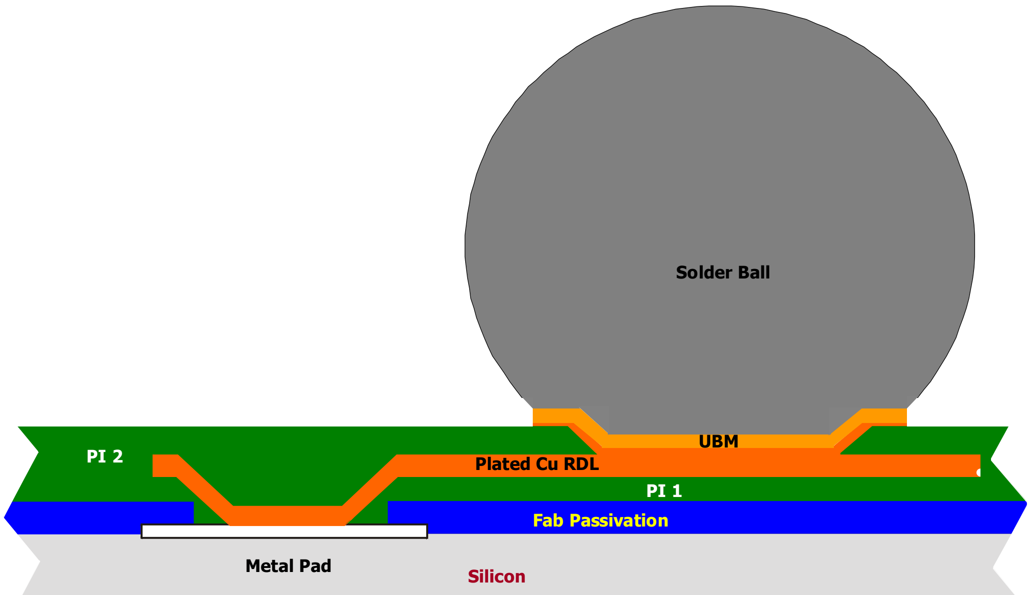

Figure 2. Cross-section Schematic of WLCSP Package with RDL

4. PCB Design Guidelines

For optimal electrical performance and highly reliable solder joints, the solder joint dimensions on the chip and the PCB side should be well-balanced and ideally within 5% tolerance of each other.

The PCB pads can be of either Solder Mask Defined (SMD) type or Non-Solder Mask Defined (NSMD) type. Figure 3 shows the top view of the two pad types.

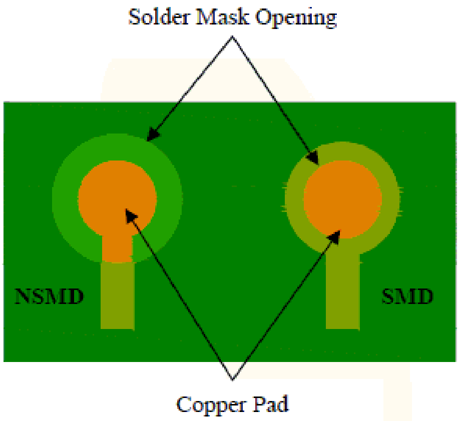

Figure 3. SMD vs NSMD Copper Pads

SMD pads are defined by the solder mask opening on the board. For SMD pads, the opening of the solder mask is smaller than the underlying copper pad for soldering to the associated bump. NSMD pads have solder mask opening larger than the copper pad. There are many factors influencing whether the PCB designer should use SMD or NSMD pads. Either type can successfully be used with WLCSP packages. However Renesas recommends using NSMD pads. In Figure 4, a cross-sectional view of the solder joint using the two pad types is shown in. In Figure 5, a cross-section of an actual recommended joint using NSMD pads is shown.

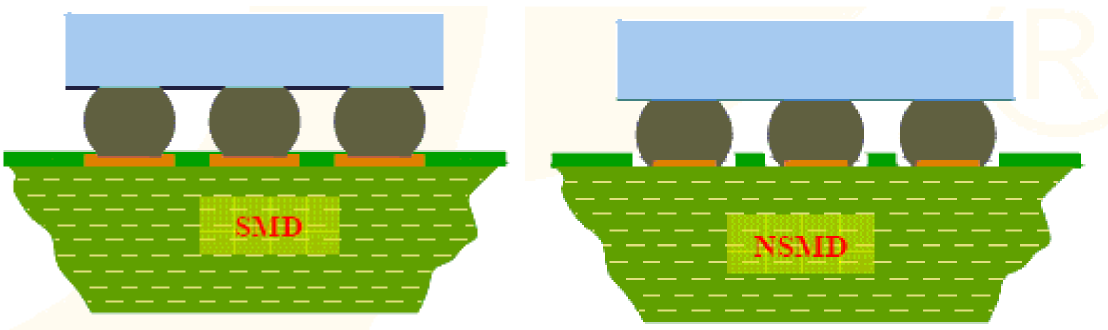

Figure 4. Sectional View of WLCSP Mounted on NSMD (left) and SMD (right) Pads

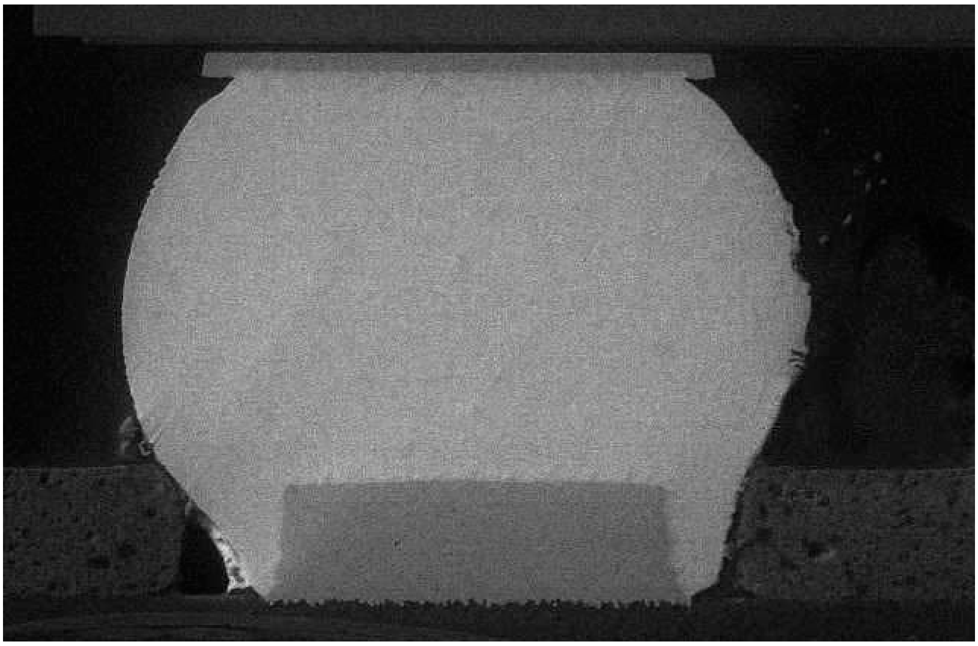

Figure 5. Cross-section of a Good Quality Joint Using NSMD Pad

4.1 Key PCB Design Considerations for NSMD-type Pads

- Solder mask is recommended between all pads, with the clearance around the copper pad and solder mask of 50µm nominal to account for the registration tolerance of the solder mask
- Limiting the thickness of the metal pad to not exceed 30µm is critical to assure a balanced joint
- To prevent solder thieving, each NSMD copper pad should be connected by only one signal trace, with the trace width being no more than 60% the diameter of the pad and having a fillet radius at the point it meets the pad, also known as "tear dropping". This prevents a stress riser that would otherwise occur at the pad/trace intersection.

Table 2. Design Guidelines for NSMD Pads

Description	0.4mm and 0.5mm Pitch WLCSP
Solder Ball Diameter	268µm ±60µm
PCB Pad Shape	Round
PCB Pad Diameter	205µm ±20µm
PCB Pad Surface Finish	OSP
PCB Pad Thickness	30µm maximum
Solder Mask Opening	305µm ±30µm
Stencil Fabrication	Laser cut stainless steel with Ni plating and electro- polishing; chemical etch method not recommended
Stencil Thickness	0.100mm to 0.125mm
Stencil Aperture	5° tapered, trapezoidal square 0.25 × 0.25 mm (±0.025mm)

4.2 Key PCB Design Considerations for SMD-type Pads

- It is critical to ensure good solder mask coverage and that no metal pad edge is exposed
- Ensure that the metal pad is clear of any solder mask related residue

Table 3. Design Guidelines for SMD Pads

Description	0.4mm and 0.5mm Pitch WLCSP
Solder Ball Diameter	268µm ±60µm
PCB Pad Shape	Round
PCB Pad Diameter	340µm ±35µm
PCB Pad Surface Finish	OSP
PCB Pad Thickness	NA
Solder Mask Opening	240µm ±25µm
Stencil Fabrication	Laser cut stainless steel with Ni plating and electro- polishing; chemical etch method not recommended
Stencil Thickness	0.100mm to 0.125mm
Stencil Aperture	5° tapered, trapezoidal square 0.25 × 0.25 mm (±0.025mm)

4.3 Via-In-Pad Structures

Via-in-pad structures will generally be determined by the design requirements. Via-in-pad designs typically result in voids and inconsistent solder joints after reflow, leading to early failures. These voids are formed due to the entrapment of air in via barrel. The size of a typical void can be same as via diameter and up to a depth of 30% the solder ball height. If via-in-pad structures must be used, it is recommended to use filled vias. As with any PCB, the quality and experience of the vendor is very important with via-in-pad designs.

4.4 Board Material

Renesas' WLCSP can be assembled on standard epoxy glass substrates. High temperature FR-4 which has smaller CTE (coefficient of thermal expansion) is preferable because it enhances package reliability as compared to standard FR-4. The actual CTE of PCB board is also affected by numerous factors such as number of metal layers in PCB, trace density, laminate material, operating environment etc. Ideally, the glass transition temperature of the substrate should be above the operating range of the intended application temperature.

Thinner boards are more flexible and result in greater reliability during thermal cycling. Moreover, they provide improved thermal fatigue life in comparison to thicker boards. Standard board thickness currently used in the industry ranges from 0.4mm to 2.3mm. The thickness is selected depending on the required robustness of the assembly.

Different bond pad surface finishes have significant effect on assembly yield and reliability. Organic Surface Preservative (OSP) is recommended as the most appropriate finish. Electroless Nickel Immersion Gold (ENIG) is a popular choice due to the higher substrate shelf- life, improved corrosion resistance and better thermal stability of solder joint. Immersion gold, immersion silver, solder on pad are also acceptable alternatives.

4.5 Stencil Design Guideline

Due to the relatively fine pitch and small terminal geometry used on a WLCSP, optimizing the paste printing process is critical to ensure the reliability of solder joints. In-process inspection for paste height, percent pad coverage, and registration accuracy to solderable land pattern is highly recommended.

Stencils should be laser cut stainless steel with Nickel plating or electroformed Cobalt or Chromium hardened Nickel for repeatable solder paste deposition from ultra-small apertures required by small pitch packages. It is recommended to inspect the stencil openings for burs and other quality issues prior to use. Both square and round shaped apertures have been used successfully, however square shaped aperture openings provide more consistent paste printing and transfer efficiency when compared to round openings. Corners may be rounded to prevent clogging.

Common stencil thicknesses for a WLCSP are 0.1mm and 0.125mm. Stencil aperture area ratio of >0.66 and aspect ratio >1.5, with 0.25mm × 0.25mm square openings (25 micron corner radius) is recommended for good solder paste deposition repeatability. Aperture aspect ratio is defined as the aperture opening area divided by the aperture side wall surface area. When these stencil design requirements conflict with other required SMT components in a mixed technology PCB assembly, a step-down stencil or two-print stencil process may be required.

5. PCB Assembly Guidelines

5.1 Assembly Process Flow

The assembly procedure for Renesas WLCSP packages is compatible with industry standard surface mount procedures, as exemplified in IPC- CM-770 and IPC-A-610 class 2 standards. ESD protection should be used in all process steps. A typical WLCSP assembly process flow is shown in Figure 6.

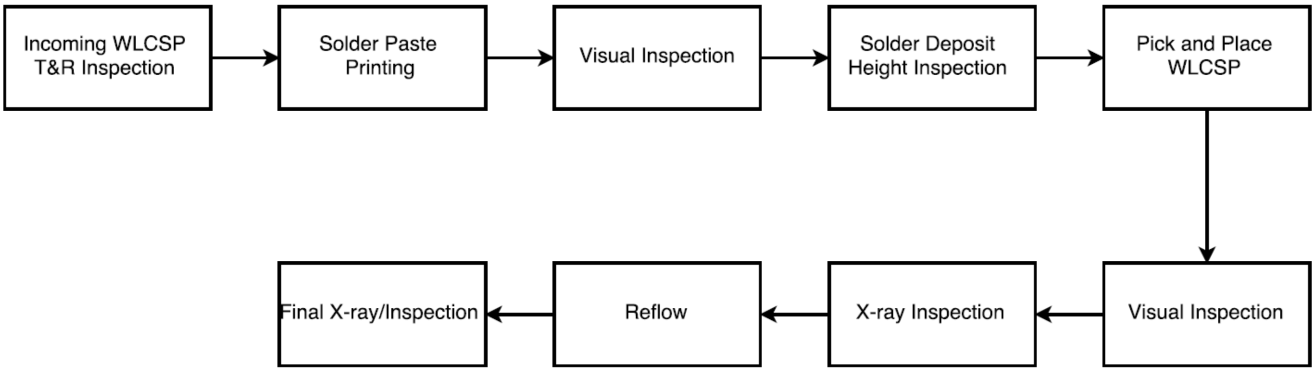

Figure 6. Typical WLCSP Assembly Process Flow

Renesas WLCSP packages do not require underfill and have been qualified without it. Renesas recommends a WLCSP assembly without any underfill. Use of underfill in application, if desired by the end-user, should involve careful selection of the material so as to avoid problems caused by a mismatched material choice.

Since the WLCSP is qualified as MSL1 at +260°C per JEDEC J-STD-020, no bake is required before assembly.

5.2 Solder Paste Material

Use of Type 4 (25 to 36 micron solder sphere particle size) or finer solder paste is recommended. It is also recommended that a low halide (< 100ppm halides), no-Clean rosin/resin flux system be used to eliminate post-reflow assembly cleaning operations.

5.3 Component Placement (Handling)

The WLCSP package is relatively small in size. For better accuracy, it is recommended to use automated fine-pitch placement machines with vision alignment instead of chip-shooters to place the parts. Local fiducials are required on the board to support the vision systems.

WLCSP devices are brittle and fragile structures and hence pick-and-place systems using mechanical centering are not recommended due to the high potential for mechanical damage. Ensure that minimal pick-and-place force is used to avoid damage, with all vertical compression forces controlled and monitored. Z-height control methods are recommended over force control. Renesas highly recommends the use of low-force nozzle options and compliant tip materials to further avoid any physical damage to the WLCSP device. Figure 7 shows mechanical damage to the WLCSP device due to improper handling.

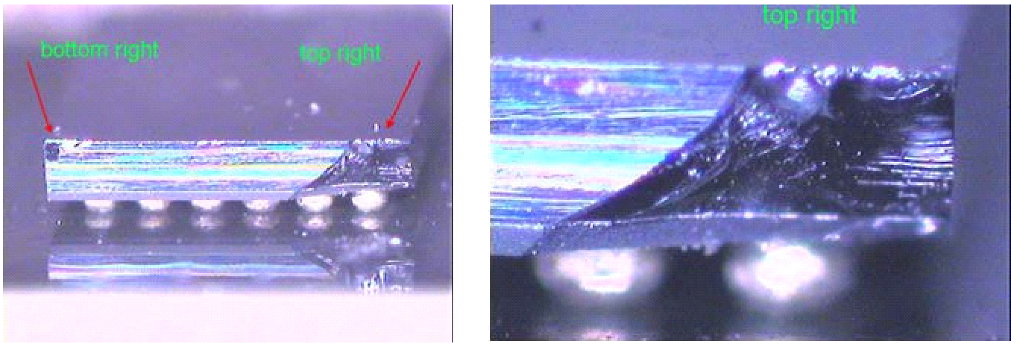

Figure 7. Mechanical Damage to WLCSP Device Due to Improper Handling

For manual handling, use only vacuum pen with compliant tip material. A sample pen type is shown in Figure 8.

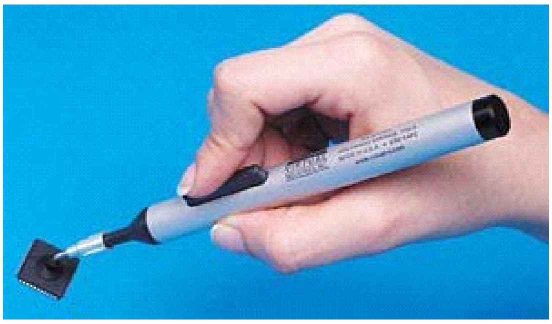

Figure 8. Manual Handling of WLCSP Device Using a Vacuum Pen

All assemblers of WLCSP components are encouraged to conduct placement accuracy studies to provide factual local knowledge about compensations needed for this package type. Renesas cannot anticipate the range of placement equipment and settings possible for package placement and, therefore, cannot make a generic recommendation on how to compensate for WLCSP interchangeability.

5.4 Reflow Profile

Temperature profile is the most important control in reflow soldering and it must be fine-tuned to establish a robust process. The actual profile depends on several factors, including complexity or products, oven type, solder type, temperature difference across the PCB, oven and thermocouple tolerances, etc. All of Renesas' WLCSP devices are qualified at Moisture Sensitivity Level 1 at 260°C. The maximum temperature at the component body should not exceed this level.

A typical reflow profile for lead-free paste is shown in Figure 9, based on IPC/JEDEC J-STD-020D. The furnace should have a nitrogen purge, with the oxygen content of the furnace monitored and kept below 100ppm.

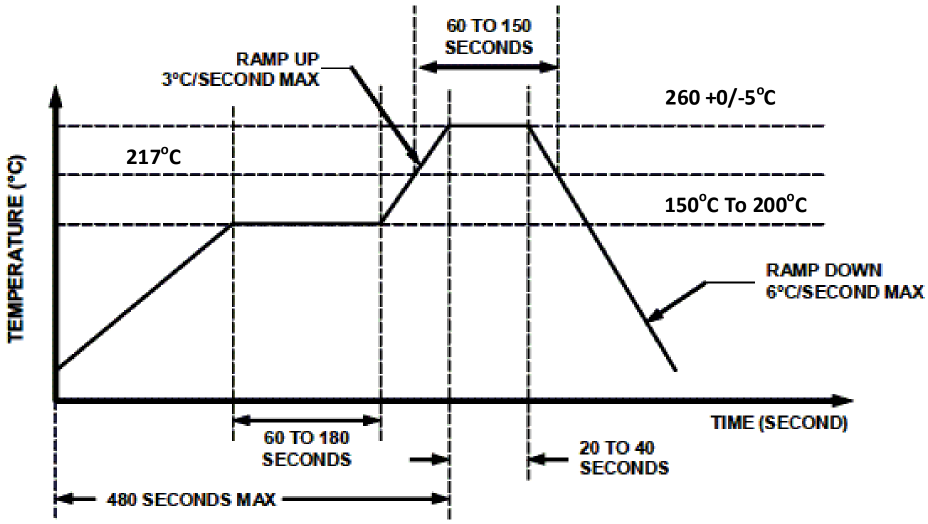

Figure 9. Typical Reflow Profile for WLCSP

Actual reflow temperature settings need to be determined by the end-user, based on the size of thermal load.

5.5 Pack and Ship

To prevent damage to the WLCSP component, care must be taken in handling, packing, and shipping WLCSP assemblies, especially when the WLCSP is mounted without epoxy encapsulation. The assembly site's packing specifications for PCB mounted with WLCSP must be reviewed and optimized.

6. WLCSP Reliability

WLCSP reliability can be divided into two categories namely, board level reliability (BLR) and component level reliability. The board level reliability is usually characterized by determining the solder joint life. The reliability results in this section utilized the board layout guidelines discussed before.

6.1 BLR Test Structure Description

The WLCSP package has a relatively shorter solder joint life compared to leaded or laminate substrate based packages. The solder joint reliability has been tested for reliability by Renesas to understand solder joint life and failure mechanism. Samples of a WLCSP in daisy chain format were used to study the solder joint reliability. BGA pairs were routed together in the WLCSP RDL layer, with a complementary pattern designed on the test PCB to provide one electrical circuit (net) through the package when the package is attached to the test PCB. Test points on the PCB exterior to the package allow one to isolate which pair of solder joints failed during testing.

6.2 Temperature Cycling Reliability Results

Assembled PCBs can be temperature cycled at a variety of temperature ranges. The most common test condition for small devices is JEDEC Condition G (-40°C to 125°C), with equally split ramp-up, hot-zone dwell, ramp-down and cold-zone dwell times for a typical frequency of one cycle per hour. This test refers to JESD22-A104D, condition G.

Board level temperature cycle was performed with the following test conditions:

- Temperature range: -40°C to +125°C
- Duration of exposure: 15 minutes exposure in each temperature extreme
- Temperature ramp: 15 minutes
- Cycle time: 60 minutes

The test setup utilized has the capability of continuously monitoring the resistance through a daisy chain package and its complementary test PCB. Failure is defined as 20% increase in resistance over the initial resistance of the daisy chain. Daisy chain nets are tested (time zero testing) prior to temperature cycling. Most nets start with initial resistance of around 1Ω.

The solder joint reliability performance results during board level temperature cycle are shown in Table 4.

Table 4. Board-level Temperature Cycle Results for Renesas WLCSP

Array Size	Ball Pitch	Test Condition	Criteria	Results
10 × 10	0.4mm	-40°C/125°C with 15 min dwell, 1 cycle/ hour	5% failure > 500 cycles, S/S = 60	Pass
12 × 12	0.4mm		5% failure > 500 cycles, S/S = 60	Pass

6.3 Mechanical Drop Test Reliability Results

WLCSP parts were tested per JEDEC's JESD22-B111 Drop Test Specification. The drop test set-up, board layout, fixtures, and criteria are all based on the JESD22-B111. All drops are carried out in the Z direction (package down).

Drop test was performed with the following test conditions:

- Pulse shape: Half-sine waveform
- Impact acceleration: 1500G (±20%)
- Pulse duration: 0.5ms (±30%)
- Velocity change: 467cm/s (±10%)

The resistance at time zero and still state after the drop are recorded. Resistance data was collected in-situ throughout the dropping process, with maximum resistance data recorded during the drop. An event is defined as resistance greater than 1,000 ohms lasting for 1 microsecond or longer. Failure is defined as three or more events during five subsequent drops.

The solder joint reliability performance results during board level temperature cycle are shown in Table 5.

Table 5. Board-level Drop Test Results for Renesas WLCSP

Array Size	Ball Pitch	Test Condition	Criteria	Results
10 × 10	0.4mm	1500G, 0.5ms half sine	10% failure > 150 drops, S/S = 60	Pass
12 × 12	0.4mm	1500G, 0.5ms half sine	10% failure > 150 drops, S/S = 60	Pass

6.4 Cyclic Bending Test Reliability Results

WLCSP parts were tested per the JEDEC JESD22-B113 Cyclic Bend Test Specification. Cyclic bend test was performed with the following test conditions:

- Span for support Anvils: 110mm
- Span for load Anvils: 75mm
- Temperature ramp: 15 minutes
- Load profile: Sinusoidal
- Cycle frequency: 1Hz

An event is defined as resistance greater than 1,000 ohms lasting for 1 microsecond or longer. Failure is defined as the first event of intermittent discontinuity with resistance peak greater than the threshold value followed by at least nine additional confirmation events within 10% of the cycles to first event.

The solder joint reliability performance results during board level temperature cycle are shown in Table 6.

Table 6. Board-level Cyclic Bending Test Results for Renesas WLCSP

Array Size	Ball Pitch	Test Condition	Criteria	Results
8 × 8	0.4mm	2mm, 1Hz	200 cycles	Pass

6.5 Component Level Reliability Results

Typical component level package stresses were also performed on the Renesas WLCSP. Table 7 lists all component level package stresses, passing criteria and results.

Table 7. Component-level Reliability Results for Renesas WLCSP

Test Items	Stress Condition	Method	Number of Lots	Duration	Qual Criteria per lot (#fails/SS)
Pre-conditioning [1]	Bake: 24 hrs, 125°C, MSL 1	J-STD-020	3	168 hrs	0/25
Temperature Cycle [1]	-55°C to 125°C	JESD22-A104	3	700 cycles	0/77
Biased HAST [1]	130°C / 85% R.H., Vcc oper max	JESD22-A110	3	96 hrs	0/77
Unbiased HAST [1]	130°C / 85% R.H.	JESD22-A118	3	96 hrs	0/77
High Temperature Storage	150°C	JESD22-A103	3	1000 hrs	0/25

1. Pre-conditioning will be performed prior to Temperature Cycle, Biased HAST, and Unbiased HAST.

7. WLCSP Rework

Rework is not recommended. Should rework be necessary, procedures are identical to BGA. Rework profile should duplicate original reflow profile used in assembly. Rework system should include localized convection heating, bottom side heating and a pick-and-place device. System should also provide thermal profile capability.

8. Revision History

Revision	Date	Description
1.01	Jan 20, 2023	Updated the document in the latest Renesas template.
-	Apr 29, 2016	Initial release.

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