Interface IP

FPD-Link Receiver for TSMC 28nm HPC+

Overview

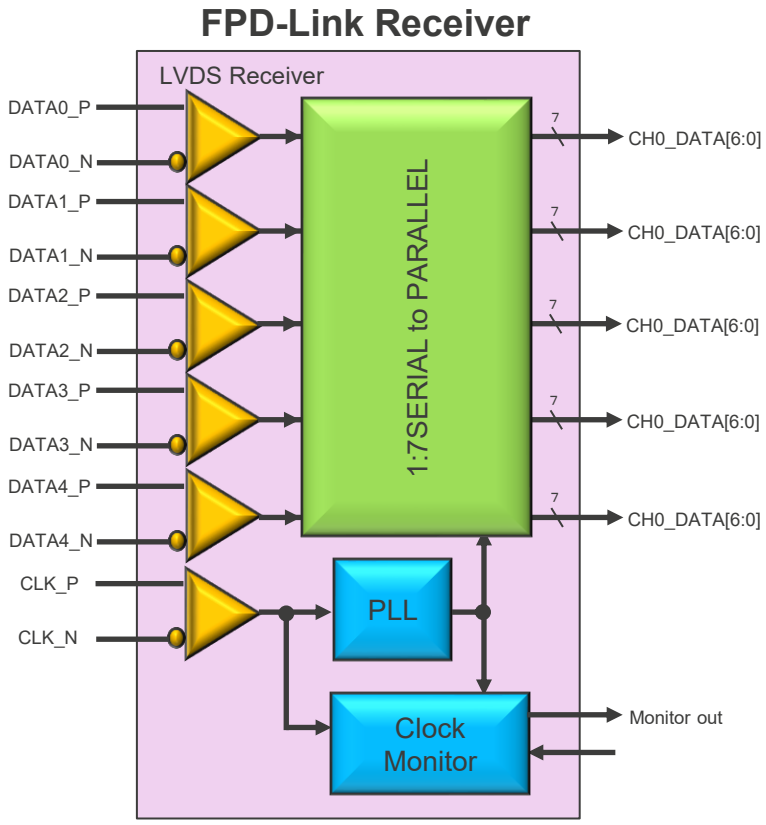
The Renesas FPD-Link Receiver is useful 5 Data Channel LVDS Receiver and 1:7 SERIAL to PARALLEL Converting of TSMC 28nm HPC+ process.

Key Features

- Renesas FPD-Link Receiver can be used for analog receiver of following interface .
  - ANSI/TIA/EIA-644※
- Technology is TSMC 28nm HPC+ 1p10M
- Supply voltage can be applied 1.0V for overdrive of core voltage, 1.8V for IO voltage.
- With an input clock at 71.5MHz, the maximum data rate of each channel is 500Mbps.
- Clock Monitor function can detect an anomaly status of the input clock(CLK_P/N) and PLL output clock.

※ Except for voltage range of Vin.

Block Diagram



*Before purchasing or using any Renesas Electronics products listed herein, please refer to the latest product manual and/or data sheet in advance.

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