Interface IP

MIPI D-PHY Receiver for TSMC 40nm LP

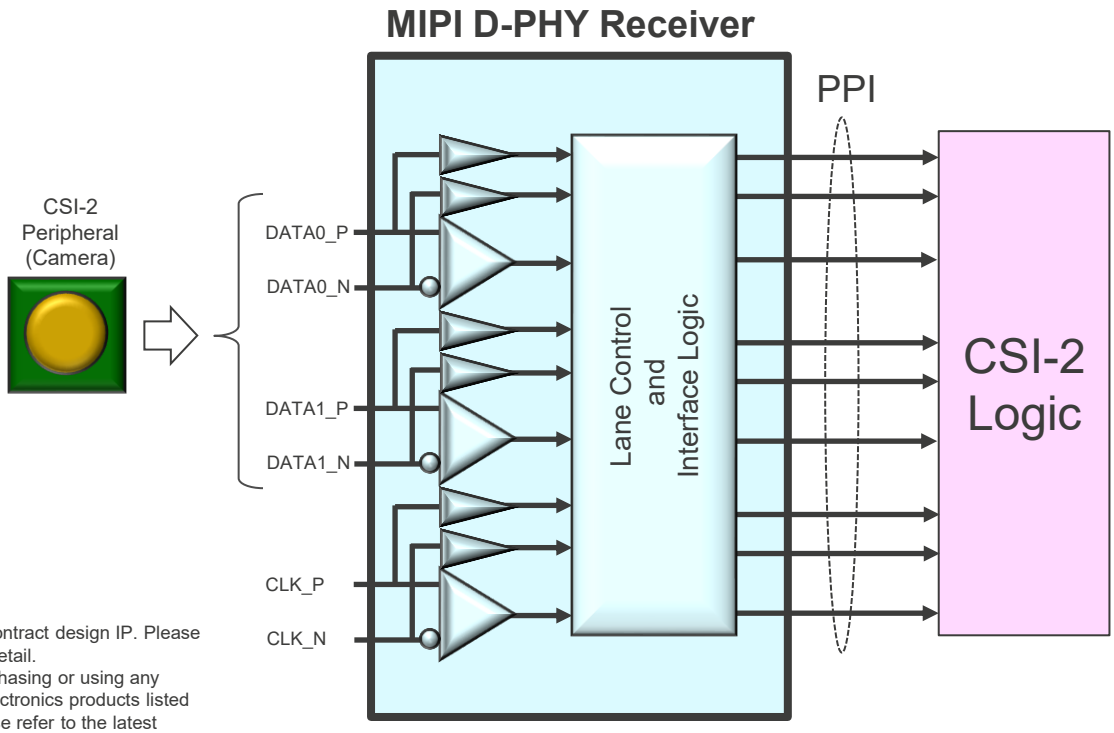
Overview

The Renesas MIPI D-PHY℠ Receiver is useful 2 Data Lane receiver hard macro for CSI-2® of TSMC 40nm LP process.

Features

- Renesas MIPI D-PHY Receiver can be used for analog Receiver of following interface .
  - MIPI alliance Specification for D-PHY Version 2.1 15 December 2016.
  - MIPI alliance Specification for Camera Serial Interface 2 (CSI-2) Version 2.0 7 Dec 2016.
- Technology is TSMC 40nm LP 1p8M.
- Supply voltage can be applied 0.90V for nominal and 1.0V for overdrive of core voltage, 1.8V for IO voltage.
- Maximum data rate of each channel is 1.0Gbps at High-speed mode.

Block Diagram



*This IP is contract design IP. Please contact for detail.
*Before purchasing or using any Renesas Electronics products listed herein, please refer to the latest product manual and/or data sheet in advance.

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