Interface IP

MIPI DSI-2 Transmitter IP Core

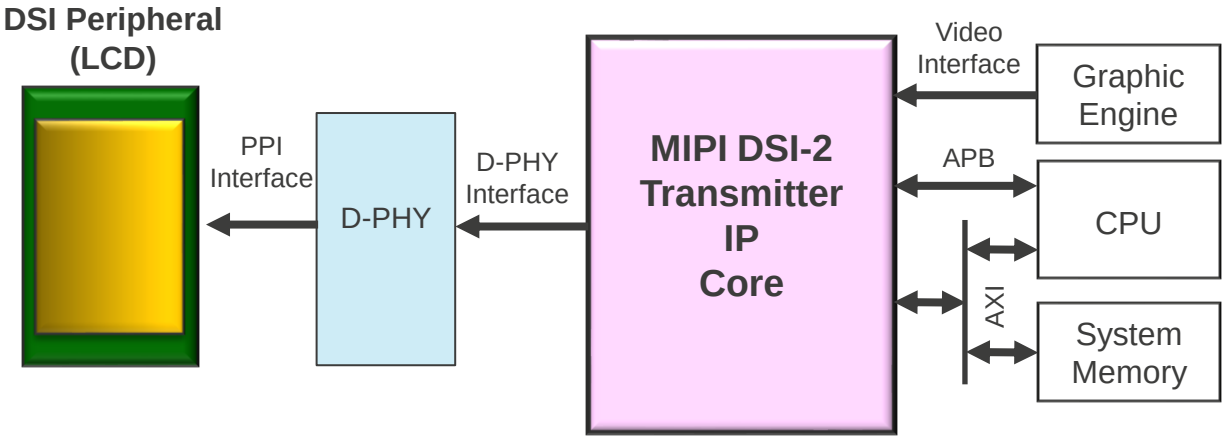
Overview

The Renesas DSI-2SM Transmitter IP is compliant with the Specification for Display Serial Interface 2 (DSI-2). This IP can be implemented in DSI-2 host processor, act as transmitter of image data.

Features

- Compliant with Specification for Display Serial Interface 2 (DSI-2SM) Version 1.1.
- Compliant with PHY Protocol Interface (PPI) to D-PHYSM Version 2.1.
- Compliant with AMBA® APB Protocol Version 2.0.
- Support PPI interface for D-PHY physical layer option
- Support De-facto standard interface for video transmission (Video Interface)
  – pixel clock, Vsync, Hsync, DE and pixel data for Video mode
- Support AXI interface for transmission and reception packets.
- Support APB interface for register access.

Block Diagram



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Functions

DSI-2 Transmitter function

- Support 1,2,3,4 D-PHY lanes.
- Support 80 Mbps to 4.5 Gbps per lane for unidirectional High-speed mode transmission.
- Support bidirectional Low-Power mode transmission and reception (only Lane 0).
- Support ULPS (Ultra Low-Power State) entry and exit.
- Support continuous clock mode and non-continuous clock mode.
- Support High-Speed packet generation from Video Interface for Video mode.
  - Support RGB formats (16-bit, 18-bit, 18-bit (Loosely Packed), 24-bit).
  - Support YCbCr 4:2:2 formats (16-bit, 20-bit (Loosely Packed), 24-bit).
  - Support Non-Burst Mode and Burst Mode.
- Support High-Speed and Low-Power packet generation through AXI for Command mode.
- Support Low-Power packet reception through AXI for Command mode.
- Support ECC and CRC generation in transmitting packet header.
- Support ECC 1bit error correction and 2bit error detection in received packet header.
- Support CRC check in received packet header.
- Support Data Scrambling
- Support PHY contention error and timeout error detection.

AXI Master Function

- Support 64bit data bus.

APB Slave Function

- Support 32bit data bus.

Sub Block Diagram