RENESAS

NETWORK PACKET SEARCH SOLUTION

Catalog

BIG IDEAS
FOR EVERY SPACE

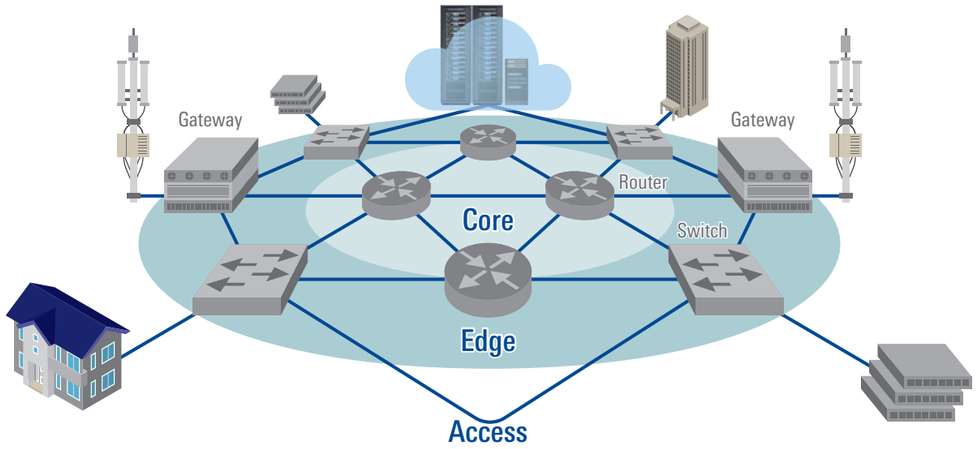
2017.06

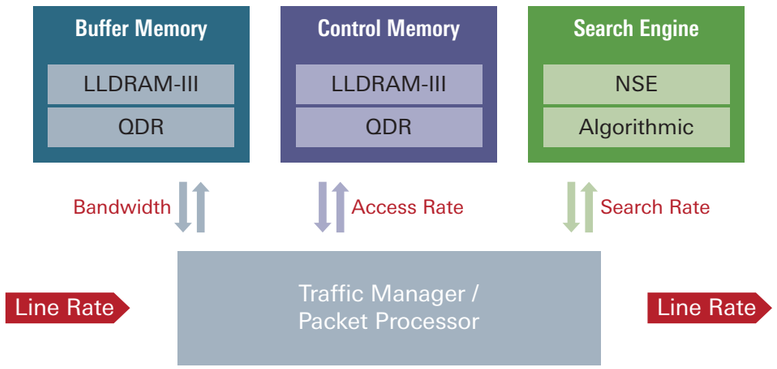
NETWORK PACKET SEARCH SOLUTION

-FOR ALL THE CONNECTING WORLD-

In a connected digital world, everything is dependent on a fast, secure and reliable infrastructure. Critical communications between machines, people and things must be distinguished from and prioritized over non critical exchanges. Awareness and intelligence is being built into information and communications systems to achieve the goals of the next generation infrastructure and at the same time securing these systems for a safe society. Renesas, a long established information and communications solution provider, supports solutions from the data center through the network to the access point with its proven technologies.

Renesas networking solutions address a wide range of applications including enterprise networking, network switch and router, internet access and network security. The explosion of cloud-based data requires network architecture to be more flexible and scalable. With a long history of offering cutting edge semiconductor products for network infrastructures, our solutions enable network appliances makers to improve time to market, with best in class performance, reliability, and scalability optimized for the digital age.





CONTENT

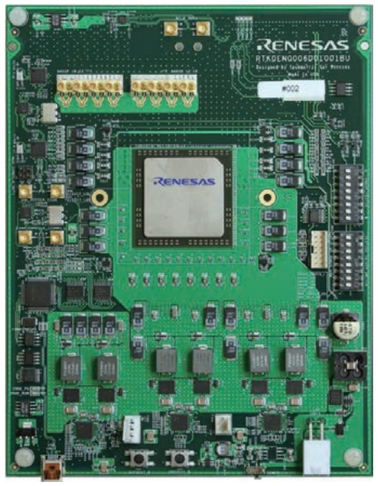
Key Features of High Speed Search Solution

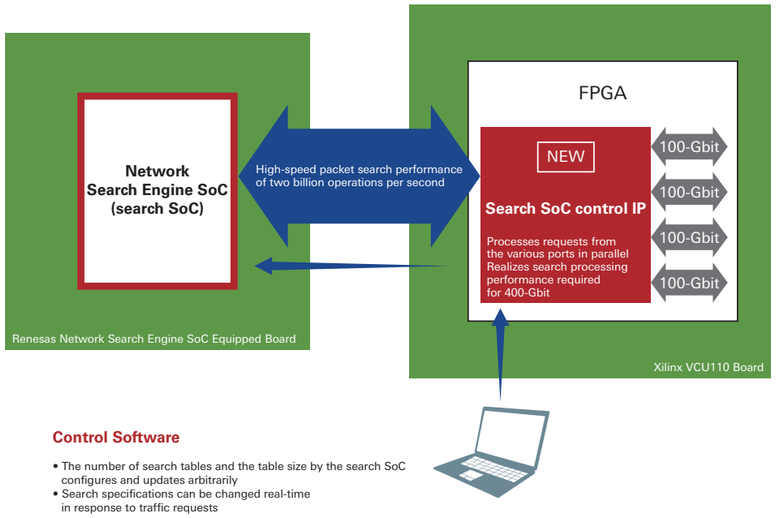
Renesas' NSE* reference design provides a flexible platform that adapts to a wide range of network topologies.
With proven design interfacing to industry standard host devices, this solution makes it possible to include a search offload engine into any network system with minimal development time.

* NSE: Network Search Engine

Evaluation Design Kit

- Reference board with onboard S-NSE-D
- Sample design with Search Engine Control IP
- Verification and evaluation applications





Item List For NSE Design Kit

Item	Content
RDK board	RDK board (FPGA board plug-in)
Control IP	NSE control IP (FPGA IP format)
Software (API)	Search control API, NSE device configuration API
Documents	Board hardware guide, software manual, control IP user guide
Sample design	Reference design data, GUI tool, GUI manual

https://www.renesas.com/en-us/search/keyword-search.html#q=r10an0013eu

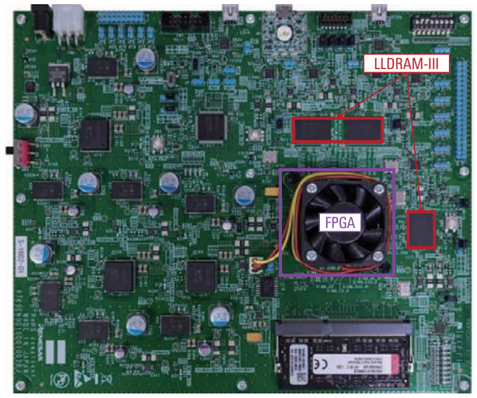
Key Features of Low Power Search Solution

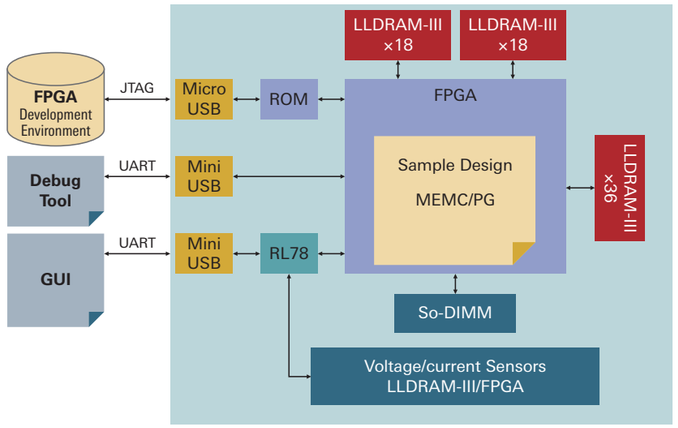
Renesas Exact Match reference design includes proprietary search algorithm, LLDRAM-III control IP on a FPGA host controller, accompanied by a suite of development tools.

1.Lookups over one million rules of packet headers for 100-Gbit network system in around 2 watts. The number of on board memory devices is reduced to 1/15th plus a 60% cut in power consumption.
2.Scales with future network protocols by flexible configuration of search key length of up to 575-bit.
3.Reduces network systems development cycle time by providing an all-in-one development platform with an on board Xilinx FPGA and *LLDRAM-III * LLDRAM: Low Latency DRAM

Evaluation Design Kit

- Reference Board with onboard FPGA and LLDRAM-III
- Sample Design With Search Engine IP
- Verification and Evaluation applications





Item List For Design Kit

Item	Content
Reference board	Interoperability verified between FPGA and LLDRAM-III
Exact match search IP	Verilog source code, AXI4 slave bridge module
API for table maintenance	ANSI-C source code
Documents	Quick start guide, exact match search IP design guide, PCB design guide, GUI software guide, API guide, LLDRAM-III data sheet
Sample design	Verilog source code, FPGA implementation environment, logic simulation environment, GUI software

https://www.renesas.com/en-us/search/keyword-search.html#q=r10an0010ej
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Product Lineup for Search Solution (1)

Item	High Speed Search Solution		
	Parallel Interface		Serial Interface
Part No.	R8A20410BG-G	R8A20611BG-G / R8A20610BG-G	R8A20646BG-G / R8A20686BG-G
Density	20-Mbit	40- / 80-Mbit	40- / 80-Mbit
Interface	80-bit	80-bit	2x Interlaken-LA ports 12 TX + 12 RX per port
Clock Frequency	360 MHz	500 MHz	10.3125 / 12.5 Gbps
Max. Search Rate / Table	360 Msps	250 Msps	500 Msps
Context Registers	128 × 320-bit	256 × 320-bit	Not supported
Cascade	2 maximum	Not supported	Not supported
Error Detection	Background Scan	Background Scan	Background Scan
Package	27 mm² 576-pin BGA	35 mm² 1152-pin BGA	37.5 mm² 1292-pin BGA
VDD / VDDQ (I/O)	1.00 V / 1.50 V	0.85 V / 1.50 V	0.90 V / 1.80 V
Availability	MP	MP	MP
Features	•Medium Density 20-Mbit •Middle Range Speed 360 Million Searches per Second (MSPS) per table. 720 Million Searches per Second with multiple search mode. •40-, 80-, 160-, 320-, 480-, or 640-bit search key-width supports •Multi-device cascading Allows the TCAM array capacity to effectively doubled to 40-Mbit •Low Latency 80-bit Parallel Interface •Flexible & Scalable Dynamic table-size remapping •Key Map Engine (KME) •Key Learning Context Registers •IO Training •Compact package 576 FCBGA(27 mm × 27 mm, flip-chip type)	•High Density 40- and 80-Mbit •Middle Range Speed 250 Million searches per Second per table. 1 Billion Searches per Second with multiple search mode. •80-, 160-, 320-, or 640-bit search key-width supports •Low Latency 80-bit parallel Interface •Low Power Consumption 28 nm process •Flexible & Scalable Dynamic table-size remapping •Key Map Engine (KME) •Key Learning Context Registers •IO Training	•High Density 40- and 80-Mbit •High Range Speed 500 Million Searches per Second per table. 2 Billion Searches per Second with multiple search mode. •80-, 160-, 320-, or 640-bit search key-width supports •Low Power Consumption 28 nm process •Flexible & Scalable Two Interlaken-LA ports Fully configurable SerDes lanes Dynamic table-size remapping Multi-bank architecture •Key Map Engine (KME)
Applications	Enterprise switches, routers, metro switches and routers, Core switches, routers, edge switches and routers, 4 G / 5 G mobile access platforms		

Product Lineup for Search Solution (2)

Architecture	Low Latency DRAM II	Low Latency DRAM III
Density	288- / 576-Mbit	1.1-Gbit
Max. Frequency	533 MHz	800 MHz
tRC	15 ns	13.75 ns
Bus Width	×9 / ×18 / ×36	×18 / ×36
Package	144-pin FBGA (11 × 18.5 mm)	180-pin FCBGA (14 × 18.5 mm)
VEXT	2.5 V	2.5 V
VDD	1.8 V	1.5 V
VDDQ (I/O)	1.5 V - 1.8 V	1.0 V / 1.2 V
Availability	MP	MP

Low Latency DRAM II: RLDRAM®II Compatible

Architecture	Double Data Rate II *1 Quad Data Rate II*2	Double Data Rate II+ Quad Data Rate II+
Density	18-, 36-, 72-, 144-Mbit	36-, 72-, 144-Mbit
Max. Frequency	333 MHz	550 MHz
Bus Width	×18 / ×36	×18 / ×36
Package	165-pin FBGA 18-, 36-, 72-Mbit: 13 × 15 mm 144-Mbit: 15 × 17 mm	165-pin FBGA 36-, 72-Mbit: 13 × 15 mm 144-Mbit: 15 × 17 mm
VDD	1.8 V	1.8 V
VDDQ (I/O)	1.4 V - 1.9 V	1.4 V - 1.9 V
Temperature	-40 to 85 °C	-40 to 85 °C
Availability	MP	MP

*1 Double Data Rate : DDR
*2 Quad Data Rate: QDR

Features

Low Latency DRAM is our newest high-density network memory. Incorporating high-performance mobile-specific RAM technology used in our synchronous SRAM and the pseudo-SRAM products, Low Latency DRAM is able to achieve ultra-fast random access time and data latency lower than commodity DRAMs.

These features, combined with large density and lower cost per bit when compared to SRAM solutions, make Low Latency DRAM an attractive choice for use in next-generation, high-performance networking products.

- A large capacity and high-speed access
- Double-data-rate architecture
- Common I/O
- PLL circuitry

Key Applications

- Packet forwarding queuing, and buffering for high speed network switches & routers.
- A large capacity and high-speed access applications for various network markets.
- Cache memory for high-end work station & servers.

Features

DDR SRAM can provide double data rate (DDR) operations on each data pin in write or read cycles. With the capability of reading and writing twice every clock cycle, DDR SRAM provides for a significantly higher transfer rate than standard synchronous SRAM devices. In applications that require continuous read/write capability such as in look-up tables for network switches and routers, DDR SRAM is an ideal solution.

In addition, independent read and write ports means QDR SRAM can provide double data rate (DDR) operation on each data pin through independently operated read and write ports, and can transfer four words of data on one clock cycle. This feature virtually eliminates bus contention between the memory controller and SRAM, making QDR SRAM an ideal solution for high-end network switches, routers and other communications products.

DDR II / II+, QDR™ II / II+ SRAMs are the ideal memory devices for high speed networking and communications systems. These ultra-fast devices can support high bandwidth systems that require memories capable of very high operating frequencies combined with low latencies and full cycle utilization.

Key Applications

- Packet forwarding queuing, and buffering for high speed network switches & routers.
- Action control, or statistic memory as a result of search.
- Communications infrastructure equipment such as base stations and switches.
- Cache memory for high-end work stations & servers.

Low Latency DRAM Product List

Part No.	Density (Mbits)	Function	Burst Length (words)	Data Width (bits)	MAX Frequency (MHz)	tRC (ns)	I/O Voltage (V)	Pin Count	Package Type
UPD48288209AF1-E24-DW1-A	288	Common I/O	2/4/8	9	400	15	1.5/1.8	144	TFBGA
UPD48288218AF1-E18-DW1-A	288	Common I/O	2/4/8	18	533	15	1.5/1.8	144	TFBGA
UPD48288218AF1-E24-DW1-A	288	Common I/O	2/4/8	18	400	15	1.5/1.8	144	TFBGA
UPD48288236AF1-E18-DW1-A	288	Common I/O	2/4	36	533	15	1.5/1.8	144	TFBGA
UPD48288236AF1-E24-DW1-A	288	Common I/O	2/4	36	400	15	1.5/1.8	144	TFBGA
UPD48288118AF1-E18-DW1-A	288	Separate I/O	2/4/8	18	533	15	1.5/1.8	144	TFBGA
UPD48288118AF1-E24-DW1-A	288	Separate I/O	2/4/8	18	400	15	1.5/1.8	144	TFBGA
UPD48576209F1-E24-DW1-A	576	Common I/O	2/4/8	9	400	15	1.5/1.8	144	TFBGA
UPD48576218F1-E18-DW1-A	576	Common I/O	2/4/8	18	533	15	1.5/1.8	144	TFBGA
UPD48576218F1-E24-DW1-A	576	Common I/O	2/4/8	18	400	15	1.5/1.8	144	TFBGA
UPD48576236F1-E18-DW1-A	576	Common I/O	2/4	36	533	15	1.5/1.8	144	TFBGA
UPD48576236F1-E24-DW1-A	576	Common I/O	2/4	36	400	15	1.5/1.8	144	TFBGA
UPD48576118F1-E18-DW1-A	576	Separate I/O	2/4/8	18	533	15	1.5/1.8	144	TFBGA
UPD48576118F1-E24-DW1-A	576	Separate I/O	2/4/8	18	400	15	1.5/1.8	144	TFBGA
RMHE41A184AGBG-120	1100	Common I/O	4	18	800	13.75	1.0/1.2	180	FCBGA
RMHE41A364AGBG-120	1100	Common I/O	4	36	800	13.75	1.0/1.2	180	FCBGA

QDR SRAM Product List (1)

Part No.	Density (Mbits)	Architecture	Burst Length (words)	Read Latency (Clock)	Data Width (bits)	Package Body Size	Pin Count	Package Type
RMQC4A1818DGBA-xxx	18	DDR-II CIO	2	1.5	18	13 × 15mm	165	LBGA
RMQC4A1836DGBA-xxx	18	DDR-II CIO	2	1.5	36	13 × 15mm	165	LBGA
RMQS2A1818DGBA-xxx	18	QDR-II	2	1.5	18	13 × 15mm	165	LBGA
RMQS2A1836DGBA-xxx	18	QDR-II	2	1.5	36	13 × 15mm	165	LBGA
RMQS3A1818DGBA-xxx	18	QDR-II	4	1.5	18	13 × 15mm	165	LBGA
RMQS3A1836DGBA-xxx	18	QDR-II	4	1.5	36	13 × 15mm	165	LBGA
RMQC4A3618DGBA-xxx	36	DDR-II CIO	2	1.5	18	13 × 15mm	165	LBGA
RMQC4A3636DGBA-xxx	36	DDR-II CIO	2	1.5	36	13 × 15mm	165	LBGA
RMQCBA3618DGBA-xxx	36	DDR-II+ CIO without ODT	2	2.5	18	13 × 15mm	165	LBGA
RMQCBA3636DGBA-xxx	36	DDR-II+ CIO without ODT	2	2.5	36	13 × 15mm	165	LBGA
RMQCEA3618DGBA-xxx	36	DDR-II+ CIO with ODT	2	2.5	18	13 × 15mm	165	LBGA
RMQCEA3636DGBA-xxx	36	DDR-II+ CIO with ODT	2	2.5	36	13 × 15mm	165	LBGA
RMQCHA3618DGBA-xxx	36	DDR-II+ CIO without ODT	2	2	18	13 × 15mm	165	LBGA
RMQCHA3636DGBA-xxx	36	DDR-II+ CIO without ODT	2	2	36	13 × 15mm	165	LBGA
RMQCLA3618DGBA-xxx	36	DDR-II+ CIO with ODT	2	2	18	13 × 15mm	165	LBGA
RMQCLA3636DGBA-xxx	36	DDR-II+ CIO with ODT	2	2	36	13 × 15mm	165	LBGA
RMQS2A3618DGBA-xxx	36	QDR-II	2	1.5	18	13 × 15mm	165	LBGA
RMQS2A3636DGBA-xxx	36	QDR-II	2	1.5	36	13 × 15mm	165	LBGA
RMQS3A3618DGBA-xxx	36	QDR-II	4	1.5	18	13 × 15mm	165	LBGA
RMQS3A3636DGBA-xxx	36	QDR-II	4	1.5	36	13 × 15mm	165	LBGA
RMQSAA3618DGBA-xxx	36	QDR-II+ without ODT	4	2.5	18	13 × 15mm	165	LBGA
RMQSAA3636DGBA-xxx	36	QDR-II+ without ODT	4	2.5	36	13 × 15mm	165	LBGA
RMQSDA3618DGBA-xxx	36	QDR-II+ with ODT	4	2.5	18	13 × 15mm	165	LBGA
RMQSDA3636DGBA-xxx	36	QDR-II+ with ODT	4	2.5	36	13 × 15mm	165	LBGA
RMQSGA3618DGBA-xxx	36	QDR-II+ without ODT	4	2	18	13 × 15mm	165	LBGA
RMQSGA3636DGBA-xxx	36	QDR-II+ without ODT	4	2	36	13 × 15mm	165	LBGA
RMQSKA3618DGBA-xxx	36	QDR-II+ with ODT	4	2	18	13 × 15mm	165	LBGA
RMQSKA3636DGBA-xxx	36	QDR-II+ with ODT	4	2	36	13 × 15mm	165	LBGA

"-xxx": Speed Grade
18-Mbit QDR/DDR-II: -302 = 333 MHz
36-Mbit QDR/DDR-II: -302 = 333 MHz
36-Mbit QDR/DDR-II+: -182 = 550 MHz, -202 = 500 MHz

QDR SRAM Product List (2)

Part No.	Density (Mbits)	Architecture	Burst Length (words)	Read Latency (Clock)	Data Width (bits)	Package Body Size	Pin Count	Package Type
R1Q2A7218ABB-xxx	72	QDR-II	2	1.5	18	13 × 15mm	165	LBGA
R1Q2A7236ABB-xxx	72	QDR-II	2	1.5	36	13 × 15mm	165	LBGA
R1Q3A7218ABB-xxx	72	QDR-II	4	1.5	18	13 × 15mm	165	LBGA
R1Q3A7236ABB-xxx	72	QDR-II	4	1.5	36	13 × 15mm	165	LBGA
R1Q4A7218ABB-xxx	72	DDR-II CIO	2	1.5	18	13 × 15mm	165	LBGA
R1Q4A7236ABB-xxx	72	DDR-II CIO	2	1.5	36	13 × 15mm	165	LBGA
R1QAA7218ABB-xxx	72	QDR-II+ without ODT	4	2.5	18	13 × 15mm	165	LBGA
R1QAA7236ABB-xxx	72	QDR-II+ without ODT	4	2.5	36	13 × 15mm	165	LBGA
R1QBA7218ABB-xxx	72	DDR-II+ CIO without ODT	2	2.5	18	13 × 15mm	165	LBGA
R1QBA7236ABB-xxx	72	DDR-II+ CIO without ODT	2	2.5	36	13 × 15mm	165	LBGA
R1QDA7218ABB-xxx	72	QDR-II+ with ODT	4	2.5	18	13 × 15mm	165	LBGA
R1QDA7236ABB-xxx	72	QDR-II+ with ODT	4	2.5	36	13 × 15mm	165	LBGA
R1QEA7218ABB-xxx	72	DDR-II+ CIO with ODT	2	2.5	18	13 × 15mm	165	LBGA
R1QEA7236ABB-xxx	72	DDR-II+ CIO with ODT	2	2.5	36	13 × 15mm	165	LBGA
R1QGA7218ABB-xxx	72	QDR-II+ without ODT	4	2	18	13 × 15mm	165	LBGA
R1QGA7236ABB-xxx	72	QDR-II+ without ODT	4	2	36	13 × 15mm	165	LBGA
R1QHA7218ABB-xxx	72	DDR-II+ CIO without ODT	2	2	18	13 × 15mm	165	LBGA
R1QHA7236ABB-xxx	72	DDR-II+ CIO without ODT	2	2	36	13 × 15mm	165	LBGA
R1QKA7218ABB-xxx	72	QDR-II+ with ODT	4	2	18	13 × 15mm	165	LBGA
R1QKA7236ABB-xxx	72	QDR-II+ with ODT	4	2	36	13 × 15mm	165	LBGA
R1QLA7218ABB-xxx	72	DDR-II+ CIO with ODT	2	2	18	13 × 15mm	165	LBGA
R1QLA7236ABB-xxx	72	DDR-II+ CIO with ODT	2	2	36	13 × 15mm	165	LBGA

"-xxx": Speed Grade
- 72-Mbit QDR/DDR-II: -33I = 300 MHz (3A, 4A), -40I = 250 MHz (2A)
- 72-Mbit QDR/DDR-II+ (RL=2.5): -19I = 533 MHz, -20I = 500 MHz
- 72-Mbit QDR/DDR-II+ (RL=2.0): -25I = 400 MHz

QDR SRAM Product List (3)

Part No.	Density (Mbits)	Architecture	Burst Length (words)	Read Latency (Clock)	Data Width (bits)	Package Body Size	Pin Count	Package Type
R1Q2A4418RBG-xxx	144	QDR-II	2	1.5	18	15 × 17mm	165	LBGA
R1Q2A4436RBG-xxx	144	QDR-II	2	1.5	36	15 × 17mm	165	LBGA
R1Q3A4418RBG-xxx	144	QDR-II	4	1.5	18	15 × 17mm	165	LBGA
R1Q3A4436RBG-xxx	144	QDR-II	4	1.5	36	15 × 17mm	165	LBGA
R1Q4A4418RBG-xxx	144	DDR-II CIO	2	1.5	18	15 × 17mm	165	LBGA
R1Q4A4436RBG-xxx	144	DDR-II CIO	2	1.5	36	15 × 17mm	165	LBGA
R1QAA4418RBG-xxx	144	QDR-II+ without ODT	4	2.5	18	15 × 17mm	165	LBGA
R1QAA4436RBG-xxx	144	QDR-II+ without ODT	4	2.5	36	15 × 17mm	165	LBGA
R1QBA4418RBG-xxx	144	DDR-II+ CIO without ODT	2	2.5	18	15 × 17mm	165	LBGA
R1QBA4436RBG-xxx	144	DDR-II+ CIO without ODT	2	2.5	36	15 × 17mm	165	LBGA
R1QDA4418RBG-xxx	144	QDR-II+ with ODT	4	2.5	18	15 × 17mm	165	LBGA
R1QDA4436RBG-xxx	144	QDR-II+ with ODT	4	2.5	36	15 × 17mm	165	LBGA
R1QEA4418RBG-xxx	144	DDR-II+ CIO with ODT	2	2.5	18	15 × 17mm	165	LBGA
R1QEA4436RBG-xxx	144	DDR-II+ CIO with ODT	2	2.5	36	15 × 17mm	165	LBGA
R1QGA4418RBG-xxx	144	QDR-II+ without ODT	4	2	18	15 × 17mm	165	LBGA
R1QGA4436RBG-xxx	144	QDR-II+ without ODT	4	2	36	15 × 17mm	165	LBGA
R1QHA4418RBG-xxx	144	DDR-II+ CIO without ODT	2	2	18	15 × 17mm	165	LBGA
R1QHA4436RBG-xxx	144	DDR-II+ CIO without ODT	2	2	36	15 × 17mm	165	LBGA
R1QKA4418RBG-xxx	144	QDR-II+ with ODT	4	2	18	15 × 17mm	165	LBGA
R1QKA4436RBG-xxx	144	QDR-II+ with ODT	4	2	36	15 × 17mm	165	LBGA
R1QLA4418RBG-xxx	144	DDR-II+ CIO with ODT	2	2	18	15 × 17mm	165	LBGA
R1QLA4436RBG-xxx	144	DDR-II+ CIO with ODT	2	2	36	15 × 17mm	165	LBGA
R1QNA4418RBG-xxx	144	QDR-II+ without ODT	2	2	18	15 × 17mm	165	LBGA
R1QNA4436RBG-xxx	144	QDR-II+ without ODT	2	2	36	15 × 17mm	165	LBGA
R1QPA4418RBG-xxx	144	QDR-II+ with ODT	2	2	18	15 × 17mm	165	LBGA
R1QPA4436RBG-xxx	144	QDR-II+ with ODT	2	2	36	15 × 17mm	165	LBGA

"-xxx": Speed Grade
- 144-Mbit QDR/DDR-II: -33I = 300 MHz, -40I = 250 MHz
- 144-Mbit QDR/DDR-II+: -18I = 550 MHz, -19I = 500 MHz, -25I = 400 MHz, -30I = 333 MHz

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   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
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