Errata

SLG47512_13

CE-GP-025

Abstract

This document contains the known errata for SLG47512_13 and the recommended workarounds.

1 Information

Package(s)	12-pin STQFN: 1.6 mm x 1.6 mm x 0.55 mm, 0.4 mm pitch 16-pin MSTQFN: 1.6 mm x 1.6 mm x 0.55 mm, 0.4 mm pitch

2 Errata Summary

Table 1: Errata Summary

Issue #	Issue Title
1	Vref Variation over Temperature
2	OSC1 May Stop Oscillating under High Frequency On/Off
3	I2C Slave Locked
4	ACMP Output LATCH
5	Shift Register Initial Value Configuration
6	Multi-Function Macrocell LATCH Enables Polarity
7	CNT/DLY and ACMP Dependency on OSC1

3 Errata Details

3.1 Vref Variation over Temperature

3.1.1 Effect

Vref

3.1.2 Conditions

Operation temperature down to -40 °C and up to +85 °C.

3.1.3 Technical Description

The Vref voltage is set to be 500 mV at 25 °C, but may drift by +26/-30 mV at -40 °C, and by +10/12 mV at +85 °C. The drift amount is scaled by the Vref voltage. For example, if Vref = 250 mV, the drift is scaled by 250/500 = 0.5, or +13/-15 mV at -40 °C and +5/-6 mV at +85 °C.

3.1.4 Workaround

Operate SLG47512_13 at 0 °C - 85 °C to keep temperature drift less than one half step (+/-12.5 mV).

3.2 OSC1 May Stop Oscillating under High Frequency On/Off

3.2.1 Effect

OSC1

3.2.2 Conditions

When OSC1 power mode is "Auto Power-On" and a high-frequency internal signal continuously turns the oscillator on/off, this may cause the OSC1 to freeze. As a result, the SLG47512_13 stops operating.

For example, this issue may happen when positive and negative inputs of ACMP are kept at the same voltage level or cross at slow ramp.

3.2.3 Technical Description

ACMP output flips back and forth with hundreds of nanoseconds width, that turns OSC1 on and off at near the megahertz frequency.

3.2.4 Workaround

Force OSC1 always on when using ACMP.

3.3 I²C Slave Locked

3.3.1 Effect

I²C

3.3.2 Conditions

I²C slave locked, if access is undefined by 254th or 255th byte.

3.3.3 Technical Description

If the User tries to access any internal register in the range of 254th or 255th bytes in an undefined space, the I²C will be locked and then return 0 only.

3.3.4 Workaround

Try not to access 254 and 255 bytes.

3.4 ACMP Output LATCH

3.4.1 Effect

ACMP

3.4.2 Conditions

ACMP output is not low when ACMP is powered down.

3.4.3 Technical Description

The ACMP output latches the last logic state before the ACMP power down. The output will not return to low after the ACMP power down.

3.4.4 Workaround

Currently, there is no workaround for this issue.

3.5 Shift Register Initial Value Configuration

3.5.1 Effect

Shift Register SHR-13 initial value

3.5.2 Conditions

The initial value of Shift Register 13 is wrong during programming.

3.5.3 Technical Description

If program the initial value of registers 91 [728:735] and 92 [736:743] in a sequence mode, the LSB code [728] will be reset to 0.

3.5.4 Workaround

Program the register 92 [736:743] before the register 91 [728:735] in a sequence mode.

3.6 Multi-Function Macrocell LATCH Enables Polarity

3.6.1 Effect

Multi-function macrocell LATCH (DFF/LATCH14 to DFF/LATCH21)

3.6.2 Conditions

LATCH enables polarity is opposite to expectation.

3.6.3 Technical Description

Expect CLK(G) high to lock the D input state and CLK(G) low to transparent D input state. The behavior of DFF/LATCH14 to DFF/LATCH21 is opposite to expectation, CLK(G) low to lock the D input state and CLK(G) high to transparent D input state.

3.6.4 Workaround

Currently, there is no workaround for this issue.

3.7 CNT/DLY and ACMP Dependency on OSC1

3.7.1 Effect

CNT/DLY in multi-function macrocell, ACMP

3.7.2 Conditions

CNT/DLY and ACMP don't work if OSC1 is powered down by the connection matrix signal.

3.7.3 Technical Description

If OSC1 is disabled by GPIO, the CNT/DLY is not functional when OSC0 is selected to be the clock source of CNT/DLY. ACMP is also not able to operate if OSC1 is disabled by GPIO.

3.7.4 Workaround

Currently, there is no workaround for this issue.

Document Revision History

Revision	Date	Description
1.0	10-Mar-2022	Renesas rebranding Initial version

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.