

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Phase-out/Discontinued

**P-CHANNEL POWER MOSFET
FOR SWITCHING**

FEATURES

- Gate drive available at logic level ($V_{GS} = -4\text{ V}$)
- High current control available in small dimension due to low $R_{DS(on)} (\cong 0.45\ \Omega)$
- 2SJ133-Z is a lead process product and is ideal for mounting a hybrid IC.

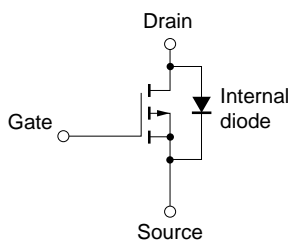
ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Conditions	Ratings	Unit
Drain to Source Voltage	V_{DS}	$V_{GS} = 0\text{ V}$	-60	V
Gate to Source Voltage	V_{GS}	$V_{DS} = 0\text{ V}$	∓ 20	V
Drain Current (DC)	$I_{D(DC)}$	$T_C = 25^\circ\text{C}$	∓ 2.0	A
Drain Current (pulse)	$I_{D(pulse)}$	$PW \leq 300\ \mu\text{s}$ duty cycle $\leq 10\%$	∓ 8.0	A
Total Power Dissipation	P_{T1}	$T_C = 25^\circ\text{C}$	20	W
Total Power Dissipation	P_{T2}	$T_A = 25^\circ\text{C}$	1.0 ^{Note 1} , 2.0 ^{Note 2}	W
Channel Temperature	T_{ch}		150	$^\circ\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^\circ\text{C}$

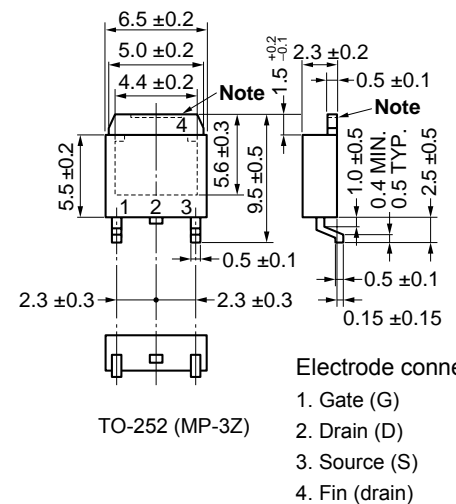
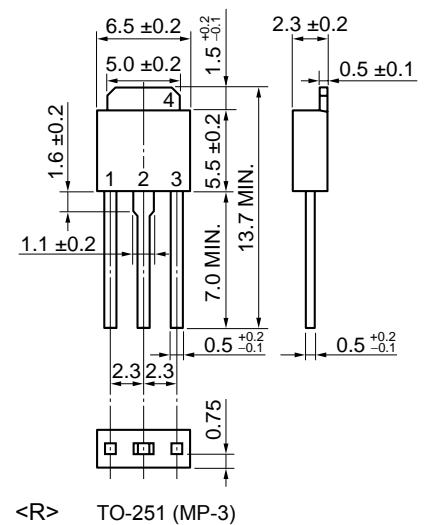
Note 1. Printing board mounted

2. $7.5\text{ cm}^2 \times 0.7\text{ mm}$ ceramic board mounted

EQUIVALENT CIRCUIT



PACKAGE DRAWING (UNIT: mm)



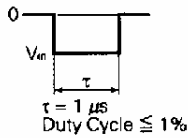
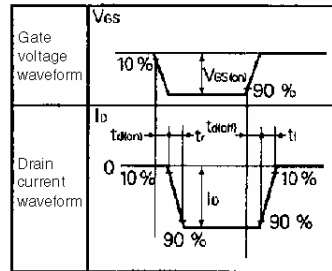
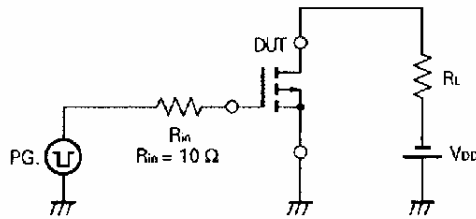
Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

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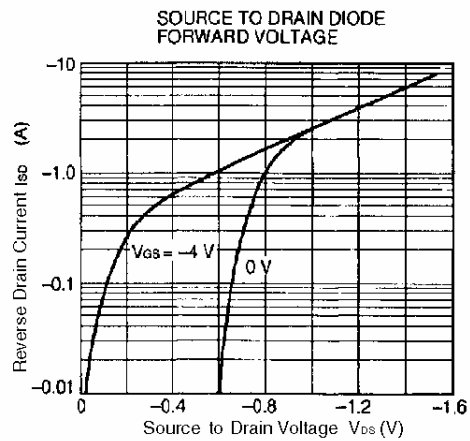
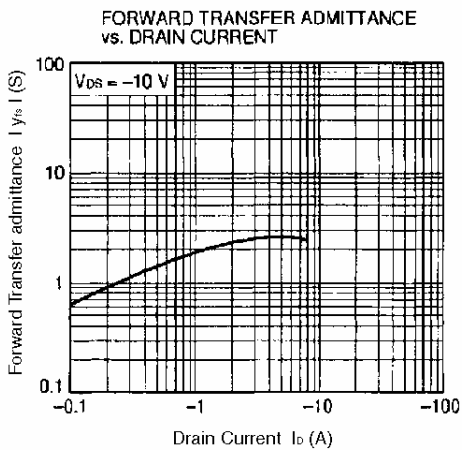
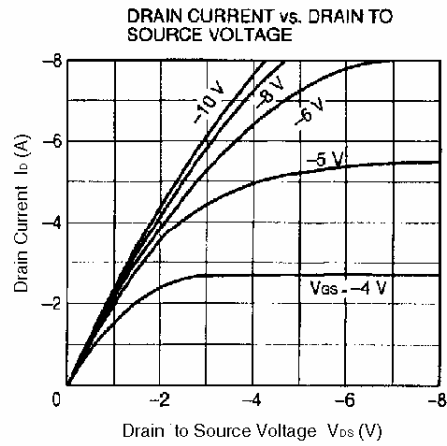
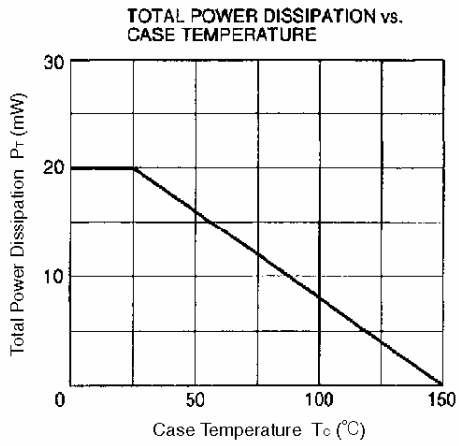
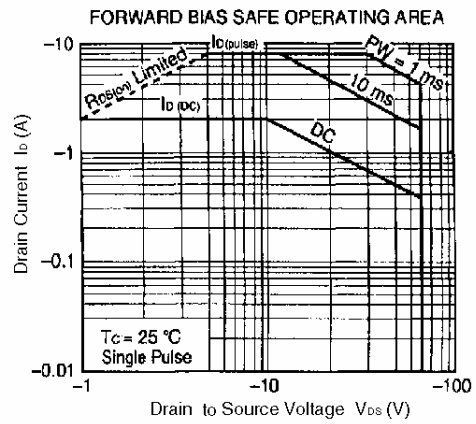
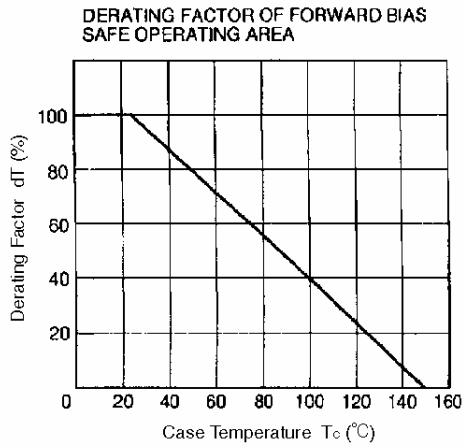
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

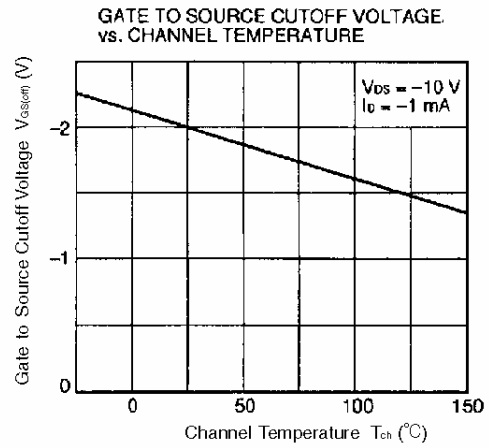
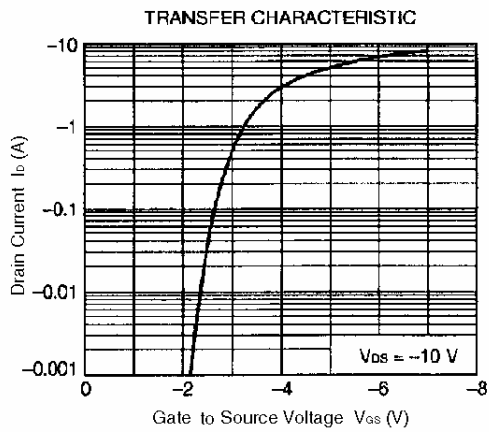
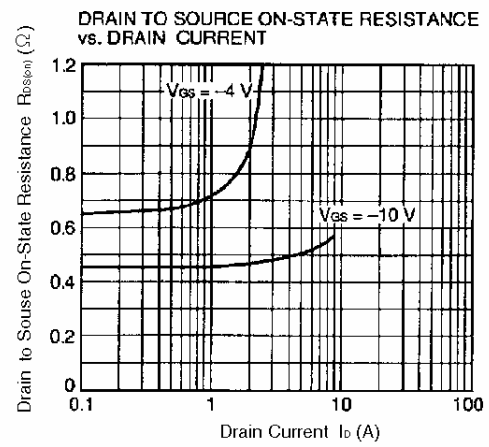
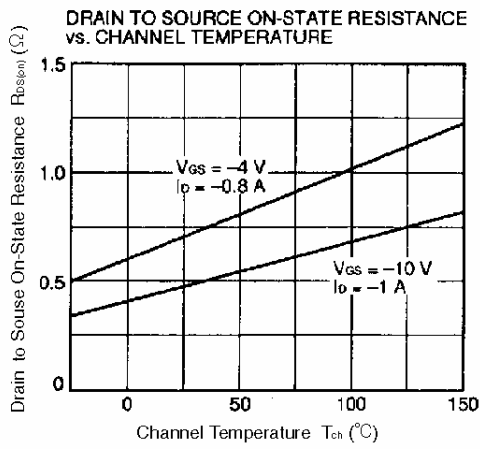
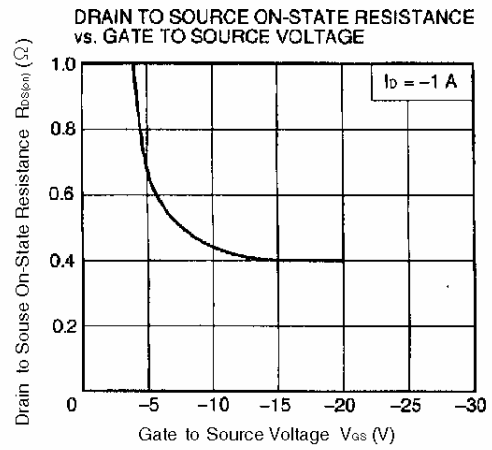
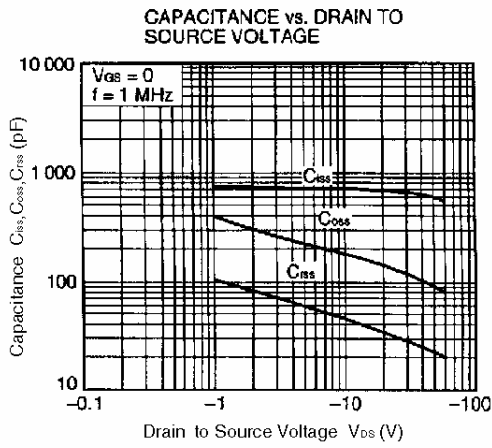
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Drain cutoff current	I _{DSS}	V _{DS} = -60 V, V _{GS} = 0 V			-10	μA
Gate cutoff current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA
Gate cutoff voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1.0 mA	-1.0	-2.0	-3.0	V
Forward transfer admittance	y _{fs}	V _{DS} = -10 V, I _D = -1.0 A	1.0	1.8		S
Drain to source on-state resistance	R _{DS(on)1}	V _{GS} = -10 V, I _D = -1.0 A		0.45	0.8	Ω
Drain to source on-state resistance	R _{DS(on)2}	V _{GS} = -4 V, I _D = -0.8 A		0.7	1.3	Ω
Input capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V		660		pF
Output capacitance	C _{oss}	f = 1 MHz		250		pF
Reverse transfer capacitance	C _{rss}			50		pF
Turn-on delay time	t _{d(on)}	I _D = -1.0 A, V _{GS(on)} = -10 V V _{DD} ≅ -30 V, R _L = 30 Ω, R _{in} = 10 Ω		30		ns
Rise time	t _r			30		ns
Turn-off delay time	t _{d(off)}			110		ns
Fall time	t _f			40		ns

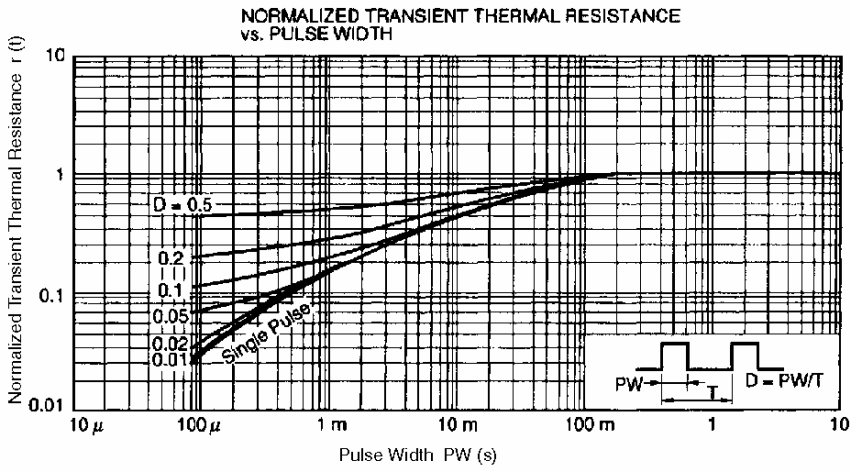
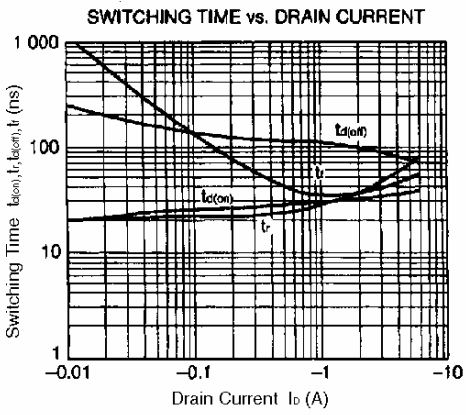
SWITCHING TIME TEST CIRCUIT, TEST CONDITION (RESISTANCE LOAD)



TYPICAL CHARACTERISTICS (T_A = 25°C)







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