

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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# MOS FIELD EFFECT POWER TRANSISTOR

## 2SK1292

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SK1292 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

#### FEATURES

- Low On-state Resistance  
 $R_{DS(on)} \leq 0.08 \Omega$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 10 \text{ A}$ )  
 $R_{DS(on)} \leq 0.1 \Omega$  ( $V_{GS} = 4 \text{ V}$ ,  $I_D = 10 \text{ A}$ )
- Low  $C_{iss}$        $C_{iss} = 2 \text{ 200 pF TYP.}$
- Built-in G-S Gate Protection Diode

#### QUALITY GRADE

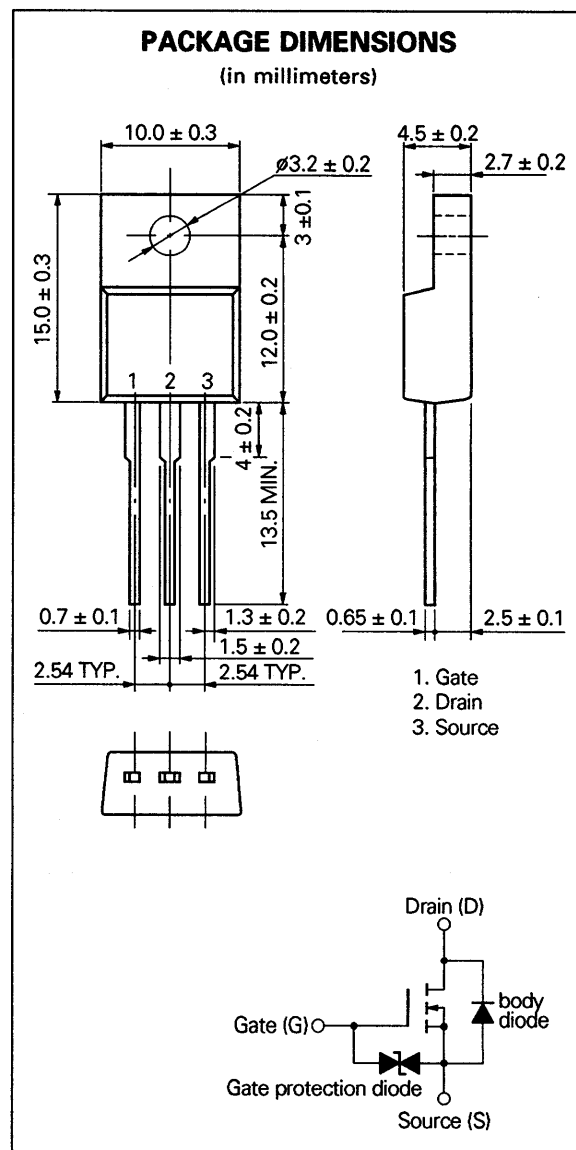
Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

#### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25 \text{ }^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	100	V
Gate to Source Voltage	$V_{GSS(AC)}$	$\pm 20$	V
Drain Current (DC)	$I_D(DC)$	$\pm 20$	A
Drain Current (pulse)	$I_D(\text{pulse})^*$	$\pm 80$	A
Total Power Dissipation ( $T_c = 25 \text{ }^\circ\text{C}$ )	$P_{T1}$	35	W
Total Power Dissipation ( $T_a = 25 \text{ }^\circ\text{C}$ )	$P_{T2}$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

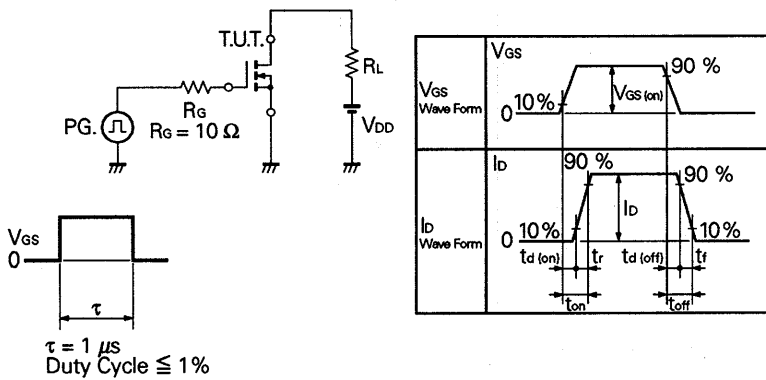
\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1 \%$



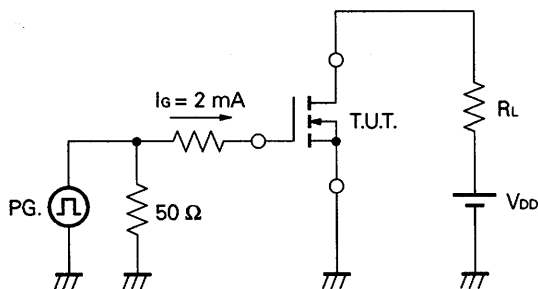
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.07	0.08	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A
Drain to Source On-state Resistance	R <sub>DS(on)</sub>		0.08	0.1	Ω	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 10 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	12			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A
Drain Leakage Current	I <sub>DSS</sub>			10	μA	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		2 200		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		550		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>res</sub>		90		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		25		ns	V <sub>GS(on)</sub> = 10 V V <sub>DD</sub> = 50 V I <sub>D</sub> = 15 A, R <sub>G</sub> = 10 Ω R <sub>L</sub> = 3.3 Ω
Rise Time	t <sub>r</sub>		160		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>		200		ns	
Fall Time	t <sub>f</sub>		150		ns	
Total Gate Charge	Q <sub>G</sub>		50		nC	V <sub>GS</sub> = 10 V I <sub>D</sub> = 30 A V <sub>DD</sub> = 80 V
Gate to Source Charge	Q <sub>GS</sub>		10		nC	
Gate to Drain Charge	Q <sub>GD</sub>		10		nC	
Diode Forward Voltage	V <sub>SD</sub>		1.1		V	I <sub>SD</sub> = 20 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		200		ns	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q <sub>rr</sub>		550		nC	

**Test Circuit 1: Switching Time**

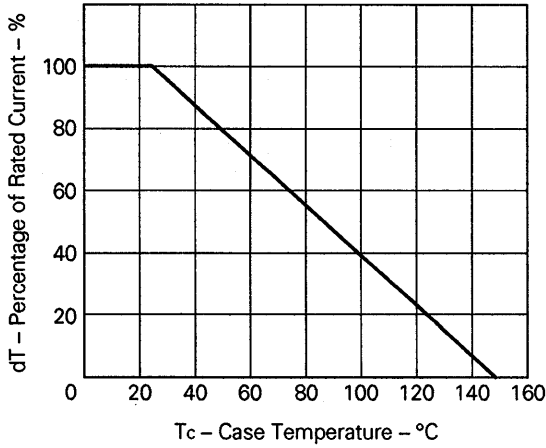


**Test Circuit 2: Gate Charge**

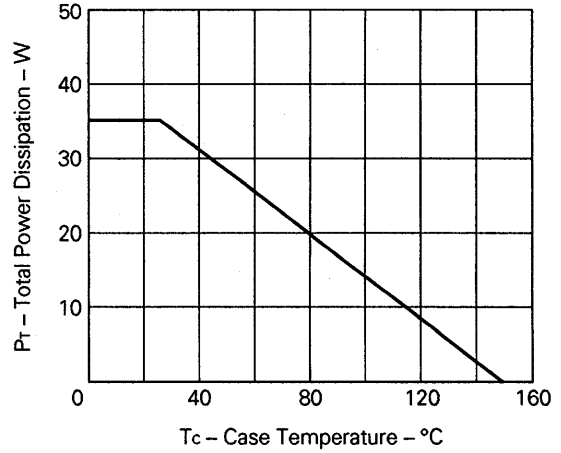


TYPICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)

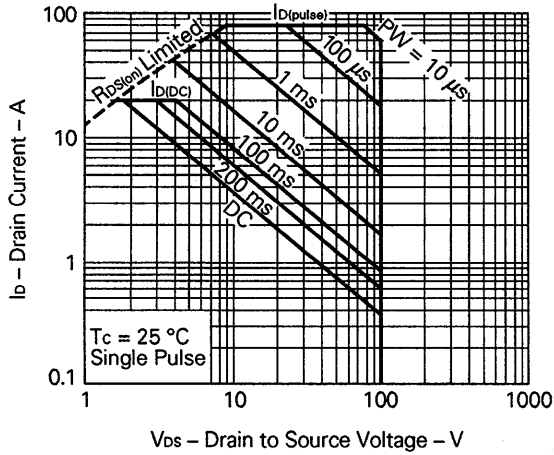
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



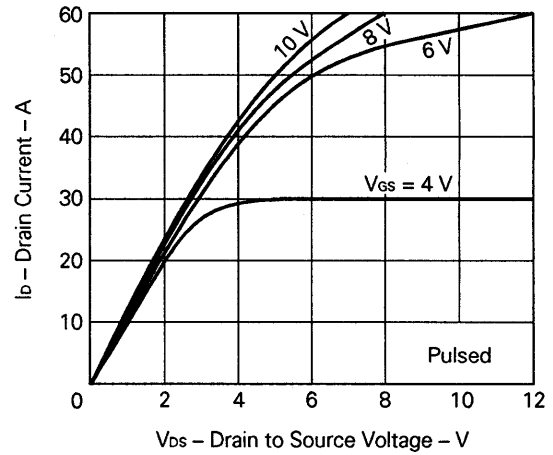
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



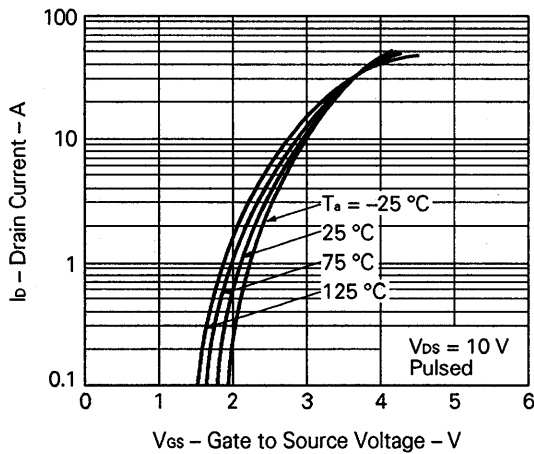
FORWARD BIAS SAFE OPERATING AREA



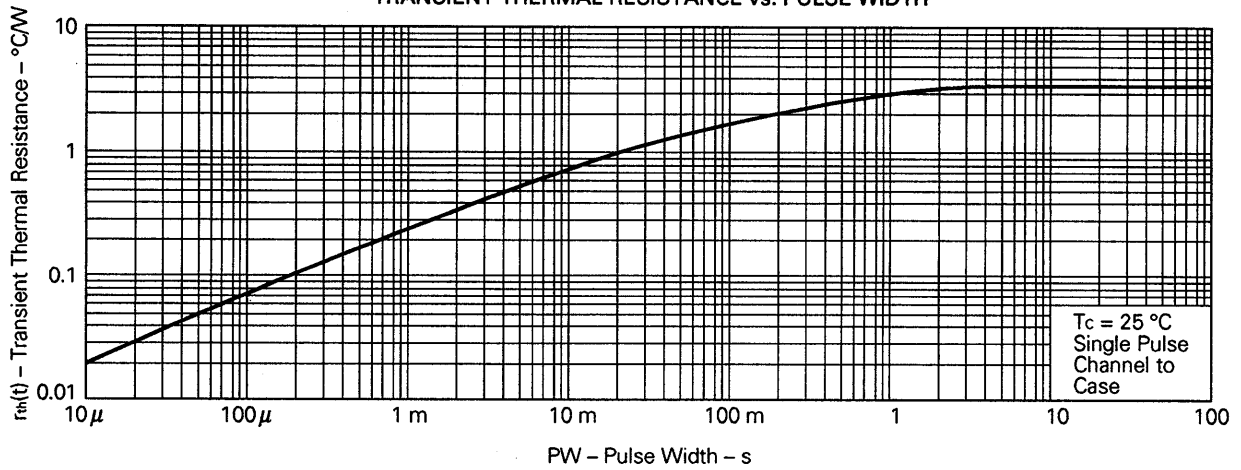
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



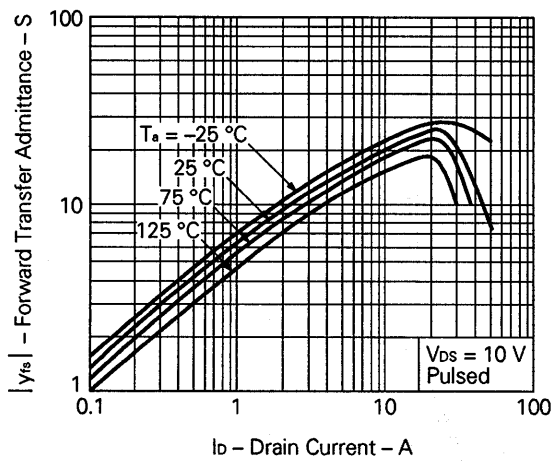
TRANSFER CHARACTERISTICS



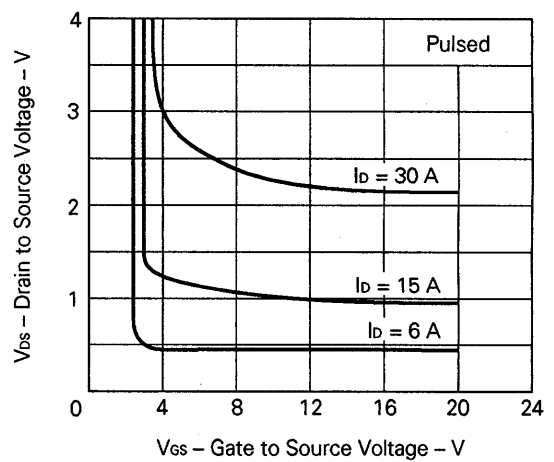
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



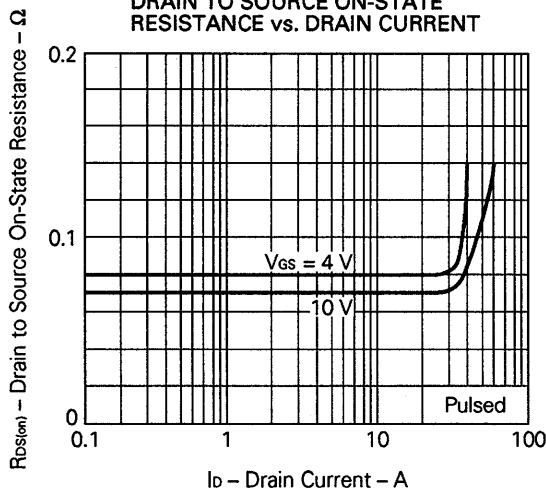
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



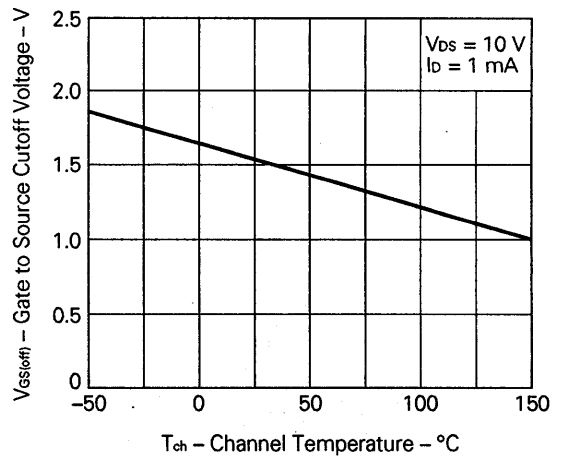
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE

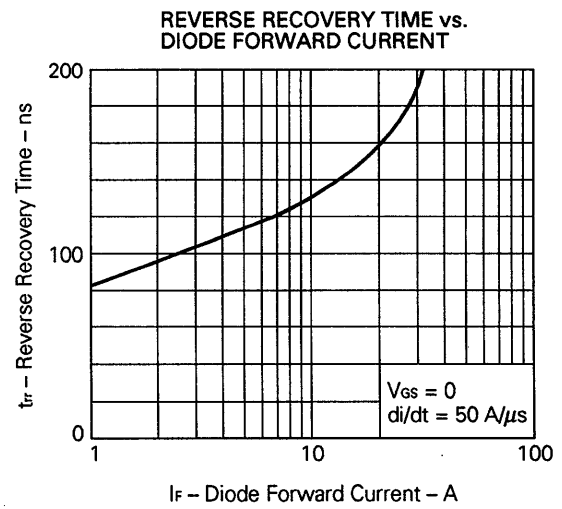
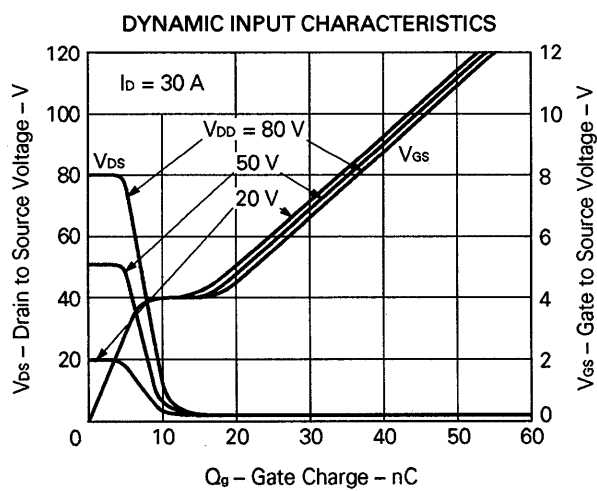
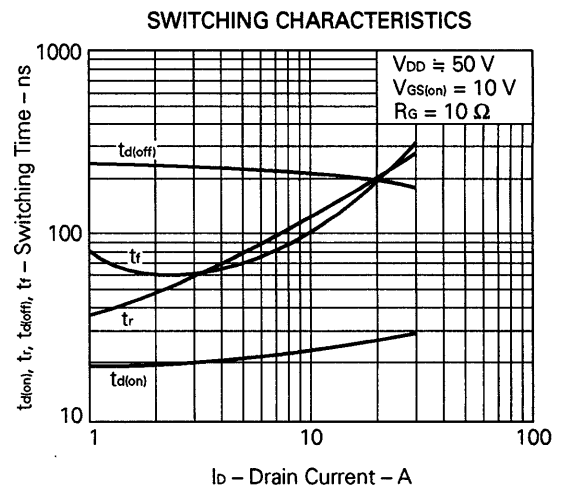
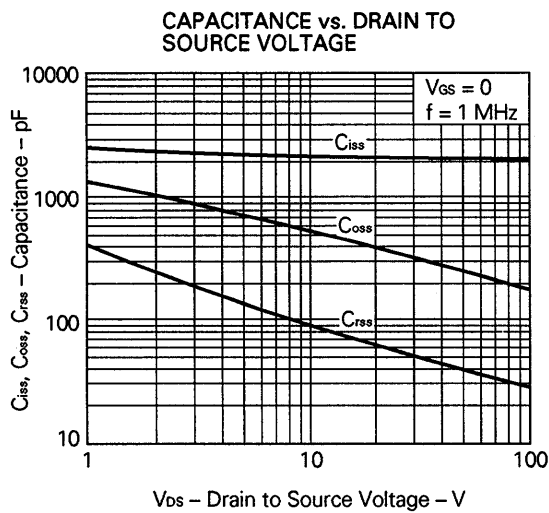
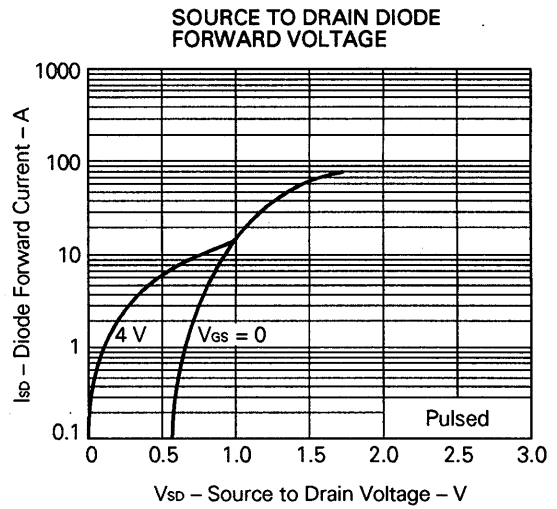
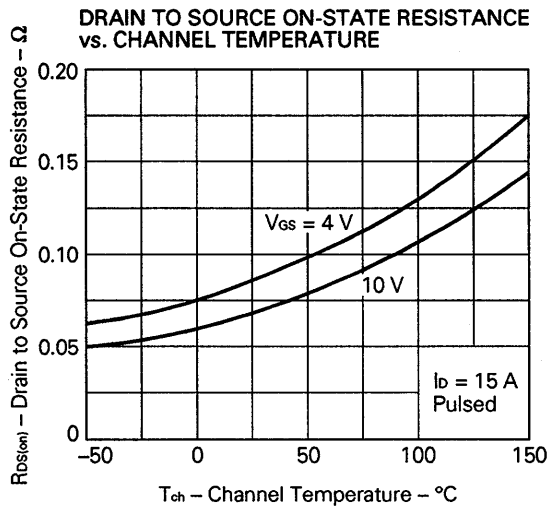


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207



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