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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Phase-out/Discontinued

2SK1595

**SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE**

DESCRIPTION

The 2SK1595 is N-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 30 \text{ m}\Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$)
 $R_{DS(on)} \leq 50 \text{ m}\Omega$ ($V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$)
- Low C_{iss} $C_{iss} = 2\,000 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diode

QUALITY GRADE

Standard

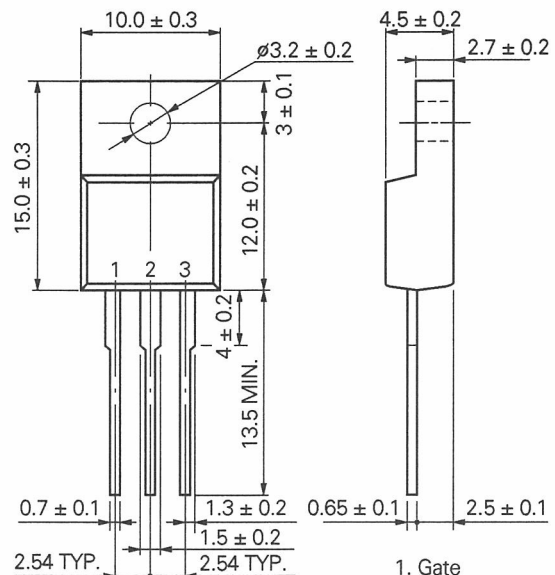
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25 \text{ }^\circ\text{C}$)

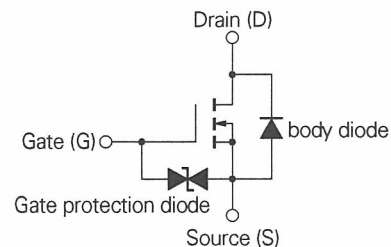
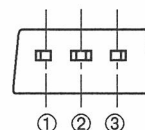
Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	$V_{GSS(AC)}$	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 30	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 120	A
Total Power Dissipation ($T_c = 25 \text{ }^\circ\text{C}$)	P_{T1}	35	W
Total Power Dissipation ($T_a = 25 \text{ }^\circ\text{C}$)	P_{T2}	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

* $PW \leq 10 \text{ } \mu\text{s}$, Duty Cycle $\leq 1 \%$

PACKAGE DIMENSIONS
(in millimeters)



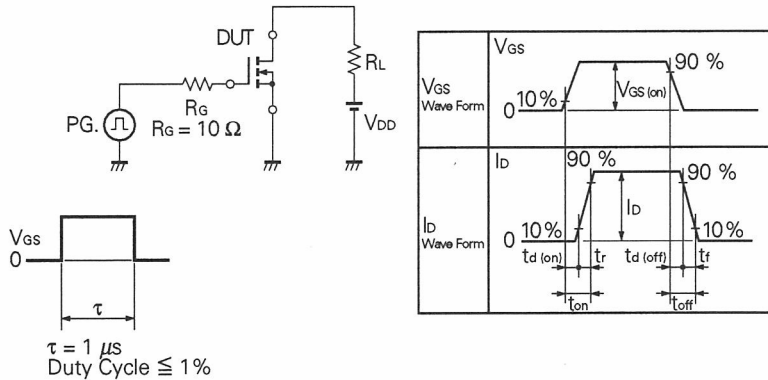
- 1. Gate
- 2. Drain
- 3. Source



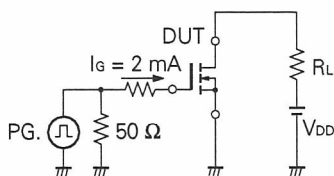
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		22	30	mΩ	V _{GS} = 10 V, I _D = 15 A
Drain to Source On-state Resistance	R _{DS(on)}		30	50	mΩ	V _{GS} = 4 V, I _D = 15 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0		2.5	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	12	25		S	V _{DS} = 10 V, I _D = 15 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = 30 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		2 000		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		1 200		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		400		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		45		ns	V _{GS(on)} = 10 V V _{DD} = 15 V I _D = 15 A, R _G = 10 Ω R _L = 1.0 Ω
Rise Time	t _r		500		ns	
Turn-Off Delay Time	t _{d(off)}		270		ns	
Fall Time	t _f		220		ns	
Total Gate Charge	Q _G		55		nC	V _{GS} = 10 V I _D = 30 A V _{DD} = 24 V
Gate to Source Charge	Q _{GS}		10		nC	
Gate to Drain Charge	Q _{GD}		20		nC	
Diode Forward Voltage	V _{SD}		1.1		V	I _F = 30 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		75		ns	I _F = 30 A, V _{GS} = 0 di/dt = 50 A/μs
Reverse Recovery Charge	Q _{rr}		100		nC	

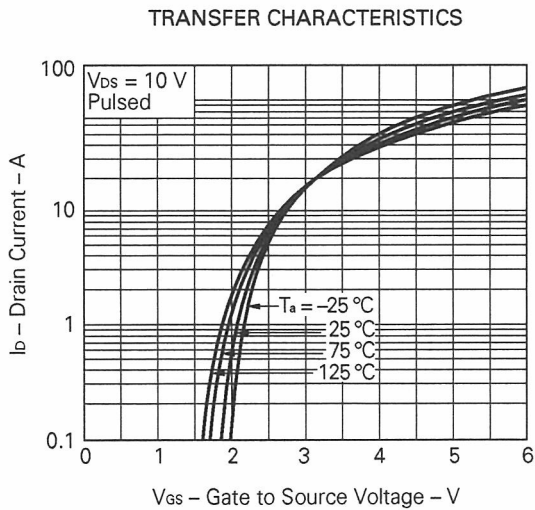
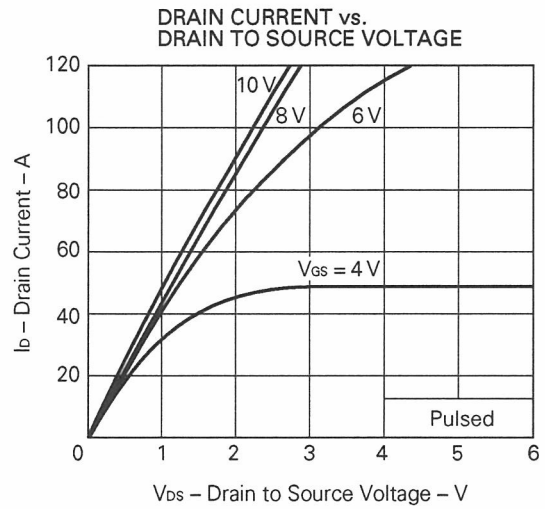
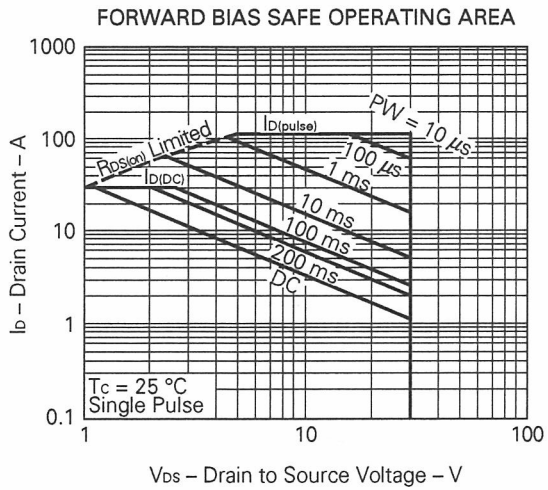
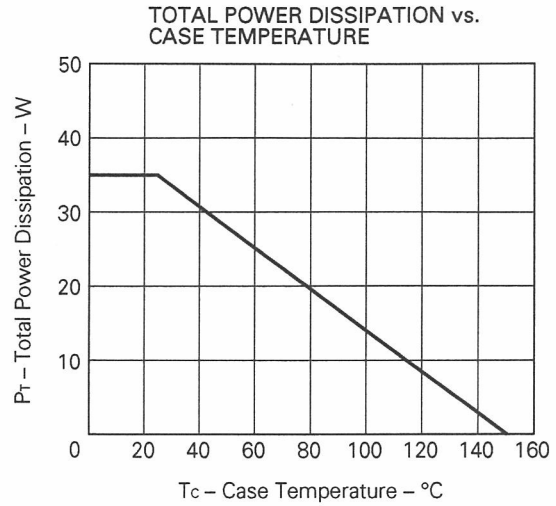
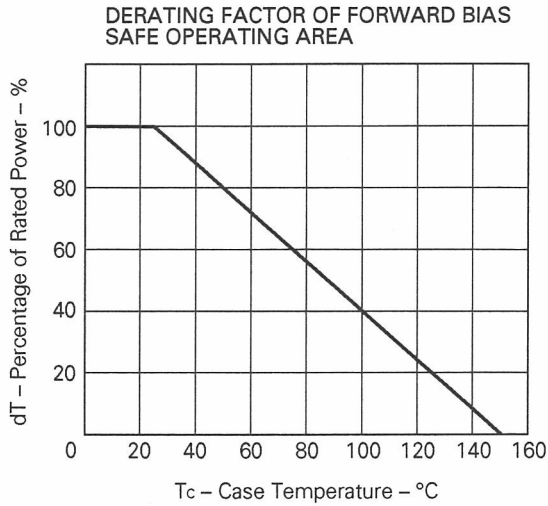
Test Circuit 1: Switching Time



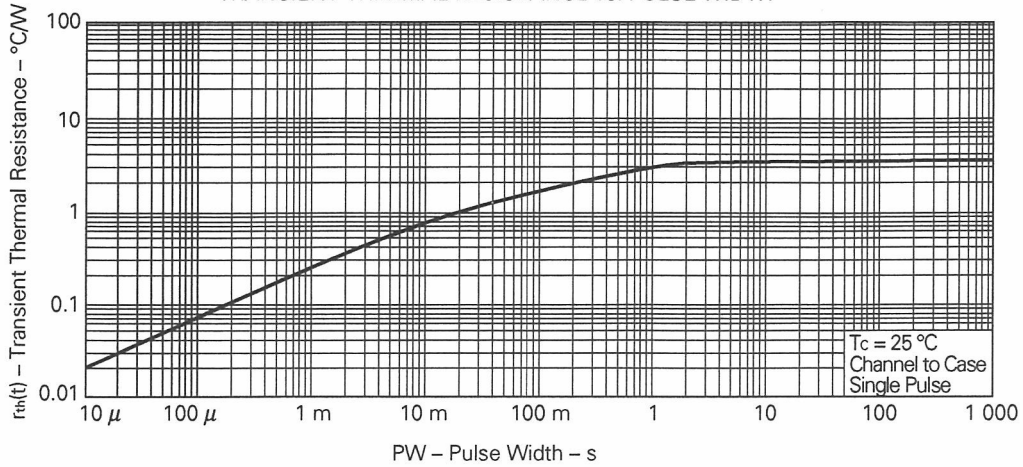
Test Circuit 2: Gate Charge



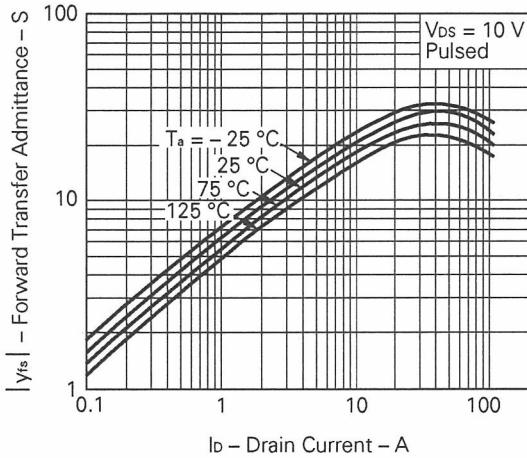
TYPICAL CHARACTERISTICS (T_a = 25 °C)



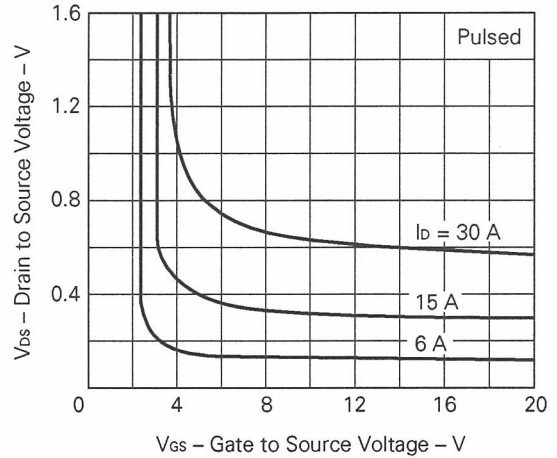
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



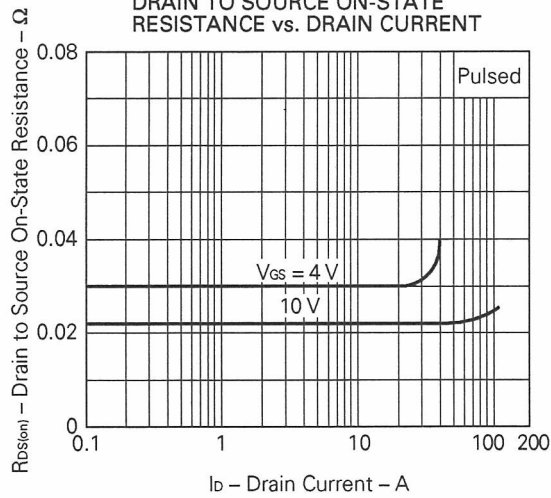
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



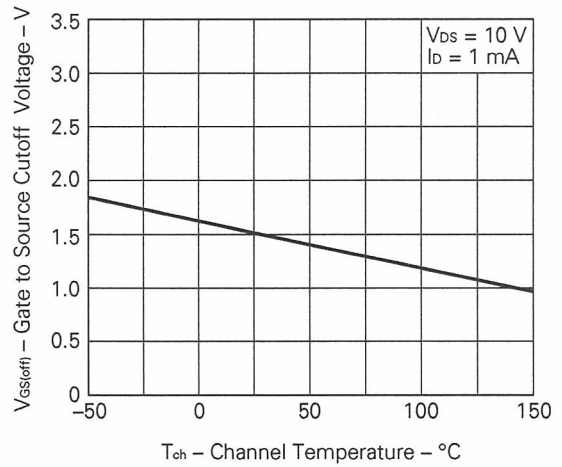
DRAIN TO SOURCE VOLTAGE vs. GATE TO SOURCE VOLTAGE

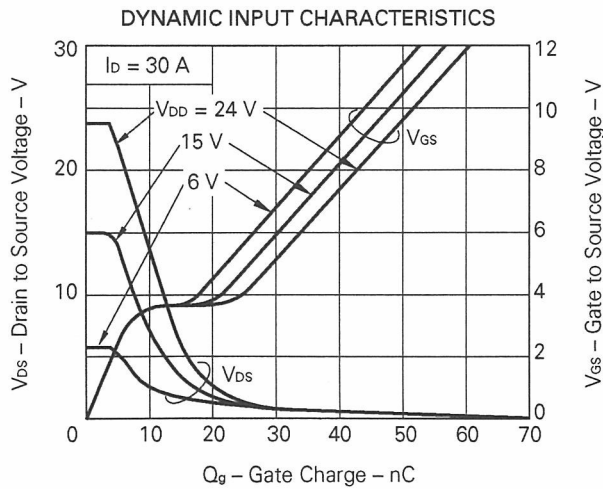
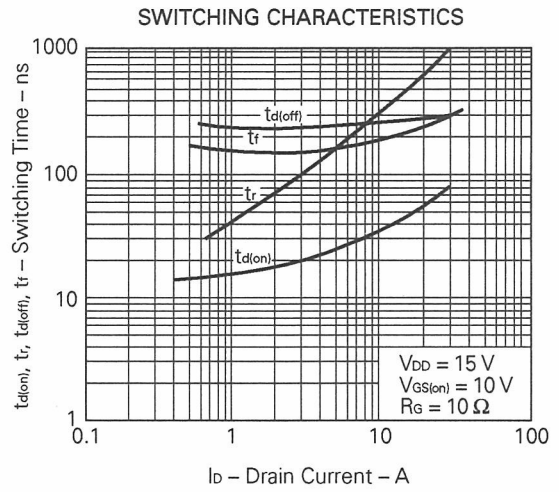
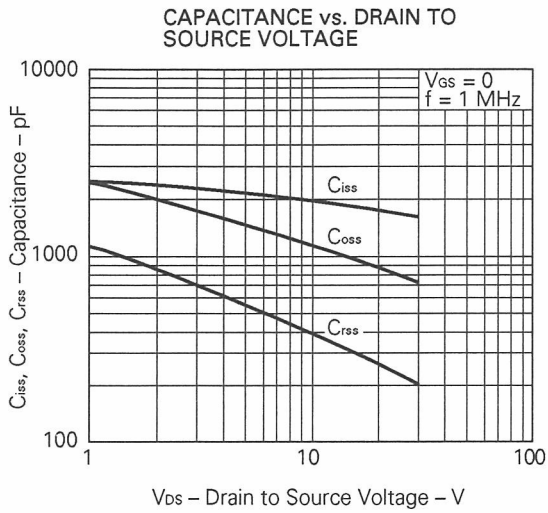
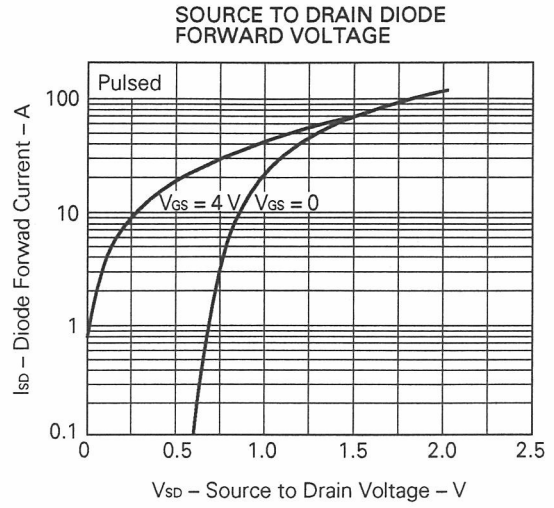
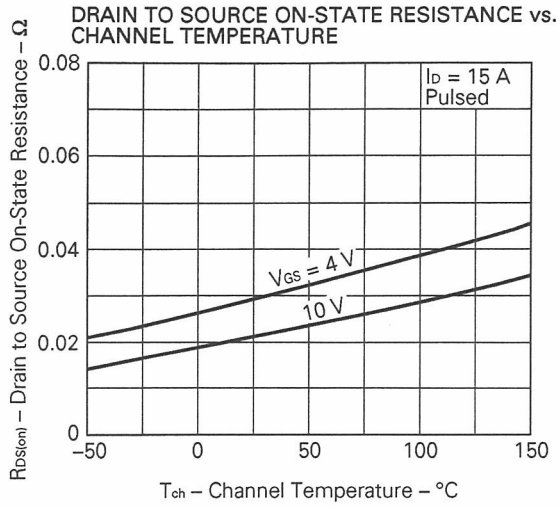


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

[MEMO]

Phase-out/Discontinued

[MEMO]

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