To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

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RENESAS

DATA SHEET

MOS FIELD EFFECT TRANSISTOR

2SK1954,1954-Z

Phase-out/Discontinued

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK1954 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 0.65 Ω MAX. (V_{GS} = 10 V, I_D = 2.0 A)
- Low C_{iss}: C_{iss} = 300 pF TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

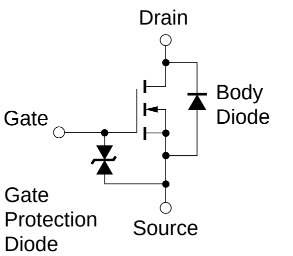
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	180	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±4.0	A
Drain Current (pulse) Note 1	$I_{D(pulse)}$	±16	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	20	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note 2	I_{AS}	4.0	A
Single Avalanche Energy Note 2	E_{AS}	44.3	mJ

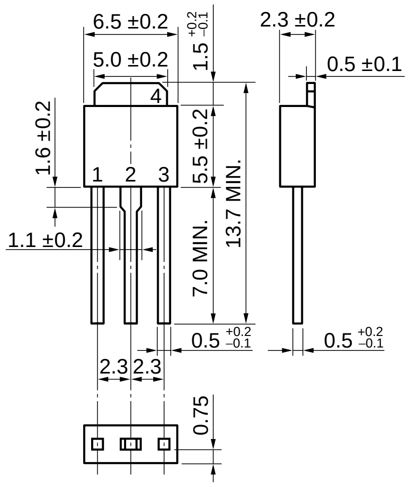
Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 → 0 V

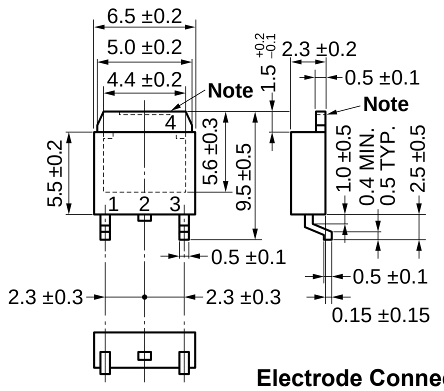
EQUIVALENT CIRCUIT



PACKAGE DRAWINGS (Unit: mm)



<R> TO-251 (MP-3)



TO-252 (MP-3Z)

Electrode Connection
1. Gate
2. Drain
3. Source
4. Drain Fin

Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

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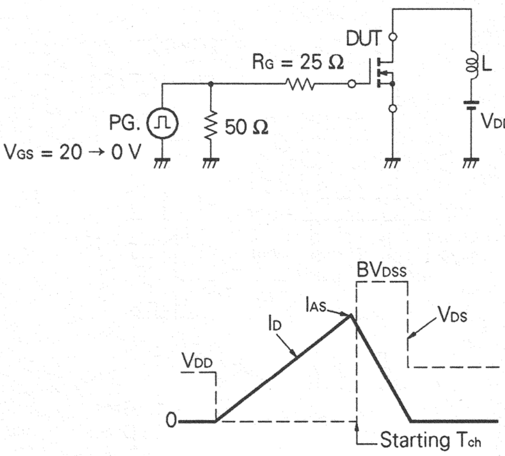
Date Published January 2007 NS CP(K)
Printed in Japan

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

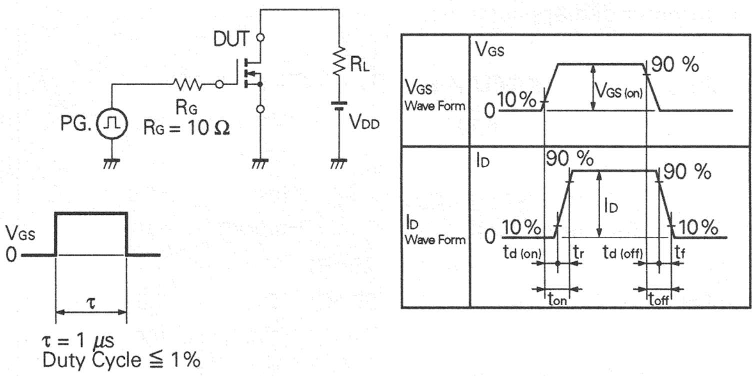
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.52	0.65	Ω	V_{GS} = 10 V, I_D = 2.0 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.0		4.0	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	0.5			S	V_{DS} = 10 V, I_D = 2.0 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 180 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±20 V, V_{DS} = 0
Input Capacitance	C_{iss}		300		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		170		pF	
Reverse Transfer Capacitance	C_{rss}		50		pF	
Turn-On Delay Time	$t_{d(on)}$		9		ns	V_{GS} = 10 V V_{DD} = 100 V I_D = 2.0 A, R_G = 10 Ω R_L = 50 Ω
Rise Time	t_r		10		ns	
Turn-Off Delay Time	$t_{d(off)}$		28		ns	
Fall Time	t_f		12		ns	
Total Gate Charge	Q_G		10		nC	V_{GS} = 10 V I_D = 4.0 A V_{DD} = 140 V
Gate to Source Charge	Q_{GS}		2.3		nC	
Gate to Drain Charge	Q_{GD}		4.7		nC	
Diode Forward Voltage	$V_{F(S-D)}$		0.9		V	I_F = 4.0 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		180		ns	I_F = 4.0 A di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		0.5		μC	

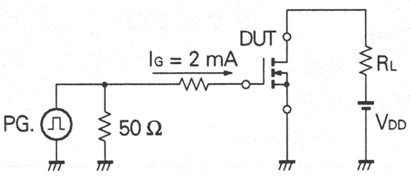
Test Circuit 1: Avalanche Capability



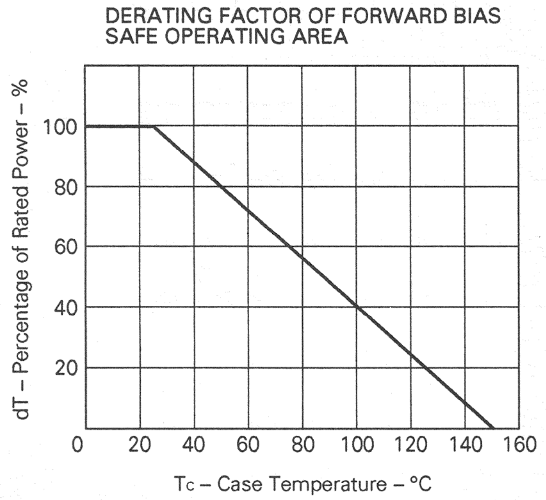
Test Circuit 2: Switching Time

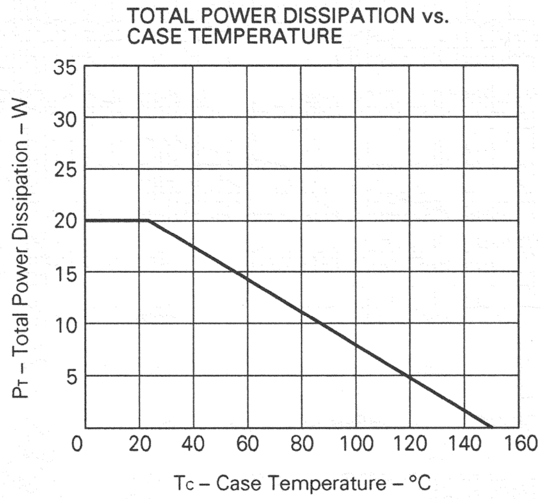


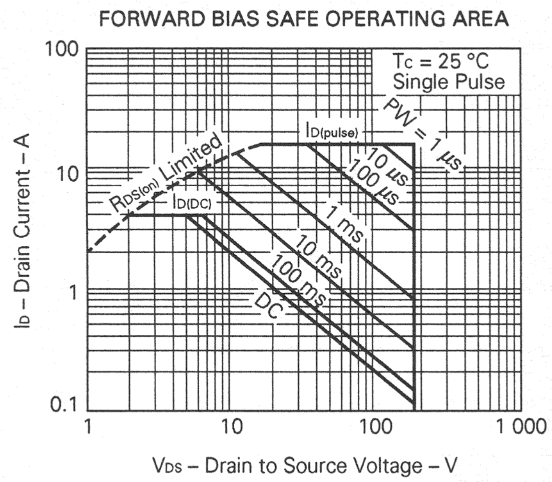
Test Circuit 3: Gate Charge

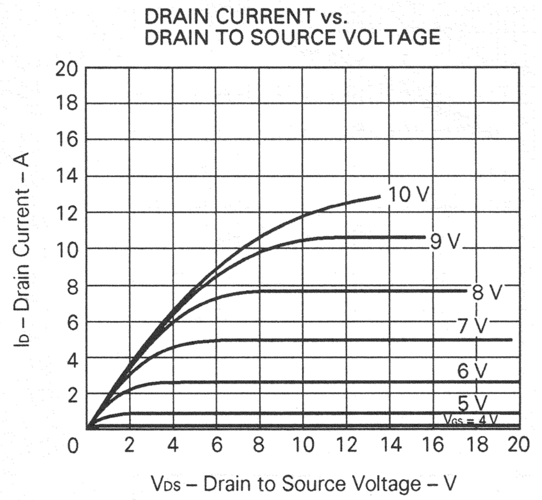


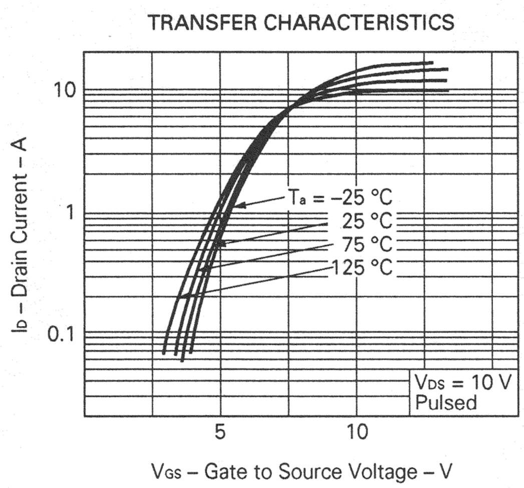
TYPICAL CHARACTERISTICS (T_a = 25 °C)



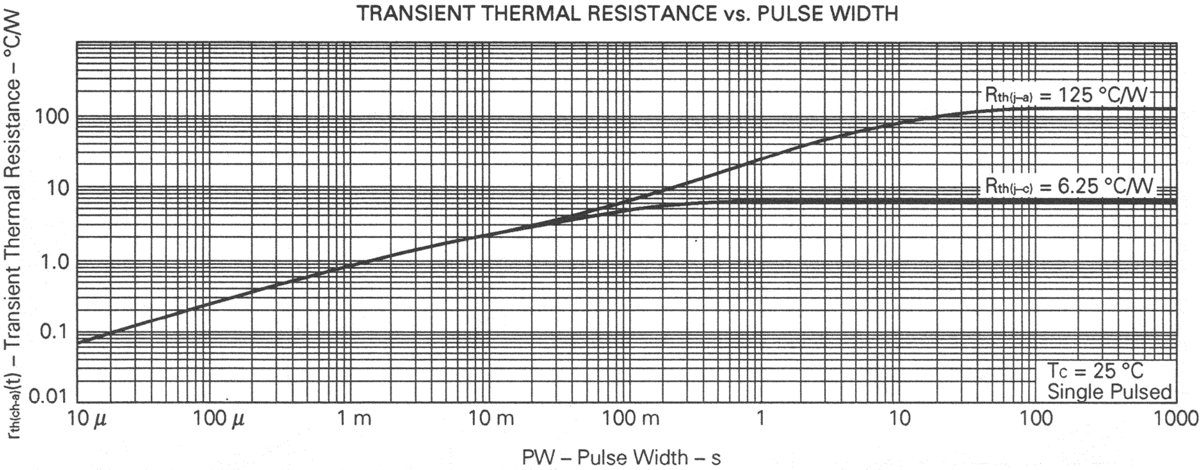




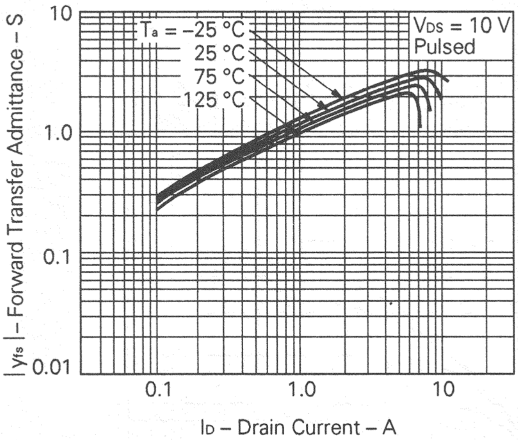




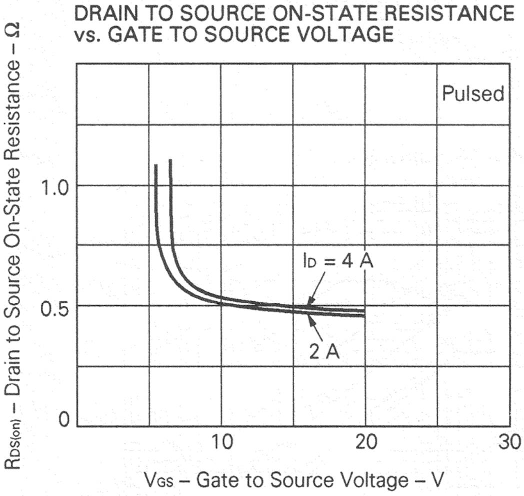
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



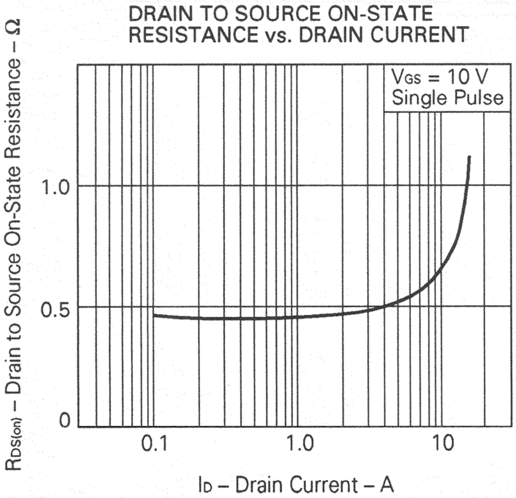
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



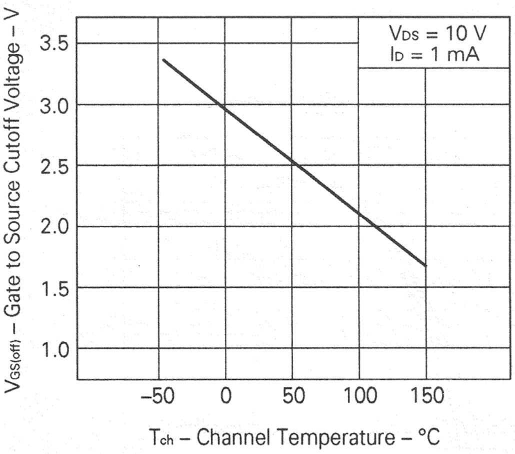
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



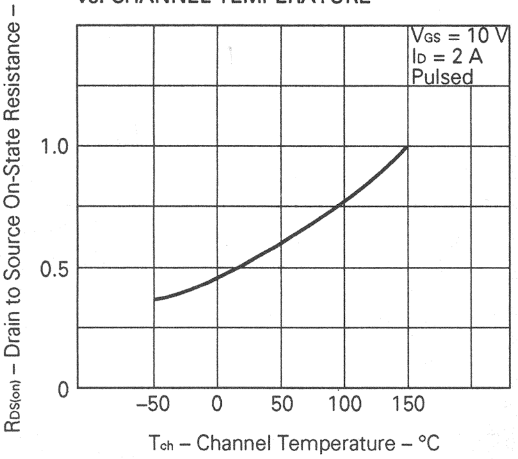
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



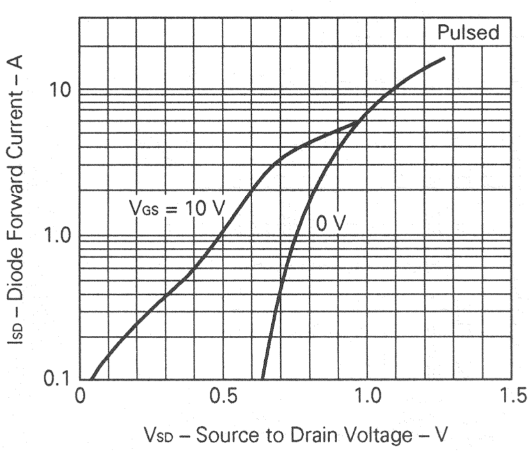
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



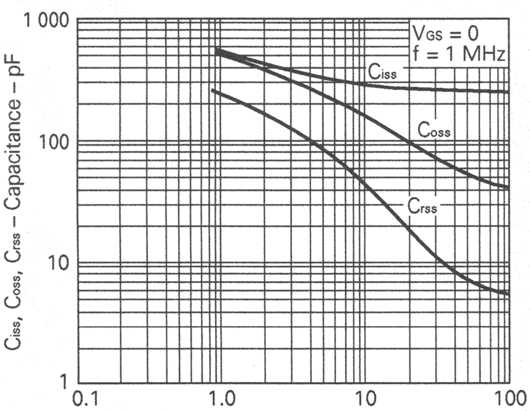
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



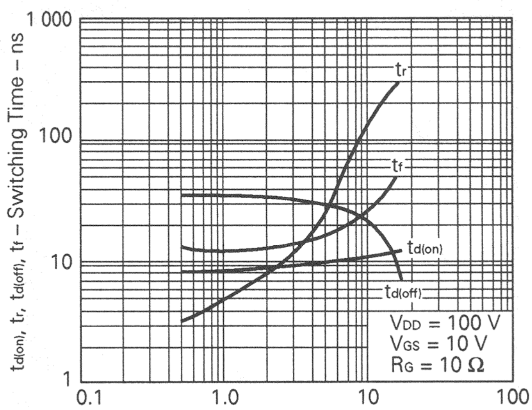
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



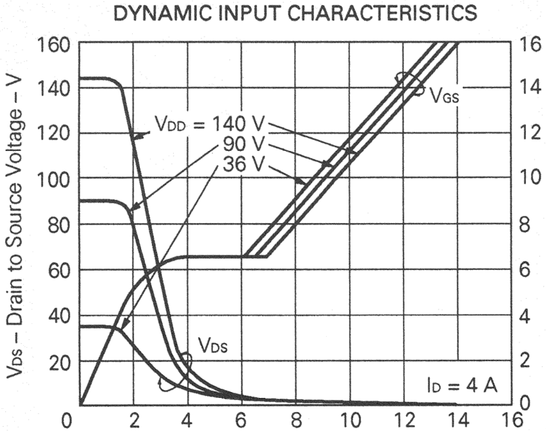
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



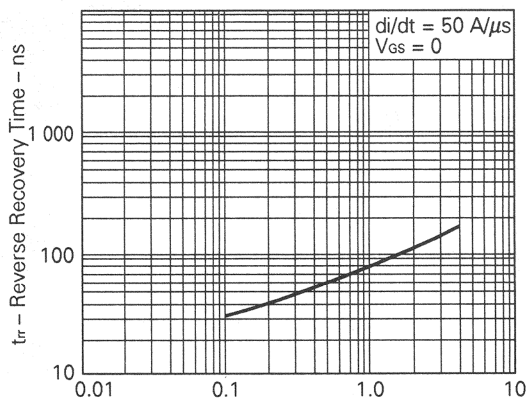
SWITCHING CHARACTERISTICS



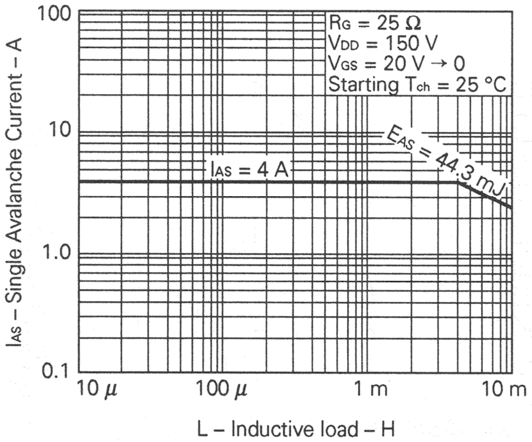
DYNAMIC INPUT CHARACTERISTICS



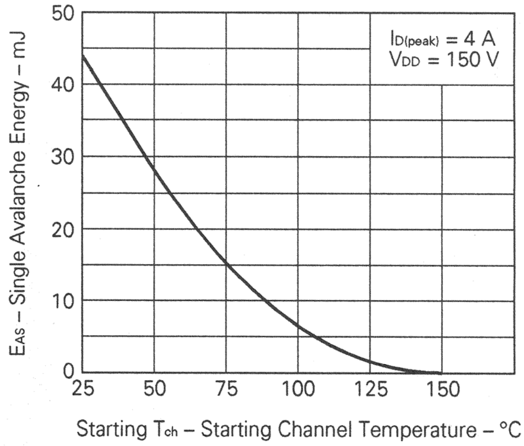
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



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