Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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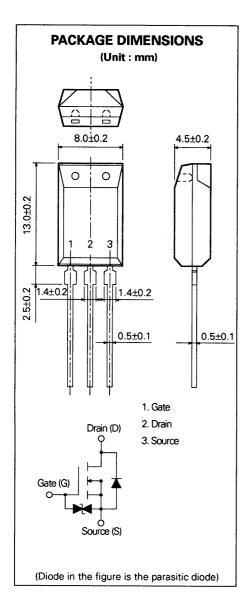
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MOS FIELD EFFECT POWER TRANSISTOR 2SK2132

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE



DESCRIPTION

The 2SK2132 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 R_{DS(on)} = 0.65 Ω MAX. (V_{GS} = 10 V, I_D = 2.0 A)
- Low Ciss Ciss = 300 pF TYP.
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS

Maximum T	emperatures		
Storage T	-55 to +150	°C	
Channel Temperature		150	°C MAX.
Maximum P	ower Dissipation		
Total Pow	1.8	W	
Maximum V	oltages and Currents ($T_a = 25$ °C)		
Voss	Drain to Source Voltage	180	V
Vgss	Gate to Source Voltage	±20	V
ID(DS)	Drain Current (DC)	±4.0	Α
D(pulse)*	Drain Current (pulse)	±16	Α
Maximum A	valanche Capability Ratings**		
las	Single Avalanche Current	4.0	Α
Eas	Single Avalanche Energy	51.2	mJ
* 514/ - 0	0 - 0 - 0 - 1 4 0/		

^{*} PW \leq 10 μ s , Duty Cycle \leq 1 %

^{**} Starting $T_{ch} = 25$ °C, $R_G = 25 \Omega$, $V_{GS} = 20 V \rightarrow 0$

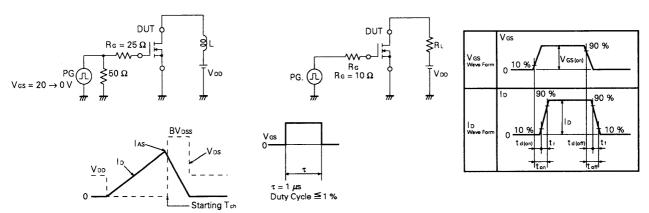


ELECTRICAL CHARACTERISTICS (Ta = 25 °C)

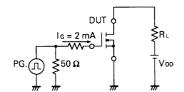
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drian to Source On-state Resistance	Ros (on)		0.52	0.65	Ω	Vgs = 10 V, ID = 18 A	
Gate to Source Cutoff Voltage	V gs (off)	2.0		4.0	V	Vos = 10 V, Io = 1 mA	
Forward Transfer Admittance	yfs	0.5			S	V DS = 10 V, I D = 18 A	
Drain Leakage Current	loss			100	μΑ	V DS = 500 V, V GS = 0	
Gate to Source Leakage Current	lgss			±10	μΑ	$V_{GS} = \pm 20 \text{ V, } V_{DS} = 0$	
Input Capacitance	Ciss		300		pF	Vps = 10 V Vps = 0 f = 1 MHz	
Output Capacitance	Coss		170		pF		
Reverse Transfer Capacitance	Ства		50		pF		
Turn-On Delay Time	ta (on)		9.0		ns	V _{GS} = 10 V	
Rise Time	tr		10		ns	V _{DD} = 100 V	
Turn-Off Delay Time	ta (off)		28		ns	ID = 2 A, RG = 10 Ω RL = 50 Ω	
Fall Time	tr		12		ns		
Total Gate Charge	QG		10		nC	V _{GS} = 10 V	
Gate to Source Charge	Qgs		2.3		nC	lo = 2 A	
Gate to Drain Charge	Q _{GD}		4.7		nC	V _{DD} = 140 V	
Diode Forward Voltage	V F(S-D)		0.9		٧	IF = 2 A, VGS = 0	
Reverse Recovery Time	trr		180		ns	IF = 2 A	
Reverse Recovery Charge	Qrr		0.5		μC	$di / dt = 50 A/\mu s$	

Test Circuit 1: Avalanche Capability Te

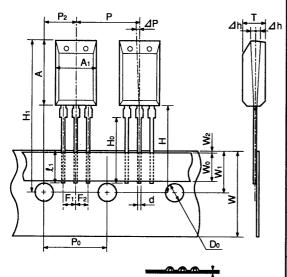
Test Circuit 2: Switching Time



Test Circuit 3: Gate Charge



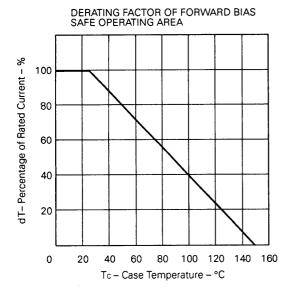
Radial Tape Specification



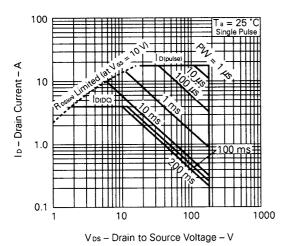
Dimension (unit: mm)

ltem		
Component Body Length along Tape	A ₁	8.0 ± 0.2
Component Body Height	Α	13.0 ± 0.2
Component Body Width	Т	4.5 ± 0.2
Component Lead Width Dimension	d	0.5 ± 0.1
Lead Wire Enclosure	l1	2.5 MIN.
Component Center Pitch	Р	12.7 ± 1.0
Feedhole Pitch	Po	12.7 ± 0.3
Feedhole Center to Center Lead	P ₂	6.35 ± 0.5
Component Lead Pitch	F1, F2	2.5 + 0.4 - 0.1
Deflection Front or Rear	⊿h	± 1.0
Deflection Left or Right	⊿P	± 1.3
Carrier Strip Width	w	18.0 ⁺ 1.0 - 0.5
Adhesive Tape Width	Wo	5.0 MIN.
Feedhole Location	W ₁	9.0 ± 0.5
Adhesive Tape Position	W ₂	0.7 MIN.
Height of Seating Plane	Н₀	16.0 ± 0.5
Feedhole to upper of Component	H1	32.2 MAX.
Feedhole to Bottom of Component	Н	20.0 MAX.
Tape Feedhole Diameter	Do	4.0 ± 0.2
Overall Taped Package Thickness	t	0.7 ± 0.2

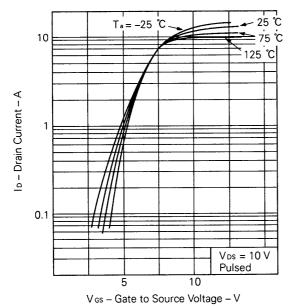
TYPICAL CHARACTERISTICS (T₈ = 25 °C)

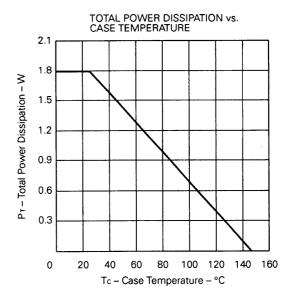


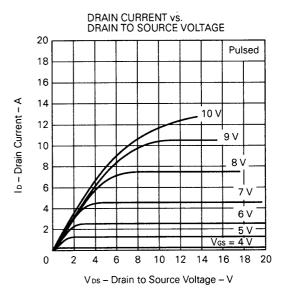




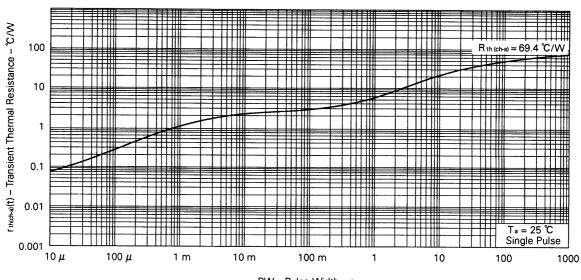
TRANSFER CHARACTERISTICS





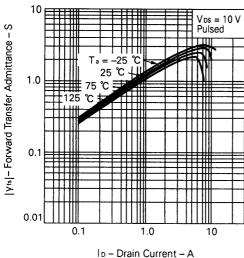


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

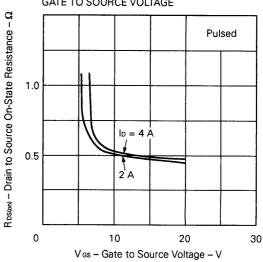


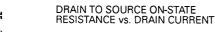
PW - Pulse Width - s

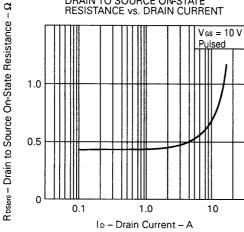


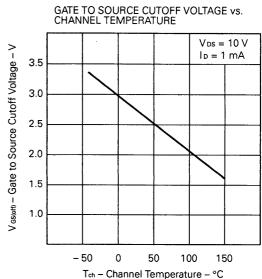


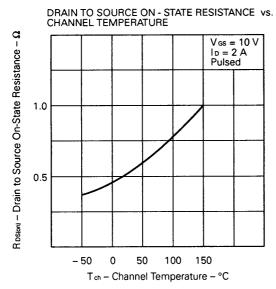
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

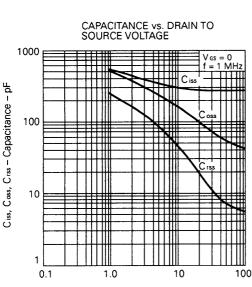


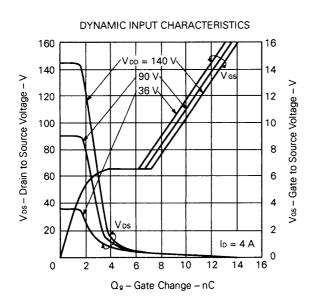




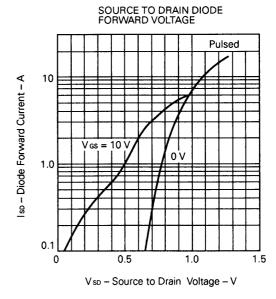


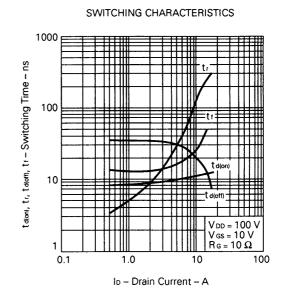


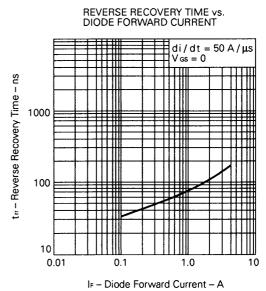


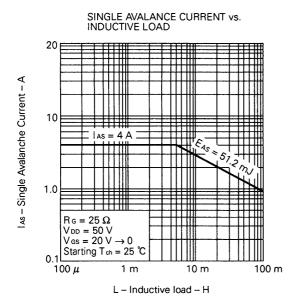


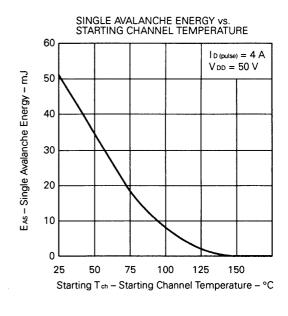
V_{DS} - Drain to Source Voltage - V











[MEMO]

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