

Description

The IDT5P49EE502 is a programmable clock generator intended for low power, battery operated consumer applications. There are four internal PLLs, each individually programmable, allowing for up to five different output frequencies. The frequencies are generated from a single reference clock. The reference clock can come from either a TCXO or fundamental mode crystal.

The IDT5P49EE502 can be programmed through the use of the I²C interfaces. The programming interface enables the device to be programmed when it is in normal operation or what is commonly known as in system programmable. An internal EEPROM allows the user to save and restore the configuration of the device without having to reprogram it on power-up.

Each of the four PLLs has an 8-bit reference divider and a 11-bit feedback divider. This allows the user to generate four unique non-integer-related frequencies. The PLL loop bandwidth is programmable to allow the user to tailor the PLL response to the application. For instance, the user can tune the PLL parameters to minimize jitter generation or to maximize jitter attenuation. Spread spectrum generation is supported on one of the PLLs.

Spread spectrum generation is supported on one of the PLLs. The device is specifically designed to work with display applications to ensure that the spread profile remains consistent for each HSYNC in order to reduce ROW noise. It also may operate in standard spread spectrum mode.

There are total five 8-bit output dividers. The outputs are connected to the PLLs via the switch matrix. The switch matrix allows the user to route the PLL outputs to any output bank. This feature can be used to simplify and optimize the board layout. In addition, each output's slew rate and enable/disable function can be programmed.

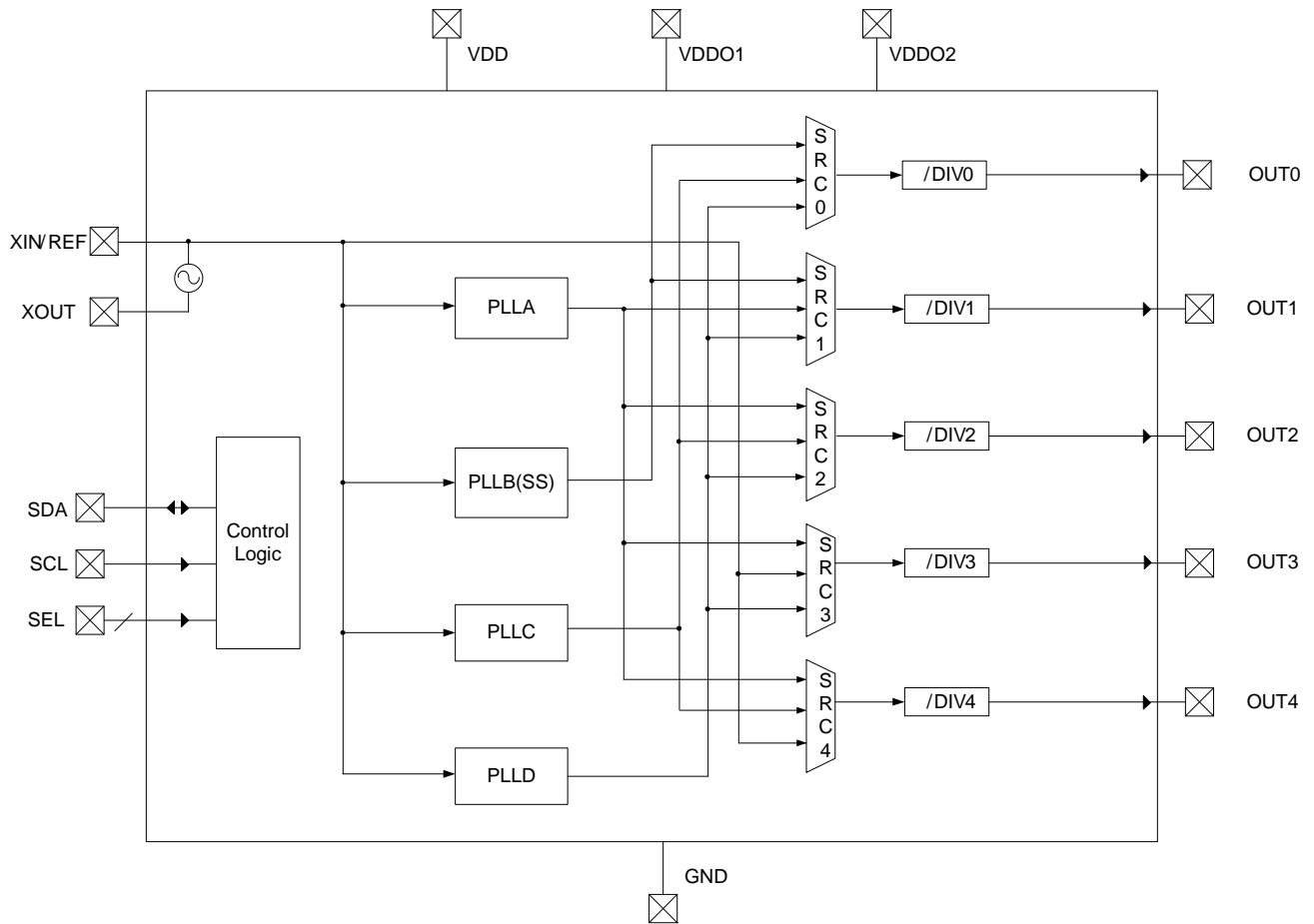
Target Applications

- Smart Mobile Handset
- Personal Navigation Device (PND)
- Camcorder
- DSC
- Portable Game Console
- Personal Media Player

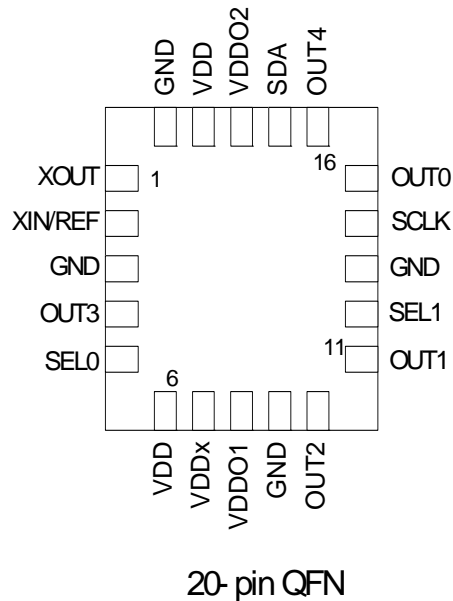
Features

- Four internal PLLs
- Internal non-volatile EEPROM
 - Internal I²C EEPROM master interface
- FAST (400kHz) mode I²C serial interfaces
- Input Frequencies
 - TCXO: 10 MHz to 40 MHz
 - Crystal: 8 MHz to 30 MHz
- Output Frequency Ranges: kHz to 120 MHz
- Each PLL has an 8-bit reference divider and a 11-bit feedback-divider
- 8-bit output-divider blocks
- One of the PLLs support Spread Spectrum generation capable of configuration to pixel rate, with adjustable modulation rate and amplitude to support video clock with no visible artifacts
- I/O Standards:
 - Outputs - 1.8V/2.5V/3.3 V LVTTTL/ LVCMOS
- 2 independent adjustable VDDO groups.
- Programmable Slew Rate Control
- Programmable Loop Bandwidth Settings
- Programmable output inversion to reduce bimodal jitter
- Individual output enable/disable
- Power-down/Sleep mode
 - 10µA max in power down mode
- 1.8V VDD Core Voltage
- Available in 20pin 3x3mm QFN packages
- -40 to +85 C Industrial Temp operation

Functional Block Diagram



Pin Assignment



Pin Descriptions

| Pin Name | Pin # | I/O | Pin Type | Pin Description |
|----------|-------|-----|------------|--|
| XOUT | 1 | O | LVTTTL | MHz CRYSTAL_OUT -- Reference crystal feedback. Float pin if using reference input clock. |
| XIN/ REF | 2 | I | LVTTTL | MHz CRYSTAL_IN -- Reference crystal input or external reference clock input. Maximum clock input voltage is 1.8V. |
| GND | 3 | | Power | Connect to Ground. |
| OUT3 | 4 | O | OUTPUT | Buffered reference clock output. Single-ended output voltage levels are register controlled by either VDDO1 or VDDO2. |
| SEL0* | 5 | I | LVTTTL | Configuration select pin. Weak internal pull down resistor. |
| VDD | 6 | | Power | Device power supply. Connect to 1.8V. |
| VDDx | 7 | | Power | Device power supply. Connect to 1.8V. |
| VDDO1 | 8 | | Power | Device power supply. Connect to 1.8 to 3.3V. VDDO1 must be the highest voltage on the device. Using register settings, select output voltage levels for OUT0-OUT3. |
| GND | 9 | | Power | Connect to Ground. |
| OUT2 | 10 | O | Adjustable | Configurable clock output 2. Single-ended output voltage levels are register controlled by either VDDO1 or VDDO2. |
| OUT1 | 11 | O | Adjustable | Configurable clock output 1. Single-ended output voltage levels are register controlled by either VDDO1 or VDDO2. |
| SEL1* | 12 | I | LVTTTL | Configuration select pin. Weak internal pull down resistor. |
| GND | 13 | | Power | Connect to Ground. |

| | | | | |
|-------|----|-----|------------|---|
| SCLK | 14 | I | LVTTL | I ² C clock. Logic levels set by VDDO1. 5V tolerant. |
| OUT0 | 15 | O | Adjustable | Configurable clock output 0. Single-ended output voltage levels are register controlled by either VDDO1 or VDDO2. |
| OUT4 | 16 | O | Adjustable | Configurable clock output 8. Single-ended output voltage levels controlled by VDDO2. |
| SDA | 17 | I/O | Open Drain | Bidirectional I ² C data. Logic levels set by VDDO1. 5V tolerant. |
| VDDO2 | 18 | | Power | Device power supply. Connect to 1.8 to 3.3V. Using register settings, select output voltage levels for OUT0-OUT4. |
| VDD | 19 | | Power | Device power supply. Connect to 1.8V. |
| GND | 20 | | Power | Connect to Ground. |

Note *: SEL pins should be controlled by 1.8V LVTTL logic; 3.3V tolerant.

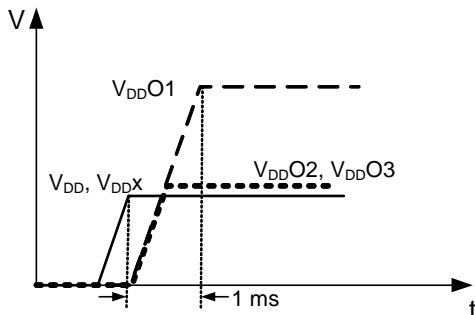
Note 1: Outputs are user programmable to drive single-ended 1.8V/2.5V/3.3V LVTTL as indicated above. Always completely power up VDD and VDDx prior to applying VDDO power.

Note 2: Default configuration CLK3=Buffered Reference output. All other outputs are off.

Note 3: Do not power up with SEL[1:0] = 00 (in Power down/Sleep mode).

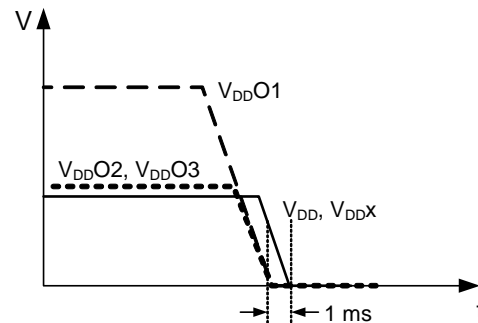
Ideal Power Up Sequence

- 1) V_{DD} and V_{DDX} must come up first, followed by V_{DDO}
- 2) V_{DDO1} must come up within 1ms after V_{DD} and V_{DDX} come up
- 3) V_{DDO2} must be equal to, or lower than, V_{DDO1}
- 4) V_{DD} and V_{DDX} have approx. the same ramp rate
- 5) V_{DDO1} and V_{DDO2} have approx. same ramp rate

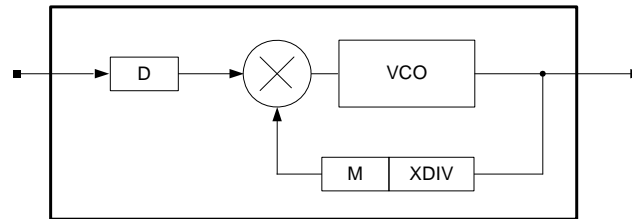


Ideal Power Down Sequence

- 1) V_{DDO} must drop first, followed by V_{DD} and V_{DDX}
- 2) V_{DD} and V_{DDX} must come down within 1ms after V_{DDO1} comes down
- 3) V_{DDO2} must be equal to, or lower than, V_{DDO1}
- 4) V_{DD} and V_{DDX} have approx. the same ramp rate
- 5) V_{DDO1} and V_{DDO2} have approx. same ramp rate



PLL Features and Descriptions



PLL Block Diagram

| | Ref-Divider (D) Values | Feedback Pre-Divider (XDIV) Values | Feedback (M) Values | Programmable Loop Bandwidth | Spread Spectrum Generation Capability |
|------|------------------------|------------------------------------|---------------------|-----------------------------|---------------------------------------|
| PLLA | 1 - 255 | 1 or 4 | 6 - 2047 | Yes | No |
| PLLB | 1 - 255 | 4 | 6 - 2047 | Yes | Yes |
| PLLC | 1 - 255 | 1 or 8 bit divide | 6 - 2047 | Yes | No |
| PLLD | 1 - 255 | 1 or 4 | 6 - 2047 | Yes | No |

Crystal Input (XIN/REF)

The crystal oscillators should be fundamental mode quartz crystals; overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 50Ω maximum equivalent series resonance. 0

ONXTALB=0 bit needs to be set for XIN/REF.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The crystal capacitors are internal to the device and have an effective value of 4pF.

Reference Pre-Divider, Reference Divider, Feedback-Divider and Post-Divider

Each PLL incorporates an 8-bit reference-scaler and a 11-bit feedback divider which allows the user to generate four unique non-integer-related frequencies. PLLA and PLLD each have a feedback pre-divider that provides additional multiplication for kHz reference clock applications. Each output divider supports 8-bit post-divider. The following equation governs how the output frequency is calculated.

$$F_{OUT} = F_{IN} * \left(\frac{XDIV * M}{D} \right) \text{ (Eq. 2)}$$

Where F_{IN} is the reference frequency, XDIV is the feedback pre-divider value, M is the feedback-divider value, D is the reference divider value, ODIV is the total post-divider value, and F_{OUT} is the resulting output frequency. Programming any of the dividers may cause glitches on the outputs.

SPREAD SPECTRUM GENERATION (PLL B)

PLL B has spread spectrum generation capability, which users have the option of turning on and off. Spread spectrum profile, frequency, and spread are fully programmable (within limits). The programmable spread spectrum generation parameters are NC[10:0], MOD[12:0], and NSS[10:0] bits. To enable spread spectrum, set SSEN B_B=0.

The spread spectrum circuitry was specifically developed to accommodate video display applications. The spread modulation frequency can be defined to exactly equal the horizontal line frequency (HSYNC)

NC[10:0]

These bits are used to determine the number of pulses per spread spectrum cycle. For video applications, NC is the number of pixels on the horizontal display row (or integer multiple of displayed pixels in a row). By matching the spread period to the screen, no tearing or “shimmer” will be apparent.

NC must be an even number to insure that the upward spread transition has the same number of steps as the downward spread transition.

For non-video applications, this can also be seen as the number of clock cycles for a complete spread spectrum period.

MOD[12:0]

These bits relate the VCO frequency to the target average spread output frequency (F_{MID}).

$$F_{MID} = (F_{VCO}) / 8$$

$$F_{MAX} = F_{MID} + (SS\% * F_{MID})$$

$$F_{MIN} = F_{MID} - (SS\% * F_{MID})$$

$$MOD = (F_{REF} * NC) / (2 * F_{MID})$$

NSS[10:0]

These bits control the amplitude of the spread modulation.

$$NSS = (NC / 2) + (NC / 8) * (F_{MAX} - F_{MIN}) / F_{MID}$$

Modulation frequency:

$$F_{MOD} = F_{MID} / NC \text{ (Eq. 11)}$$

Video Example

$F_{REF} = 27 \text{ MHz}$, $F_{OUT} = 27 \text{ MHz}$, 640 pixels per line, center spread of $\pm 1\%$. Using $F_{VCO} = 432 \text{ MHz}$, find the necessary spread spectrum register settings.

$$F_{MID} = F_{VCO} / 8$$

$$NC = 640 \text{ (integer number of spread periods/screen)}$$

$$MOD = (25 \text{ MHz} * 640) / (2 * 54 \text{ MHz}) = 160$$

$$NSS = (640/2) + (640/8) * (27.27 \text{ MHz} - 26.73 \text{ MHz}) / 27 \text{ MHz} = 321.$$

$$F_{MOD} = 27 \text{ MHz} / 640 = 11.8 \text{ kHz}.$$

Non-Video Example

$F_{REF} = 25 \text{ MHz}$, $F_{OUT} = 27 \text{ MHz}$, 31.25kHz modulation rate, center spread of $\pm 1\%$. Find the necessary spread spectrum register settings.

$$F_{MID} = F_{VCO} / 8$$

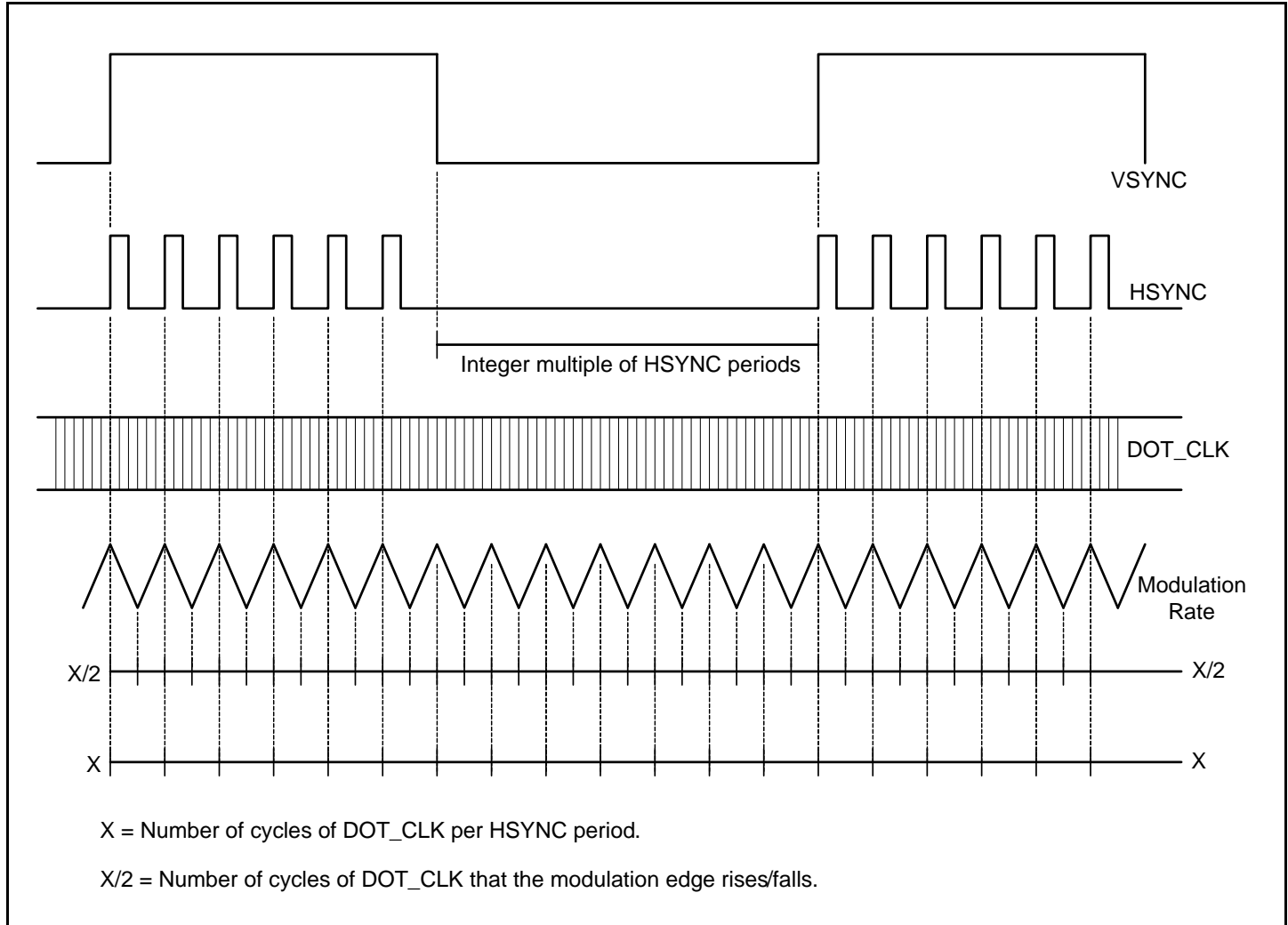
$$F_{MOD} = 31.25 \text{ kHz} = 50.625 \text{ MHz} / NC.$$

$$NC = 1620$$

$$MOD = (25 \text{ MHz} * 1620) / (2 * 50.625 \text{ MHz}) = 400$$

$$NSS = (1620/2) + (1620/8) * (27.27 \text{ MHz} - 26.73 \text{ MHz}) / 27 \text{ MHz} = 814.$$

VSYNC, HSYNC, DOT_CLK – Modulation Rate Relationship



LOOP FILTER

The loop filter for each PLL can be programmed to optimize the jitter performance. The low-pass frequency response of the PLL is the mechanism that dictates the jitter transfer characteristics. The loop bandwidth can be extracted from the jitter transfer. A narrow loop bandwidth is good for jitter attenuation while a wide loop bandwidth is best for low jitter generation. The specific loop filter components that can be programmed are the resistor via the RZ[4:0] bits, zero capacitor via the CZ[2:0] bits, pole capacitor via the CP[1:0] bits, and the charge pump current via the IP#[2:0] bits.

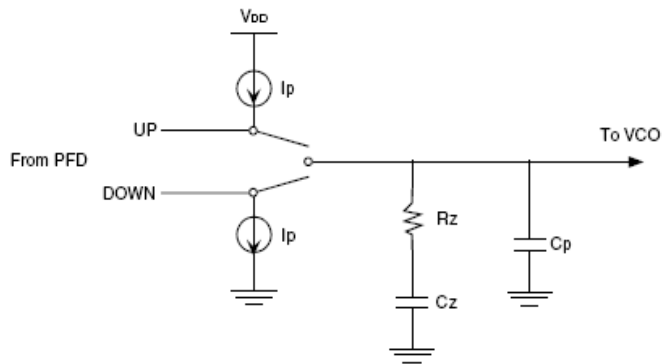
The following equations govern how the loop filter is set:

$$\text{Zero capacitor (Cz)} = 280\text{pF}$$

$$\text{Pole capacitor (Cp)} = 30\text{pF}$$

$$\text{Charge pump (Ip)} = \text{IP}\#[2:0] \text{ }\mu\text{A}$$

$$\text{VCO gain (Kvco)} = 350\text{MHz/V} * 2\pi$$



PLL Loop Bandwidth:

Charge pump gain ($K\phi$) = $I_p / 2\pi$

VCO gain (K_{VCO}) = $350\text{MHz/V} * 2\pi$

M = Total multiplier value (See the PRE-SCALERS, FEEDBACK-DIVIDERS, POST-DIVIDERS section for more detail)

$$\omega_c = (R_z * K\phi * K_{VCO} * C_z) / (M * (C_z + C_p))$$

$$F_c = \omega_c / 2\pi$$

Note, the phase/frequency detector frequency (F_{PFD}) is typically seven times the PLL closed-loop bandwidth (F_c) but too high of a ratio will reduce your phase margin thus compromising loop stability.

To determine if the loop is stable, the phase margin (ϕ_m) would need to be calculated as follows.

Phase Margin:

$$\omega_z = 1 / (R_z * C_z)$$

$$\omega_p = (C_z + C_p) / (R_z * C_z * C_p)$$

$$\phi_m = (360 / 2\pi) * [\tan^{-1}(\omega_c / \omega_z) - \tan^{-1}(\omega_c / \omega_p)]$$

To ensure stability in the loop, the phase margin is recommended to be $> 60^\circ$ but too high will result in the lock time being excessively long. Certain loop filter parameters would need to be compromised to not only meet a required loop bandwidth but to also maintain loop stability.

Damping Factor:

$$\zeta = R_z / 2 * (K_{VCO} * I_p * C_z)^{1/2} / M$$

Example

$F_c = 150\text{kHz}$ is the desired loop bandwidth. The total $A * M$ value is 160. The ζ (damping factor) target should be 0.7, meaning the loop is critically damped. Given F_c and $A * M$, an optimal loop filter setting needs to be solved for that will meet both the PLL loop bandwidth and maintain loop stability.

Choose a mid-range charge pump from register table

$$I_{cp} = 11.9\mu\text{A}$$

$$K\phi * K_{VCO} = 350\text{MHz/V} * 40\mu\text{A} = 12000\text{A/Vs}$$

$$\omega_c = 2\pi * F_c = 9.42 \times 10^5 \text{ s}^{-1}$$

$$\omega_p = (C_z + C_p) / (R_z * C_z * C_p) = \omega_z (1 + C_z / C_p)$$

Solving for R_z , the best possible value $R_z = 30\text{k}\Omega$ ($RZ[1:0] = 10$) gives

$$\zeta = 1.4 \text{ (Ideal range for } \zeta \text{ is 0.7 to 1.4)}$$

Solving back for the PLL loop bandwidth, $F_c = 149\text{kHz}$.

The phase margin must be checked for loop stability.

$$\phi_m = (360 / 2\pi) * [\tan^{-1}(9.42 \times 10^5 \text{ s}^{-1} / 1.19 \times 10^5 \text{ s}^{-1}) - \tan^{-1}(9.42 \times 10^5 \text{ s}^{-1} / 1.23 \times 10^6 \text{ s}^{-1})] = 45^\circ$$

The phase margin would be acceptable with a fairly stable loop.

SEL[1:0] Function

The IDT5P49EE502 can support up to three unique configurations. Users may pre-program all configurations, selected using SEL[1:0] pins. Alternatively, users may use I2C interface to configure these registers on- the-fly.

Always power with SEL1=1 and/or SEL0=1.

| SEL1 | SEL0 | Configuration Selections |
|------|------|--------------------------|
| 0 | 0 | Power Down/Sleep Mode |
| 0 | 1 | Select CONFIG0 |
| 1 | 0 | Select CONFIG1 |
| 1 | 1 | Select CONFIG2 |

Configuration OUTx IO Standard

Users can configure the individual output IO standard from a single 1.8V power supply. Each output can support 1.8V/

2.5V or 3.3V LVCMOS. VDDO1 must have the highest voltage of any pin on the device. VDDO2 may have any value between 1.8V and VDDO1.

Programming the Device

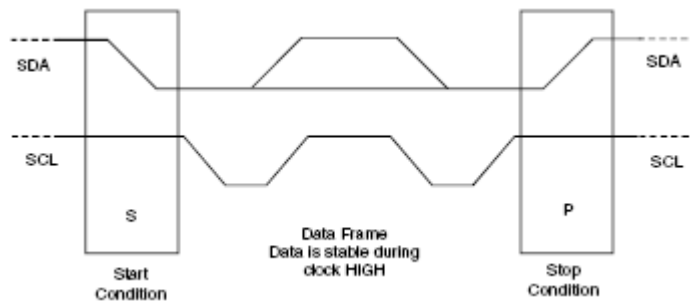
I²C may be used to program the IDT5P49EE502.

– Device (slave) address = 7'b1101010

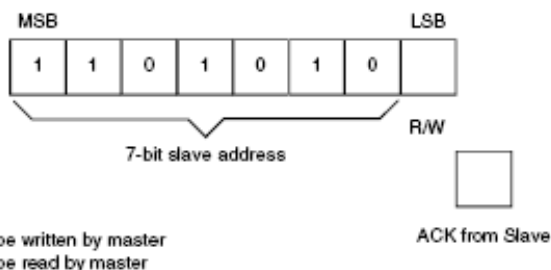
I²C Programming

The IDT5P49EE502 is programmed through an I²C-Bus serial interface, and is an I²C slave device. The read and write transfer formats are supported. The first byte of data after a write frame to the correct slave address is interpreted as the register address; this address auto-increments after each byte written or read.

The frame formats are shown in the following illustration.



Framing



The first byte transmitted by the Master is the Slave Address followed by the R/W bit. The Slave acknowledges by sending a "1" bit.

First Byte Transmitted on I²C Bus

External I²C Interface Condition

KEY:

From Master to Slave

From Master to Slave, but can be omitted if followed by the correct sequence

Normally data transfer is terminated by a STOP condition generated by the Master. However, if the Master still wishes to communicate on the bus, it can generate a repeated START condition, and address another Slave address without first generating a STOP condition.

From Slave to Master

SYMBOLS:

ACK - Acknowledge (SDA LOW)

NACK - Not Acknowledge (SDA HIGH)

Sr - Repeated Start Condition

S - START Condition

P - STOP Condition

EEPROM Interface

The IDT5P49EE502 can store its configuration in an internal EEPROM. The contents of the device's internal programming registers can be saved to the EEPROM by issuing a save instruction (ProgSave) and can be loaded back to the internal programming registers by issuing a restore instruction (ProgRestore).

To initiate a save or restore using I²C, only two bytes are transferred. The Device Address is issued with the read/write bit set to "0", followed by the appropriate command code. The save or restore instruction executes

after the STOP condition is issued by the Master, during which time the IDT5P49EE502 will not generate Acknowledge bits. The IDT5P49EE502 will acknowledge the instructions after it has completed execution of them. During that time, the I²C bus should be interpreted as busy by all other users of the bus.

On power-up of the IDT5P49EE502, an automatic restore is performed to load the EEPROM contents into the internal programming registers. The IDT5P49EE502 will be ready to accept a programming instruction once it acknowledges its 7-bit I²C address.

Progwrite

| S | Address | R/W | ACK | Command Code | ACK | Register | ACK | Data | ACK | P |
|---|---------|-----|-------|------------------|-------|----------|-------|--------|-------|---|
| | 7-bits | 0 | 1-bit | 8-bits: xxxxxx00 | 1-bit | 8-bits | 1-bit | 8-bits | 1-bit | |

Progwrite Command Frame

Writes can continue as long as a Stop condition is not sent and each byte will increment the register address.

Progreed

Note: If the expected read command is not from the next higher register to the previous read or write command, then set a known “read” register address prior to a read operation by issuing the following command:

| S | Address | R/W | ACK | Command Code | ACK | Register | ACK | P |
|---|---------|-----|-------|------------------|-------|----------|-------|---|
| | 7-bits | 0 | 1-bit | 8-bits: xxxxxx00 | 1-bit | 8-bits | 1-bit | |

Prior to Progreed Command Set Register Address

The user can ignore the STOP condition above and use a repeated START condition instead, straight after the slave acknowledgement bit (i.e., followed by the Progreed command):

| S | Address | R/W | ACK | ID Byte | ACK | Data_1 | ACK | Data_2 | ACK | Data_last | NACK | P |
|---|---------|-----|-------|---------|-------|--------|-------|--------|-------|-----------|-------|---|
| | 7-bits | 1 | 1-bit | 8-bits | 1-bit | 8-bits | 1-bit | 8-bits | 1-bit | 8-bits | 1-bit | |

Progreed Command Frame

Progsave

| S | Address | R/W | ACK | Command Code | ACK | P |
|---|---------|-----|-------|------------------|-------|---|
| | 7-bits | 0 | 1-bit | 8-bits: xxxxxx01 | 1-bit | |

Note:

PROGWRITE is for writing to the IDT5P49EE502 registers.

PROGREAD is for reading the IDT5P49EE502 registers.

PROGSAVE is for saving all the contents of the IDT5P49EE502 registers to the EEPROM.

PROGRESTORE is for loading the entire EEPROM contents to the IDT5P49EE502 registers.

Progrestore

| S | Address | R/W | ACK | Command Code | ACK | P |
|---|---------|-----|-------|------------------|-------|---|
| | 7-bits | 0 | 1-bit | 8-bits: xxxxxx10 | 1-bit | |

During PROGRESTORE, outputs will be turned off to ensure that no improper voltage levels are experienced before initialization.

I²C Bus DC Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-----------------------|------------------------|------------|-----|-----------|------|
| V _{IH} | Input HIGH Level | | 0.7xVDDO1 | | 5.5 | V |
| V _{IL} | Input LOW Level | | | | 0.3xVDDO1 | V |
| V _{HYS} | Hysteresis of Inputs | | 0.05xVDDO1 | | | V |
| I _{IN} | Input Leakage Current | V _{DD} = 0V | | | ±1.0 | μA |
| V _{OL} | Output LOW Voltage | I _{OL} = 3 mA | | | 0.4 | V |

I²C Bus AC Characteristics for Standard Mode¹

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------------|--|-----|-----|------|------|
| F _{SCLK} | Serial Clock Frequency (SCL) | 0 | | 100 | kHz |
| t _{BUF} | Bus free time between STOP and START | 4.7 | | | μs |
| t _{SU:START} | Setup Time, START | 4.7 | | | μs |
| t _{HD:START} | Hold Time, START | 4 | | | μs |
| t _{SU:DATA} | Setup Time, data input (SDA) | 250 | | | ns |
| t _{HD:DATA} | Hold Time, data input (SDA) ² | 0 | | | μs |
| t _{OVD} | Output data valid from clock | | | 3.45 | μs |
| C _B | Capacitive Load for Each Bus Line | | | 400 | pF |
| t _R | Rise Time, data and clock (SDA, SCLK) | | | 1000 | ns |
| t _F | Fall Time, data and clock (SDA, SCLK) | | | 300 | ns |
| t _{HIGH} | HIGH Time, clock (SCLK) | 4 | | | μs |
| t _{LOW} | LOW Time, clock (SCLK) | 4.7 | | | μs |
| t _{SU:STOP} | Setup Time, STOP | 4 | | | μs |

1) No activity is allowed on I²C lines until VDD>1.62V.

2) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}MIN of the SCLK signal) to bridge the undefined region of the falling edge of SCLK.

I²C Bus AC Characteristics for Fast Mode¹

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------------|--|-------------------------|-----|-----|------|
| F _{SCLK} | Serial Clock Frequency (SCL) | 0 | | 400 | kHz |
| t _{BUF} | Bus free time between STOP and START | 1.3 | | | μs |
| t _{SU:START} | Setup Time, START | 0.6 | | | μs |
| t _{HD:START} | Hold Time, START | 0.6 | | | μs |
| t _{SU:DATA} | Setup Time, data input (SDA) | 100 | | | ns |
| t _{HD:DATA} | Hold Time, data input (SDA) ¹ | 0 | | | μs |
| t _{OVD} | Output data valid from clock | | | 0.9 | μs |
| C _B | Capacitive Load for Each Bus Line | | | 400 | pF |
| t _R | Rise Time, data and clock (SDA, SCL) | 20 + 0.1xC _B | | 300 | ns |
| t _F | Fall Time, data and clock (SDA, SCL) | 20 + 0.1xC _B | | 300 | ns |
| t _{HIGH} | HIGH Time, clock (SCL) | 0.6 | | | μs |
| t _{LOW} | LOW Time, clock (SCL) | 1.3 | | | μs |
| t _{SU:STOP} | Setup Time, STOP | 0.6 | | | μs |

1) No activity is allowed on I²C lines until VDD>1.62V.

2) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}MIN of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5P49EE502. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Symbol | Description | Max | Unit |
|------------------|--------------------------------------|------------------------------|------|
| V _{DD} | Internal Power Supply Voltage | -0.5 to +4.6 | V |
| V _I | Input Voltage | -0.5 to +4.6 | V |
| V _O | Output Voltage (not to exceed 4.6 V) | -0.5 to V _{DD} +0.5 | V |
| T _J | Junction Temperature | 150 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |

Recommended Operation Conditions

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------------------------|--|-------|-----|-------|------|
| V _{DD} , V _{DDX} | Power supply voltage for VDD | 1.71 | 1.8 | 1.89 | V |
| V _{DDOX} | Power supply voltage for outputs VDDO1/2/3 | 1.71 | 1.8 | 1.89 | V |
| | | 2.375 | 2.5 | 2.625 | V |
| | | 3.135 | 3.3 | 3.465 | V |
| T _A | Operating temperature, ambient | -40 | | +85 | °C |
| C _{LOAD_OUT} | Maximum load capacitance (3.3V LVTTTL only) | | | 15 | pF |
| C _{LOAD_OUT} | Maximum load capacitance (1.8V or 2.5V LVTTTL only) | | | 8 | pF |
| F _{IN} | External reference crystal | 8 | | 30 | MHz |
| | External reference clock CLKIN | 1 | | 40 | |
| XIN/REF | Voltage swing for clock input | | | VDD | V |
| t _{PU} | Power up time for all V _{DD} s to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | | 5 | ms |

Capacitance (T_A = +25 °C, f = 1 MHz)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|-----|-----|-----|------|
| C _{IN} | Input Capacitance | | 3 | | pF |
| Crystal Specifications | | | | | |
| XTAL_FREQ | Crystal frequency | 8 | | 30 | MHz |
| XTAL_MIN | Minimum crystal load capacitance | | 7 | | pF |
| XTAL_MAX | Maximum crystal load capacitance | | 20 | | pF |

DC Electrical Characteristics for 3.3 Volt LVTTTL ¹

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-------------------|------------------------|------------------------|-----|-----|------|------|
| V _{OH} | Output HIGH Voltage | I _{OH} = 33mA | 2.4 | | VDDO | V |
| V _{OL} | Output LOW Voltage | I _{OH} = 33mA | | | 0.4 | V |
| I _{OZDD} | Output Leakage Current | 3-state outputs | | | 5 | µA |

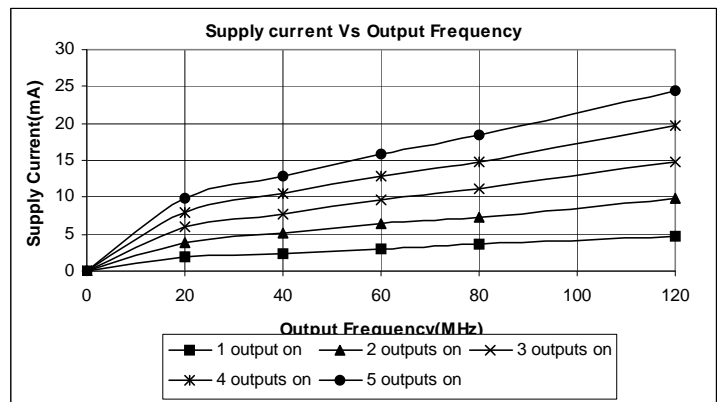
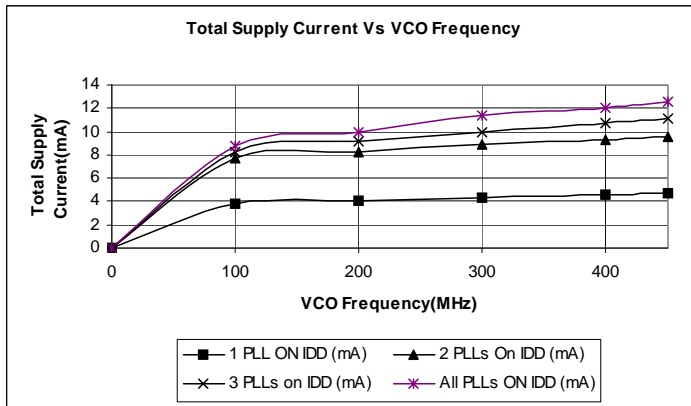
DC Electrical Characteristics for 2.5Volt LVTTTL ¹

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-------------------|------------------------|------------------------|-----|-----|------|------|
| V _{OH} | Output HIGH Voltage | I _{OH} = 25mA | 2.1 | | VDDO | V |
| V _{OL} | Output LOW Voltage | I _{OH} = 25mA | | | 0.4 | V |
| I _{OZDD} | Output Leakage Current | 3-state outputs | | | 5 | µA |

DC Electrical Characteristics for 1.8Volt LVTTTL ¹

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-------------------|------------------------|-------------------------|-----------|-----|-----------|------|
| V _{OH} | Output HIGH Voltage | VDD = 1.71V to 1.89V | 0.65*VDDO | | VDDO | V |
| V _{OL} | Output LOW Voltage | | | | 0.35*VDDO | V |
| V _{IH} | Input HIGH Voltage | SEL[1:0], 3.3V tolerant | 0.75VDD | | | V |
| V _{IL} | Input LOW Voltage | SEL[1:0], 3.3V tolerant | | | 0.25VDD | V |
| I _{OZDD} | Output Leakage Current | 3-state outputs | | | 5 | µA |

Power Supply Characteristics for LVTTTL Outputs



1: See “Recommended Operating Conditions” table. Always completely power up VDD and VDDx prior to applying VDDO power.

AC Timing Electrical Characteristics

(Spread Spectrum Generation = OFF)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|-----------|-----------------------------|--|------------------|------|------|-------|
| f_{IN} | Input Frequency | Input Frequency Limit (CLKIN) | 1 ¹ | | 40 | MHz |
| 1 / t1 | Output Frequency | Single Ended Clock output limit (LVTTTL) 3.3V | 0.001 | | 120 | MHz |
| | | Single Ended Clock output limit (LVTTTL) 2.5V | | | 110 | MHz |
| | | Single Ended Clock output limit (LVTTTL) 1.8V | | | 100 | MHz |
| f_{VCO} | VCO Frequency | VCO operating Frequency Range | 100 | | 475 | MHz |
| f_{PFD} | PFD Frequency | PFD operating Frequency Range | 0.5 ¹ | | 20 | MHz |
| t2 | Input Duty Cycle | Duty Cycle for Input | 40 | | 60 | % |
| t3 | Output Duty Cycle | Measured at VDD/2 | 45 | | 55 | % |
| t4 | Slew Rate, SLEWx(bits) = 00 | Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF) | | 5.1 | | V/ns |
| | Slew Rate, SLEWx(bits) = 01 | Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF) | | 4.4 | | |
| | Slew Rate, SLEWx(bits) = 10 | Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF) | | 2.8 | | |
| | Slew Rate, SLEWx(bits) = 11 | Single-Ended 3.3V LVCMOS Output clock rise and fall time, 20% to 80% of VDD (Output Load = 7 pF) | | 1.8 | | |
| t5 | Clock Jitter | Peak-to-peak period jitter, CLK outputs measured at VDD/2; $f_{PFD} \geq 10$ MHz Single output frequency only. | | | 100 | ps |
| | | Peak-to-peak period jitter, CLK outputs measured at VDD/2; $f_{PFD} \geq 10$ MHz Multiple output frequencies switching. | | | 200 | ps |
| t6 | Output Skew | Skew between any output (Same freq and IO type, FOUT >10MHz) | | | 200 | ps |
| t7 | Lock Time | PLL Lock Time from Power-up (using MHz reference clock) ² | | 5 | 20 | ms |
| | | PLL Lock time from shutdown mode | | 5 | 10 | ms |

1. Input clock (square wave) may be used at 1 MHz.

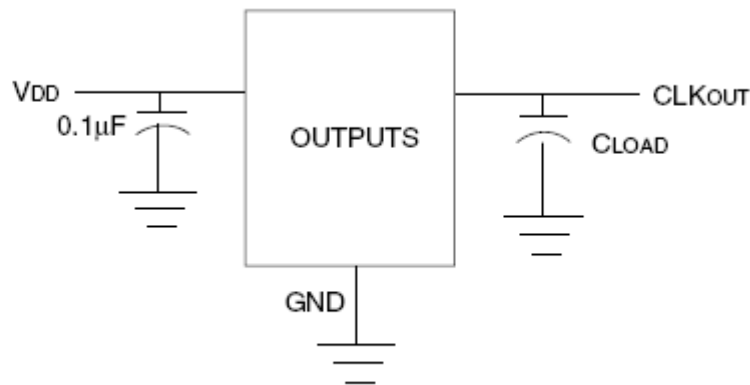
2. Time from supply voltage crosses VDD=1.62V to PLLs are locked.

Spread Spectrum Generation Specifications

| Symbol | Parameter | Description | Min | Typ | Max | Unit |
|--------------|-----------------|---|----------------|-----|-----|-------------|
| f_{IN} | Input Frequency | Input Frequency Limit | 1 ¹ | | 40 | MHz |
| f_{MOD} | Mod Frequency | Modulation Frequency | 32 | | 120 | kHz |
| f_{SPREAD} | Spread Value | Amount of Spread Value (programmable) - Down Spread | Programmable | | | % f_{OUT} |
| | | Amount of Spread Value (programmable) - Center Spread | Programmable | | | |
| | | Total Spread Value | 0.5 | | 4.0 | |

1) Practical lower frequency is determined by loop filter settings.

Test Circuits and Conditions ¹

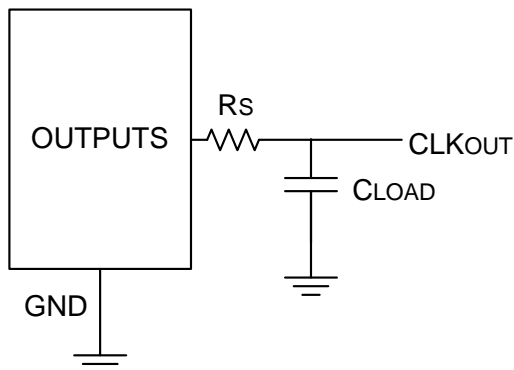


NOTE:

1. All V_{DD} pins must be tied together.

Test Circuits for DC Outputs

Termination Scheme (Block Diagram)



LVTTTL Output Load: ~7pF for each output

Programming Registers Table

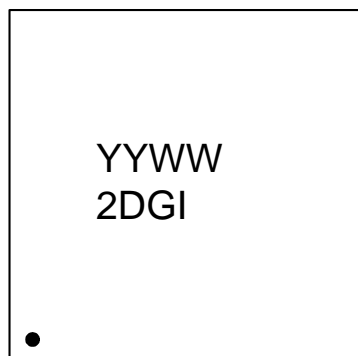
| Addr | Default Register Hex Value | Bit # | | | | | | | | Description | |
|------|----------------------------|-----------|------------|------------|----------|----------|---|----------|---|--|----------------------------------|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
| 0x00 | 04 | ONXTALB | Reserved | | | | | | | | ONXTALB - MHz Crystal active low |
| 0x01 | 00 | INV[0] | SLEW0[1:0] | | Reserved | PS0[2:1] | | Reserved | | INV[#] - Invert output# SLEW#[0:1] - output# slew setting | |
| 0x02 | 00 | Reserved | | | | | | | | 0 0 - 5.1V/ns | |
| 0x03 | 00 | Reserved | | | | | | | | 0 1 - 4.4V/ns | |
| 0x04 | 00 | INV[1] | SLEW1[1:0] | | Reserved | PS1[2:1] | | Reserved | | 1 0 - 2.8V/ns 1 1 - 1.8V/ns | |
| 0x05 | 00 | INV[2] | SLEW2[1:0] | | Reserved | PS2[2:1] | | Reserved | | PS#[2:1] -Power Select | |
| 0x06 | 00 | INV[3] | SLEW3[1:0] | | Reserved | PS3[2:1] | | Reserved | | 00 - Reserved 01 - OUT# connects to VDDO1 10 - OUT# connects to VDDO2 11 - Reserved | |
| 0x07 | 00 | Reserved | | | | | | | | CLK4 is tied to VDDO2 | |
| 0x08 | 00 | Reserved | | | | | | | | | |
| 0x09 | 00 | Reserved | INV[4] | SLEW4[1:0] | | Reserved | | | | | |
| 0x0A | 00 | Reserved | | | | | | | | | |
| 0x0B | 00 | Reserved | | | | | | | | | |
| 0x0C | 00 | Reserved | | | | | | | | | |
| 0x0D | 00 | Reserved | | | | | | | | | |
| 0x0E | 00 | REFA[7:0] | | | | | | | | Configuration0 REFA[7:0] - Reference Divide PLLA | |
| 0x0F | 00 | FBA[10:3] | | | | | | | | FBA[10:0] - Feedback Divide PLLA | |
| 0x10 | 00 | Reserved | | | | FBA[2:0] | | | | | |
| 0x11 | 00 | Reserved | XDIVA | RZA[1:0] | | IPA[2:0] | | Reserved | | XDIVA - FB predivide PLLA; 0 - /1; 1 - /4 RZA[1:0] - Zero Resistor PLLA 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPA[2:0] - charge Pump Current PLLA 100 - 6.3uA 101 - 11.9 uA 110 - 17.7 uA 111 - 22.7uA | |
| 0x12 | 00 | REFB[7:0] | | | | | | | | REFB[7:0] - Reference Divide PLLB | |
| 0x13 | 00 | FBB[10:3] | | | | | | | | FBB[10:0] - Feedback Divide PLLB | |
| 0x14 | 00 | MOD[4:0] | | | | FBB[2:0] | | | | PLLB Spread Parameters MOD[12:0] | |
| 0x15 | 00 | MOD[12:5] | | | | | | | | NC[10:0] | |
| 0x16 | 00 | NC[10:3] | | | | | | | | NSS[12:0] | |
| 0x17 | 00 | NSS[4:0] | | | | NC[2:0] | | | | | |
| 0x18 | 00 | NSS[12:5] | | | | | | | | | |
| 0x19 | 20 | Reserved | | IPB[2:0] | | RZB[1:0] | | | | RZB[1:0] - Zero Resistor PLLB | |
| 0x1A | 00 | Reserved | | | | | | SSENB_B | | 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPB[2:0] - charge Pump Current PLLB 000 - 0.37uA, 100 - 6.3uA 001 - 1.1uA, 101 - 11.9uA 010 - 1.8 uA, 110 - 17.7uA 011 - 3.4uA, 111 - 22.7uA | |
| 0x1B | 00 | REFC[7:0] | | | | | | | | REFC[7:0] - Reference Divide PLLC | |
| 0x1C | 00 | FBC[10:3] | | | | | | | | FBC[10:0] - Feedback Divide PLLC | |
| 0x1D | 00 | Reserved | | | | FBC[2:0] | | | | | |
| 0x1E | 00 | FBC2[7:0] | | | | | | | | FBC2 - Feedback Predivide PLLC Turn on using XDIVC=1 | |

| Addr | Default Register Hex Value | Bit # | | | | | | | | Description |
|------|----------------------------|-----------|----------|-----------|----------|----------|----------|-----------|---|--|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x1F | 00 | IPC[2:0] | | | RZC[1:0] | | Reserved | XDIVC | Reserved | RZC[1:0] - Zero Resistor PLLC 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPC[2:0] - charge Pump Current PLLC 100 - 6.3uA 101 - 11.9 uA 110 - 17.7 uA 111 - 22.7uA |
| 0x20 | 00 | REFD[7:0] | | | | | | | | REFD[7:0] - Reference Divide PLLD |
| 0x21 | 00 | FBD[10:3] | | | | | | | | FBD[10:0] - Feedback Divide PLLD |
| 0x22 | 00 | Reserved | | | | FBD[2:0] | | | | |
| 0x23 | 00 | XDIVD | RZD[1:0] | | IPD[2:0] | | | Reserved | | XDIVD - FB predivide PLLD; 0 - /1; 1 - /4 RZD[1:0] - Zero Resistor PLLD 00 - 5kOhm 01 - 10kOhm 10 - 30kOhm 11 - 80kOhm IPD[2:0] - charge Pump Current PLLD 100 - 6.3uA 101 - 11.9 uA 110 - 17.7 uA 111 - 22.7uA |
| 0x24 | 00 | OD0[7:0] | | | | | | | | |
| 0x25 | 00 | Reserved | | | | | | | | |
| 0x26 | 00 | Reserved | | | | | | | | |
| 0x27 | 00 | OD1[7:0] | | | | | | | | |
| 0x28 | 00 | OD2[7:0] | | | | | | | | |
| 0x29 | 00 | OD3[7:0] | | | | | | | | |
| 0x2A | 00 | Reserved | | | | | | | | |
| 0x2B | 00 | Reserved | | | | | | | | |
| 0x2C | 00 | OD4[7:0] | | | | | | | | |
| 0x2D | 00 | SCR4[1:0] | | Reserved | | | | SCR3[1:0] | | SRC3[1:0] - OD4 source 00 - off; 10 - PLLA 01 - Reference; 11 - PLLD SRC4[1:0] - OD4 source 00 - off; 10 - PLLC 01 - PLLA; 11 - Reference |
| 0x2E | 00 | SCR2[1:0] | | SCR1[1:0] | | Reserved | | | | SRC1[1:0] - OD1 source 00 - off; 10 - PLLB 01 - PLLA; 11 - PLLD SRC2[1:0] - OD2 source 00 - off; 10 - PLLC 01 - PLLA; 11 - PLLD |
| 0x2F | 01 | SCR0[1:0] | | Reserved | | | | | | SRC0[1:0] - OD0 source 00 - off; 10 - PLLC 01 - PLLB; 11 - PLLD |
| 0x30 | FF | Reserved | | | | | | | | |
| 0x31 | 00 | PDB[4] | Reserved | | OE[4] | Reserved | | | | PDB[4:0] - Powerdown OUT#. PDB#=0, OUT# driven low |
| 0x32 | 00 | Reserved | | OE[3] | OE[2] | OE[1] | Reserved | | OE[4:0] - Output enable OUT#. OE#=0, OUT# tri-stated. | |
| 0x33 | 00 | Reserved | | PDB[3] | PDB[2] | PDB[1] | Reserved | | PDB[0] If PDB#=OE#=0, OUT# driven low | |

| Addr | Default Register Hex Value | Bit # | | | | | | | | Description |
|------|----------------------------|-----------|----------|-----------|----------|----------|----------|-----------|--------|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x34 | 00 | REFA[7:0] | | | | | | | | Configuration1 (See definitions from Configuration0 above) |
| 0x35 | 00 | FBA[10:3] | | | | | | | | |
| 0x36 | 00 | Reserved | | | | FBA[2:0] | | | | |
| 0x37 | 00 | Reserved | XDIVA | RZA[1:0] | | IPA[2:0] | | Reserved | | |
| 0x38 | 00 | REFB[7:0] | | | | | | | | |
| 0x39 | 00 | FBB[10:3] | | | | | | | | |
| 0x3A | 00 | MOD[4:0] | | | | FBB[2:0] | | | | |
| 0x3B | 00 | MOD[12:5] | | | | | | | | |
| 0x3C | 00 | NC[10:3] | | | | | | | | |
| 0x3D | 00 | NSS[4:0] | | | | NC[2:0] | | | | |
| 0x3E | 00 | NSS[12:5] | | | | | | | | |
| 0x3F | 40 | Reserved | | IPB[2:0] | | | RZB[1:0] | | | |
| 0x40 | 00 | Reserved | | | | Reserved | Reserved | SSENB_B | | |
| 0x41 | 00 | REFC[7:0] | | | | | | | | |
| 0x42 | 00 | FBC[10:3] | | | | | | | | |
| 0x43 | 00 | Reserved | | | | FBC[2:0] | | | | |
| 0x44 | 00 | FBC2[7:0] | | | | | | | | |
| 0x45 | 00 | IPC[2:0] | | RZC[1:0] | | Reserved | XDIV | Reserved | | |
| 0x46 | 00 | REFD[7:0] | | | | | | | | |
| 0x47 | 00 | FBD[10:3] | | | | | | | | |
| 0x48 | 00 | Reserved | | | | FBD[2:0] | | | | |
| 0x49 | 00 | XDIVD | RZD[1:0] | | IPD[2:0] | | Reserved | | | |
| 0x4A | 00 | OD0[7:0] | | | | | | | | |
| 0x4B | 00 | Reserved | | | | | | | | |
| 0x4C | 00 | Reserved | | | | | | | | |
| 0x4D | 00 | OD1[7:0] | | | | | | | | |
| 0x4E | 00 | OD2[7:0] | | | | | | | | |
| 0x4F | 00 | OD3[7:0] | | | | | | | | |
| 0x50 | 00 | Reserved | | | | | | | | |
| 0x51 | 00 | Reserved | | | | | | | | |
| 0x52 | 00 | OD4[7:0] | | | | | | | | |
| 0x53 | 00 | SCR4[1:0] | | Reserved | | | | SCR3[1:0] | | |
| 0x54 | 00 | SCR2[1:0] | | SCR1[1:0] | | Reserved | | | | |
| 0x55 | 01 | SCR0[1:0] | | Reserved | | | | | | |
| 0x56 | FF | Reserved | | | | | | | | |
| 0x57 | 00 | PDB[4] | Reserved | | OE[4] | Reserved | | | | |
| 0x58 | 00 | Reserved | | OE[3] | OE[2] | OE[1] | Reserved | | OE[0] | |
| 0x59 | 00 | Reserved | | PDB[3] | PDB[2] | PDB[1] | Reserved | | PDB[0] | |

| Addr | Default Register Hex Value | Bit # | | | | | | | | Description |
|------|----------------------------|-----------|----------|-----------|----------|----------|----------|-----------|--------|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 0x5A | 00 | REFA[7:0] | | | | | | | | Configuration2 (See definitions from Configuration0 above) |
| 0x5B | 00 | FBA[10:3] | | | | | | | | |
| 0x5C | 00 | Reserved | | | | FBA[2:0] | | | | |
| 0x5D | 00 | Reserved | XDIVA | RZA[1:0] | | IPA[2:0] | | Reserved | | |
| 0x5E | 00 | REFB[7:0] | | | | | | | | |
| 0x5F | 00 | FBB[10:3] | | | | | | | | |
| 0x60 | 00 | MOD[4:0] | | | | FBB[2:0] | | | | |
| 0x61 | 00 | MOD[12:5] | | | | | | | | |
| 0x62 | 00 | NC[10:3] | | | | | | | | |
| 0x63 | 00 | NSS[4:0] | | | | NC[2:0] | | | | |
| 0x64 | 00 | NSS[12:5] | | | | | | | | |
| 0x65 | 40 | Reserved | | IPB[2:0] | | | RZB[1:0] | | | |
| 0x66 | 00 | Reserved | | | | Reserved | Reserved | SSENB_B | | |
| 0x67 | 00 | REFC[7:0] | | | | | | | | |
| 0x68 | 00 | FBC[10:3] | | | | | | | | |
| 0x69 | 00 | Reserved | | | | FBC[2:0] | | | | |
| 0x6A | 00 | FBC2[7:0] | | | | | | | | |
| 0x6B | 00 | IPC[2:0] | | RZC[1:0] | | Reserved | XDIV | Reserved | | |
| 0x6C | 00 | REFD[7:0] | | | | | | | | |
| 0x6D | 00 | FBD[10:3] | | | | | | | | |
| 0x6E | 00 | Reserved | | | | FBD[2:0] | | | | |
| 0x6F | 00 | XDIVD | RZD[1:0] | | IPD[2:0] | | Reserved | | | |
| 0x70 | 00 | OD0[7:0] | | | | | | | | |
| 0x71 | 00 | Reserved | | | | | | | | |
| 0x72 | 00 | Reserved | | | | | | | | |
| 0x73 | 00 | OD1[7:0] | | | | | | | | |
| 0x74 | 00 | OD2[7:0] | | | | | | | | |
| 0x75 | 00 | OD3[7:0] | | | | | | | | |
| 0x76 | 00 | Reserved | | | | | | | | |
| 0x77 | 00 | Reserved | | | | | | | | |
| 0x78 | 00 | OD4[7:0] | | | | | | | | |
| 0x79 | 00 | SCR4[1:0] | | Reserved | | | | SCR3[1:0] | | |
| 0x7A | 00 | SCR2[1:0] | | SCR1[1:0] | | Reserved | | | | |
| 0x7B | 01 | SCR0[1:0] | | Reserved | | | | | | |
| 0x7C | FF | Reserved | | | | | | | | |
| 0x7D | 00 | PDB[4] | Reserved | | OE[4] | Reserved | | | | |
| 0x7E | 00 | Reserved | | OE[3] | OE[2] | OE[1] | Reserved | | OE[0] | |
| 0x7F | 00 | Reserved | | PDB[3] | PDB[2] | PDB[1] | Reserved | | PDB[0] | |

Marking Diagram (ND20)



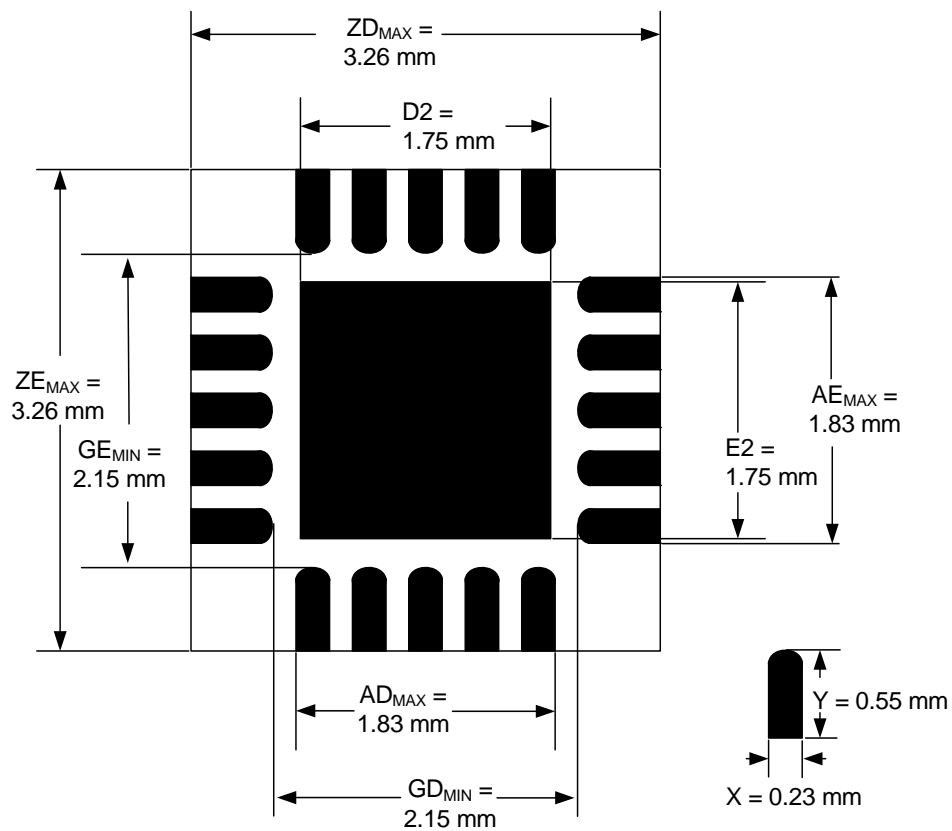
Notes:

1. YYWW is the last two digits of the year and week that the part was assembled.
2. "G" indicates Pb-free, RoHS compliant package.
3. "I" at the end of part number indicates industrial temperature range.

Thermal Characteristics 20-pin VFQFPN

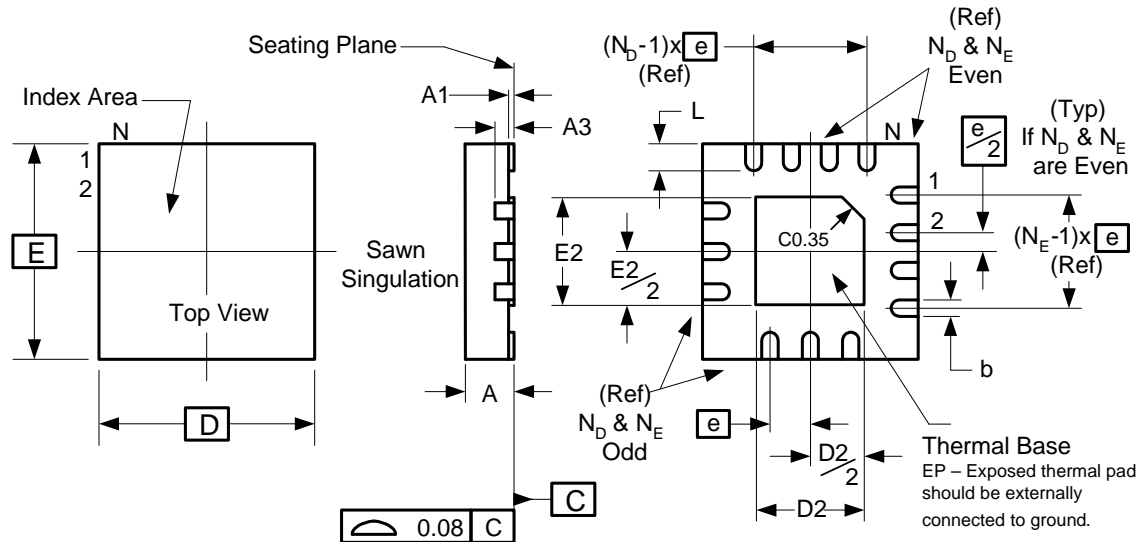
| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 64 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 56.6 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 51.8 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 84.3 | | °C/W |

20-pin QFN PCB Land Pattern



Package Outline and Package Dimensions (20-pin QFN)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | |
|-------------|----------------|------|
| | Min | Max |
| A | 0.80 | 1.00 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Reference | |
| b | 0.15 | 0.23 |
| e | 0.40 BASIC | |
| N | 20 | |
| ND | 5 | |
| NE | 5 | |
| D x E BASIC | 3.00 x 3.00 | |
| D2 | 1.55 | 1.75 |
| E2 | 1.55 | 1.75 |
| L | 0.30 | 0.50 |

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|--------------|---------------|
| 5P49EE502NDGI | See page 22 | Tubes | 20pin VFQFPN | -40 to +85° C |
| 5P49EE502NDGI8 | See page 22 | Tape and Reel | 20pin VFQFPN | -40 to +85° C |

“G” after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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Revision History

| Rev. | Date | Originator | Description of Change |
|------|----------|------------|--|
| -- | 10/27/09 | R.Willner | Initial Preliminary Datasheet |
| A | 11/10/09 | R.Willner | Revised pinout. |
| B | 3/25/10 | R.Willner | Typographical changes. Register corrections. Correct spread spectrum calculations. |
| C | 6/11/10 | R. Willner | Default configuration. Clarification of OUT4 is tied to VDDO2. |
| D | 07/26/10 | R. Willner | Updated thermal pad and dimensions on package drawing. |
| E | 8/30/10 | R.Willner | Input Clock max voltage swing 1.8V. |
| F | 9/08/10 | R.Willner | Power ramp sequence. |
| G | 10/18/10 | R.Willner | Typographical changes. Loop filter calculations. Default register bit corrections. |
| H | 01/19/11 | R.Willner | Corrected notes for top-side marking. |
| J | 04/13/11 | R. Willner | 1. Updated SCLK and SDA pin descriptions 2. Updated DC Electrical Char table for 1.8V LVTTTL; added VIH and VIL. 3. Updated "Lock Time/PLL Lock Time from shutdown mode" Typ. and Max. specs in AC Timing Electrical Char table. |
| K | 09/30/11 | R. Willner | Updated Power-up/Power-down Sequence notes. |
| L | 11/17/14 | R. Willner | Added pin 1 dot indicator on marking diagram. Corrected typo in Register Map table; SLEWx[0:1] was changed to SLEWx[1:0] |

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VERSACLOCK® LOW POWER CLOCK GENERATOR

EEPROM CLOCK GENERATOR

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