

## Description

The 5PB12xx is a high-performance TCXO/LVCMOS clock fanout buffer family with individual OE pin for each output. The CLKIN pin can accept either a square wave (LVCMOS) or clipped sine wave (such as TCXO clipped sine wave output) as input.

There are 3 different fan-out versions available: 1:3, 1:4 and 1:6.

The 5PB12xx has industry-leading low jitter and extremely low current consumption, making it ideal for smart mobile devices.

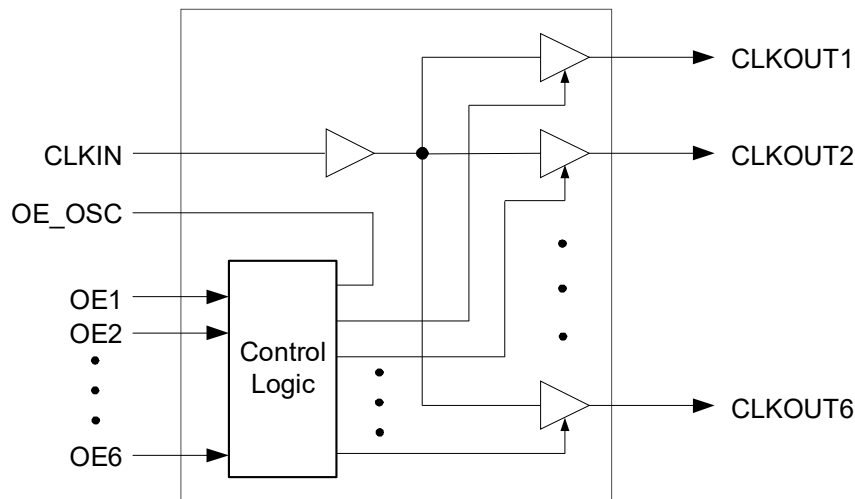
## Typical Applications

- Smart Mobile Handsets
- RF and baseband peripheral clock distribution
- Automotive

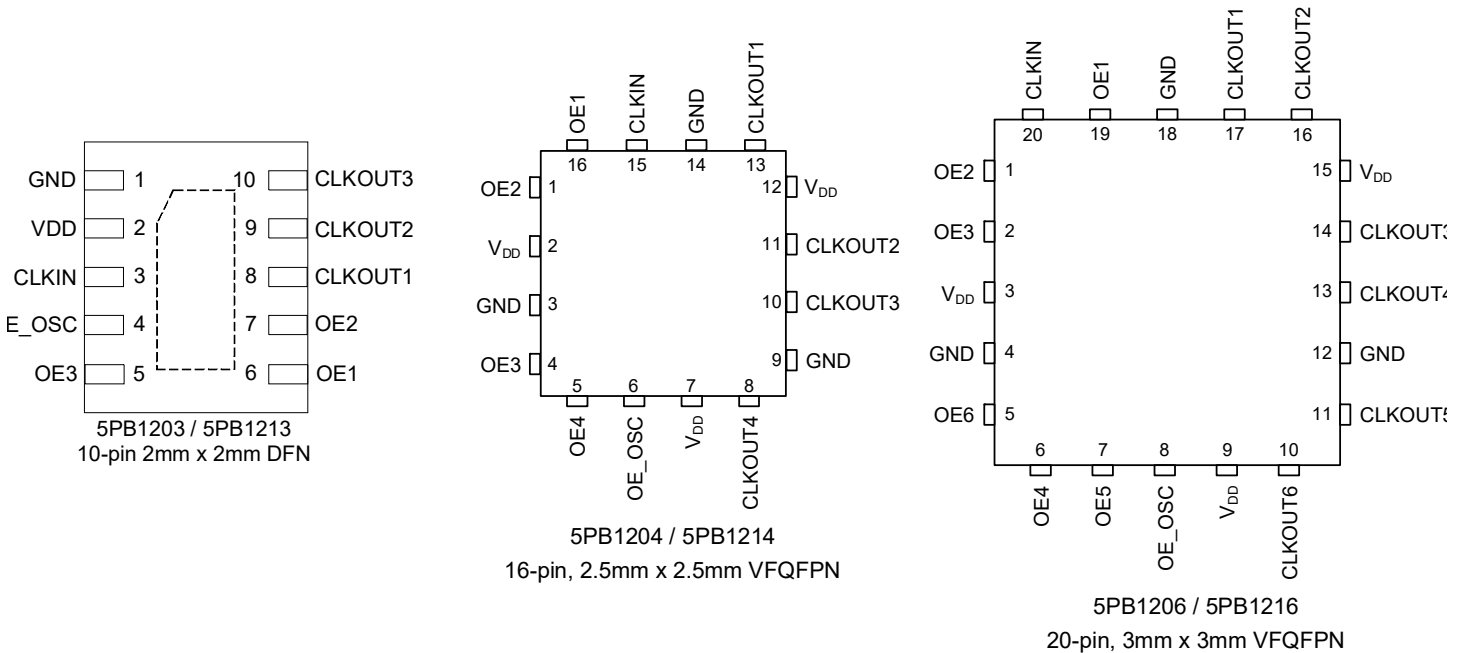
## Features

- Extremely low operating and standby current consumption
- Low RMS additive phase jitter
- Family supports 1.8V to 3.3V power supply voltage:
  - For 1.8V supply: 5PB1203, 5PB1204, 5PB1206
  - For 2.5V / 3.3V supply: 5PB1213, 5PB1214, 5PB1216
- Three, four, and six outputs with individual Output Enable pin
- One input
- OE\_ OSC control pin to enable/disable reference TCXO/XO
- Small 10-pin, 16-pin and 20-pin packages available
- Industrial -40° to +105°C temperature range

## Block Diagram



## Pin Assignments



## Pin Descriptions

| Pin Name | Pin Number         |                    |                    | Pin Type | Pin Description   |
|----------|--------------------|--------------------|--------------------|----------|---|
|          | 5PB1203<br>5PB1213 | 5PB1204<br>5PB1214 | 5PB1206<br>5PB1216 |          |   |
| VDD      | 2                  | 2, 7, 12           | 3, 9, 15           | Power    | Connect 1.8V to 5PB1203/5PB1204/5PB1206.<br>Connect 2.5V or 3.3V to 5PB1213/5PB1214/5PB1216.  |
| GND      | 1                  | 3, 9, 14           | 4, 12, 18          | Power    | Power supply ground.  |
| CLKIN    | 3                  | 15                 | 20                 | Input    | Single-ended clock input. Typically connected to a single-ended clock output.   |
| OE_osc   | 4                  | 6                  | 8                  | Output   | Status pin to indicate that all OE pins are low (all outputs disabled). This pin may be used to disable an external oscillator when all outputs are disabled. Refer to Enable Function Truth Table for additional details.<br>0 = All OE pins indicate disabled (off)<br>1 = At least one OE pin indicates enabled (on) |
| OE1      | 6                  | 16                 | 19                 | Input    | Output Enable pin for CLKOUT1. Active High. Internal 120kΩ pull-down.   |
| OE2      | 7                  | 1                  | 1                  | Input    | Output Enable pin for CLKOUT2. Active High. Internal 120kΩ pull-down.   |
| OE3      | 5                  | 4                  | 2                  | Input    | Output Enable pin for CLKOUT3. Active High. Internal 120kΩ pull-down.   |
| OE4      | —                  | 5                  | 6                  | Input    | Output Enable pin for CLKOUT4. Active High. Internal 120kΩ pull-down.   |
| OE5      | —                  | —                  | 7                  | Input    | Output Enable pin for CLKOUT5. Active High. Internal 120kΩ pull-down.   |
| OE6      | —                  | —                  | 5                  | Input    | Output Enable pin for CLKOUT6. Active High. Internal 120kΩ pull-down.   |
| CLKOUT1  | 8                  | 13                 | 17                 | Output   | Clock Output 1. Same frequency as CLKIN.  |
| CLKOUT2  | 9                  | 11                 | 16                 | Output   | Clock Output 2. Same frequency as CLKIN.  |
| CLKOUT3  | 10                 | 10                 | 14                 | Output   | Clock Output 3. Same frequency as CLKIN.  |
| CLKOUT4  | —                  | 8                  | 13                 | Output   | Clock Output 4. Same frequency as CLKIN.  |
| CLKOUT5  | —                  | —                  | 11                 | Output   | Clock Output 5. Same frequency as CLKIN.  |
| CLKOUT6  | —                  | —                  | 10                 | Output   | Clock Output 6. Same frequency as CLKIN.  |

## Enable Function Truth Table

| Input |     |     |     |     |     | Output  |         |         |         |         |         |         |
|-------|-----|-----|-----|-----|-----|---------|---------|---------|---------|---------|---------|---------|
| OE1   | OE2 | OE3 | OE4 | OE5 | OE6 | OE_ OSC | CLKOUT1 | CLKOUT2 | CLKOUT3 | CLKOUT4 | CLKOUT5 | CLKOUT6 |
| 0     | 0   | 0   | 0   | 0   | 0   | 0       | Hi-Z    | Hi-Z    | Hi-Z    | Hi-Z    | Hi-Z    | Hi-Z    |
| 1     | 0   | 0   | 0   | 0   | 0   | 1       | CLOCK   | Hi-Z    | Hi-Z    | Hi-Z    | Hi-Z    | Hi-Z    |
| 1     | 1   | 0   | 0   | 0   | 0   | 1       | CLOCK   | CLOCK   | Hi-Z    | Hi-Z    | Hi-Z    | Hi-Z    |
| ...   | ... | ... | ... | ... | ... | ...     | ...     | ...     | ...     | ...     | ...     | ...     |
| 1     | 1   | 1   | 1   | 1   | 1   | 1       | CLOCK   | CLOCK   | CLOCK   | CLOCK   | CLOCK   | CLOCK   |

## External Components

A minimum number of external components are required for proper operation. A 0.01µF bypass capacitor should be used on each VDD pin. Use a separate ground via to the board ground plane for the capacitor. Use a separate ground via for each GND pin. Do not share the ground via. Route power from the via to the VDD plane through the bypass capacitor and then to the VDD pin. A 33Ω series termination resistor should be used on each clock output pin.

To achieve the low output skew that the 5PB12xx is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30Ω series termination on one output (with 33Ω on the others) will cause at least 15ps of skew.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5PB12xx. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                                     | Rating                |
|--|-----------------------|
| Supply Voltage, VDD                      | 3.8V                  |
| Output Enable and All Inputs/Outputs     | -0.5 V to VDD + 0.5 V |
| Ambient Operating Temperature (extended) | -40 to +105°C         |
| Storage Temperature                      | -65 to +150°C         |
| Junction Temperature                     | 125°C                 |
| Soldering Temperature                    | 260°C                 |

## DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

**VDD = 1.8V ±5%**, for **5PB1203 / 1204 / 1206**, ambient temperature -40° to +105°C, unless stated otherwise.

| Parameter                       | Symbol          | Conditions                                | Min.        | Typ. | Max.        | Units |
|---------------------------------|-----------------|---|-------------|------|-------------|-------|
| Operating Voltage               | VDD             |   | 1.71        |      | 1.89        | V     |
| Input High Voltage, CLKIN       | V <sub>IH</sub> | LVC MOS input. Note 1                     | VDD/2 + 200 |      | VDD         | mV    |
| Input Low Voltage, CLKIN        | V <sub>IL</sub> | LVC MOS input. Note 1                     |             |      | VDD/2 - 200 | mV    |
| Input High Voltage, OE          | V <sub>IH</sub> |   | 0.7xVDD     |      | VDD         | V     |
| Input Low Voltage, OE           | V <sub>IL</sub> |   |             |      | 0.3xVDD     | V     |
| Output High Voltage             | V <sub>OH</sub> | I <sub>OH</sub> = -4mA                    | 0.8xVDD     |      |             | V     |
| Output Low Voltage              | V <sub>OL</sub> | I <sub>OL</sub> = 4mA                     |             |      | 0.2xVDD     | V     |
| Nominal Output Impedance        | Z <sub>O</sub>  |   |             | 17   |             | Ω     |
| Input Capacitance               | C <sub>IN</sub> |   |             | 5    |             | pF    |
| <b>Operating Supply Current</b> |                 |   |             |      |             |       |
| 5PB1203                         | IDD             | CLKIN = 26MHz, all outputs enabled        |             | 4.76 | 5.91        | mA    |
|                                 |                 | CLKIN = Low or High, all outputs disabled |             | 0.01 | 0.01        |       |
| 5PB1204                         |                 | CLKIN = 26MHz, all outputs enabled        |             | 5.99 | 7.22        |       |
|                                 |                 | CLKIN = Low or High, all outputs disabled |             | 0.01 | 0.01        |       |
| 5PB1206                         |                 | CLKIN = 26MHz, all outputs enabled        |             | 9.15 | 11.39       |       |
|                                 |                 | CLKIN = Low or High, all outputs disabled |             | 0.01 | 0.01        |       |

**VDD = 2.5V ±5%**, for **5PB1213 / 1214 / 1216**, ambient temperature -40° to +105°C, unless stated otherwise.

| Parameter                       | Symbol          | Conditions                                | Min.        | Typ.  | Max.        | Units |
|---------------------------------|-----------------|---|-------------|-------|-------------|-------|
| Operating Voltage               | VDD             |   | 2.375       |       | 2.625       | V     |
| Input High Voltage, CLKIN       | V <sub>IH</sub> | LVC MOS input. Note 1                     | VDD/2 + 200 |       | VDD         | mV    |
| Input Low Voltage, CLKIN        | V <sub>IL</sub> | LVC MOS input. Note 1                     |             |       | VDD/2 - 200 | mV    |
| Input High Voltage, OE          | V <sub>IH</sub> |   | 0.7xVDD     |       | VDD         | V     |
| Input Low Voltage, OE           | V <sub>IL</sub> |   |             |       | 0.3xVDD     | V     |
| Output High Voltage             | V <sub>OH</sub> | I <sub>OH</sub> = -4mA                    | 0.8xVDD     |       |             | V     |
| Output Low Voltage              | V <sub>OL</sub> | I <sub>OL</sub> = 4mA                     |             |       | 0.2xVDD     | V     |
| Nominal Output Impedance        | Z <sub>O</sub>  |   |             | 17    |             | Ω     |
| Input Capacitance               | C <sub>IN</sub> | ICLK, OE pin                              |             | 5     |             | pF    |
| <b>Operating Supply Current</b> |                 |   |             |       |             |       |
| 5PB1213                         | IDD             | CLKIN = 26MHz, all outputs enabled        |             | 6.66  | 8.54        | mA    |
|                                 |                 | CLKIN = Low or High, all outputs disabled |             | 0.01  | 0.02        |       |
| 5PB1214                         |                 | CLKIN = 26MHz, all outputs enabled        |             | 8.36  | 10.48       |       |
|                                 |                 | CLKIN = Low or High, all outputs disabled |             | 0.01  | 0.03        |       |
| 5PB1216                         |                 | CLKIN = 26MHz, all outputs enabled        |             | 12.58 | 16.30       |       |
|                                 |                 | CLKIN = Low or High, all outputs disabled |             | 0.01  | 0.04        |       |

**VDD = 3.3V ±5%**, for **5PB1213 / 1214 / 1216**, ambient temperature -40° to +105°C, unless stated otherwise

| Parameter                       | Symbol          | Conditions                                | Min.        | Typ.  | Max.        | Units |
|---------------------------------|-----------------|---|-------------|-------|-------------|-------|
| Operating Voltage               | VDD             |   | 3.135       |       | 3.465       | V     |
| Input High Voltage, CLKIN       | V <sub>IH</sub> | LVC MOS input. Note 1                     | VDD/2 + 200 |       | VDD         | mV    |
| Input Low Voltage, CLKIN        | V <sub>IL</sub> | LVC MOS input. Note 1                     |             |       | VDD/2 - 200 | mV    |
| Input High Voltage, OE          | V <sub>IH</sub> |   | 0.7xVDD     |       | VDD         | V     |
| Input Low Voltage, OE           | V <sub>IL</sub> |   |             |       | 0.3xVDD     | V     |
| Output High Voltage             | V <sub>OH</sub> | I <sub>OH</sub> = -4mA                    | 0.8xVDD     |       |             | V     |
| Output Low Voltage              | V <sub>OL</sub> | I <sub>OL</sub> = 4mA                     |             |       | 0.2xVDD     | V     |
| Nominal Output Impedance        | Z <sub>O</sub>  |   |             | 17    |             | Ω     |
| Input Capacitance               | C <sub>IN</sub> | ICLK, OE pin                              |             | 5     |             | pF    |
| <b>Operating Supply Current</b> |                 |   |             |       |             |       |
| 5PB1213                         | IDD             | CLKIN = 26MHz, all outputs enabled        |             | 8.96  | 11.65       | mA    |
|                                 |                 | CLKIN = Low or High, all outputs disabled |             | 0.14  | 0.45        |       |
| 5PB1214                         |                 | CLKIN = 26MHz, all outputs enabled        |             | 11.34 | 14.06       |       |
|                                 |                 | CLKIN = Low or High, all outputs disabled |             | 0.20  | 0.63        |       |
| 5PB1216                         |                 | CLKIN = 26MHz, all outputs enabled        |             | 16.87 | 21.72       |       |
|                                 |                 | CLKIN = Low or High, all outputs disabled |             | 0.22  | 0.70        |       |

Notes: 1. Nominal switching threshold is VDD/2.

## AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

**VDD = 1.8V ±5%**; for 5PB1203 / 1204 / 1206, ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter   | Symbol                            | Conditions   | Min. | Typ. | Max. | Units |
|---|-----------------------------------|--|------|------|------|-------|
| Input Frequency   |                                   |  | 0    |      | 200  | MHz   |
| Output Rise Time  | t <sub>OR</sub>                   | 0.36 to 1.44V, C <sub>L</sub> = 5pF                                      |      | 0.6  | 1.0  | ns    |
| Output Fall Time  | t <sub>OF</sub>                   | 1.44 to 0.36V, C <sub>L</sub> = 5pF                                      |      | 0.6  | 1.0  | ns    |
| Propagation Delay                                       | Note 1                            | Note 1   | 1.5  | 2.0  | 2.5  | ns    |
| Buffer Additive Phase Jitter, RMS                       |                                   | 26MHz TCXO clipped sine wave input, Integration Range: 12kHz to 20MHz    |      | 420  |      | fs    |
|   |                                   | 125MHz LVCMOS input, Integration Range: 12kHz to 20MHz                   |      | 42   |      | fs    |
| Output to Output Skew                                   | t <sub>SKEWO-O</sub>              | Note 2, Rising edges at VDD/2  |      | 20   | 50   | ps    |
| Device to Device Skew                                   | t <sub>SKEWD-D</sub>              | Rising edges at VDD/2  |      |      | 200  | ps    |
| Output Enable/Disable time (OEx to CLKOUTx driven/Hi-Z) | t <sub>EN</sub> /t <sub>DIS</sub> | CL < 5pF   |      |      | 5.5  | ns    |
| Start-up Time   | t <sub>START-UP</sub>             |  |      |      | 2    | ms    |
| TCXO Clock Clipped Sine Wave Input Voltage Swing Level  | V <sub>INpp</sub>                 | VDD = 1.8V, should connect to CLKIN through AC coupling and bias circuit |      | 0.8  |      | V     |

**VDD = 2.5V ±5%**; for 5PB1213 / 1214 / 1216, ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter   | Symbol                            | Conditions   | Min. | Typ. | Max. | Units |
|---|-----------------------------------|--|------|------|------|-------|
| Input Frequency   |                                   |  | 0    |      | 200  | MHz   |
| Output Rise Time  | t <sub>OR</sub>                   | 0.5 to 2.0V, C <sub>L</sub> = 5pF  |      | 0.6  | 1.0  | ns    |
| Output Fall Time  | t <sub>OF</sub>                   | 2.0 to 0.5V, C <sub>L</sub> = 5pF  |      | 0.6  | 1.0  | ns    |
| Propagation Delay                                       | Note 1                            | Note 1   | 1.7  | 2.2  | 2.7  | ns    |
| Buffer Additive Phase Jitter, RMS                       |                                   | 26MHz TCXO clipped sine wave input, Integration Range: 12kHz to 20MHz    |      | 280  |      | fs    |
|   |                                   | 125MHz LVCMOS input, Integration Range: 12kHz to 20MHz                   |      | 30   |      | fs    |
| Output to Output Skew                                   | t <sub>SKEWO-O</sub>              | Note 2, Rising edges at VDD/2  |      | 20   | 50   | ps    |
| Device to Device Skew                                   | t <sub>SKEWD-D</sub>              | Rising edges at VDD/2  |      |      | 200  | ps    |
| Output Enable/Disable time (OEx to CLKOUTx driven/Hi-Z) | t <sub>EN</sub> /t <sub>DIS</sub> | CL < 5pF   |      |      | 3.8  | ns    |
| Start-up Time   | t <sub>START-UP</sub>             | Part start-up time for valid outputs after VDD ramp-up                   |      |      | 2    | ms    |
| TCXO Clock Clipped Sine Wave Input Voltage Swing Level  | V <sub>INpp</sub>                 | VDD = 2.5V, should connect to CLKIN through AC coupling and bias circuit |      | 0.8  |      | V     |

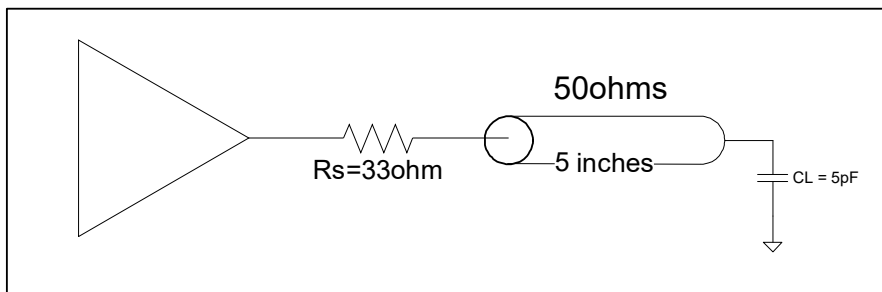
VDD = 3.3V ±5%; for 5PB1213 / 1214 / 1216, ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter   | Symbol                            | Conditions   | Min. | Typ. | Max. | Units |
|---|-----------------------------------|--|------|------|------|-------|
| Input Frequency   |                                   |  | 0    |      | 200  | MHz   |
| Output Rise Time  | t <sub>OR</sub>                   | 0.66 to 2.64V, C <sub>L</sub> = 5pF                                      |      | 0.6  | 1.0  | ns    |
| Output Fall Time  | t <sub>OF</sub>                   | 2.64 to 0.66V, C <sub>L</sub> = 5pF                                      |      | 0.6  | 1.0  | ns    |
| Propagation Delay                                       | Note 1                            | Note 1   | 1.4  | 1.9  | 2.4  | ns    |
| Buffer Additive Phase Jitter, RMS                       |                                   | 26MHz TCXO clipped sine wave input, Integration Range: 12kHz to 20MHz    |      | 377  |      | fs    |
|   |                                   | 125MHz LVCMOS input, Integration Range: 12kHz to 20MHz                   |      | 18   |      | fs    |
| Output to Output Skew                                   | t <sub>SKEWO-O</sub>              | Note 2, Rising edges at VDD/2  |      | 20   | 50   | ps    |
| Device to Device Skew                                   | t <sub>SKEWD-D</sub>              | Rising edges at VDD/2  |      |      | 200  | ps    |
| Output Enable/Disable time (OEx to CLKOUTx driven/Hi-Z) | t <sub>EN</sub> /t <sub>DIS</sub> | CL < 5pF   |      |      | 3.2  | ns    |
| Start-up Time   | t <sub>START-UP</sub>             | Part start-up time for valid outputs after VDD ramp-up                   |      |      | 2    | ms    |
| TCXO Clock Clipped Sine Wave Input Voltage Swing Level  | VIN <sub>pp</sub>                 | VDD = 3.3V, should connect to CLKIN through AC coupling and bias circuit |      | 0.5  |      | V     |

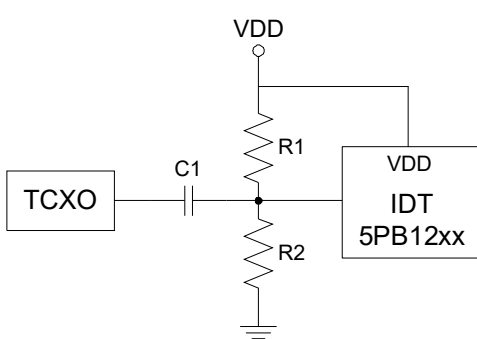
Notes:

1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

### Test Load and Circuit



### AC Coupling and Bias Circuit



| Component | Value |
|-----------|-------|
| C1        | 0.1µF |
| R1        | 10k   |
| R2        | 10k   |

## Package Outline Drawings

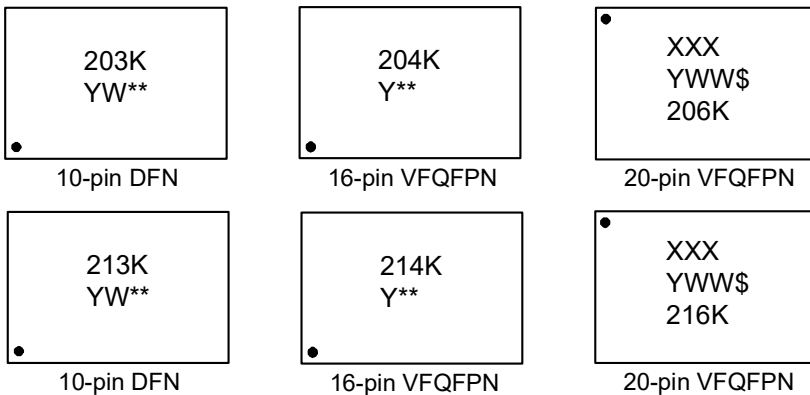
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

## Ordering Information

| Part Number  | Carrier       | Package Description           | Temp. Range   |
|--------------|---------------|-------------------------------|---------------|
| 5PB1203NTGK  | Cut Tape      | <a href="#">10-pin DFN</a>    | -40 to +105°C |
| 5PB1203NTGK8 | Tape and Reel | <a href="#">10-pin DFN</a>    | -40 to +105°C |
| 5PB1213NTGK  | Cut Tape      | <a href="#">10-pin DFN</a>    | -40 to +105°C |
| 5PB1213NTGK8 | Tape and Reel | <a href="#">10-pin DFN</a>    | -40 to +105°C |
| 5PB1204CMGK  | Cut Tape      | <a href="#">16-pin VFQFPN</a> | -40 to +105°C |
| 5PB1204CMGK8 | Tape and Reel | <a href="#">16-pin VFQFPN</a> | -40 to +105°C |
| 5PB1214CMGK  | Cut Tape      | <a href="#">16-pin VFQFPN</a> | -40 to +105°C |
| 5PB1214CMGK8 | Tape and Reel | <a href="#">16-pin VFQFPN</a> | -40 to +105°C |
| 5PB1206NDGK  | Tube          | <a href="#">20-pin VFQFPN</a> | -40 to +105°C |
| 5PB1206NDGK8 | Tape and Reel | <a href="#">20-pin VFQFPN</a> | -40 to +105°C |
| 5PB1216NDGK  | Tube          | <a href="#">20-pin VFQFPN</a> | -40 to +105°C |
| 5PB1216NDGK8 | Tape and Reel | <a href="#">20-pin VFQFPN</a> | -40 to +105°C |

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

## Marking Diagrams



### Notes:

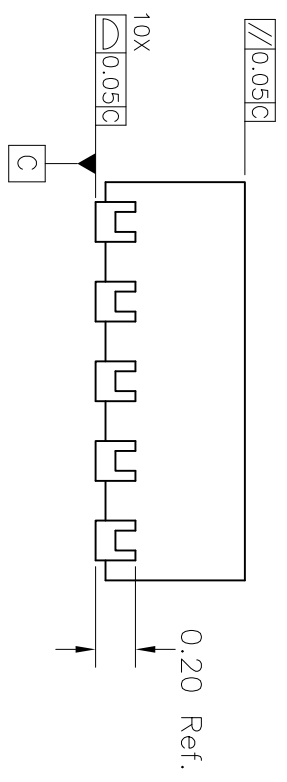
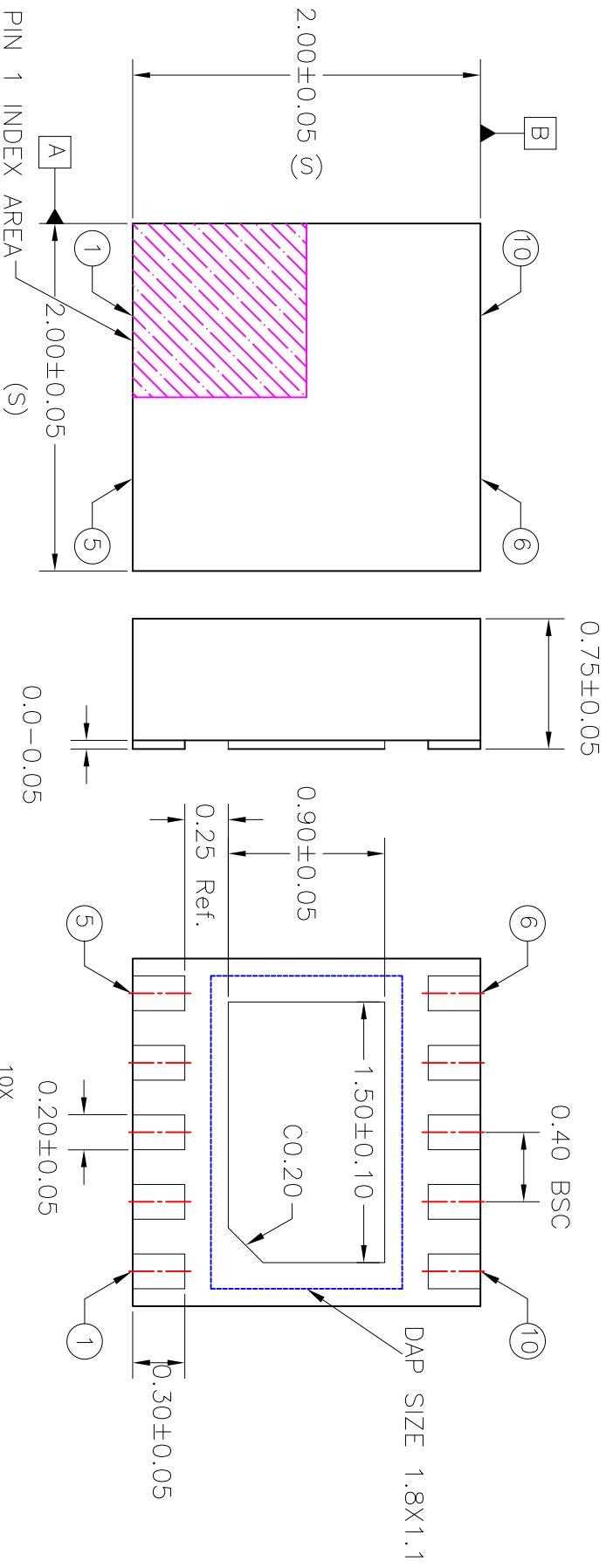
1. “\*\*” is the lot number.
2. “YWW”, “YW”, or “Y” are the last digit(s) of the year and week that the part was assembled.
3. “\$” denotes mark location code.
4. “K” denotes extended temperature range device.
5. “XXX” denotes last three characters of Asm lot.



## Revision History

| Date              | Description of Change   |
|-------------------|---|
| June 7, 2022      | <ul style="list-style-type: none"> <li>▪ Updated pin 1 dot location for 20-pin VFQFPN <a href="#">Marking Diagrams</a>.</li> <li>▪ Updated <a href="#">Package Outline Drawings</a> and <a href="#">Ordering Information</a> section.</li> </ul>  |
| December 7, 2021  | <ul style="list-style-type: none"> <li>▪ Updated <a href="#">Pin Descriptions</a>.</li> <li>▪ Corrected <a href="#">Output Enable/Disable time (OEx to CLKOUTx driven/Hi-Z)</a> enable/disable time for 1.8V, 2.5V, and 3.3V AC Electrical Characteristics.</li> </ul>  |
| January 15, 2021  | Updated 1st paragraph text in External Components section.  |
| February 3, 2020  | <ul style="list-style-type: none"> <li>▪ Updated the capacitor value for C1 in <a href="#">AC Coupling and Bias Circuit</a></li> </ul>  |
| November 22, 2019 | <ul style="list-style-type: none"> <li>▪ Updated "Operating Supply Current" data in <a href="#">DC Electrical Characteristics</a> for VDD = 1.8V ±5%, VDD = 2.5V ±5%, and VDD = 3.3V ±5%</li> <li>▪ Updated <a href="#">Package Outline Drawings</a>; however, no mechanical changes</li> </ul>   |
| February 28, 2018 | <ul style="list-style-type: none"> <li>▪ Updated CLKIN input high and low voltage ratings in DC characterization tables.</li> <li>▪ Updated Absolute Maximum supply voltage (VDD) from 3.465V to 3.8V.</li> </ul>   |
| April 10, 2017    | <ul style="list-style-type: none"> <li>▪ Updated Operating Supply Current and Operating Voltage values in DC electrical characteristics tables.</li> <li>▪ Updated Propagation Delay and Output skew values in AC electrical characteristics tables.</li> <li>▪ Updated package outline drawings.</li> <li>▪ Updated legal disclaimer.</li> </ul> |
| July 11, 2016     | Initial release.  |

| REVISIONS |                 |         |          |
|-----------|-----------------|---------|----------|
| REV       | DESCRIPTION     | DATE    | APPROVED |
| 00        | INITIAL RELEASE | 5/20/15 | J.HUA    |

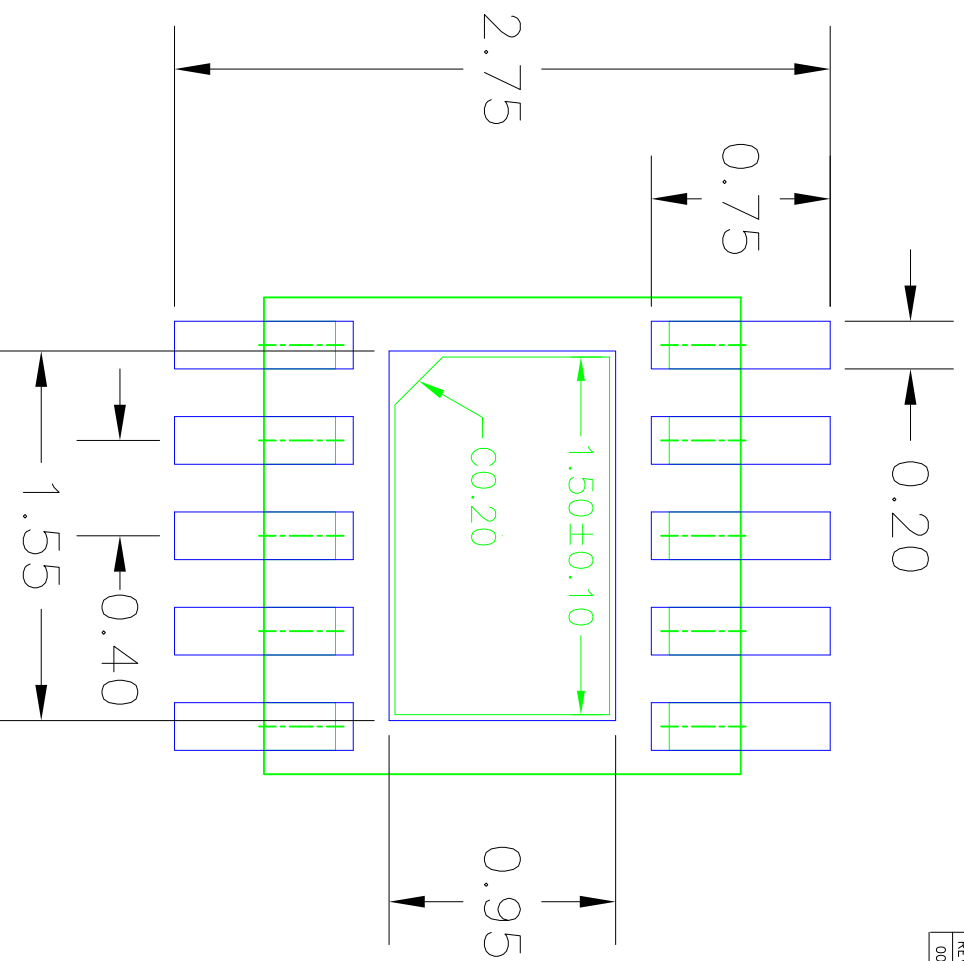


NOTES:

1. ALL DIMENSIONS IN MM.

|                             |         |                    |         |   |             |
|-----------------------------|---------|--------------------|---------|---|-------------|
| TOLERANCES UNLESS SPECIFIED |         |                    |         | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674 |             |
| DECIMAL                     | ANGULAR | <b>www.IDT.com</b> |         | TITLE NTG10 PACKAGE OUTLINE<br>2.0 x 2.0 mm BODY<br>0.75 mm THICK                                 |             |
| ±                           | ±       | APPROVALS          | DATE    | SIZE  | DRAWING No. |
| XXXX                        | XXXX    | DRAWN <i>QAC</i>   | 5/20/15 | C   | PSC-4612    |
| XXXX                        | XXXX    | CHECKED            |         |   |             |
| DO NOT SCALE DRAWING        |         |                    | SHEET   | 1   | OF 2        |


| REVISIONS |                 |         |          |
|-----------|-----------------|---------|----------|
| REV       | DESCRIPTION     | DATE    | APPROVED |
| 00        | INITIAL RELEASE | 5/20/15 | JHUA     |



RECOMMENDED LAND PATTERN DIMENSION

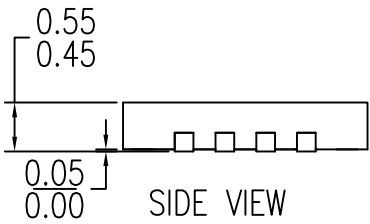
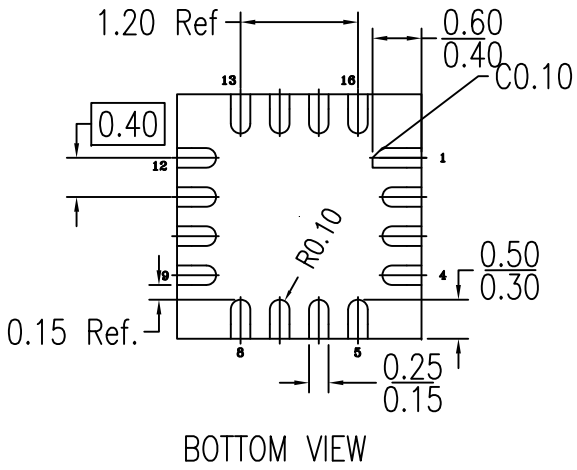
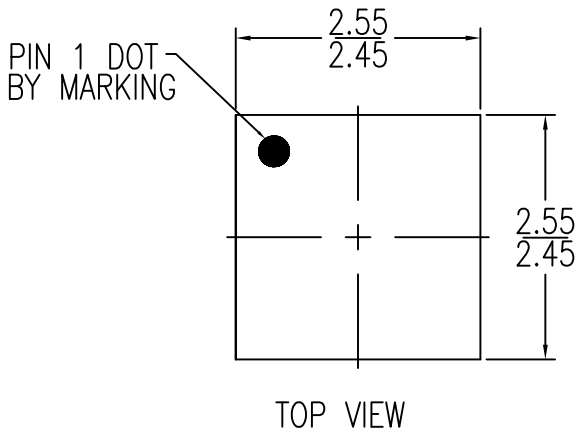
NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE IS SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.


|                              |         |   |  |
|------------------------------|---------|---|--|
| TOLERANCES UNLESS SPECIFIED  |         | 6024 Silver Creek Valley Rd   |  |
| DECIMAL                      | ANGULAR | San Jose, CA 95138  |  |
| ±                            | ±       | PHONE: (408) 727-6116   |  |
| ±                            | ±       | FAX: (408) 492-8874   |  |
| DRAWN BY: JALG               |         |  <b>IDT</b><br>6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8874 |  |
| DATE: 5/20/15                |         |   |  |
| TITLE: NIG10 PACKAGE OUTLINE |         | www.IDT.com   |  |
| SIZE: 2.0 x 2.0 mm BODY      |         | PSC-4612  |  |
| CHECKED: JALG                |         | DRAWING No. PSC-4612  |  |
| DO NOT SCALE DRAWING         |         | SHEET 2 OF 2  |  |

| REVISIONS    |     |  |        |
|--------------|-----|--|--------|
| DATE CREATED | REV | DESCRIPTION                                    | AUTHOR |
| 4/3/14       | 00  | INITIAL RELEASE                                | JH     |
| 12/11/14     | 01  | ADD PIN1 CHAMFER                               | JH     |
| 4/5/18       | 02  | CHANGE QFN TO VFQFPN, RECALCULATE LAND PATTERN | RC     |

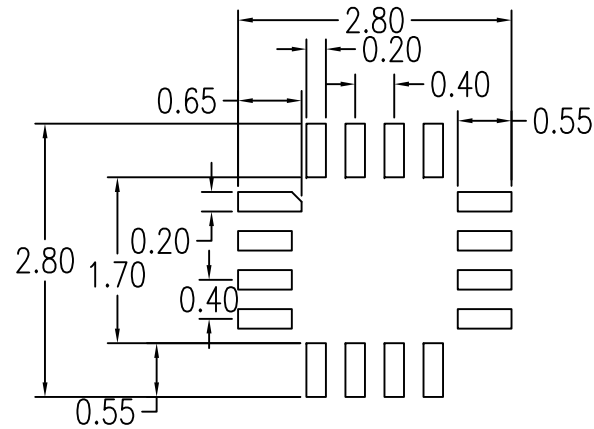
NOE: REFER TO DCP FOR OFFICIAL RELEASE DATE



- NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
  2. ALL DIMENSIONS ARE IN MILLIMETERS.

|  |                |  |  |  |
|--|----------------|--|--|--|
| TOLERANCES<br>UNLESS SPECIFIED<br>DECIMAL<br>X±<br>XX±<br>XXX± | ANGULAR<br>±1° |  <b>IDT™</b><br>www.IDT.com | 6024 Silver Creek Valley Road<br>San Jose CA 95138<br>PHONE: (408) 284-8200<br>FAX: (408) 284-8591 |  |
|  |                |  | TITLE CMG16 Package Outline Drawing<br>2.5 x 2.5 x 0.5 mm Body<br>0.40mm Pitch VFQFPN              |  |
| DRAWN  | SIZE           | DRAWING No.  | REV  |  |
|  | C              | PSC-4478   | 02   |  |
| DO NOT SCALE DRAWING   |                |  | SHEET 1 OF 2   |  |


| REVISIONS                                   |     |  |        |
|---|-----|--|--------|
| DATE CREATED                                | REV | DESCRIPTION                                    | AUTHOR |
| 4/3/14                                      | 00  | INITIAL RELEASE                                | JH     |
| 12/11/14                                    | 01  | ADD PIN1 CHAMFER                               | JH     |
| 4/5/18                                      | 02  | CHANGE QFN TO VFQFPN, RECALCULATE LAND PATTERN | RC     |
| NOE: REFER TO DCP FOR OFFICIAL RELEASE DATE |     |  |        |

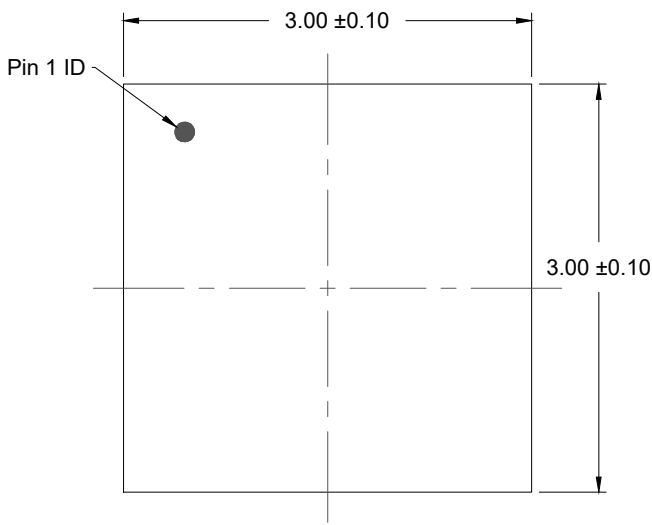


RECOMMENDED LAND PATTERN DIMENSION

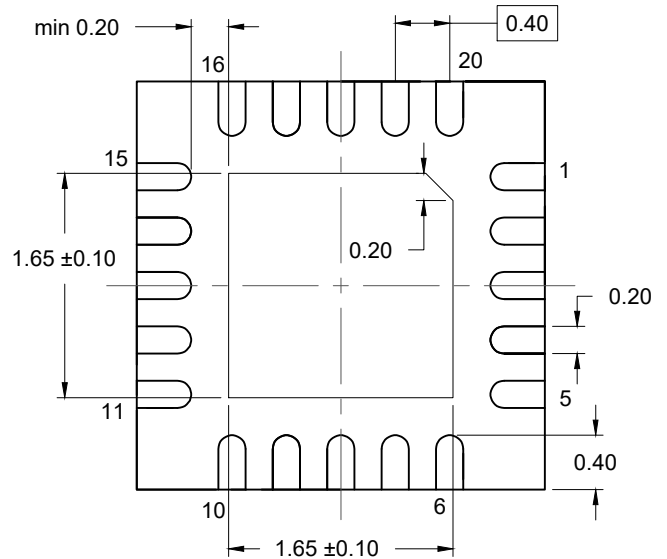
NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

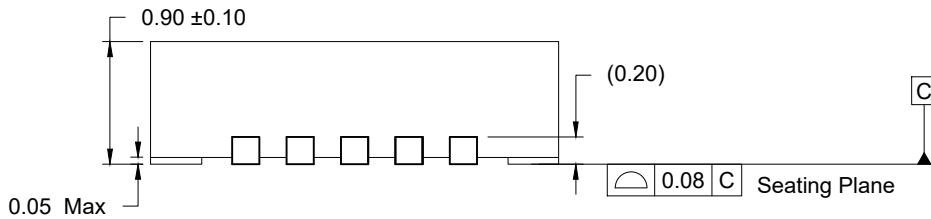
|                             |   |   |
|-----------------------------|---|---|
| TOLERANCES UNLESS SPECIFIED |   |  <b>IDT™</b> 6024 Silver Creek Valley Road<br>San Jose CA 95138<br>PHONE: (408) 284-8200<br>FAX: (408) 284-8591<br>www.IDT.com |
| DECIMAL                     | ANGULAR   |   |
| X±                          | ±1°   |   |
| XX±                         |   |   |
| XXX±                        |   |   |
| DRAWN                       | TITLE CMG16 Package Outline Drawing<br>2.5 x 2.5 x 0.5 mm Body<br>0.40mm Pitch VFQFPN |   |
|                             | SIZE  | DRAWING No.   |
|                             | C   | PSC-4478  |
|                             | REV   | 02  |
| DO NOT SCALE DRAWING        |   | SHEET 2 OF 2  |



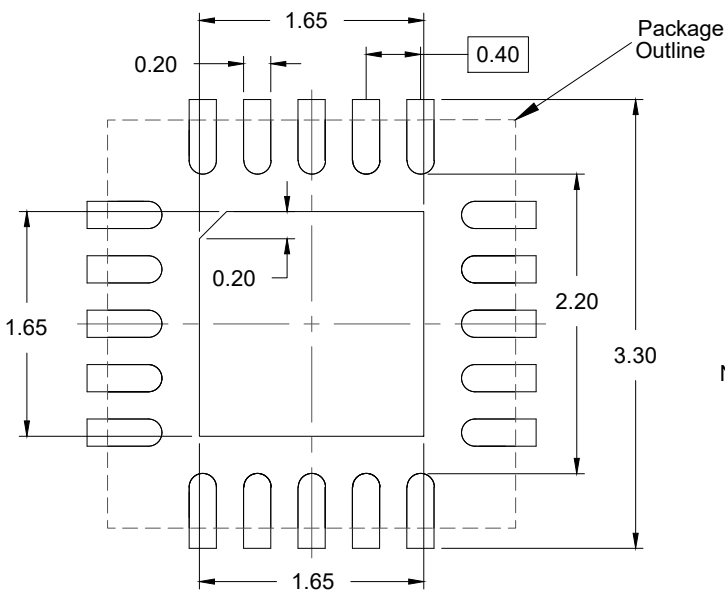
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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