

## General Description

The 840002I-01 is a two output LVCMOS/LVTTL Synthesizer optimized to generate Ethernet reference clock frequencies. Using a 25MHz 18pF parallel resonant crystal, the following frequencies can be generated based on the two frequency select pins (F\_SEL[1:0]): 156.25MHz, 125MHz, and 62.5MHz. The 840002I-01 uses IDT's 3<sup>RD</sup> generation low phase noise VCO technology and can achieve 1ps or lower typical random rms phase jitter, easily meeting Ethernet jitter requirements. The 840002I-01 is packaged in a small 16-pin TSSOP package.

Frequency Select Function Table

Inputs				Output Frequency (25MHz Ref.)
F_SEL1	F_SEL0	M Divider Value	N Divider Value	
0	0	25	4	156.25
0	1	25	5	125
1	0	25	10	62.5
1	1	25	5	125

## Features

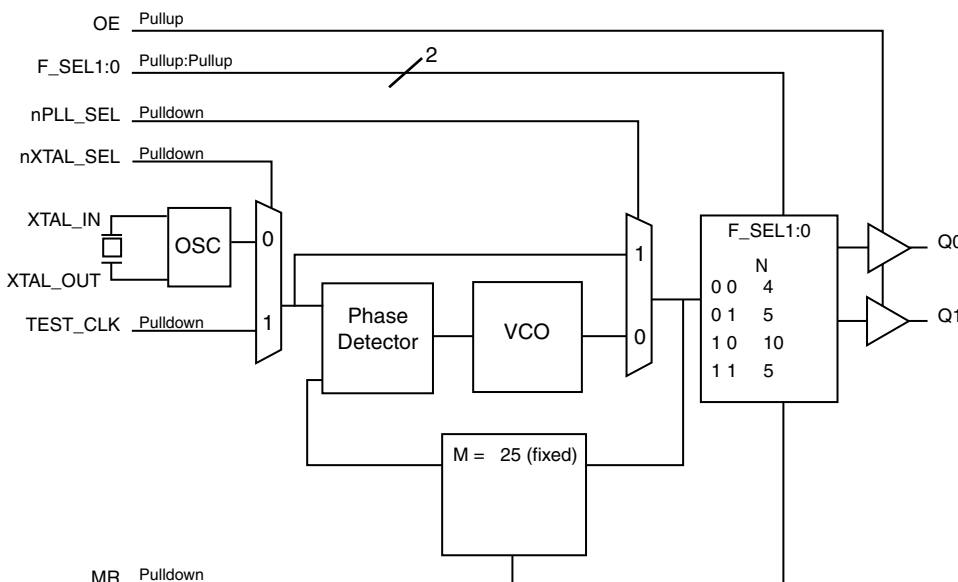
- Two LVCMOS/LVTTL outputs@ 3.3V, 17Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended TEST\_CLK
- Supports the following output frequencies: 156.25MHz, 125MHz and 62.5MHz
- Output frequency range: 56MHz to 175MHz
- VCO range: 560MHz to 700MHz
- Output skew: 12ps (maximum)
- RMS phase jitter at 156.25MHz, (1.875MHz to 20MHz): 0.47ps (typical)

### Phase Noise:

Offset	Noise Power
100Hz .....	-97.4 dBc/Hz
1kHz .....	-120.2 dBc/Hz
10kHz .....	-127.6 dBc/Hz
100kHz .....	-126.1 dBc/Hz

- Power Supply Modes:  
Core / Output  
3.3V / 3.3V  
3.3V / 2.5V  
2.5V / 2.5V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram



## Pin Assignment

F_SEL0	1	16	F_SEL1
nXTAL_SEL	2	15	GND
TEST_CLK	3	14	GND
OE	4	13	Q0
MR	5	12	Q1
nPLL_SEL	6	11	VDD0
VDDA	7	10	XTAL_IN
VDD	8	9	XTAL_OUT

840002I-01

16-Lead TSSOP

4.4mm x 5.0mm x 0.925mm  
package body  
G Package  
Top View

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	F_SEL0	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
2	nXTAL_SEL	Input	Pulldown	Selects between crystal or TEST_CLK inputs as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.
3	TEST_CLK	Input	Pulldown	Single-ended test clock input. LVCMOS/LVTTL interface levels.
4	OE	Input	Pullup	Output enable. When logic HIGH, the outputs are active. When LOW, the outputs are in high-impedance state. LVCMOS/LVTTL interface levels.
5	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the active outputs to go low. When Logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	nPLL_SEL	Input	Pulldown	PLL Bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = reference clock frequency/N output divider. LVCMOS/LVTTL interface levels.
7	V <sub>DDA</sub>	Power		Analog supply pin.
8	V <sub>DD</sub>	Power		Core supply pin.
9, 10	XTAL_OUT XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
11	V <sub>DDO</sub>	Power		Output supply pin.
12, 13	Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
14, 15	GND	Power		Power supply ground.
16	F_SEL1	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
C <sub>PD</sub>	Power Dissipation Capacitance			8		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance	V <sub>DDO</sub> = 3.3V ± 5%	14	17	21	Ω
		V <sub>DDO</sub> = 2.5V ± 5%	16	21	25	Ω

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$ XTAL_IN Other Inputs	0V to $V_{DD}$ -0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	89°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				100	mA
$I_{DDA}$	Analog Supply Current				12	mA
$I_{DDO}$	Output Supply Current				5	mA

**Table 3B. Power Supply DC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDA}$	Analog Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
$I_{DD}$	Power Supply Current				95	mA
$I_{DDA}$	Analog Supply Current				12	mA
$I_{DDO}$	Output Supply Current				5	mA

**Table 3C. LVC MOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ; or  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		$V_{DD} = 3.3V$	-0.3		0.8	V
			$V_{DD} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	OE, F_SEL0, F_SEL1	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu\text{A}$
		MR, TEST_CLK, nXTAL_SEL, nPLL_SEL	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	OE, F_SEL0, F_SEL1	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu\text{A}$
		MR, TEST_CLK, nXTAL_SEL, nPLL_SEL	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu\text{A}$
$V_{OH}$	Output High Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$	2.6			V
			$V_{DDO} = 2.5V \pm 5\%$	1.8			V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$			0.5	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement Information section, *Output Load Test Circuit diagrams*.

**Table 4. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance ( $C_O$ )				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

## AC Electrical Characteristics

**Table 5A. AC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	F_SEL[1:0] = 00	140		175	MHz
		F_SEL[1:0] = 01 or 11	112		140	MHz
		F_SEL[1:0] = 10	56		70	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2				12	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 3	156.25MHz, (1.875MHz - 20MHz)		0.47		ps
		125MHz, (1.875MHz - 20MHz)		0.57		ps
		62.5MHz, (1.875MHz - 20MHz)		0.51		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		46		54	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Refer to Phase Noise Plots.

**Table 5B. AC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	F_SEL[1:0] = 00	140		175	MHz
		F_SEL[1:0] = 01 or 11	112		140	MHz
		F_SEL[1:0] = 10	56		70	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2				12	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 3	156.25MHz, (1.875MHz - 20MHz)		0.47		ps
		125MHz, (1.875MHz - 20MHz)		0.55		ps
		62.5MHz, (1.875MHz - 20MHz)		0.49		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		46		54	%

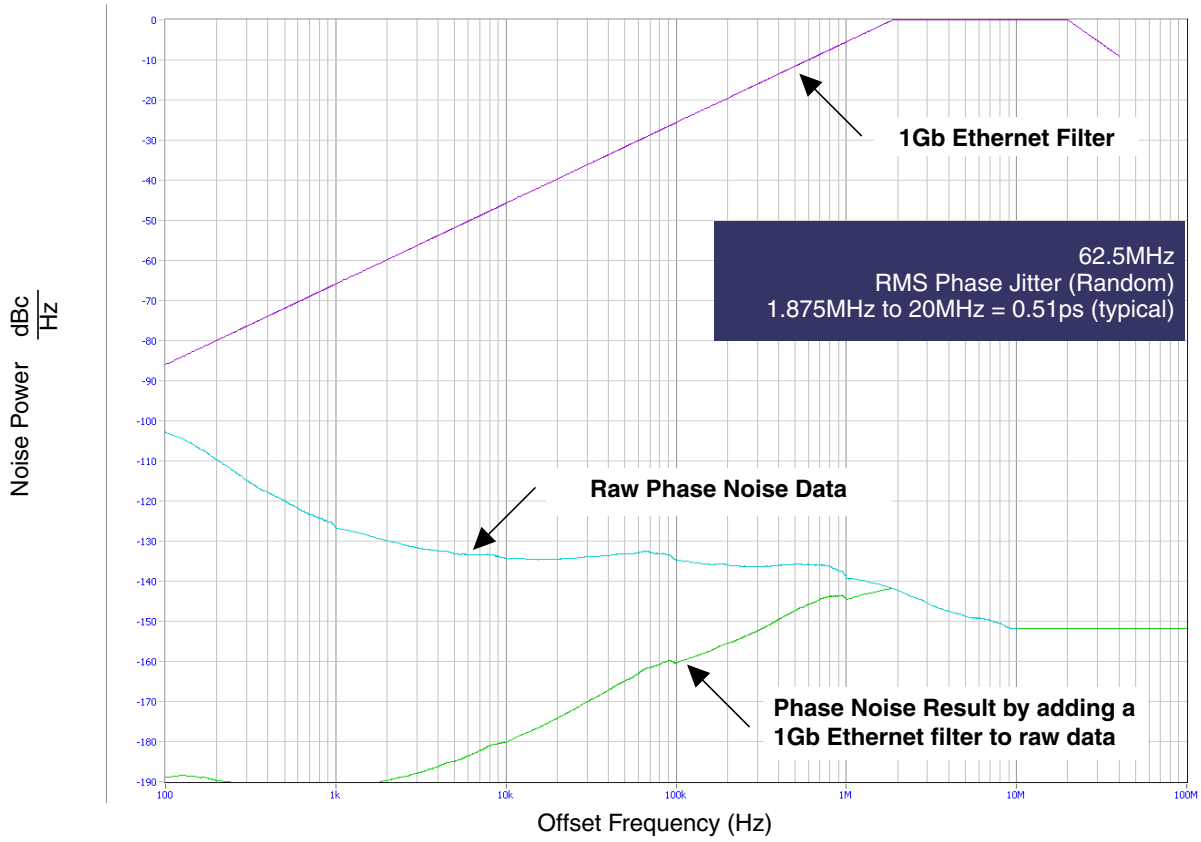
For NOTES, see Table 5A above.

**Table 5C. AC Characteristics,  $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

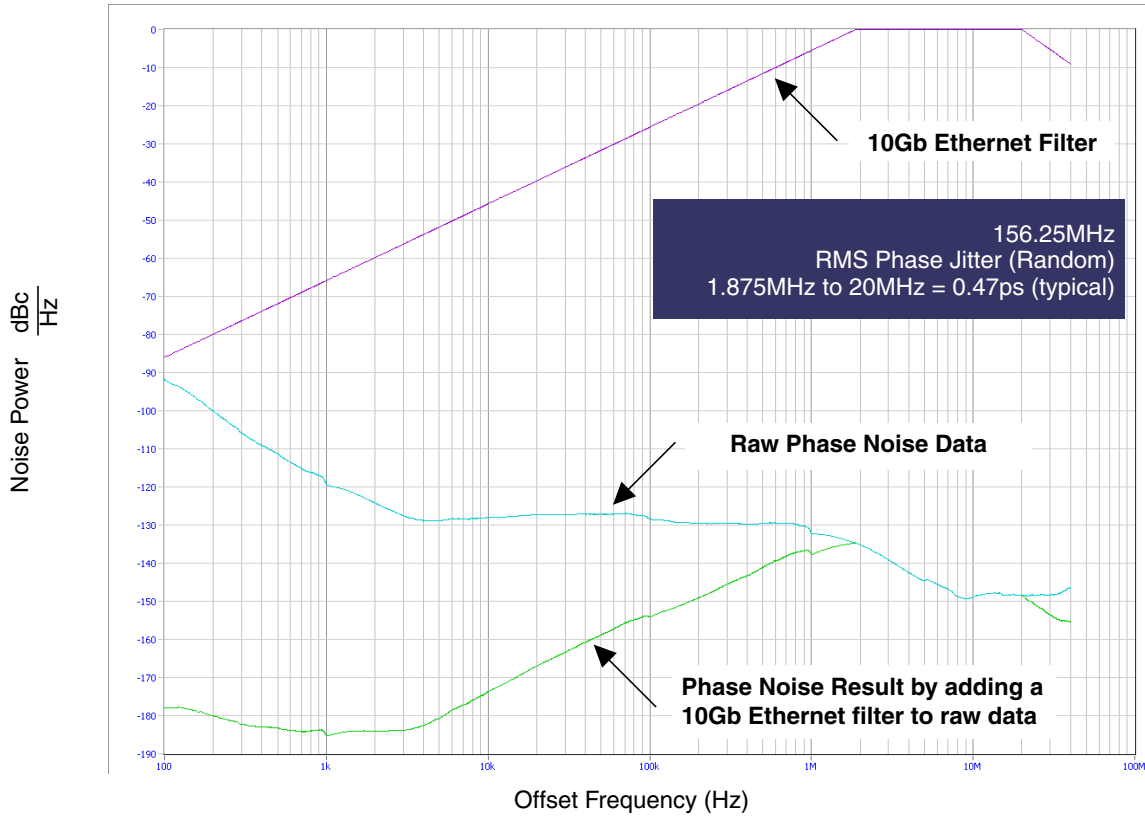
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	F_SEL[1:0] = 00	140		175	MHz
		F_SEL[1:0] = 01 or 11	112		140	MHz
		F_SEL[1:0] = 10	56		70	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2				12	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter, Random; NOTE 3	156.25MHz, (1.875MHz - 20MHz)		0.49		ps
		125MHz, (1.875MHz - 20MHz)		0.56		ps
		62.5MHz, (1.875MHz - 20MHz)		0.52		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		46		54	%
		$f_{OUT} = 125\text{MHz}$	47		53	%

For NOTES, see Table 5A above.

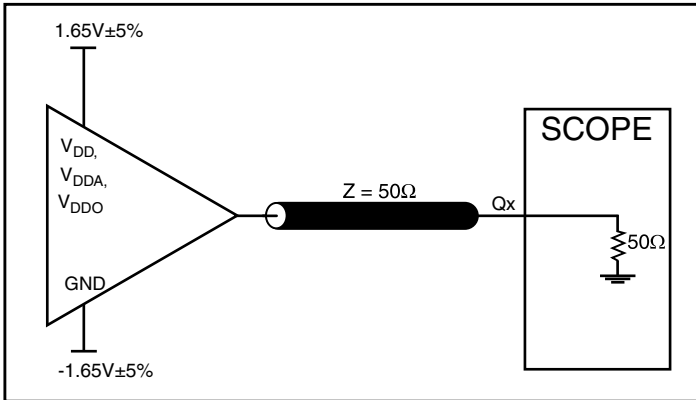
## Typical Phase Noise at 62.5MHz (3.3V)



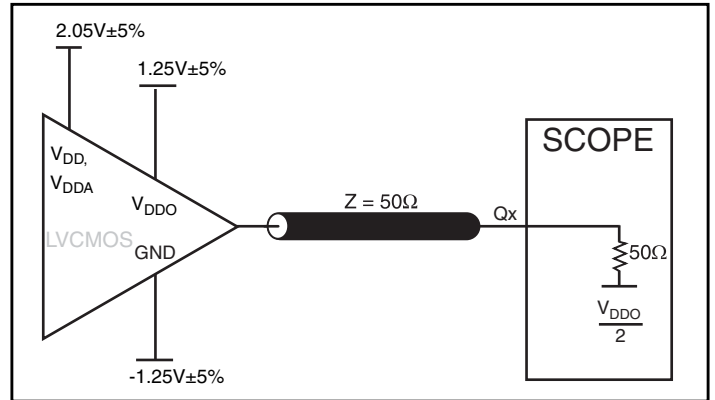
Typical Phase Noise at 156.25MHz (3.3V)



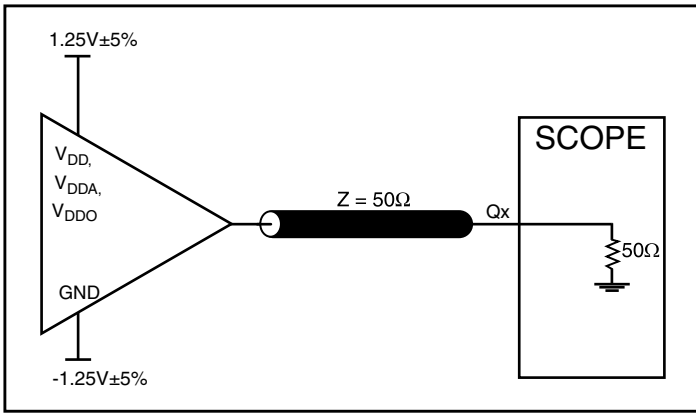
## Parameter Measurement Information



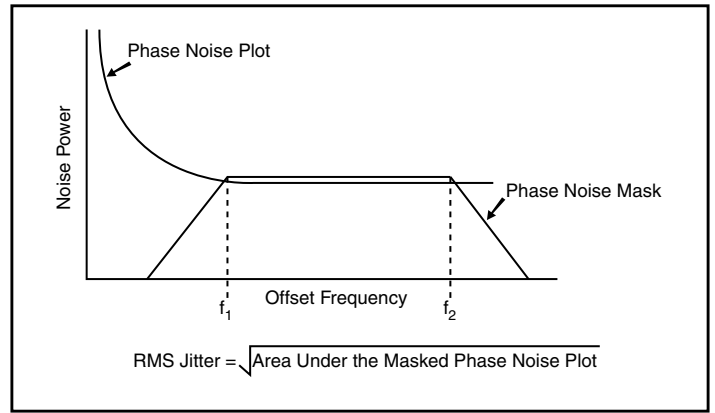
3.3V Core/3.3V Output Load AC Test Circuit



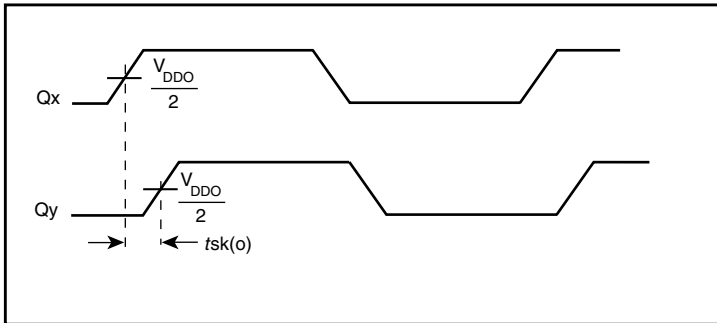
3.3V Core/2.5V Output Load AC Test Circuit



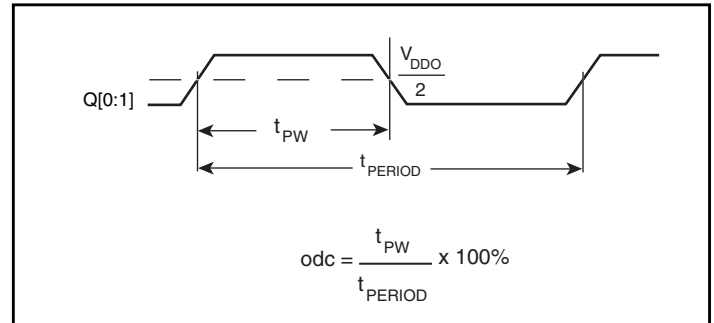
2.5V Core/2.5V Output Load AC Test Circuit



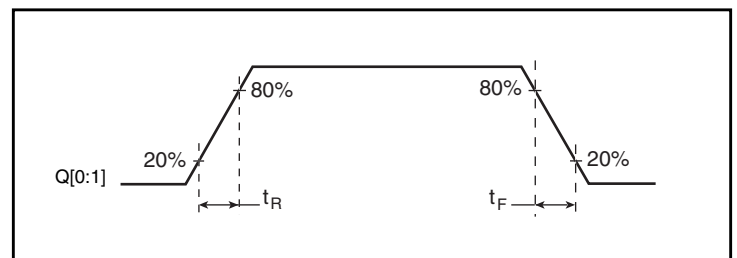
RMS Phase Jitter



Output Skew



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time



## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

##### TEST\_CLK Input

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the TEST\_CLK to ground.

##### LVC MOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### Outputs:

##### LVC MOS Outputs

All unused LVC MOS outputs can be left floating. We recommend that there is no trace attached.

## Overdriving the XTAL Interface

The XTAL\_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 1A*. The XTAL\_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition,

matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and making  $R_2$  50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

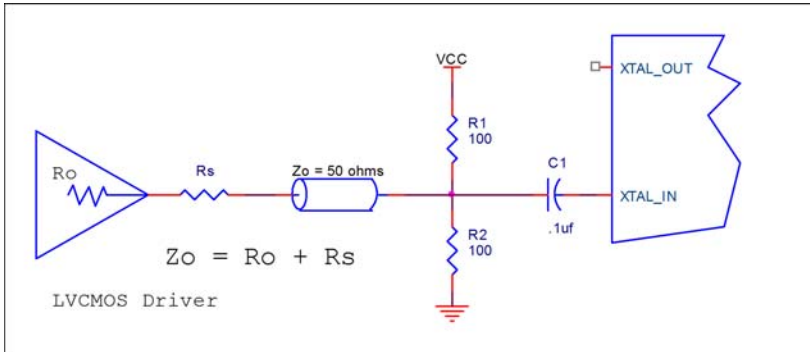


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

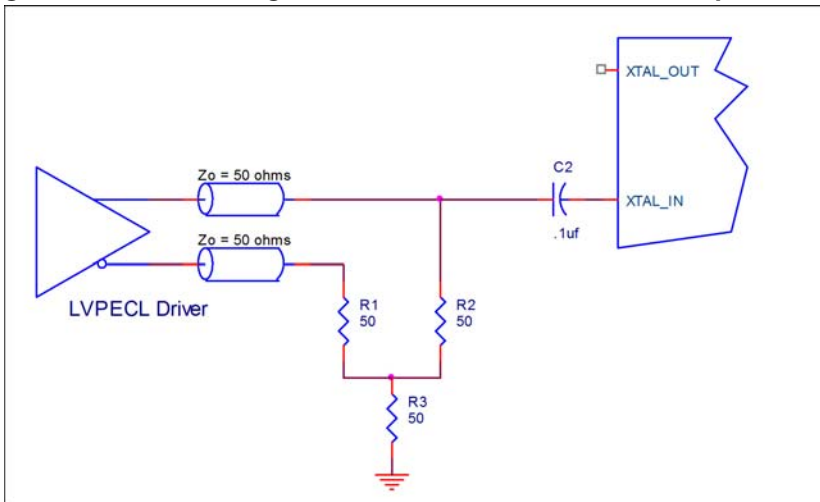


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

## Layout Guideline

Figure 2 shows a schematic example of the 840002I-01 application schematic. In this example, the device is operated at  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V$ . The 18pF parallel resonant 25MHz crystal is used. The load capacitance  $C1 = 22pF$  and  $C2 = 22pF$  are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will required adjusting  $C1$  and  $C2$ .

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The 840002I-01 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the

0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.

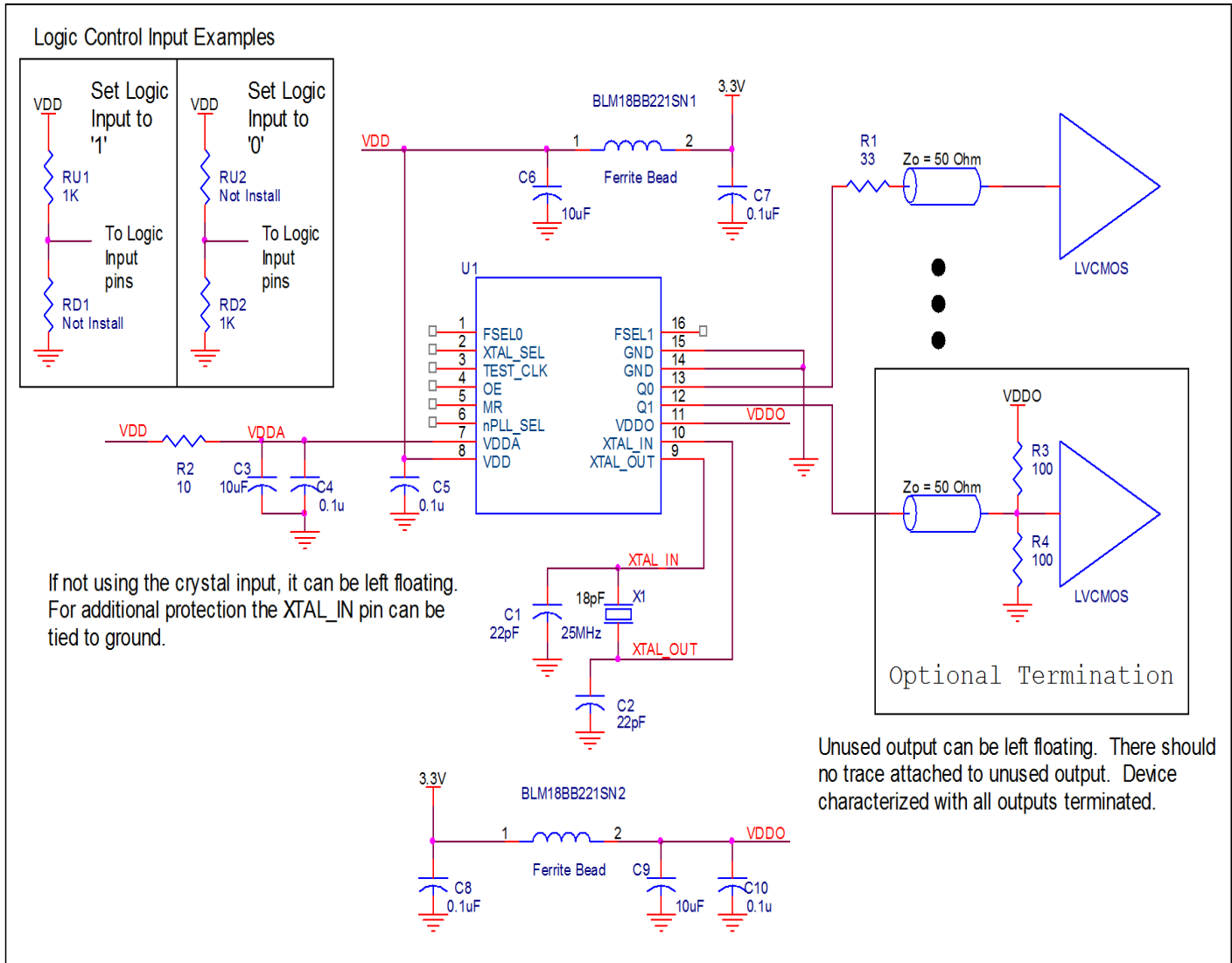


Figure 2. 840002I-01 Application Schematic Example

## Reliability Information

Table 6.  $\theta_{JA}$  vs. Air Flow Table for a 16 Lead TSSOP

Linear Feet per Minute	$\theta_{JA}$ by Velocity		
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

## Transistor Count

The transistor count for 840002I-01 is: 3356

## Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

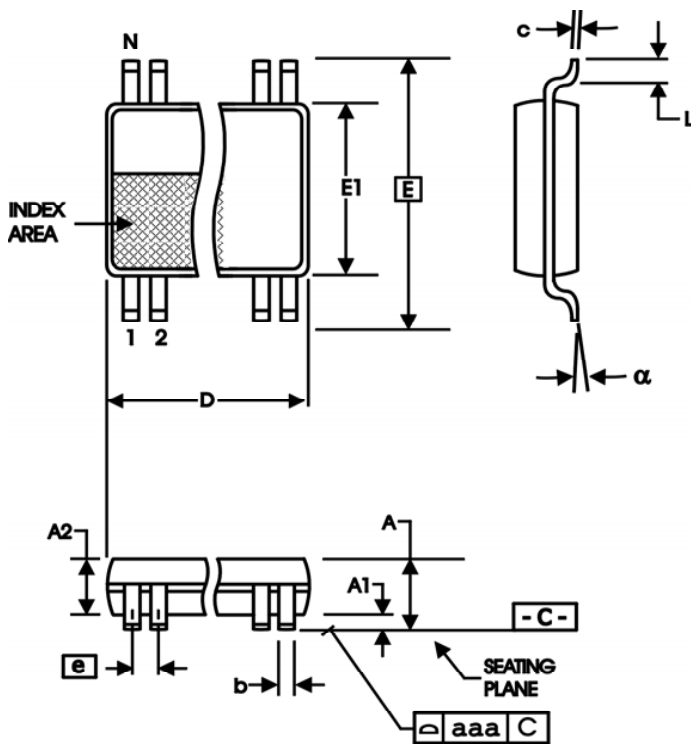


Table 7. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	16	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

**Table 8. Ordering Information**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840002AGI-01LF	002AI01L	"Lead-Free", 16 Lead LQFP	Tube	-40°C to 85°C
840002AGI-01LFT	002AI01L	"Lead-Free", 16 Lead LQFP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T8	12	Ordering Information Table - corrected standard marking and added Lead-Free part number, marking and note.	10/18/07
A	T8	12 14	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	11/18/10
A	T5A - T5C	4 - 5 8 9 10	AC Characteristics Tables - added thermal note. Power Supply Filtering Techniques - corrected figure 1. Added Overdriving the Crystal Interface section. Added Recommendations for Unused Input & Output Pins section.	12/6/10
B	T5B	5	3.3V/2.5V AC Characteristics Table -corrected F <sub>OUT</sub> from 56MHz min - 68MHz max to 56MHz min - 70MHz max.	2/3/11
	T5C	5	2.5V AC Characteristics Table - added 2nd odc spec and added thermal note. Corrected F <sub>OUT</sub> from 56MHz min - 68MHz max to 56MHz min - 70MHz max.	
		8	Deleted Power Supply Filtering Techniques section, added to schematic layout.	
		8	Deleted Crystal Input Interface section.	
		9	Added Overdriving the XTAL Interface section.	
		10	Updated Layout Guideline and diagram. Converted datasheet format.	
B	5A, 5B, 5C	5	AC Table; f <sub>OUT</sub> = F_SEL[1:0] = 01 or 11, F_SEL[1:0] = 10	9/28/12
B	8	13	Deleted Quantity from Tape and Reel	
B	T8	13	Ordering Information - removed leaded devices. Updated data sheet format.	8/5/15



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