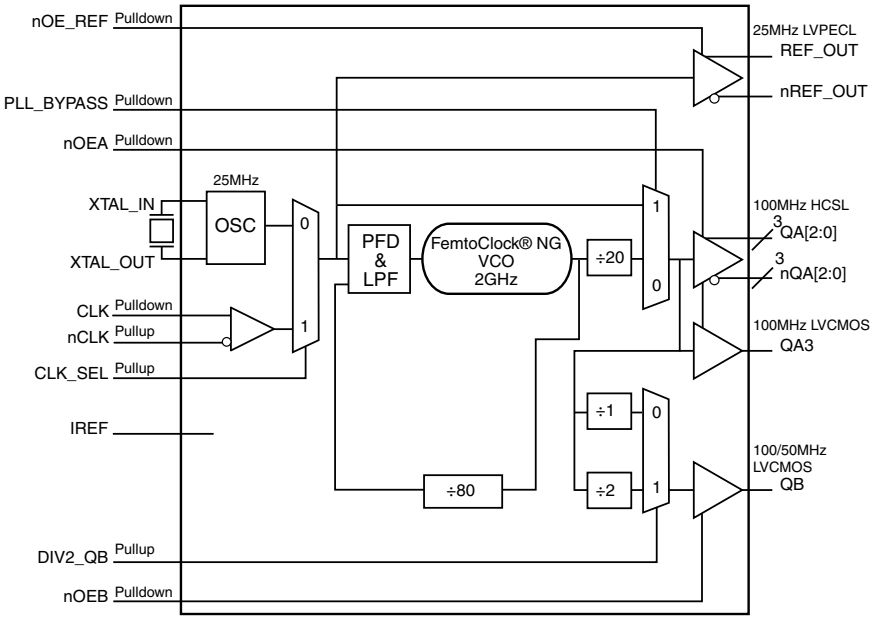
General Description

The 841N4830 is a 3 HCSL, 1 LVPECL and 2 LVCMOS output Synthesizer optimized to generate PCI Express reference clock frequencies. The device uses IDT's fourth generation FemtoClock® NG technology for synthesis of high clock frequency at very low phase noise. It provides low power consumption with good power supply noise rejection. Using a 25MHz, 12pF parallel resonant crystal, the following frequencies can be generated: 100MHz, 50MHz and 25MHz. Maximum rms phase jitter of 0.36ps, easily meets PCI Express jitter requirements. The 841N4830 is packaged in a small 32-pin VFQFN package.

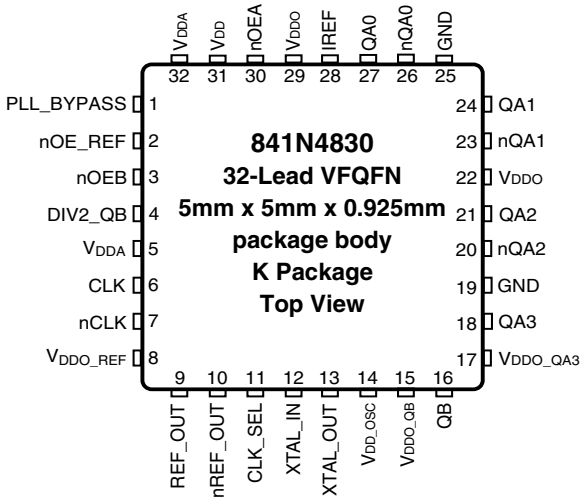
Features

- Fourth generation FemtoClock® Next Generation (NG) technology
- Three differential HCSL outputs, one differential LVPECL and two single-ended LVCMOS/LVTTL outputs
- Crystal oscillator interface designed for a 25MHz, 12pF parallel resonant crystal
- CLK/nCLK input pair can accept the following differential input levels: LVPECL, LVDS, HCSL
- A 25MHz crystal generates output frequencies of: 100MHz, 50MHz and 25MHz
- VCO frequency: 2GHz
- RMS Phase Jitter @ 100MHz, (12kHz – 20MHz) using a 25MHz crystal: 0.36ps (maximum)
- Power supply noise rejection PSNR: -45dB (typical)
- PCI Express Gen 2 (5 Gb/s) jitter compliant
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1	PLL_BYPASS	Input	Pulldown	When HIGH, PLL is bypassed and outputs are driven by input crystal or clock. When LOW outputs are driven by PLL. LVCMOS/LVTTL interface levels. See Table 3D.
2	nOE_REF	Input	Pulldown	Output enable signal for REF_OUT output. When LOW, outputs are enabled. LVCMOS/LVTTL interface levels. See Table 3C.
3	nOEB	Input	Pulldown	Output enable signal for Bank B. When LOW, QB output is enabled. When HIGH, selects high impedance mode. LVCMOS/LVTTL interface levels.See Table 3B.
4	DIV2_QB	Input	Pullup	Select signal for the output divider for Bank B. LVCMOS/LVTTL clock output. See Table 3F.
5, 32	V_{DDA}	Power		Analog supply pins.
6	CLK	Input	Pulldown	Non-inverting differential clock input.
7	nCLK	Input	Pullup	Inverting differential clock input.
8	V_{DDO_REF}	Power		Output power supply pin for LVPECL reference outputs.
9, 10	REF_OUT, nREF_OUT	Output		25MHz differential reference output pair. LVPECL interface levels.
11	CLK_SEL	Input	Pullup	Input select signal. When HIGH, selects CLK, nCLK inputs. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.See Table 3E.
12 13	XTAL_IN XTAL_OUT	Input		Crystal oscillator interface XTAL_IN is the input, XTAL_OUT is the output.
14	V_{DD_OSC}	Power		Core supply pin for crystal oscillator.
15	V_{DDO_QB}	Power		Output power supply pin for Bank B LVCMOS output.
16	QB	Output		Single-ended output. LVCMOS/LVTTL interface levels.
17	V_{DDO_QA3}	Power		Output power supply pin for QA3 LVCMOS output.
18	QA3	Output		Single-ended output. LVCMOS/LVTTL interface levels.
19, 25	GND	Power		Power supply ground.
20, 21	nQA2, QA2	Output		100MHz differential output pair. HCSL interface levels.
22, 29	V_{DDO}	Power		Output power supply pins for Bank A HCSL outputs.
23, 24	nQA1, QA1	Output		100MHz differential output pair. HCSL interface levels.
26, 27	nQA0, QA0	Output		100MHz differential output pair. HCSL interface levels.
28	IREF			0.7V current reference resistor output. An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QAx, nQAx clock outputs.
30	nOEA	Input	Pulldown	Output Enable signal for Bank A. When LOW enables output. When HIGH selects high impedance mode. LVCMOS/LVTTL interface levels.See Table 3A.
31	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance		CLK, nCLK		2		pF
			Control Pins		4		pF
R_{PULLUP}	Input Pullup Resistors				100		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistors				100		kΩ
C_{PD}	Power Dissipation Capacitance (per output)		V_{DD}, V_{DD_OSC}, V_{DDO}, V_{DDO_REF}, V_{DDO_QA3}, V_{DDO_QB} = 3.6V		5		pF
R_{OUT}	Output Impedance	QA3, QB	V_{DDO_QA3}, V_{DDO_QB} = 3.6V		25		Ω

Function Tables

Table 3A. nOEA Function Table

Input	Outputs
nOEA	**QA**
0 (default)	Active
1	High-Impedance

Table 3B. nOEB Function Table

Input	Outputs
nOEB	**QB**
0 (default)	Active
1	High-Impedance

Table 3C. nOE_REF Function Table

Input	Outputs
nOE_REF	**REF_OUT**
0 (default)	Active
1	High-Impedance

Table 3D. PLL_BYPASS Function Table

Input	Outputs
PLL_BYPASS	**QA, QB**
0 (default)	PLL
1	Bypass PLL

Table 3E. CLK_SEL Function Table

Input	
CLK_SEL	**Selected Input**
0	XTAL
1 (default)	CLK, nCLK

Table 3F. DIV2_QB Function Table

Input	
DIV2_QB	**Output Frequency**
0	100MHz
1 (default)	50MHz

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	3.63V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O (LVCMOS, HCSL) Outputs, I_O (LVPECL) Continuos Current Surge Current	-0.5V to V_{DDO} + 0.5V 50mA 100mA
Package Thermal Impedance, θ_{JA}	37.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DD\_OSC}$ = 3.0V to 3.6V, $V_{DDO} = V_{DDO\_QA3} = V_{DDO\_QB} = V_{DDO\_REF}$ = 2.7V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}, V_{DD_OSC}	Core Supply Voltage		3.0	3.3	3.6	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.32	3.3	V_{DD}	V
V_{DDO}, V_{DDOx}	Output Supply Voltage		2.7	3.3	3.6	V
I_{EE}	Power Supply Current				170	mA
I_{DDA}	Analog Supply Current	Included in I_{EE}			32	mA

V_{DDOx} denotes V_{DDO_REF}, V_{DDO_QA3} and V_{DDO_QB}.

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.0V to 3.6V, $V_{DDO\_QA3} = V_{DDO\_QB}$ = 2.7V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, DIV2_QB	$V_{DD} = V_{IN}$ = 3.6V			5	µA
		nOEA, nOEB, nOE_REF, PLL_BYPASS	$V_{DD} = V_{IN}$ = 3.6V			150	µA
I_{IL}	Input Low Current	CLK_SEL, DIV2_QB	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
		nOEA, nOEB, nOE_REF, PLL_BYPASS	V_{DD} = 3.6V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.0V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.6V			150	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.6V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.6V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVPECL DC Characteristics, V_{DDO_REF} = 2.7V to 3.6V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{DDO_REF} – 1.4		V_{DDO_REF} – 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO_REF} – 2.0		V_{DDO_REF} – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Output termination with 50Ω to V_{DDO_REF} – 2V.

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6A. LVCMOS AC Characteristics, V_{DD} = 3.0V to 3.6V, V_{DDO_QA3} = V_{DDO_QB} = 2.7V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QB	PLL mode		50		MHz
		QA3	PLL mode		100		MHz
			PLL Bypass	20			MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1		100MHz, Integration Range: 12kHz – 20MHz			0.34	ps
t_R / t_F	Output Rise/Fall Time			200		600	ps
odc	Output Duty Cycle			47		53	%
V_{OH}	Output High Voltage; NOTE 2	QA3, QB		2.2			V
V_{OL}	Output Low Voltage; NOTE 2	QA3, QB	$f \leq$ 100MHz			0.9	V

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
Using a 25MHz, 12pF quartz crystal.
NOTE 1: Refer to the Phase Noise plot.
NOTE 2: Outputs are terminated with 50Ω to V_{DDO_X}/2. See Parameter Measurement Information, *Output Load Test Circuit diagram.*

Table 6B. LVPECL AC Characteristics, V_{DD} = 3.0V to 3.6V, V_{DDO_REF} = 2.7V to 3.6V, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	REF_OUT, nREF_OUT			25		MHz
t_R / t_F	Output Rise/Fall Time	REF_OUT, nREF_OUT	20% to 80%	100		600	ps
odc	Output Duty Cycle	REF_OUT, nREF_OUT		49		51	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Table 6C. HCSL AC Characteristics, V_{DD} = 3.0V to 3.6V, V_{DDO} = 2.7V to 3.6V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	PLL		100		MHz
		PLL Bypass	20			MHz
f_{REF}	Reference Frequency			25		MHz
tsk(b)	Bank Skew; NOTE 1, 10				50	ps
*t*jit(Ø)	Phase Jitter, RMS (Random); NOTE 11	100MHz, Integration Range: 12kHz – 20MHz			0.36	ps
$t_{REFCLK\_HF\_RMS}$	Phase Jitter RMS; NOTE 2	100MHz, 25MHz crystal input High Band: 1.5MHz - Nyquist (clock frequency/2)		0.600		ps
$t_{REFCLK\_LF\_RMS}$	Phase Jitter RMS; NOTE 2	100MHz, 25MHz crystal input Low Band: 10kHz - 1.5MHz		0.023		ps
*t*jit(cc)	Cycle-to-Cycle Jitter	PLL Mode			30	ps
t_L	PLL Lock Time				10	ms
V_{RB}	Ring-back Voltage Margin; NOTE 4, 9		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed; NOTE 4, 9		500			ps
V_{HIGH}	Voltage High		520		920	mV
V_{LOW}	Voltage Low		-150		150	mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 3, 6, 7		160		460	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 3, 6, 8				140	mV
	Rising Edge Rate; NOTE 4, 5		0.6		4.0	V/ns
	Falling Edge Rate; NOTE 4, 5		0.6		4.0	V/ns
PSNR	Power Supply Noise Reduction			-45		dB
odc	Output Duty Cycle; NOTE 4		49		51	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Defined as skew within a bank of outputs at the same voltage and with equal load conditions.

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band). See IDT Application Note *PCI Express Reference Clock Requirements* and also the PCI Express Application section of this datasheet which show each individual transfer function and the overall composite transfer function.

NOTE 3: Measurement taken from single ended waveform.

NOTE 4: Measurement taken from differential waveform.

NOTE 5: Measured from -150mV to +150mV on the differential waveform (derived from Q minus nQ). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

NOTE 6: Measured at the crosspoint where the instantaneous voltage value of the rising edge of Q equals the falling edge of nQ.

NOTE 7: Refers to the total variation from the lowest crosspoint to the highest, regardless of which edge is crossing. Refers to all crosspoints for this measurement.

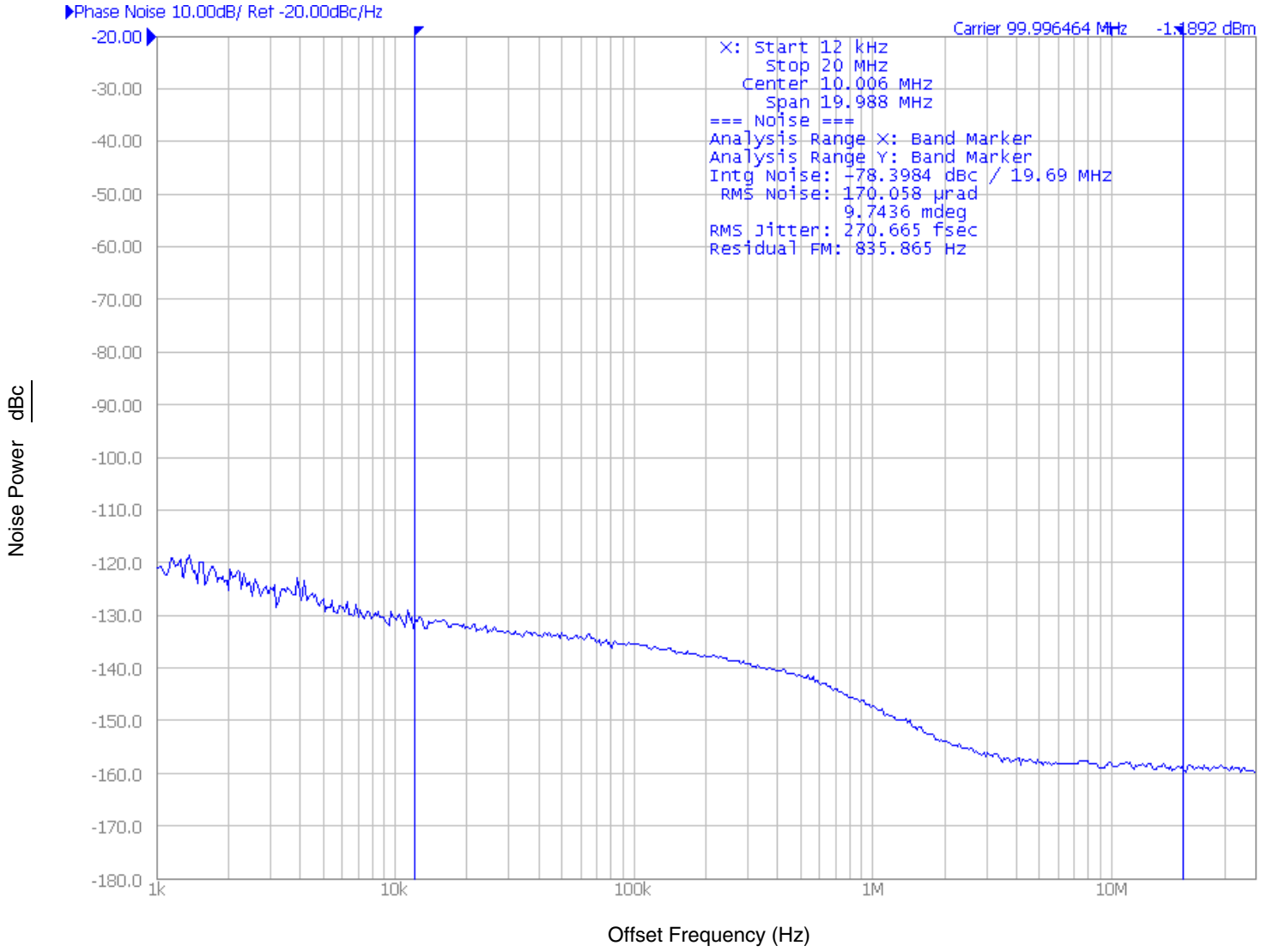
NOTE 8: Defined as the total variation of all crossing voltages of rising Q and falling nQ, This is the maximum allowed variance in V_{CROSS} for any particular system.

NOTE 9: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV differential range.

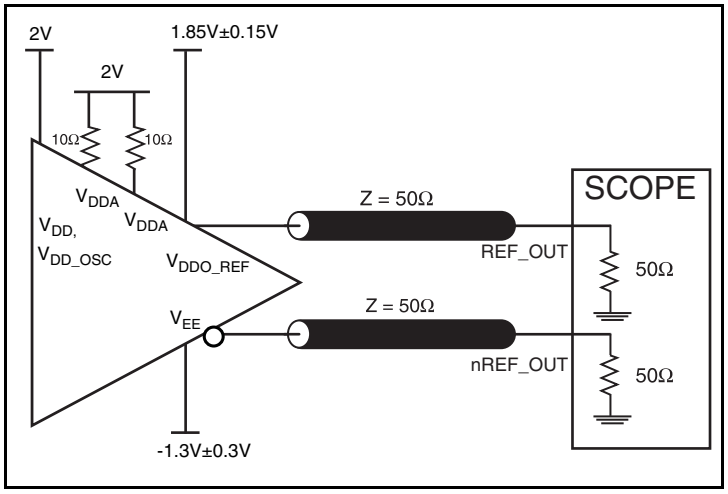
NOTE 10: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 11: See Phase Noise Plot.

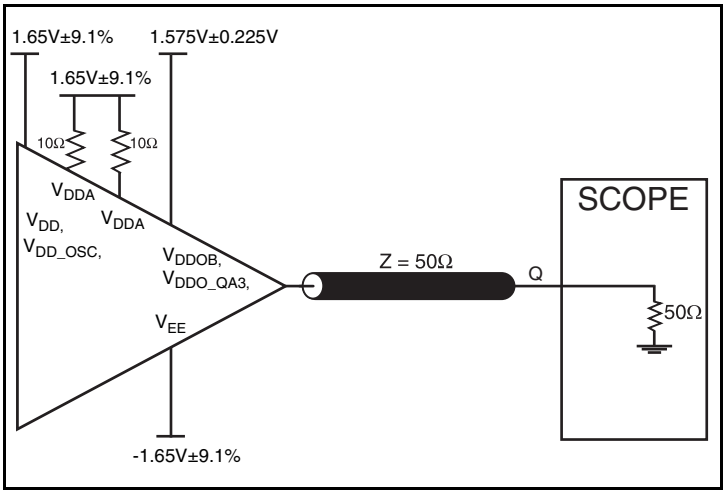
Typical Phase Noise at 100MHz (3.3V)



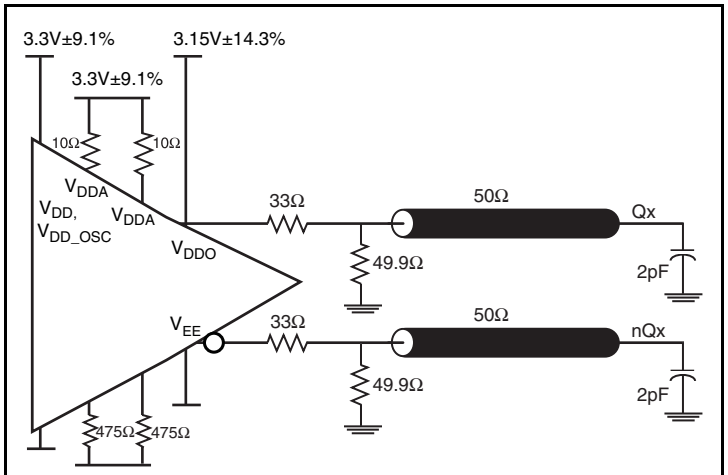
Parameter Measurement Information



3.3V LVPECL Output Load Test Circuit

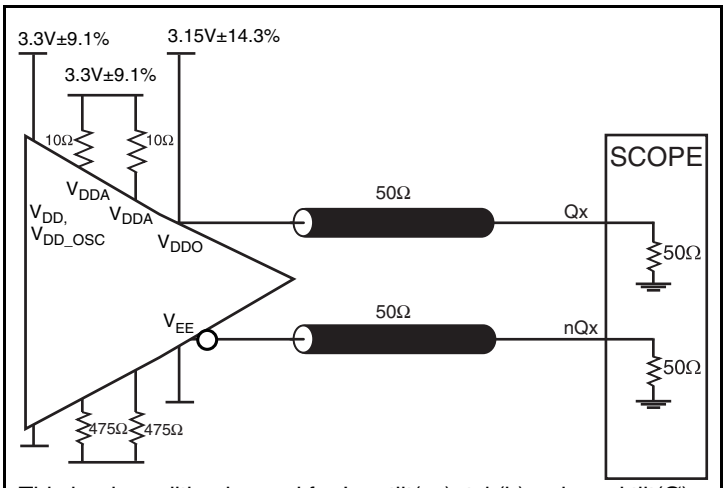


3.3V LVCMOS Output Load Test Circuit



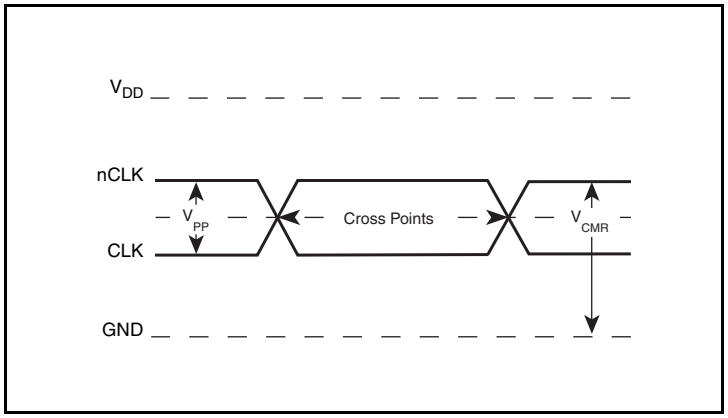
This load condition is used for V_{HIGH}, V_{LOW}, V_{RB}, t_{STABLE} and V_{CROSS}, ΔV_{CROSS} measurements.

3.3V HCSL Output Load Test Circuit

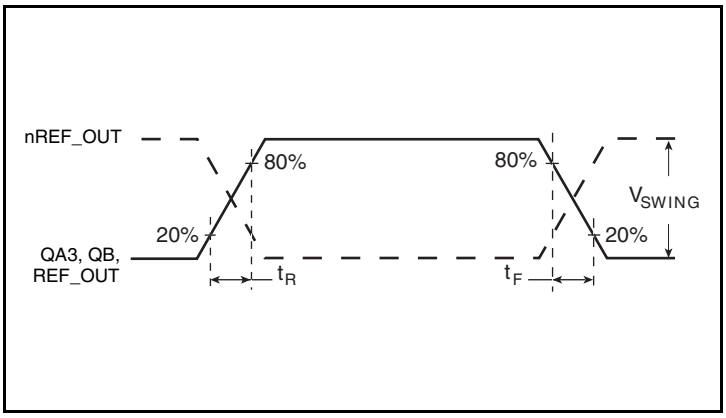


This load condition is used for I_{DD}, tjit(cc), tsk(b), odc and tjit(Ø) measurements.

3.3V HCSL Output Load Test Circuit

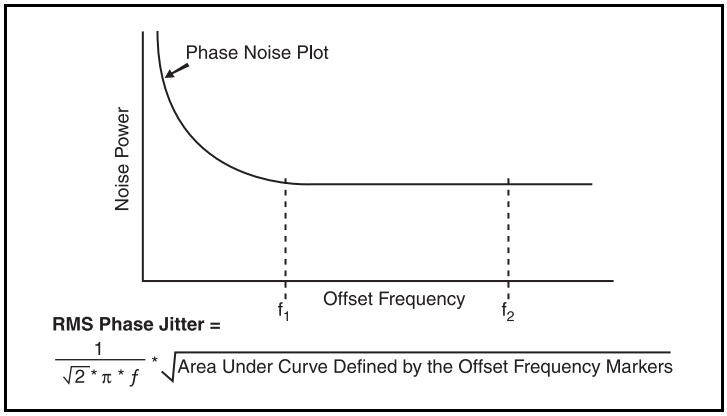


Differential Input Level

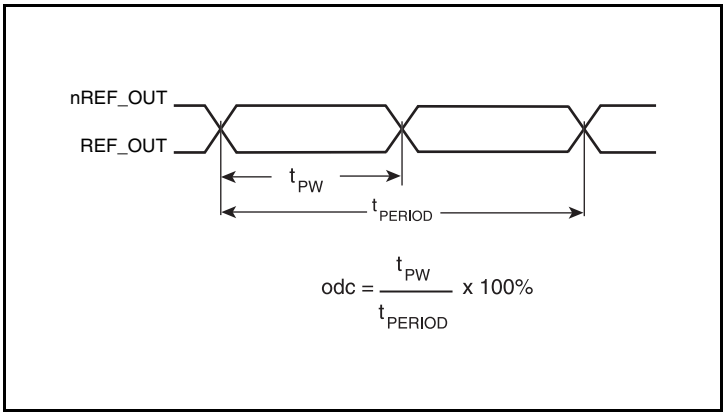


Output Rise/Fall Time (LVPECL, LVCMOS)

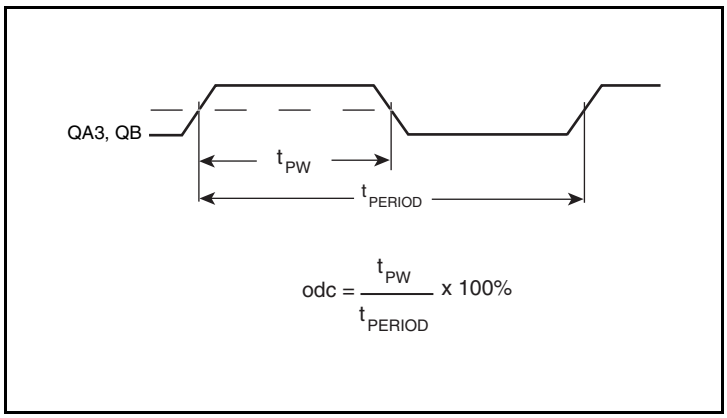
Parameter Measurement Information, continued



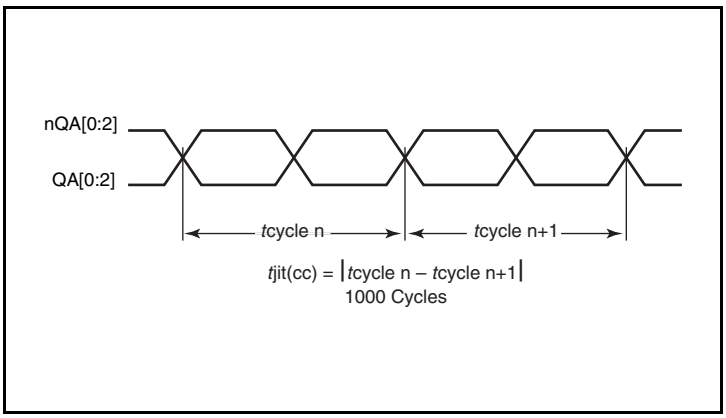
RMS Phase Jitter



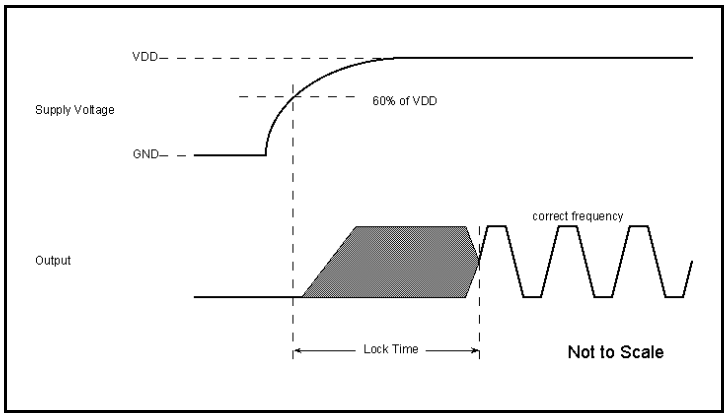
LVPECL Output Duty Cycle/Pulse Width/Period



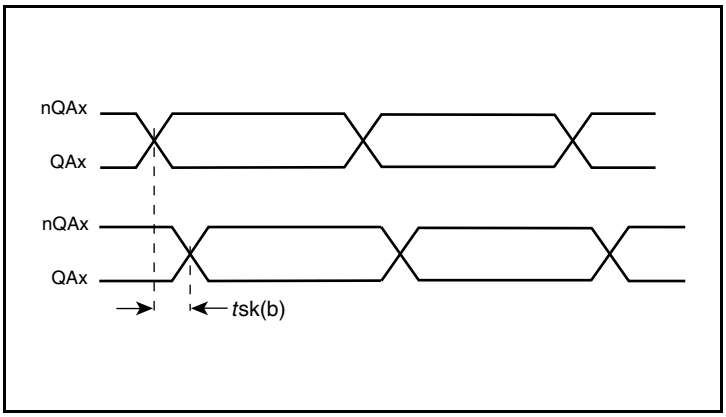
LVCMOS Output Duty Cycle/Pulse Width/Period



Cycle-to-Cycle Jitter

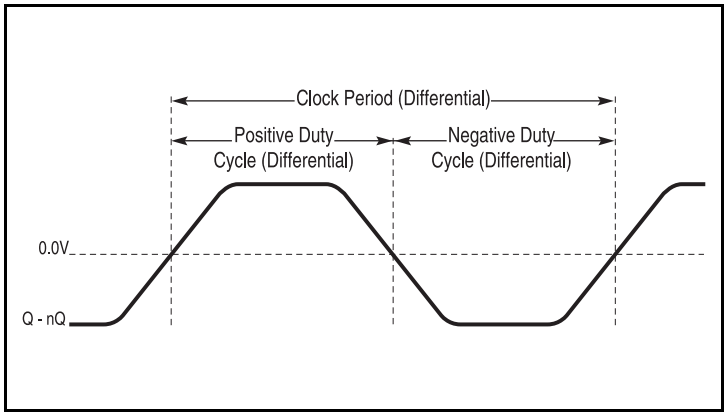


PLL Lock Time

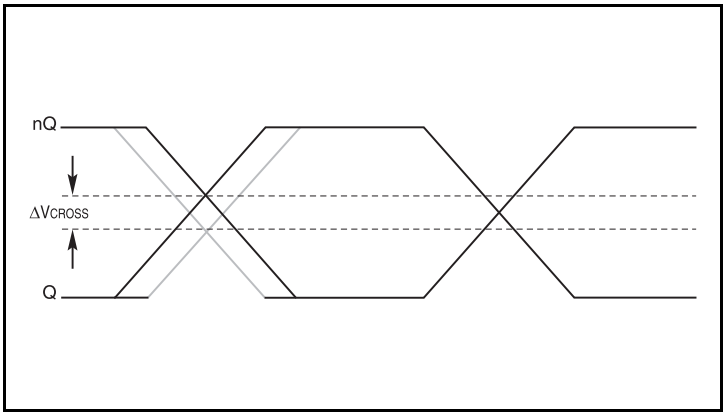


Bank Skew

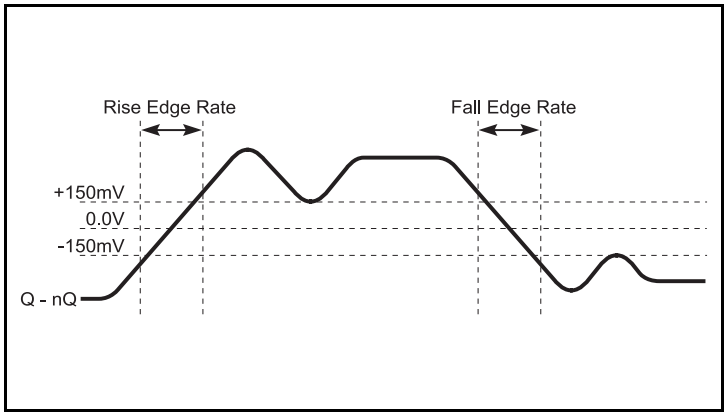
Parameter Measurement Information, continued



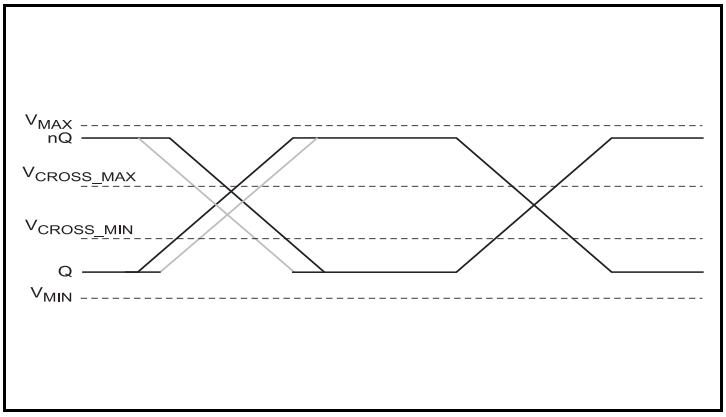
Differential Measurement Points for Duty Cycle/Period



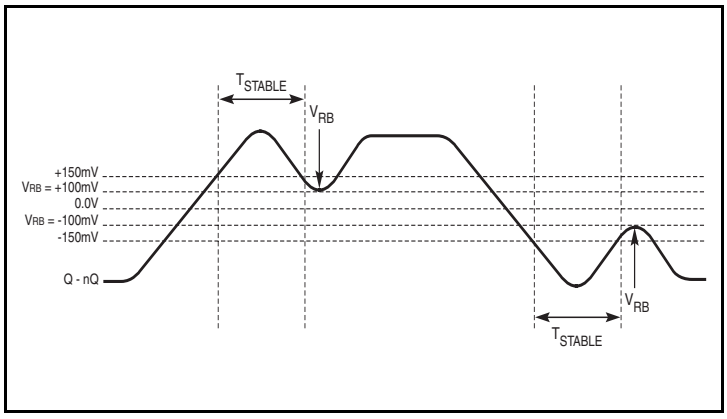
Single-ended Measurement Points for Delta Cross Point



Differential Measurement Points for Rise/Fall Edge Rate



Single-ended Measurement Points for Absolute Cross Point/Swing



Differential Measurement Points for Ringback

Applications Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 841N4830 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DD_OSC}, V_{DDA}, V_{DDO}, and V_{DDOx} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

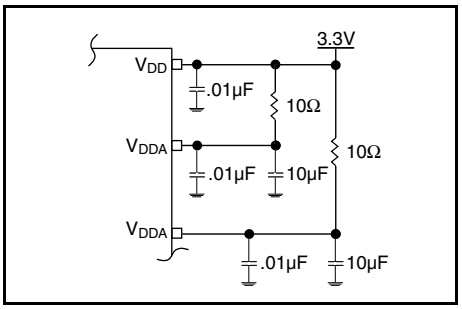


Figure 1. Power Supply Filtering

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

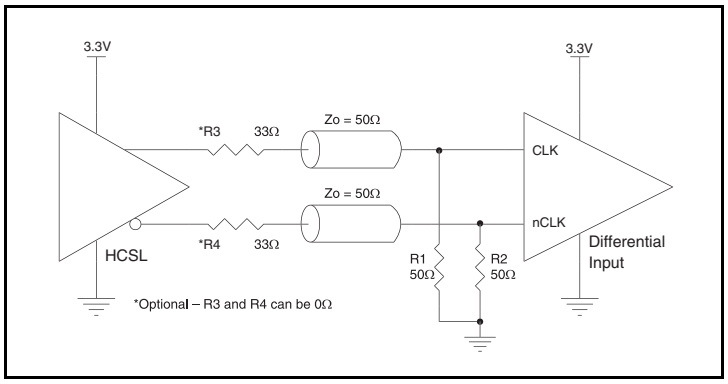


Figure 2A. CLK/nCLK Input Driven by a 3.3V HCSL Driver

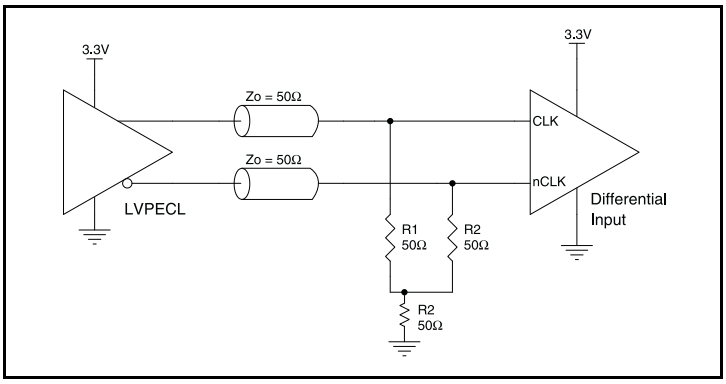


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

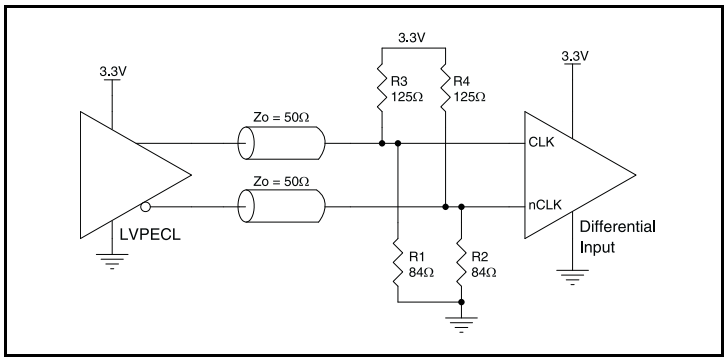


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

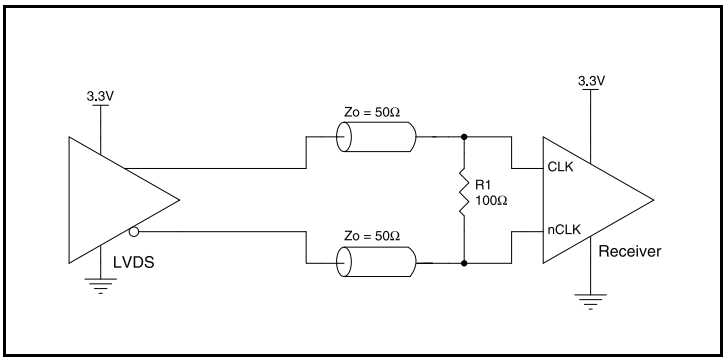


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

Crystal Input Interface

The 841N4830 has been characterized with 12pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 3* below were determined using a 25MHz, 12pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

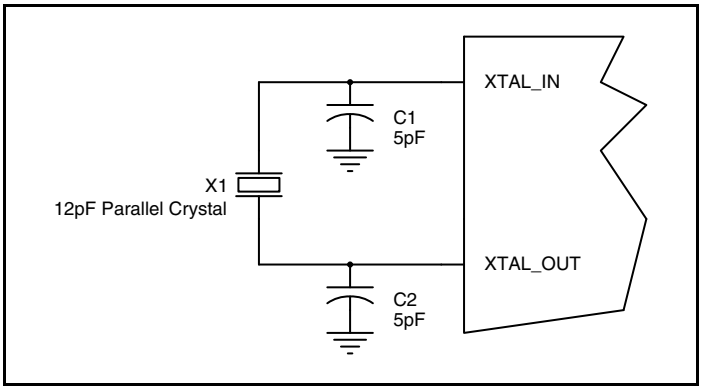


Figure 3. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 4A.* The XTAL_OUT pin can be left floating. The maximum amplitude of the input signal should not exceed 2V and the input edge rate can be as slow as 10ns. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

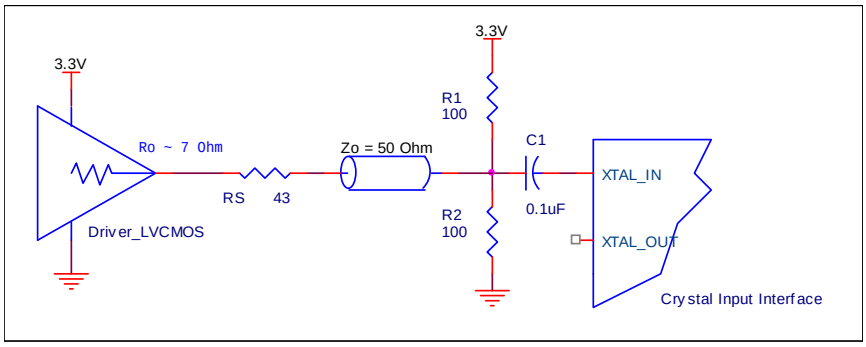


Figure 4A. General Diagram for LVCMOS Driver to XTAL Input Interface

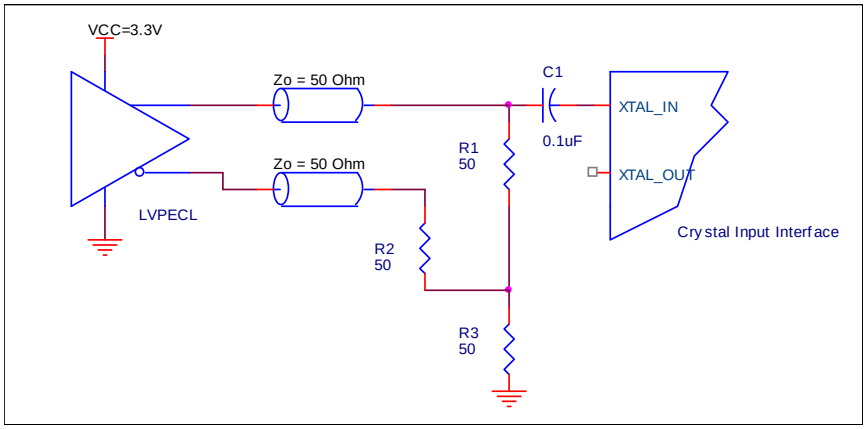


Figure 4B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommended Termination

Figure 5A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

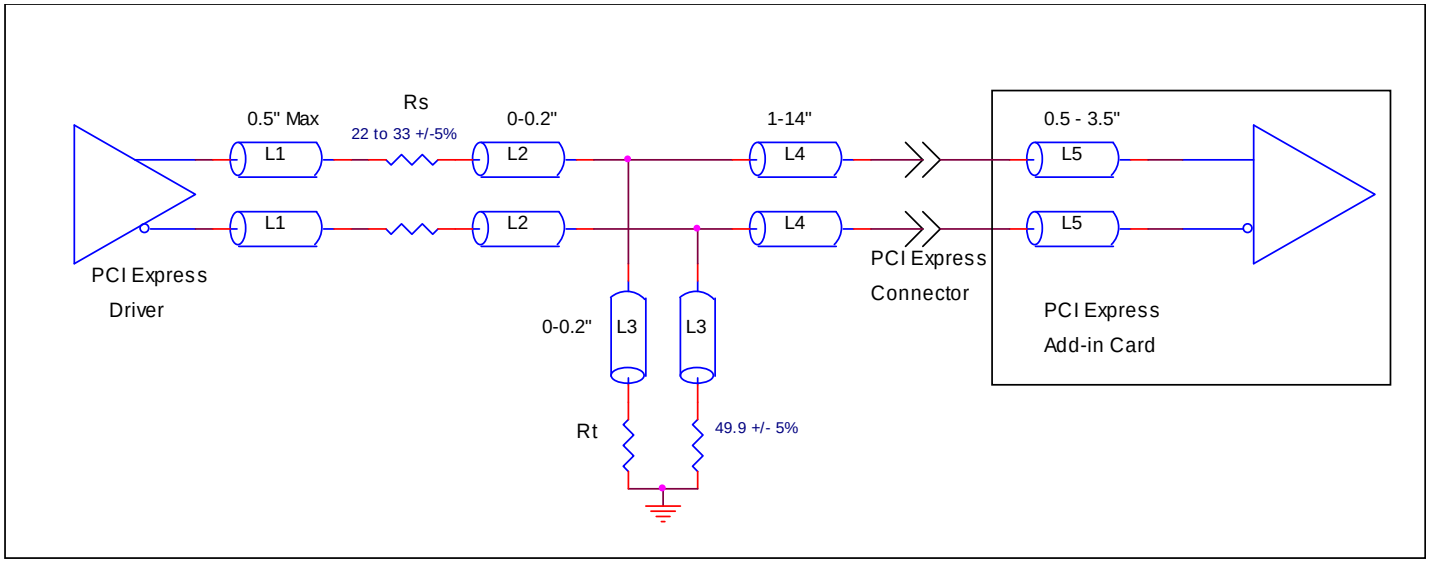


Figure 5A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 5B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

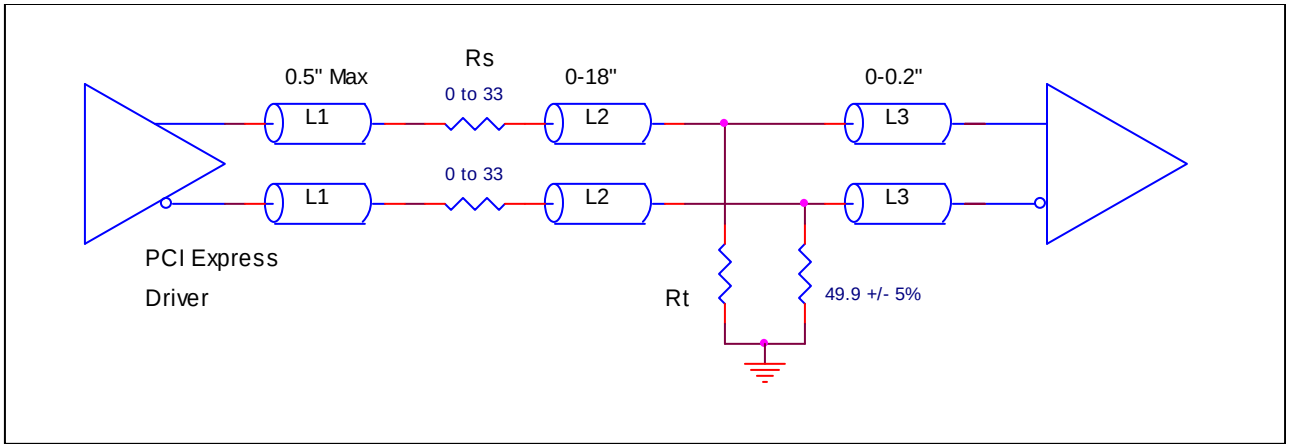


Figure 5B. Recommended Termination (where a point-to-point connection can be used)

Recommendations for Unused Input Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Output

The unused LVPECL output pair can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

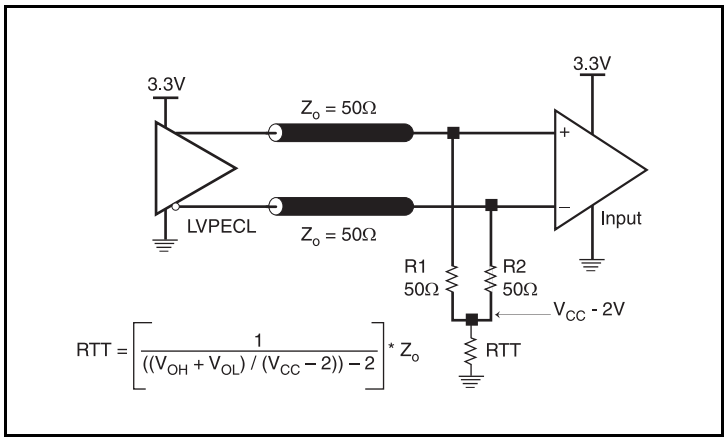


Figure 6A. 3.3V LVPECL Output Termination

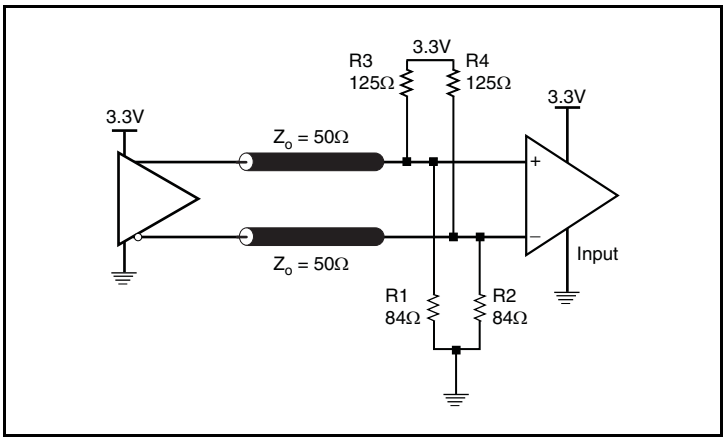


Figure 6B. 3.3V LVPECL Output Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 7.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

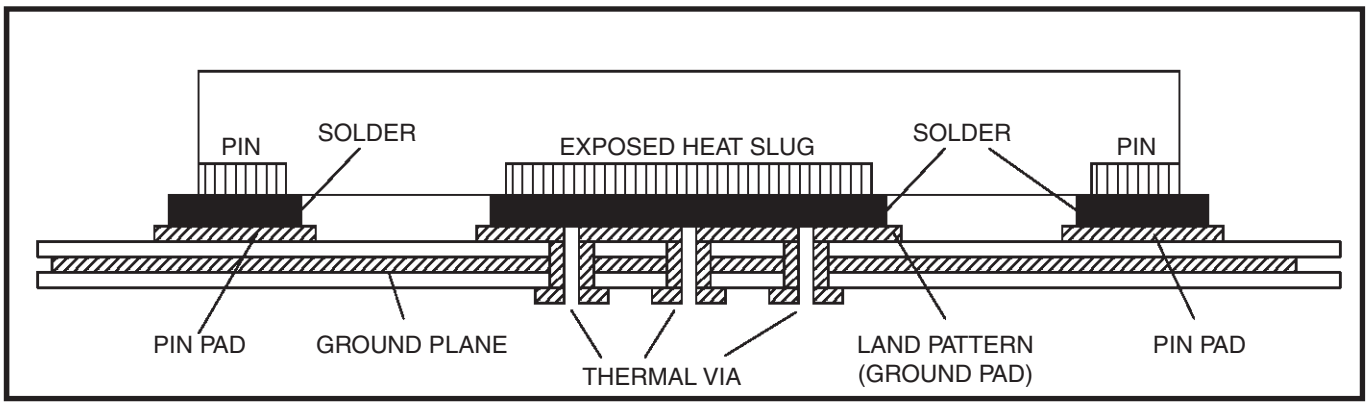


Figure 7. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 8 shows an example of 841N4830 application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

In this example, the device is operated at V_{DD} = V_{DDO_REF} = V_{DD_OSC} = V_{DDO} = 3.3V. The 12pF parallel resonant 25MHz crystal is used. The C1 = 5pF and C2 = 5pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. When designing the circuit board, return the capacitors to ground though a single point contact close to the package.

Two examples of HCSL terminations are shown in this schematic. The decoupling capacitors should be located as close as possible to the power pin.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 841N4830 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

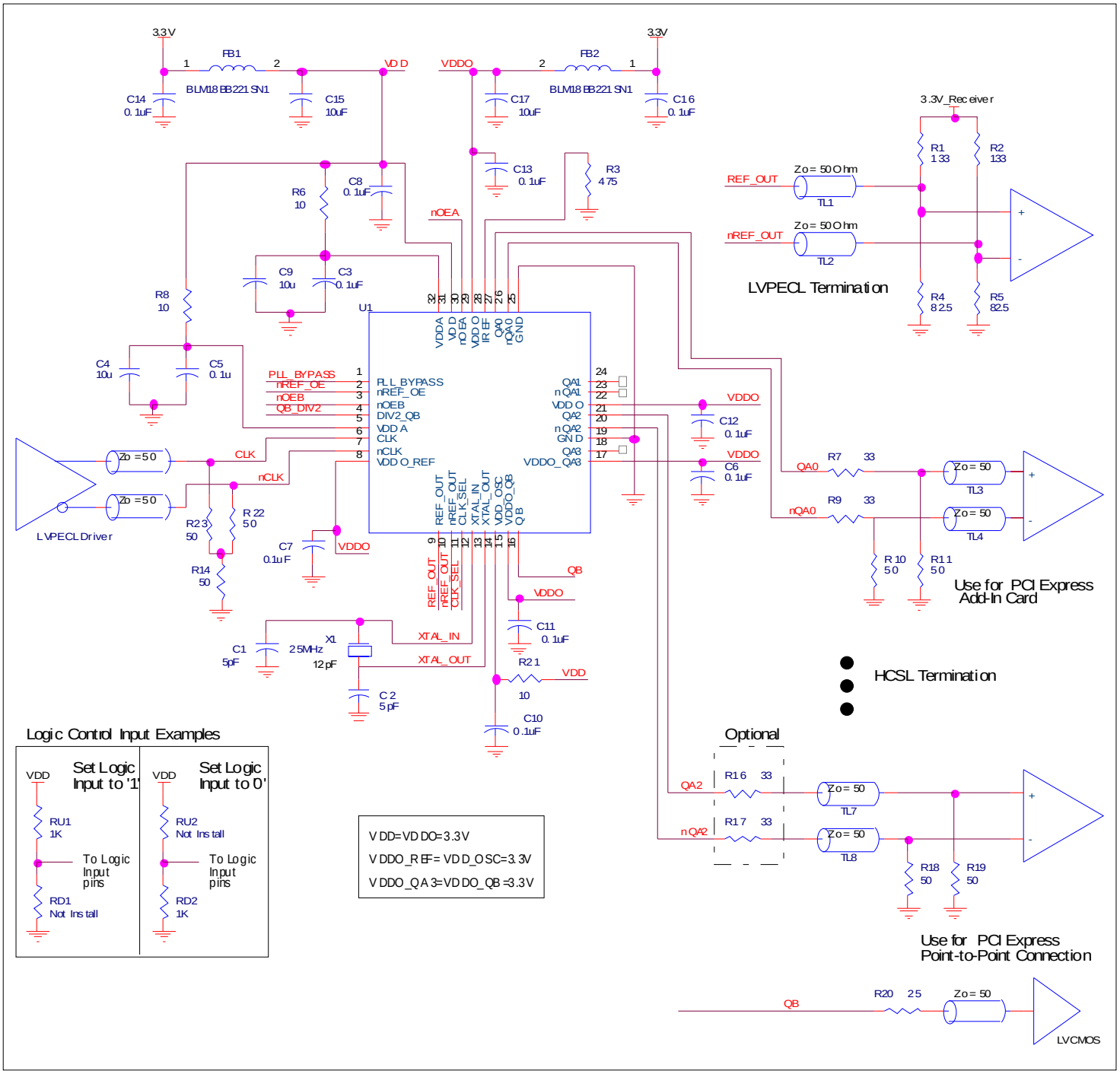


Figure 8. 841N4830 Application Schematic

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

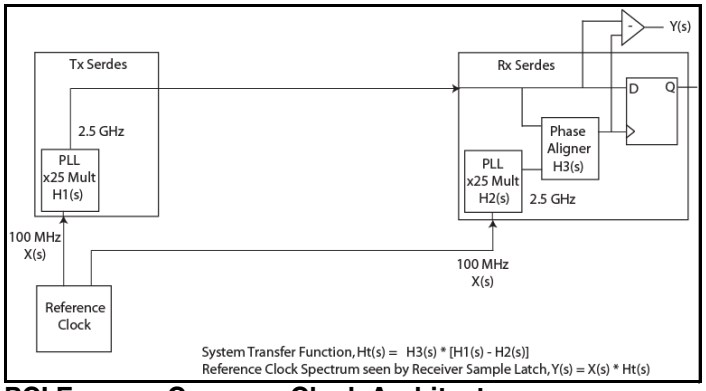
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

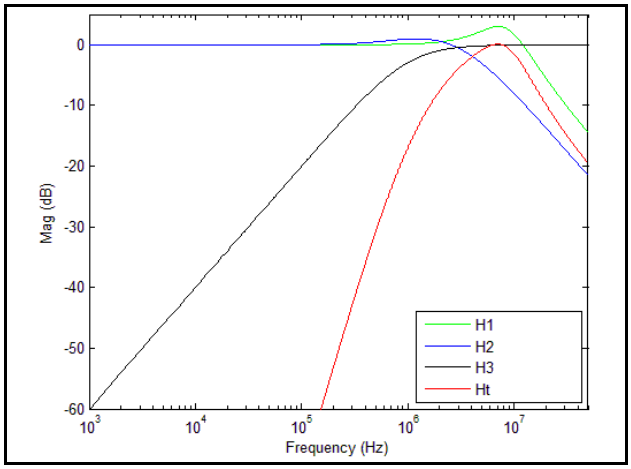
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].

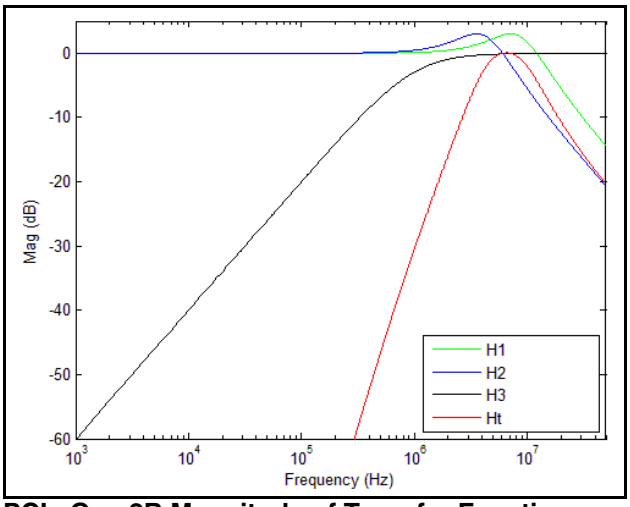


PCI Express Common Clock Architecture

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.



PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Power Considerations

This section provides information on power dissipation and junction temperature for the 841N4830.
Equations and example calculations are also provided.

1. Power Dissipation

The total power dissipation for the 841N4830 is the sum of the core power plus the power dissipated due to loading. The following is the power dissipation for V_{DD} = 3.3V + 0.3V = 3.6V, which gives worst case results.

NOTE: Please refer to Section 3A and 3B for details on calculating power dissipation due to loading.

Core

- Power(core) = V_{DD_MAX} * I_{EE} = 3.6V * 170mA = **612mW**

LVPECL Output
LVPECL driver power dissipation is 30mW/Loaded output pair, total LVPECL output dissipation:

- Power(LVPECL) = 30mW

HSCL Output
HSCL driver power dissipation is 46.8mW/Loaded output pair, total HSCL output dissipation:

- Power(HSCL) = 46.75mW * 3 = 140.25mW

LVCMOS Output

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50Ω + R_{OUT})] = 3.6V / [2 * (50Ω + 25Ω)]$ = **24mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = $R_{OUT} * (I_{OUT})^2 = 25Ω * (24mA)^2$ = **14.4mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 14.4mW * 2 = **28.8mW**

Dynamic Power Dissipation at 100MHz

Power (100MHz) = C_{PD} * Frequency * $(V_{DD})^2$ = 5pF * 100MHz * $(3.6V)^2$ = **6.48mW per output**
Total Power (100MHz) = 6.48mW * 2 = **12.96mW**

Total Power Dissipation

- **Total Power**
  = Power (core) + Power(LVPECL) + Power(HCSL) + Total Power (R_{OUT}) + Total Power (100MHz)
  = 612mW + 30mW + 140.25mW + 28.8mW +12.96mW
  = 824mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature for devices is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37.7°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.824W *37.7°C/W = 116°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.7°C/W	32.9°C/W	29.5°C/W

3A. Calculations and Equations for LVPECL.

The purpose of this section is to calculate power dissipation on the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 9.*

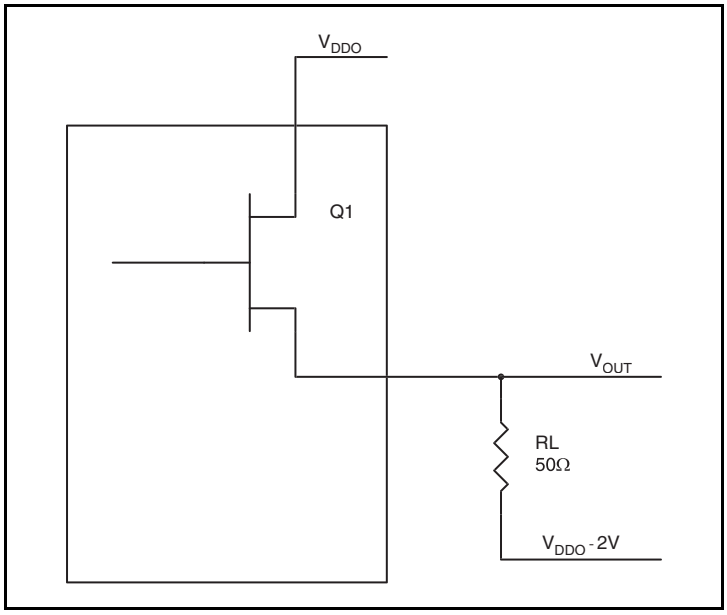


Figure 9. LVPECL Driver Circuit and Termination

To calculate power dissipation per output due to loading, use the following equations which assume a 50Ω load, and a termination voltage of V_{DDO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{DDO\_MAX} - 0.9V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{DDO\_MAX} - 1.7V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{DDO\_MAX} - 2V))/R_L] * (V_{DDO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{DDO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{DDO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{DDO\_MAX} - 2V))/R_L] * (V_{DDO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{DDO\_MAX} - V_{OL\_MAX}))/R_{L]} * (V_{DDO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

3B. Calculations and Equations for HCSL.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pairs.

HCSL output driver circuit and termination are shown in *Figure 10.*

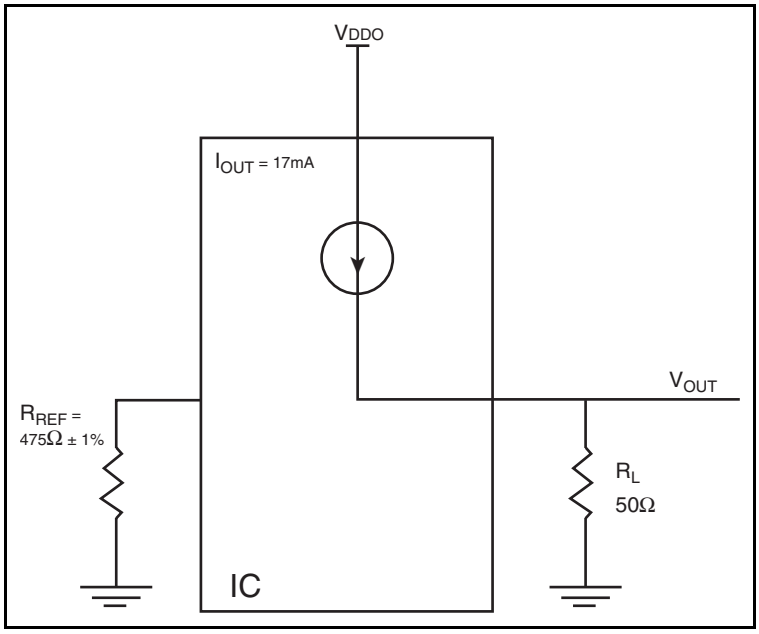


Figure 10. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX}.

Power $= (V_{DD\_MAX} - V_{OUT}) * I_{OUT}$,
since $V_{OUT} - I_{OUT} * R_L$

$= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.6V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **46.75mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

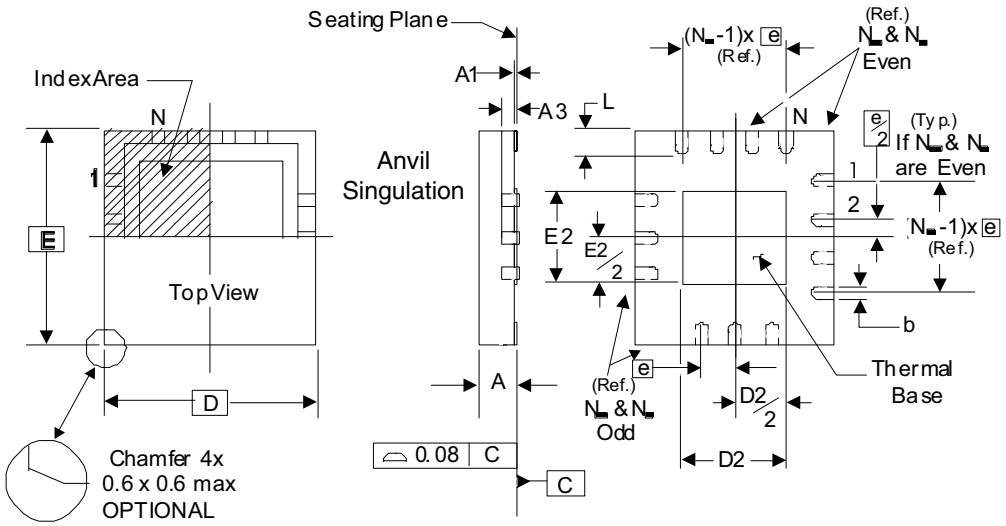
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.7°C/W	32.9°C/W	29.5°C/W

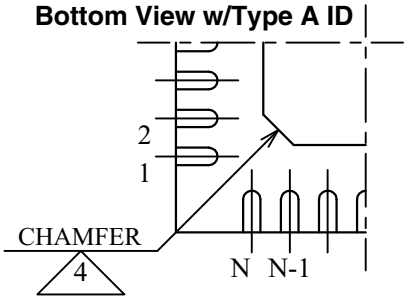
Transistor Count

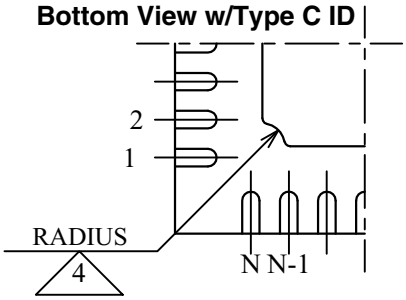
The transistor count for 841N4830 is: 23,123

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

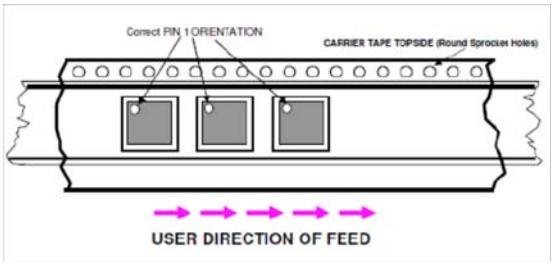
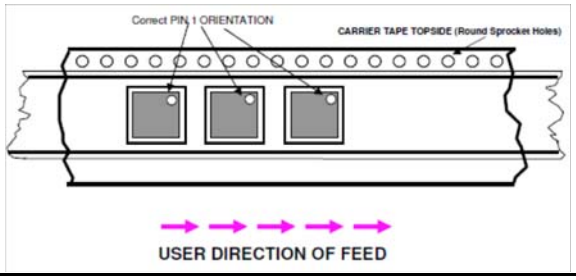
NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin-out are shown on the front page. The package dimensions are in Table 9.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
841N4830BKILF	ICSN4830BIL	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
841N4830BKILFT	ICSN4830BIL	“Lead-Free” 32 Lead VFQFN	Tape & Reel, pin 1 orientation: EIA-481-C	-40°C to 85°C
841N4830BKILF/W	ICSN4830BIL	“Lead-Free” 32 Lead VFQFN	Tape & Reel, pin 1 orientation EIA-481-D	-40°C to 85°C

Table 11. Pin 1 Orientation in Tape and Reel Packaging

Part Number Suffix	Pin 1 Orientation	Illustration
T	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		4	Supply Voltage, $V_{DD.}$ Rating changed from 4.5V min. to 3.63V per Errata NEN-11-03.	5/3/11
B		1	General Description: Maximum rms phase jitter changed to 0.34ps Per PCN: Features: changed to: RMS Phase Jitter @ 100MHz, (12kHz – 20MHz) using a 25MHz crystal: 0.34ps (maximum)	3/5/12
	T6A	6	Added 0.34 Maximum to tjit RMS Phase Jitter.	
	T6C	7	Added 0.34 Maximum to tjit, RMS Phase Jitter., Added 0.582 Typical to $t_{REFCLK\_HF\_RMS}$ RMS Phase Jitter. Added 0.023 Typical to $t_{REFCLK\_LF\_RMS}$ RMS Phase Jitter.	
		8	Added updated Phase Noise Plot.	
		18	Added updated PCI Express Application Note	
		23	Changed Package Drawing	
		24	Changed Marking to ICSN4830BIL.	
C	T4A	4	Per PCN #N1206-01, changed I_{EE} to 170mA Max. Changed device reference to ICS841N4830BKI throughout the datasheet.	8/29/12
D			Per PCN #N1206-01 Updated V_{DD} min/max voltage from 3.135V min/3.465V max to 3.0V min / 3.6V max. Updated V_{DDO} min/max voltage from 3.135V min/3.465V max to 2.7V min / 3.6V max.	1/22/2013
		1	General Description and Features, updated RMS Phase Jitter spec to 0.36ps.	
		4 - 7	DC / AC Characteristic Tables - changed voltage supply table descriptions.	
	T4A	4	Power Supply DC Characteristics Table - changed Core supply voltage min / max specs; changed V_{DDO} supply voltage min / max specs; corrected V_{DDA} min spec from V_{DD} - 0.16V to V_{DD} - 0.32V.	
	T6A	6	LVCMOS AC Characteristic Table - changed odc min / max spec.	
	T6C	7	HCSL AC Characteristic Table - changed Phase Jitter, RMS (Random) max spec.; changed Phase Jitter (HF_RMS) typical spec.; changed Cycle-to-Cycle max spec.	
		9	Parameter Measurement Information - updated Test Circuit diagrams.	
		18	PCI Express Application Note - deleted Gen 1 information.	
		19 - 20, 22	Power Considerations - changed V_{DD} = 3.465V to V_{DD} = 3.6V, updated equations.	
D		17, 18	Updated schematic	8/5/2013
E	T11	26	Added P1 Orientation in Tape and Reel Table.	7/1/15
	T10	26	Ordering Information - Added W part number.	
F			Updated datasheet header/footer.	5/23/16

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