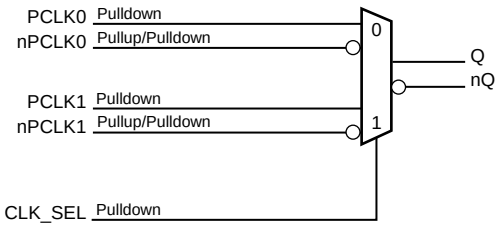
General Description

The 854S01I is a high performance 2:1 Differential-to-LVDS Multiplexer. The 854S01I can also perform differential translation because the differential inputs accept LVPECL, LVDS or CML levels. The 854S01I is packaged in a small 3mm x 3mm 16 VFQFPN package, making it ideal for use on space constrained boards.

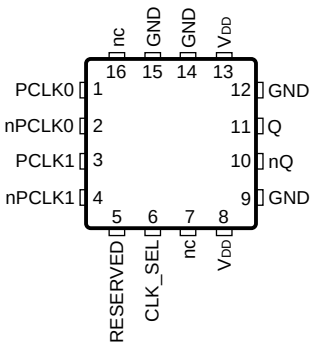
Features

- 2:1 LVDS MUX
- One LVDS output pair
- Two differential clock inputs can accept: LVPECL, LVDS, CML
- Maximum input/output frequency: 2.5GHz
- Translates LVCMOS/LVTTL input signals to LVDS levels by using a resistor bias network on nPCLK0, nPCLK1
- RMS additive phase jitter: 0.06ps (typical)
- Propagation delay: 600ps (maximum)
- Part-to-part skew: 350ps (maximum)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Supports case temperature up to +105°C
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



854S01I

16-Lead VFQFPN
3mm x 3mm x 0.925mm package body
K Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	PCLK0	Input	Pulldown	Non-inverting differential clock input.
2	nPCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
3	PCLK1	Input	Pulldown	Non-inverting differential clock input.
4	nPCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. $V_{DD}/2$ default when left floating.
5	RESERVED	Reserve		Reserve pin.
6	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects PCLK1, nPCLK1 inputs. When LOW, selects PCLK0, nPCLK0 inputs. LVCMOS / LVTTL interface levels.
7, 16	nc	Unused		No connects.
8, 13	V_{DD}	Power		Power supply pins.
9, 12, 14, 15	GND	Power		Power supply ground.
10, 11	nQ, Q	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			2		pF
R_{PULLUP}	Input Pullup Resistor			37		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			37		kΩ

Function Tables

Table 3. Control Input Function Table

CLK_SEL	PCLK Selected
0	PCLK0, nPCLK0
1	PCLK1, nPCLK1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	74.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				40	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA

Table 4C. LVPECL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	PCLK0, nPCLK0, PCLK1, nPCLK1	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		nPCLK0, nPCLK1	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.2	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			1.2		V_{DD}	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		247		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.125		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

AC Electrical Characteristics

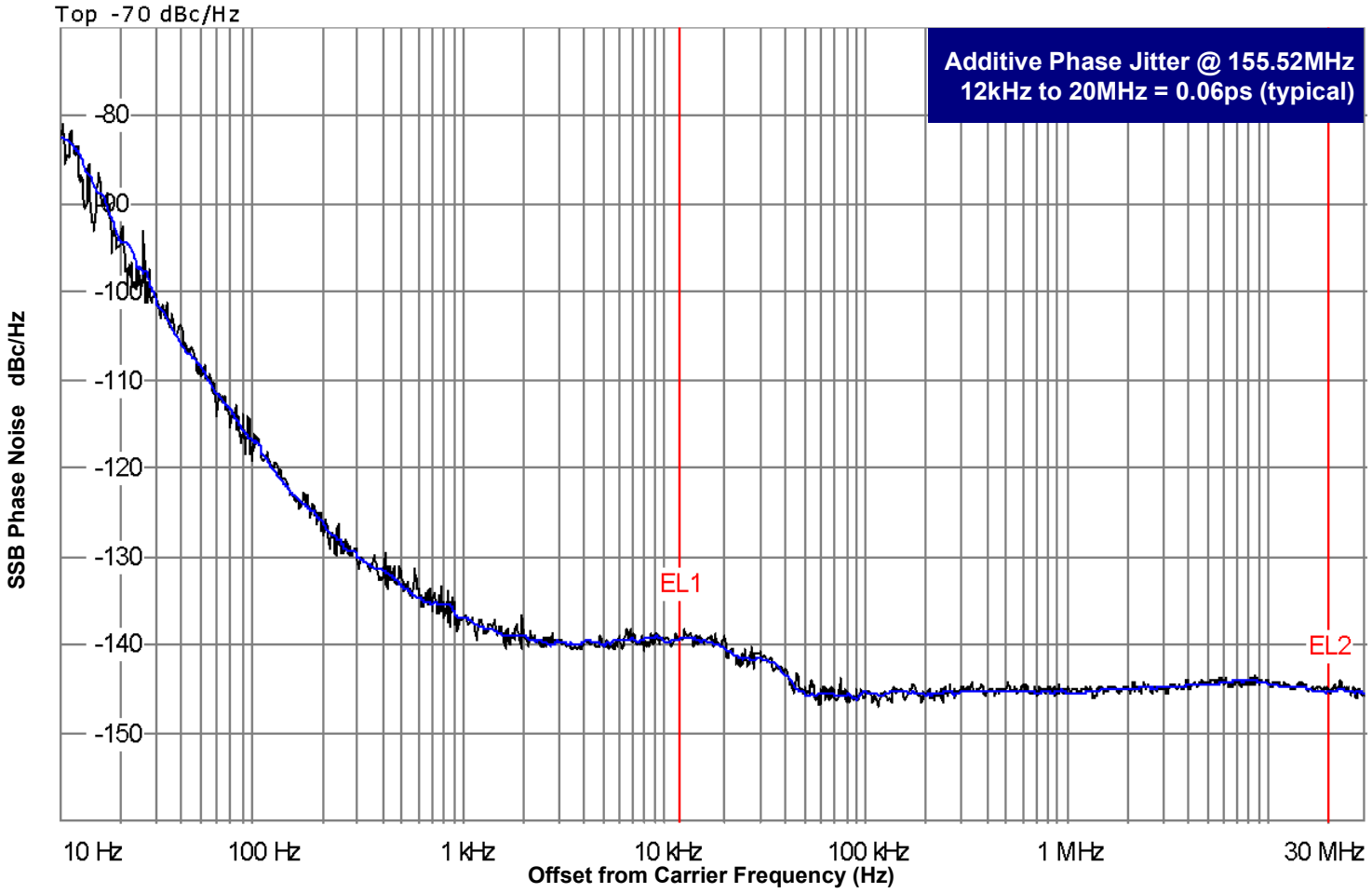
Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		250	400	600	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.52MHz, Integration Range: 12kHz – 20MHz)		0.06		ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3				350	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		275	ps
odc	Output Duty Cycle		49		51	%
$MUX_{\_ISOLATION}$	MUX Isolation; NOTE 4	f_{OUT} = 155.52MHz, V_{PP} = 400mV		86		dB

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at ≤ 1.0GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage, same temperature, same frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Q, nQ outputs measured differentially. See Parameter Measurement Information to MUX Isolation diagram.

Additive Phase Jitter

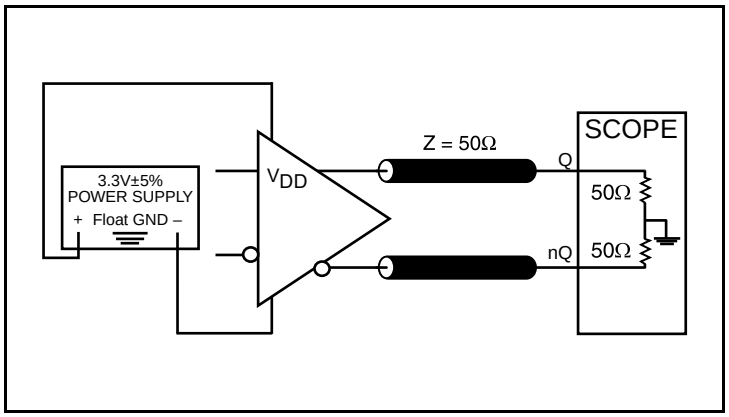
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



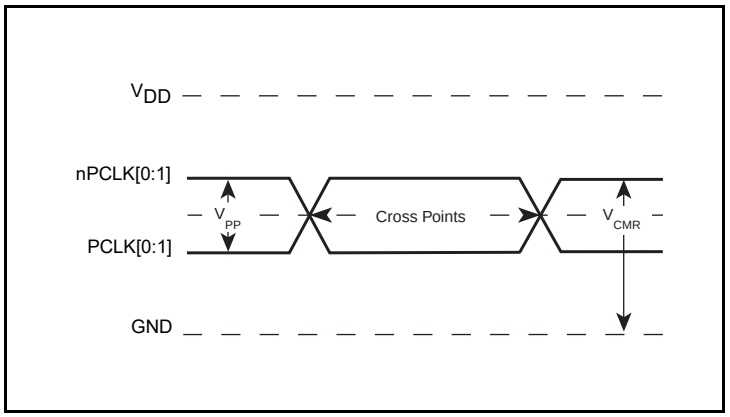
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator “IFR2042 10kHz – 56.4GHz Low Noise Signal Generator as external input to an Agilent 8133A 3GHz Pulse Generator”

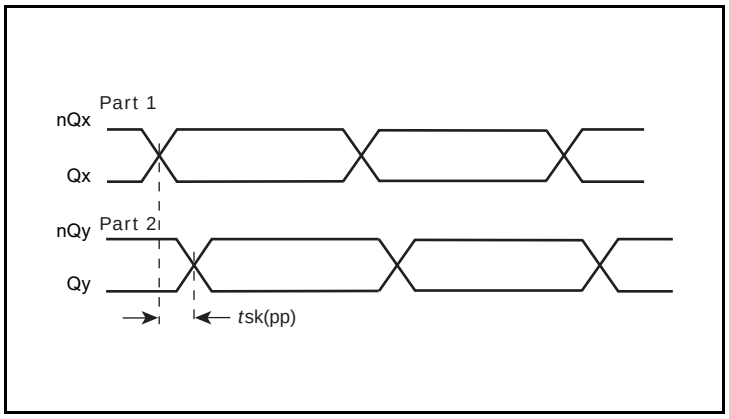
Parameter Measurement Information



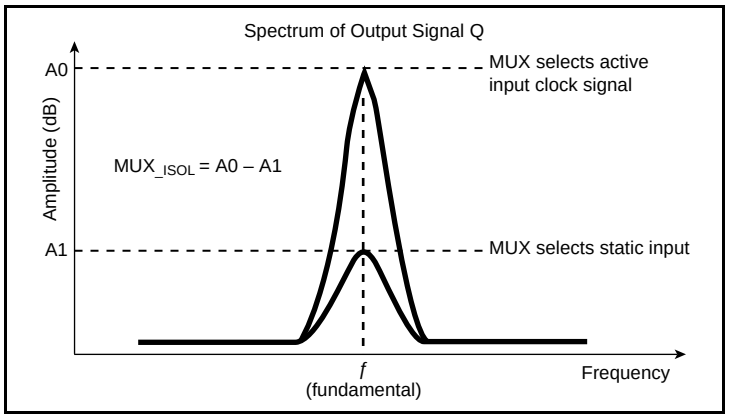
LVDS Output Load AC Test Circuit



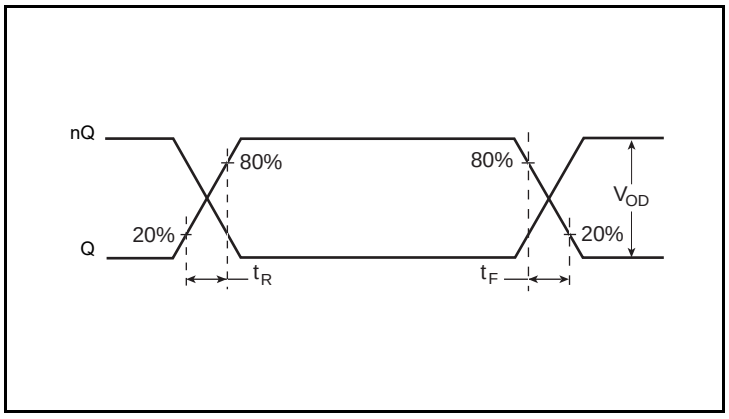
Differential Input Level



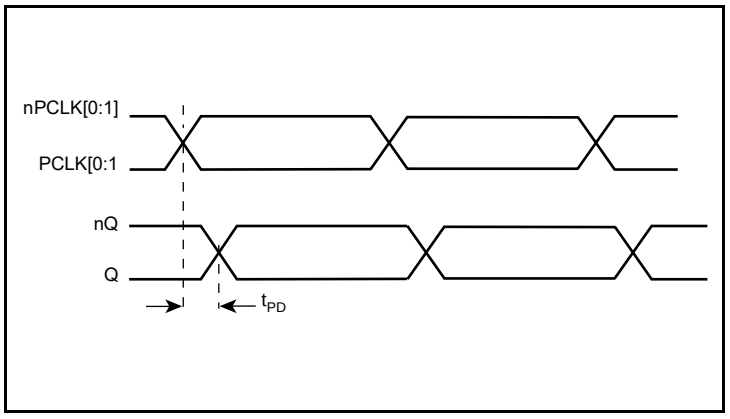
Part-to-Part Skew



MUX Isolation

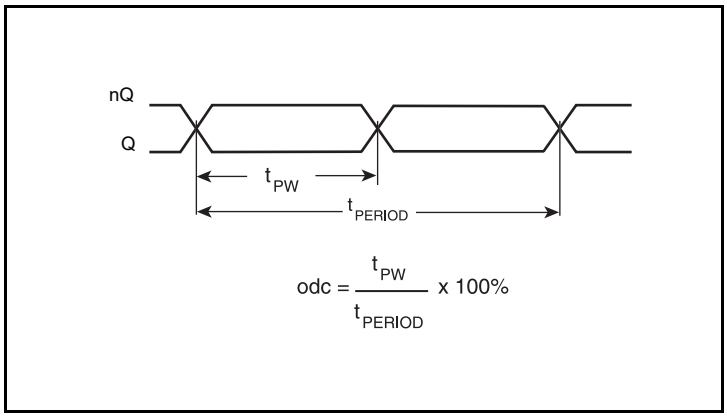


Output Rise/Fall Time

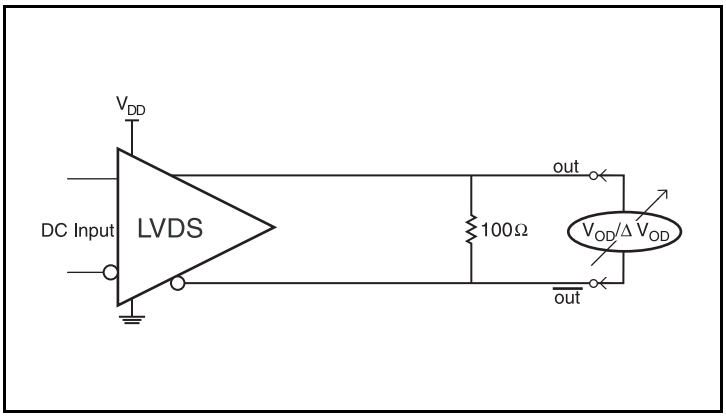


Propagation Delay

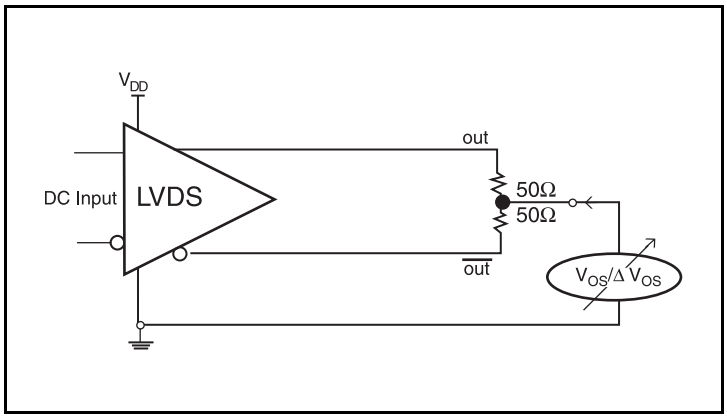
Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period



Differential Output Voltage Setup



Offset Voltage Setup

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

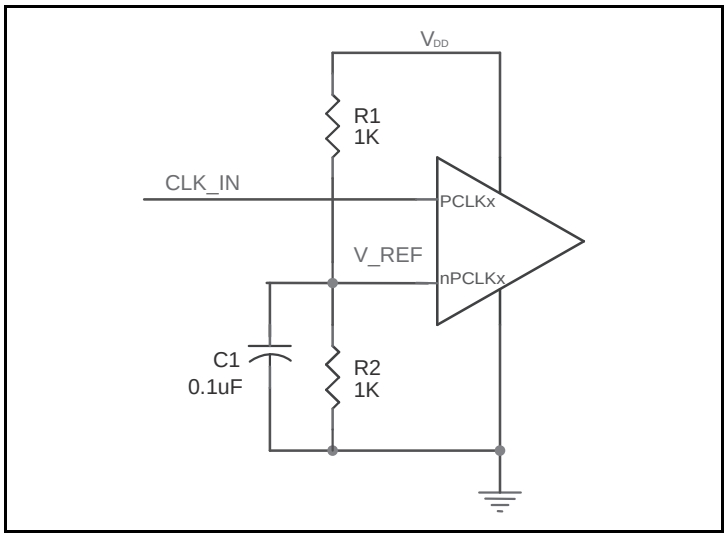


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Input Pins

Inputs:

PCLK/nPCLK Inputs:

For applications not requiring the use of the differential input, both PCLK and nPCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, LVDS and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2C* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

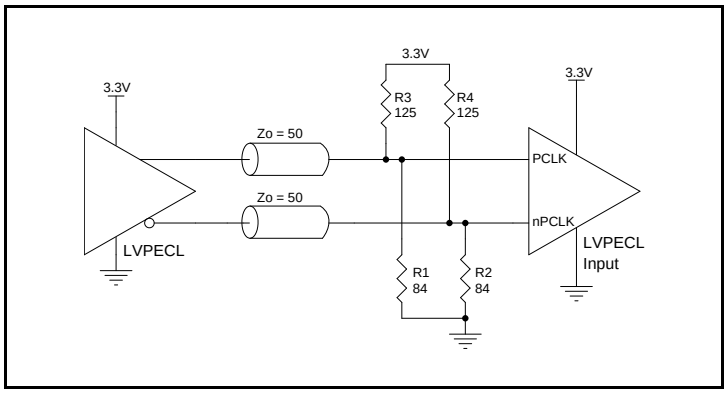


Figure 2A. PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

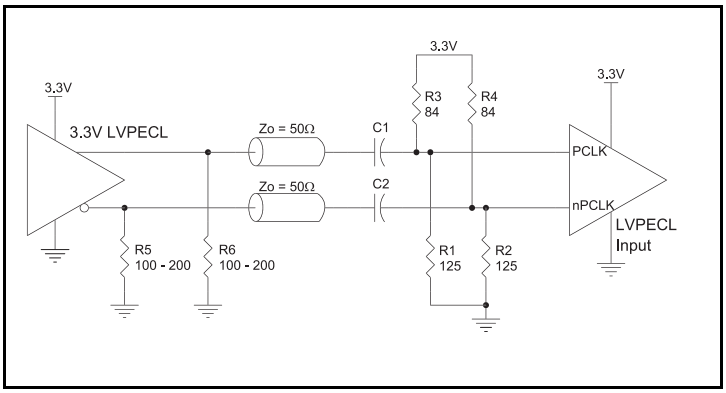


Figure 2B. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

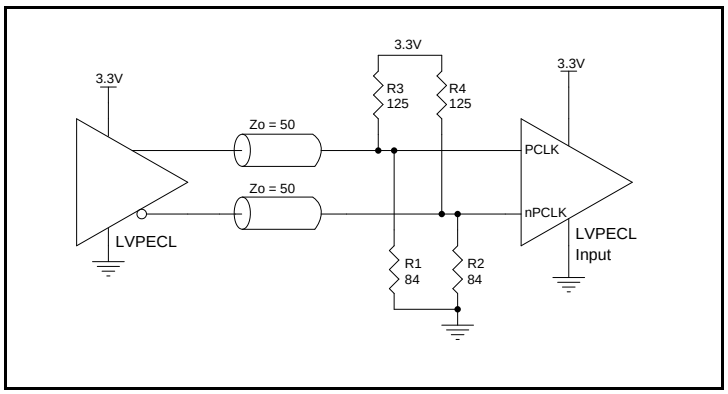


Figure 2C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

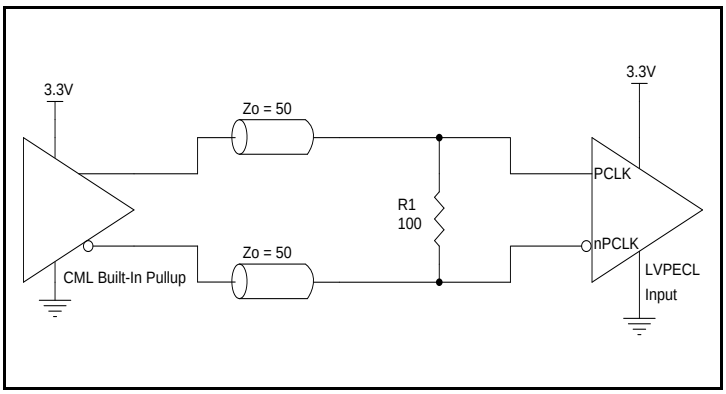


Figure 2D. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

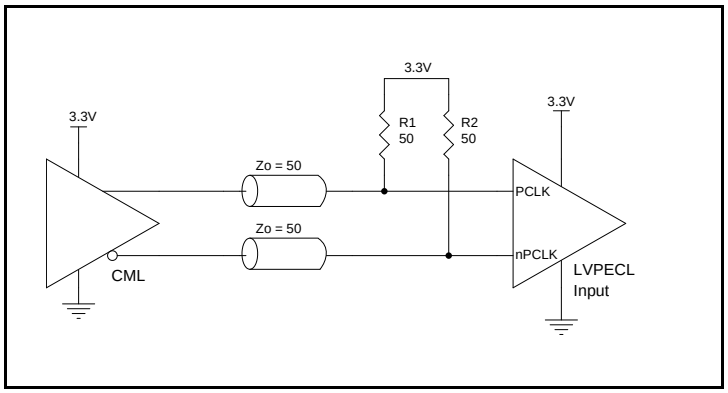


Figure 2E. PCLK/nPCLK Input Driven by a CML Driver

Application Schematic Example

Figure 3 shows an example of 854S01I application schematic. This device can accept different types of input signal. In this example, the input is driven by a LVDS driver. The decoupling capacitor should be located as close as possible to the power pin.

Note: Thermal pad (E-pad) must be connected to ground (GND).

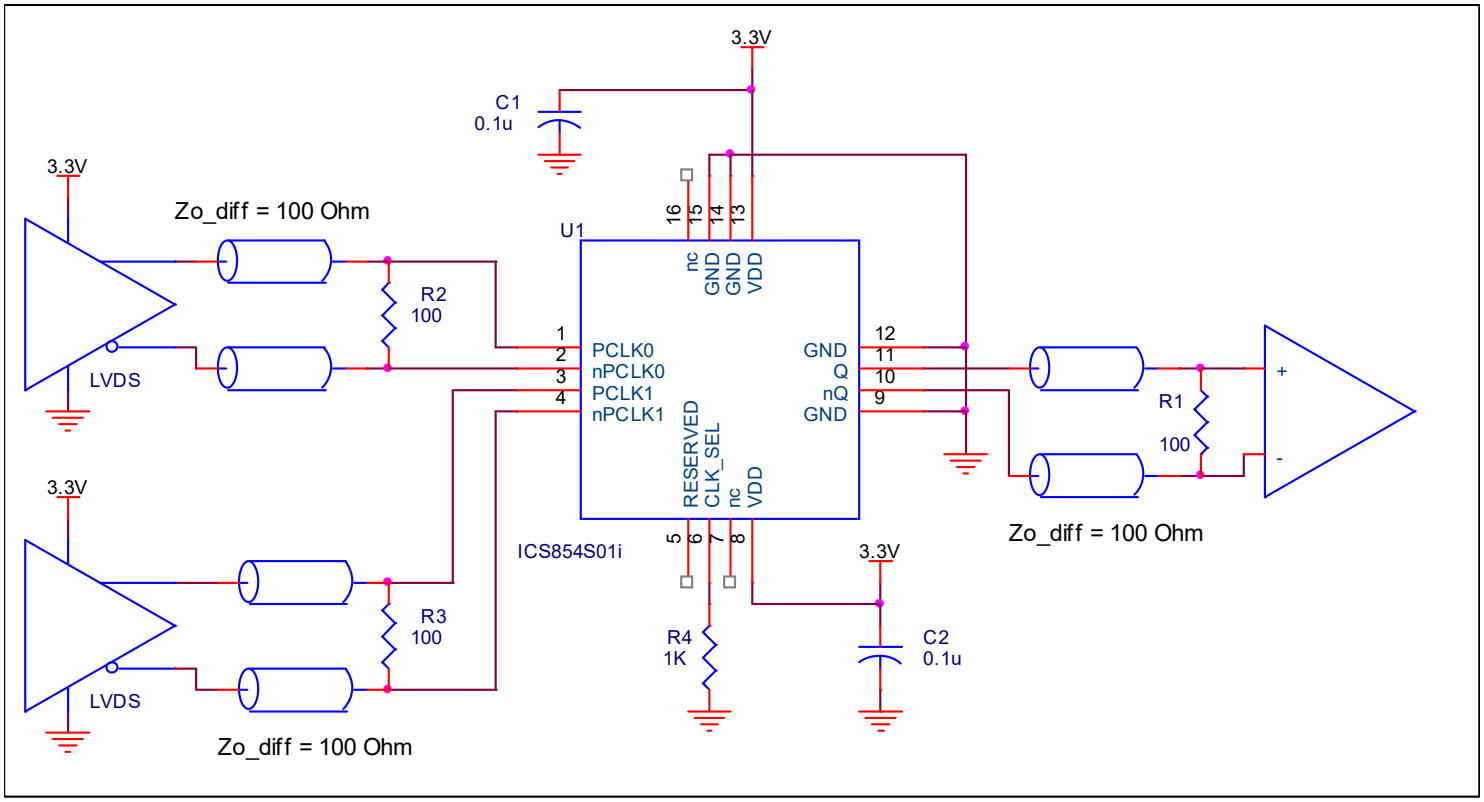


Figure 3. 854S01I Application Schematic Example

VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

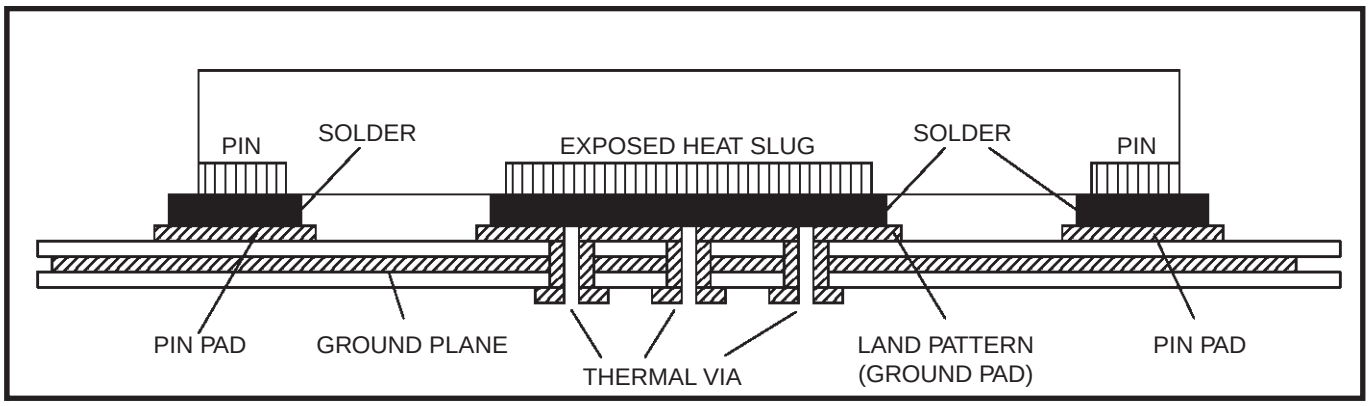


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 5* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

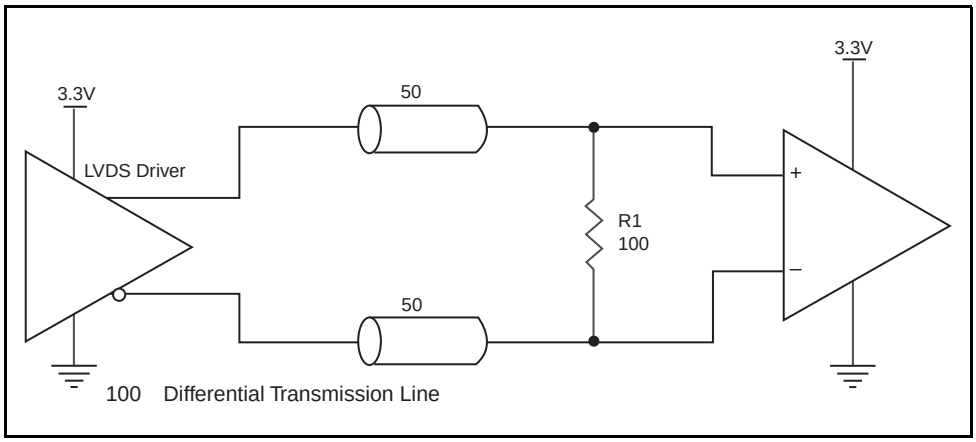


Figure 5. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the 854S01I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the854S01I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 40mA = **138.6mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.139W * 74.7°C/W = 95.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFPN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFPN

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

Transistor Count

The transistor count for 854S01I is: 257

This is a suggested replacement for ICS85401

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

Table 9. Ordering Information

Part Number	Marking	Package	Carrier Type	Temperature Range
854S01AKILF	4S1A	“Lead-Free” 16 Lead VFQFPN	Tray	-40°C to 85°C
854S01AKILFT	4S1A	“Lead-Free” 16 Lead VFQFPN	Tape & Reel	-40°C to 85°C

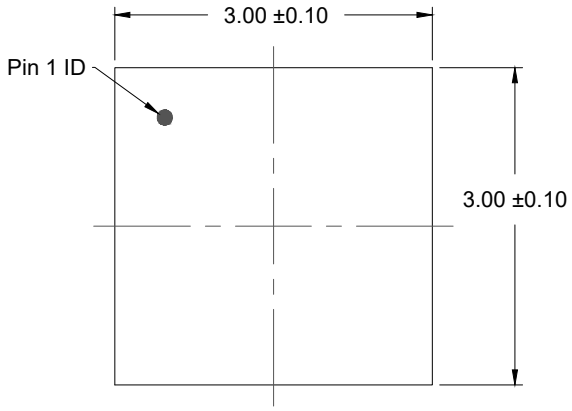
NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

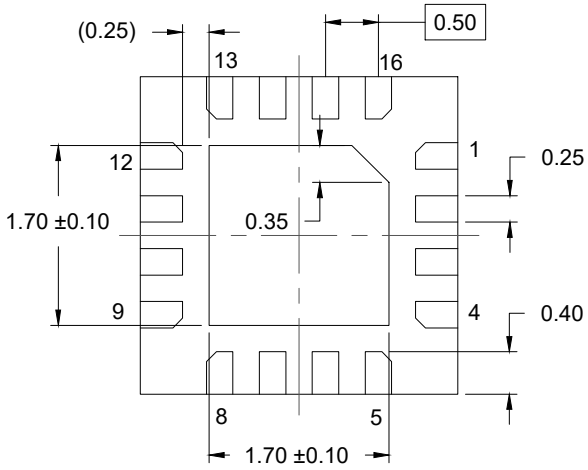
Date	Description of Change
September 29, 2022	Changed carrier type from “Tube” to “Tray” in Ordering Information for 854S01AKILF.
November 17, 2021	Added “Supports case temperature up to +105°C” to Features. Completed other minor changes.
June 15, 2017	Updated the package drawings.
November 2, 2012	Added Note: Thermal pad (E-pad) must be connected to ground (GND).
October 29, 2012	Deleted HiperClockS Logo. Updated GD paragraph to include CML.. Added CML to 3rd bullet. Added figures 2D and 2E. Deleted quantity from tape and reel.

Package Outline Drawing

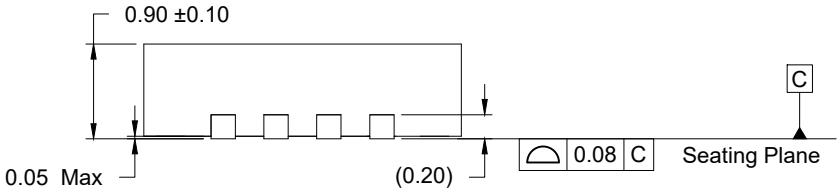
Package Code: NLG16P2
16-VFQFPN 3.0 x 3.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4169-02, Revision: 06, Date Created: Aug 18, 2023



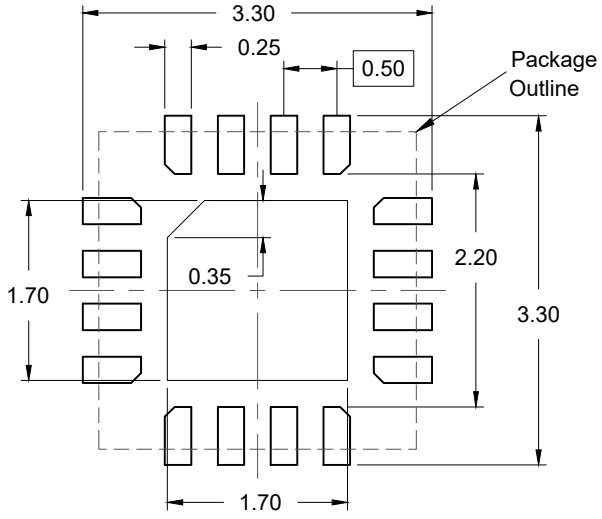
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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