Low Skew, 1-to-5, Differential-to-3.3V LVPECL/ECL Fanout Buffer

8735BI-01

DATA SHEET

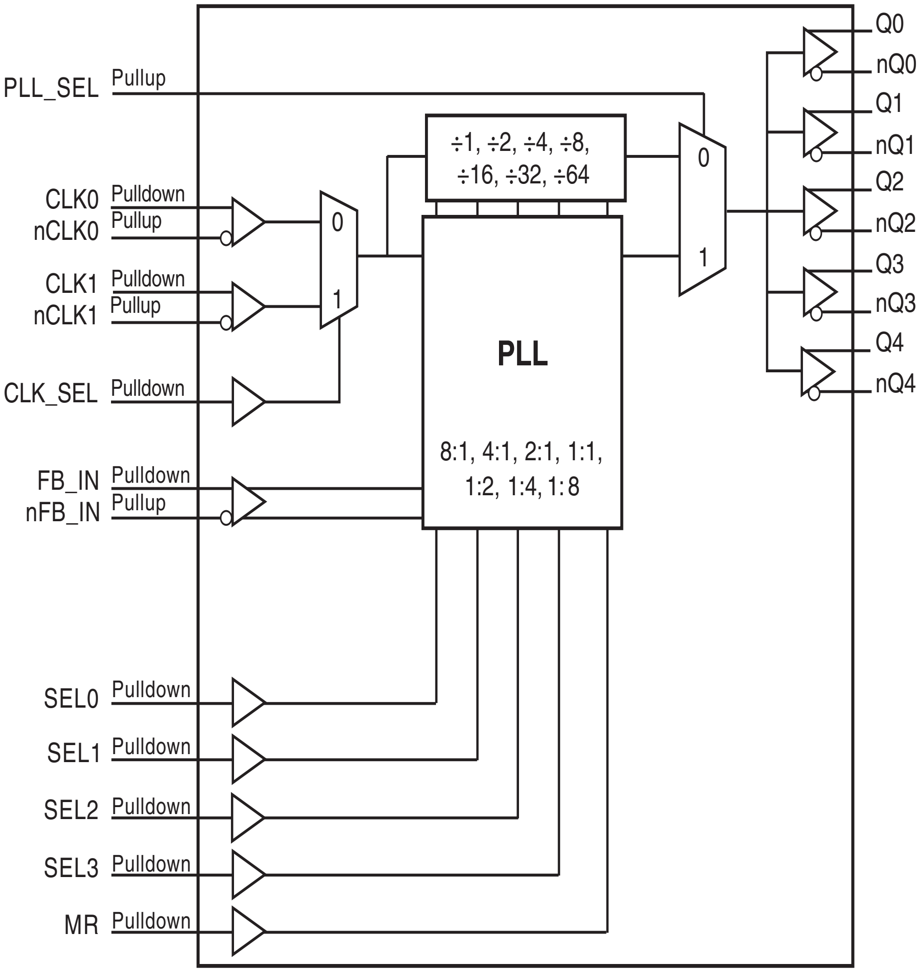
General Description

The 8735BI-01 is a highly versatile 1:5 Differential- to-3.3V LVPECL clock generator. The 8735BI-01 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 700MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

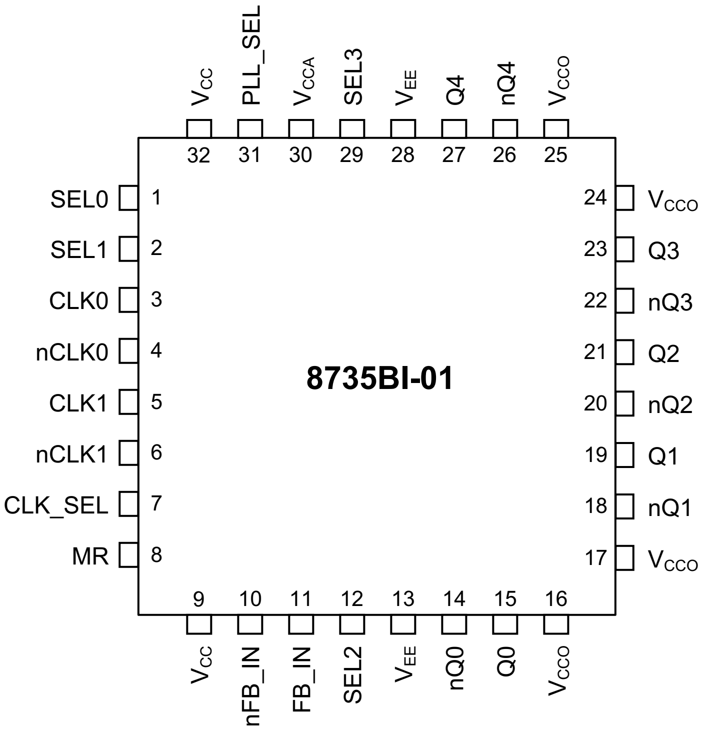
Features

- Five differential 3.3V LVPECL output pairs
- Selectable differential input pairs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Static phase offset: 200ps (maximum)
- Cycle-to-cycle jitter: 50ps (maximum)
- Output skew: 55ps (maximum)
- 3.3V output operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

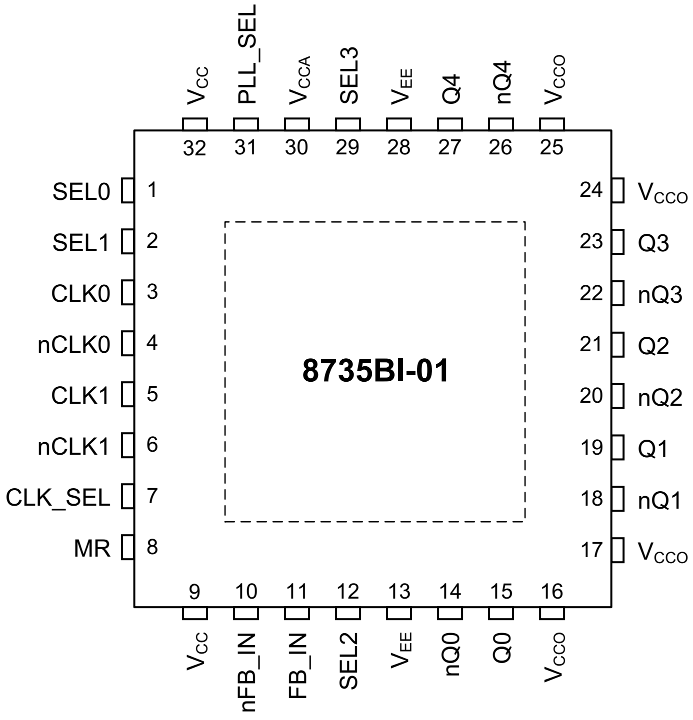
Block Diagram



Pin Assignments



32-pin, 7mm x 7mm LQFP Package



32-pin, 5mm x 5mm VFQFN Package

Pin Description and Pin Characteristic Table

Table 1. Pin Descriptions

Number	Name	Type		Description
1	SEL0	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
2	SEL1	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
3	CLK0	Input	Pulldown	Non-inverting differential clock input.
4	nCLK0	Input	Pullup	Inverting differential clock input.
5	CLK1	Input	Pulldown	Non-inverting differential clock input.
6	nCLK1	Input	Pullup	Inverting differential clock input.
7	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS/LVTTL interface levels.
8	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
9	V_{CC}	Power		Core supply pins.
10	nFB_IN	Input	Pullup	Feedback input to phase detector for regenerating clocks with “Zero Delay.”
11	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with “Zero Delay.”
12	SEL2	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
13	V_{EE}	Power		Negative power supply pins.
14	nQ0	Output		Differential output pair. LVPECL interface levels.
15	Q0	Output		Differential output pair. LVPECL interface levels.
16	V_{CCO}	Power		Output supply pins.

Number	Name	Type		Description
17	V_{CCO}	Power		Output supply pins.
18	nQ1	Output		Differential output pair. LVPECL interface levels.
19	Q1	Output		Differential output pair. LVPECL interface levels.
20	nQ2	Output		Differential output pair. LVPECL interface levels.
21	Q2	Output		Differential output pair. LVPECL interface levels.
22	nQ3	Output		Differential output pair. LVPECL interface levels.
23	Q3	Output		Differential output pair. LVPECL interface levels.
24	V_{CCO}	Power		Output supply pins.
25	V_{CCO}	Power		Output supply pins.
26	nQ4	Output		Differential output pair. LVPECL interface levels.
27	Q4	Output		Differential output pair. LVPECL interface levels.
28	V_{EE}	Power		Negative power supply pins.
29	SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
30	V_{CCA}	Power		Analog supply pin.
31	PLL_SEL	Input	Pullup	PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS/LVTTL interface levels.
32	V_{CC}	Power		Core supply pins.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Control Input Function Table

Inputs					Outputs
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)*	PLL_SEL = 1; PLL Enable Mode; Q[0:4], nQ[0:4]
0	0	0	0	250 - 700	÷1
0	0	0	1	125 - 350	÷1
0	0	1	0	62.5 - 175	÷1
0	0	1	1	31.25 - 87.5	÷1
0	1	0	0	250 - 700	÷2
0	1	0	1	125 - 350	÷2
0	1	1	0	62.5 - 175	÷2
0	1	1	1	250 - 700	÷4
1	0	0	0	125 - 350	÷4
1	0	0	1	250 - 700	÷8
1	0	1	0	125 - 350	x2
1	0	1	1	62.5 - 175	x2
1	1	0	0	31.25 - 87.5	x2
1	1	0	1	62.5 - 175	x4
1	1	1	0	31.25 - 87.5	x4
1	1	1	1	31.25 - 87.5	x8

*NOTE: VCO frequency range for all configurations above is 250MHz to 700MHz.

Table 3B. PLL Bypass Function Table

Inputs				Outputs
SEL3	SEL2	SEL1	SEL0	PLL_SEL = 0; PLL Bypass Mode; Q[0:4], nQ[0:4]
0	0	0	0	÷4
0	0	0	1	÷4
0	0	1	0	÷4
0	0	1	1	÷8
0	1	0	0	÷8
0	1	0	1	÷8
0	1	1	0	÷16
0	1	1	1	÷16
1	0	0	0	÷32
1	0	0	1	÷64
1	0	1	0	÷2
1	0	1	1	÷2
1	1	0	0	÷4
1	1	0	1	÷1
1	1	1	0	÷2
1	1	1	1	÷1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	**Rating**
Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC}+ 0.5V
Junction Temperature, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVPECL Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				155	mA
I_{CCA}	Analog Supply Current				17	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	SEL[3:0], MR, CLK_SEL	$V_{CC} = V_{IN} = 3.465V$			150	µA
		PLL_SEL	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	SEL[3:0], MR, CLK_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		PLL_SEL	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA

Table 4C. Differential DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	FB_IN, CLK[0:1]	$V_{CC} = V_{IN} = 3.465V$			150	µA
		nFB_IN, nCLK[0:1]	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	FB_IN, CLK[0:1]	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-5			µA
		nFB_IN, nCLK[0:1]	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			$V_{EE} + 0.5$		$V_{CC} – 0.85$	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2. Common mode voltage is defined as V_{IH}.

Table 4D. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} – 1.4$		$V_{CCO} – 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} – 2.1$		$V_{CCO} – 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} – 2V. See Parameter Measurement Information section, *3.3V Output Load Test Circuit.*

Table 5. Input Frequency Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLK[0:1], nCLK[0:1]	PLL_SEL = 1	31.25		700	MHz
		CLK[0:1], nCLK[0:1]	PLL_SEL = 0			700	MHz

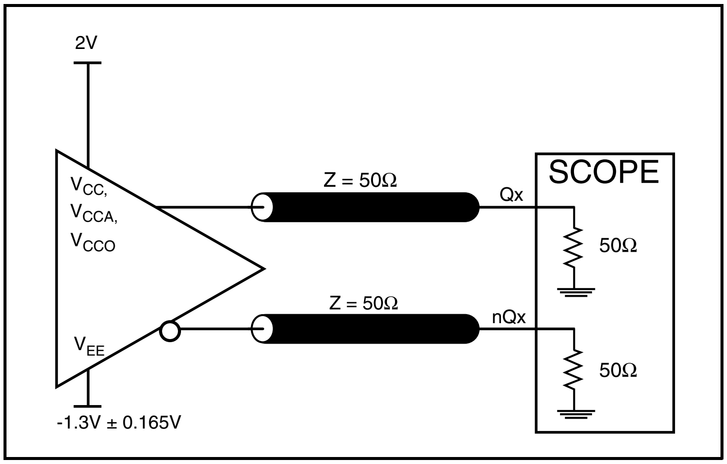
AC Electrical Characteristics

Table 6. AC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

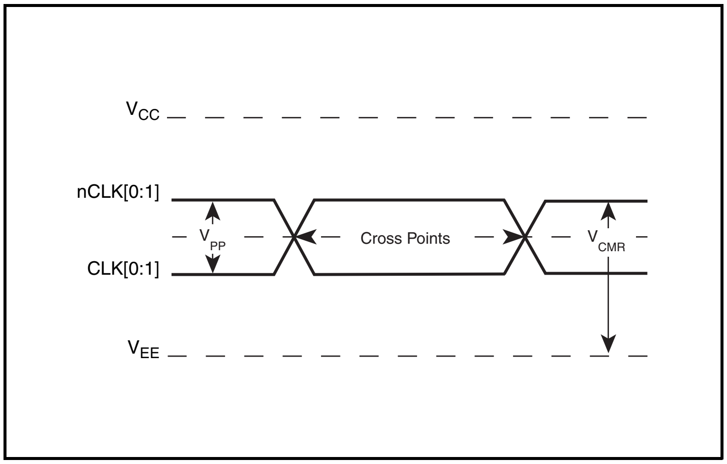
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1	PLL_SEL = 0V, $f_{OUT} \leq 700MHz$	2.8		4.9	ns
$t(Ø)$	Static Phase Offset; NOTE 2, 4	PLL_SEL = 3.3V	-100		200	ps
$tsk(o)$	Output Skew; NOTE 3, 4				55	ps
$tjit(cc)$	Cycle-to-Cycle Jitter: NOTE 4, 5				50	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle	$f_{OUT} \leq 250MHz$	47		53	%
t_{LOCK}	PLL Lock Time				1	ms

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the differential output crosspoint.
NOTE 2: Defined as the time difference between the input reference clock and the averaged feedback input signal across all conditions, when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoint.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: Characterized at VCO frequency of 622MHz.

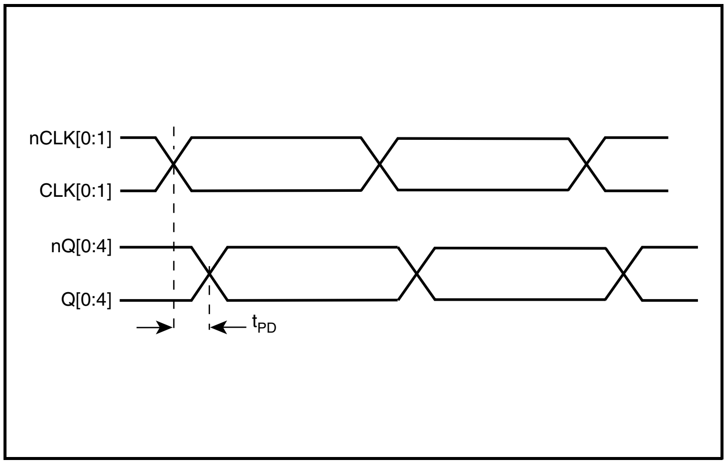
Parameter Measurement Information



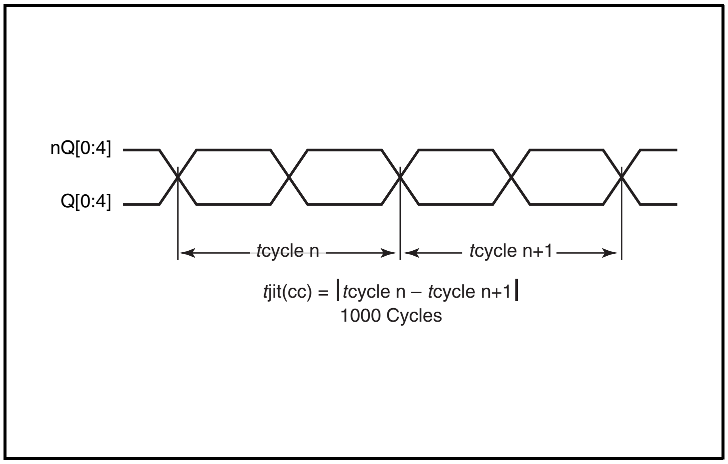
3.3V LVPECL Output Load AC Test Circuit



Differential Input Level

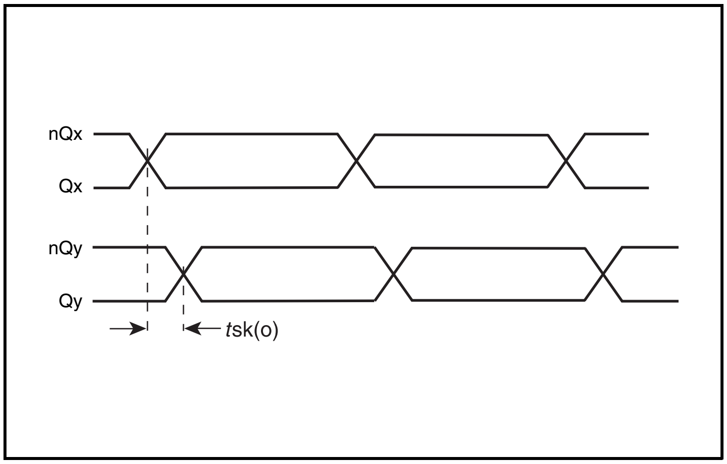


Propagation Delay

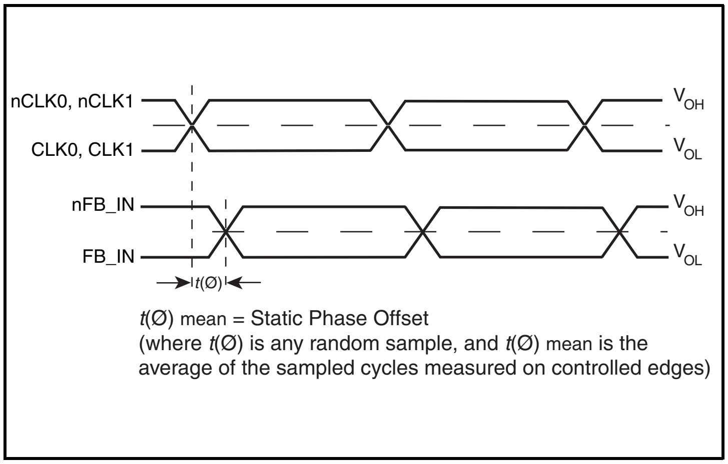


$t_{jit}(cc) = |t_{cycle\ n} - t_{cycle\ n+1}|$
1000 Cycles

Cycle-to-Cycle Jitter



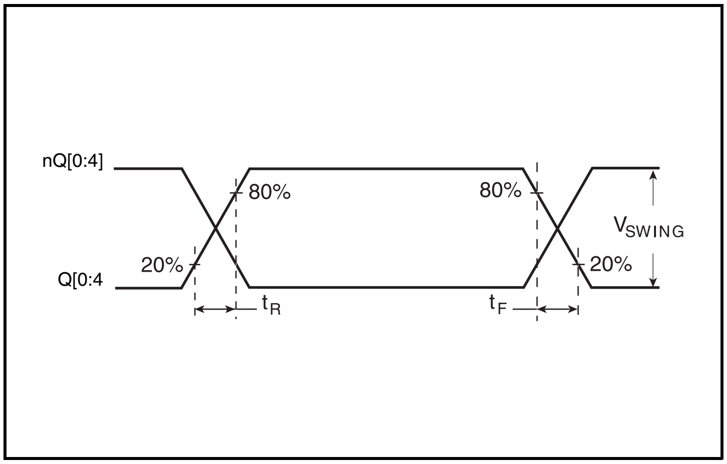
Output Skew



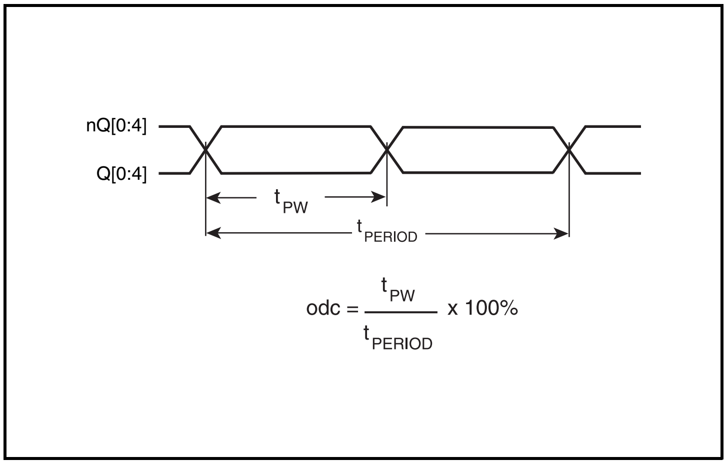
t(Ø) mean = Static Phase Offset
(where *t*(Ø) is any random sample, and *t*(Ø) mean is the average of the sampled cycles measured on controlled edges)

Static Phase Offset

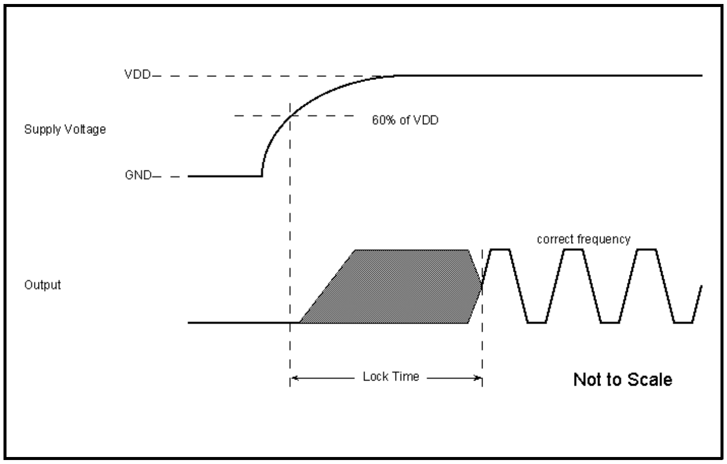
Parameter Measurement Information



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



PLL Lock Time

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage V_1= $V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

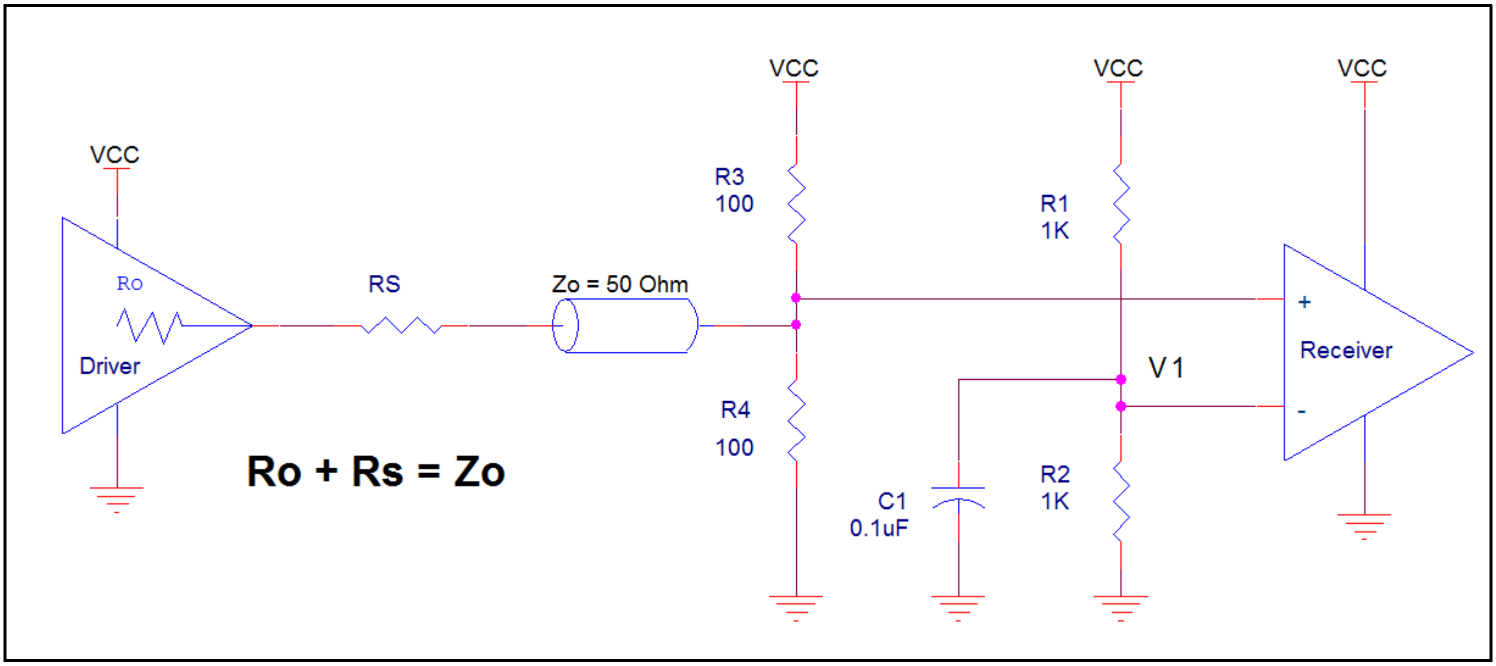


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 2A to* Figure 2E show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in *Figure 2A*, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

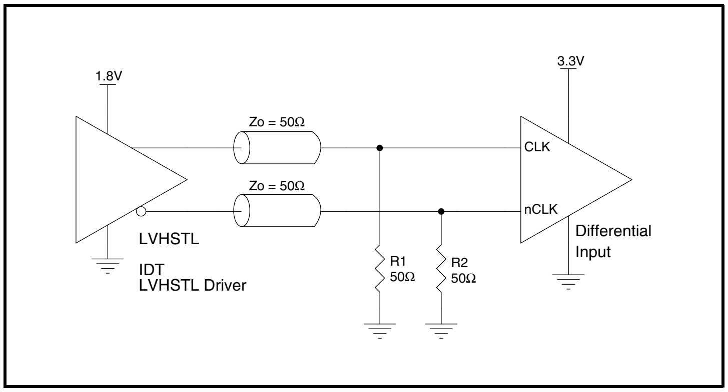


Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

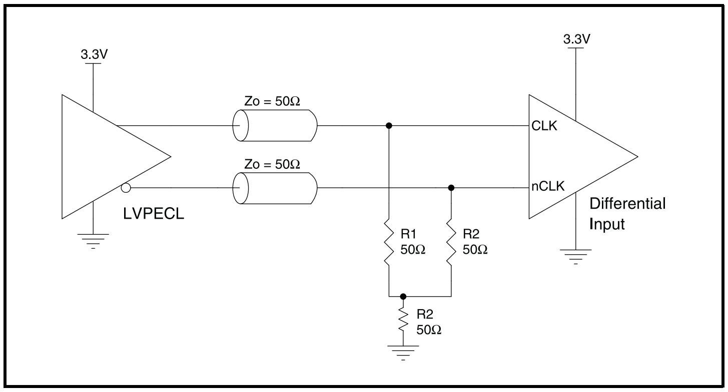


Figure 2D. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

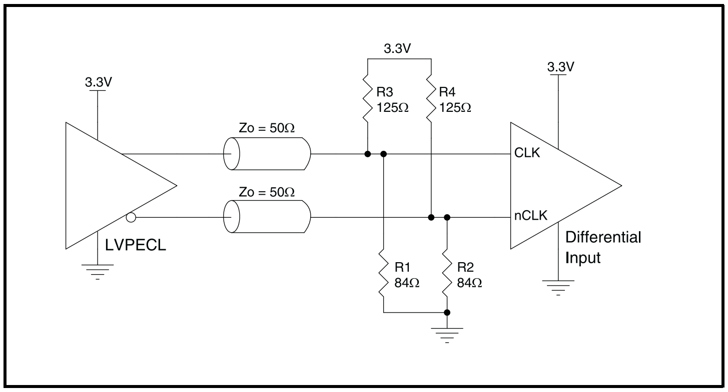


Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

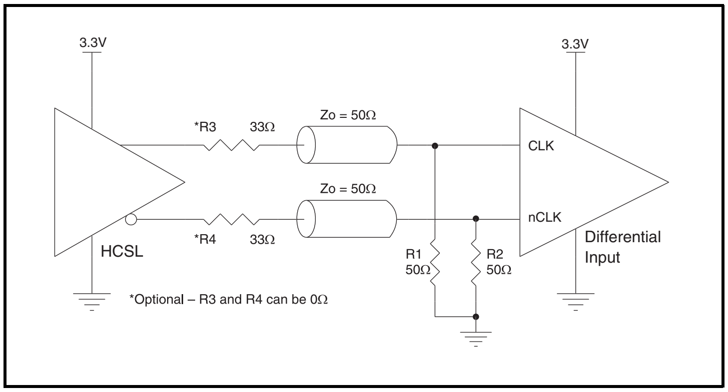


Figure 2E. CLK/nCLK Input Driven by a 3.3V HCSL Driver

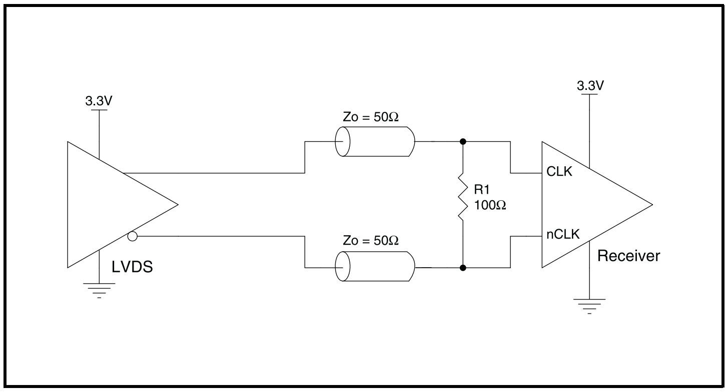


Figure 2C. CLK/nCLK Input Driven by a 3.3V LVDS Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

FB_IN/nFB_IN Inputs

For applications not requiring the use of the differential feedback input, both FB_IN and nFB_IN can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from FB_IN to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figure 3A and* Figure 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

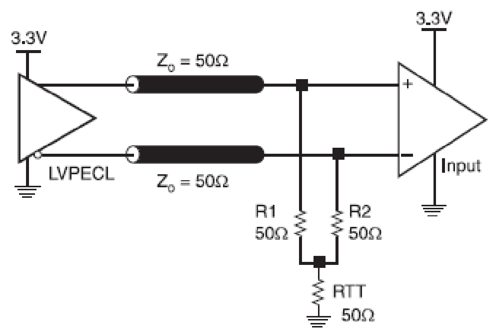


Figure 3A. Figure 4A. 3.3V LVPECL Output Termination

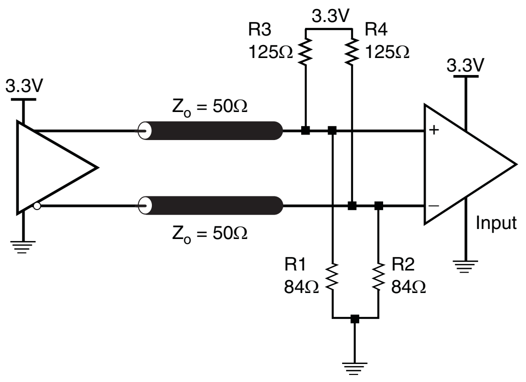


Figure 3B. Figure 4B. 3.3V LVPECL Output Termination

Schematic Layout

Figure 4 (next page) shows an example 8735BI-01 application schematic in which the device operates at V_{CC} = 3.3V.

This example focuses on functional connections is shown configured as a zero delay buffer. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

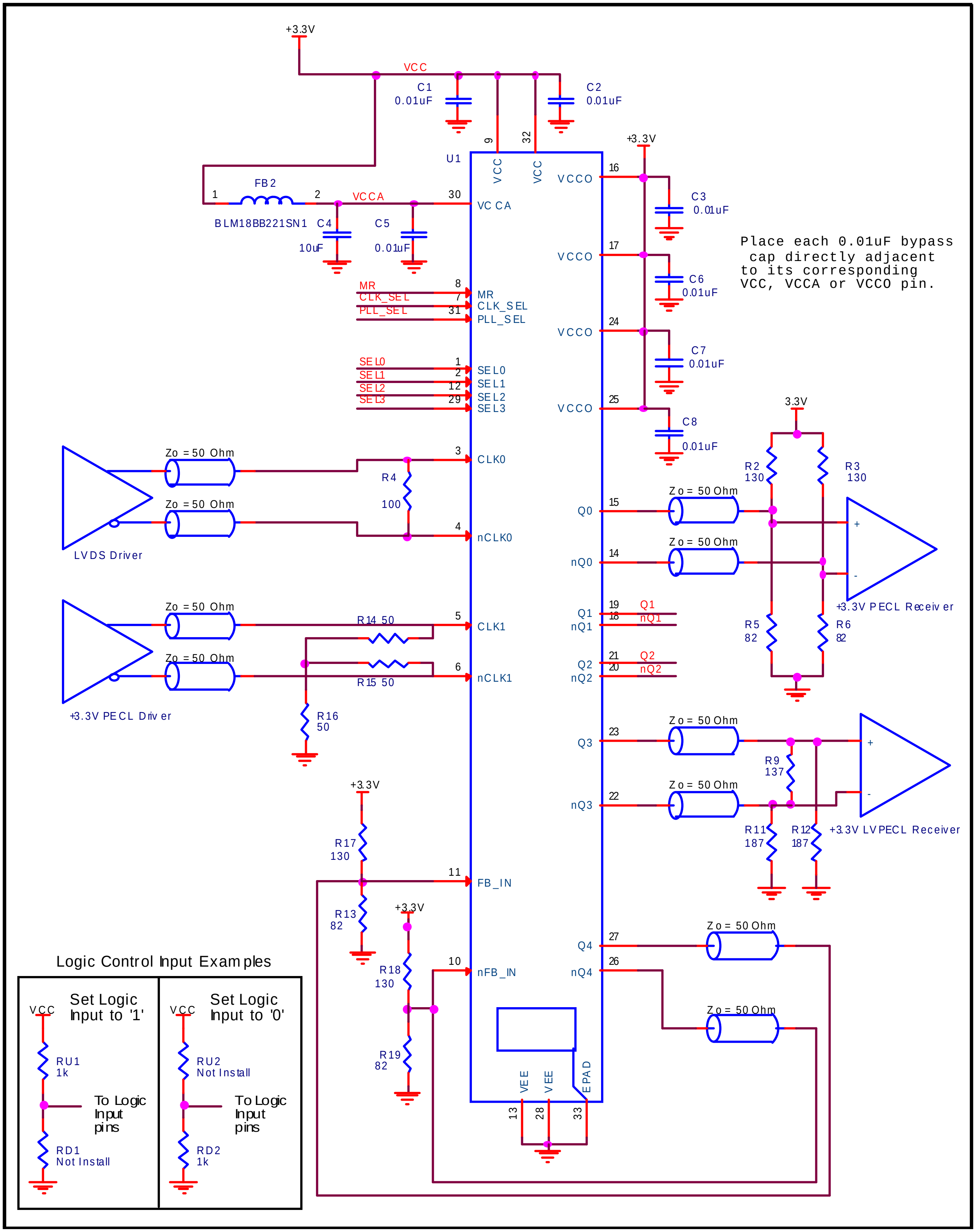
In addition to the standard LVDS termination shown for CLK0, nCLK0, this example shows four different LVPECL terminations; the standard Thevenin equivalent termination on Q0, a T or Wye termination on CLK1, nCLK1, the PI or Wye equivalent of the T on Q3, nQ3 and an AC coupled termination to the standard IDT CLK, nCLK clock buffer input biased by a 51kΩ resistor on the CLK input and either a 51kΩ pull down on nCLK or a 51kΩ pull-down and a 51kΩ pull-up on nCLK.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8735BI-01 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the V_{CCA} bead and the 0.01uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Pull-up and pull-down resistors to set configuration pins can all be placed on the PCB side opposite the device side to free up device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

For additional layout recommendations and guidelines, contact clocks@idt.com.



Place each 0.01uF bypass cap directly adjacent to its corresponding VCC, VCCA or VCCO pin.

Figure 4. 8735BI-01 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8735BI-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8735BI-01 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{CCO} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

The maximum current at 85°C is as follows:

I_{EE_MAX} = 155mA

- Power $(core)_{MAX}$ = V_{CCO_MAX} * I_{EE_MAX} = 3.465V * 155mA = **537.075mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 5 * 30mW = **150mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 537.075mW + 150mW = **687.075mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 47.9°C/W per Table 7A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.687W * 47.9°C/W = 118°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7A. Thermal Resistance θ_{JA} for 32-LeadLQFP, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

Table 7B. θ_{JA} vs. Air Flow Table for a 32-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 5.*

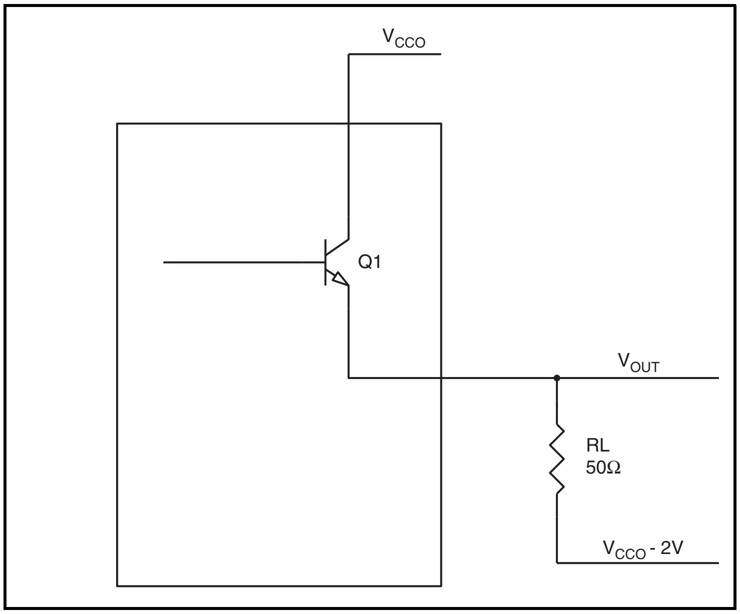


Figure 5. LVPECL Driver Circuit and Termination

To calculate power dissipation per output due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX}} - \mathbf{1.7}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 8A. θ_{JA} vs. Air Flow Table for a 32-Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

Table 8B. θ_{JA} vs. Air Flow Table for a 32-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

Transistor Count

The transistor count for 8735BI-01 is: 2969

32-Lead LQFP Package Outline and Package Dimensions

Package Outline - Y Suffix for 32-Lead LQFP

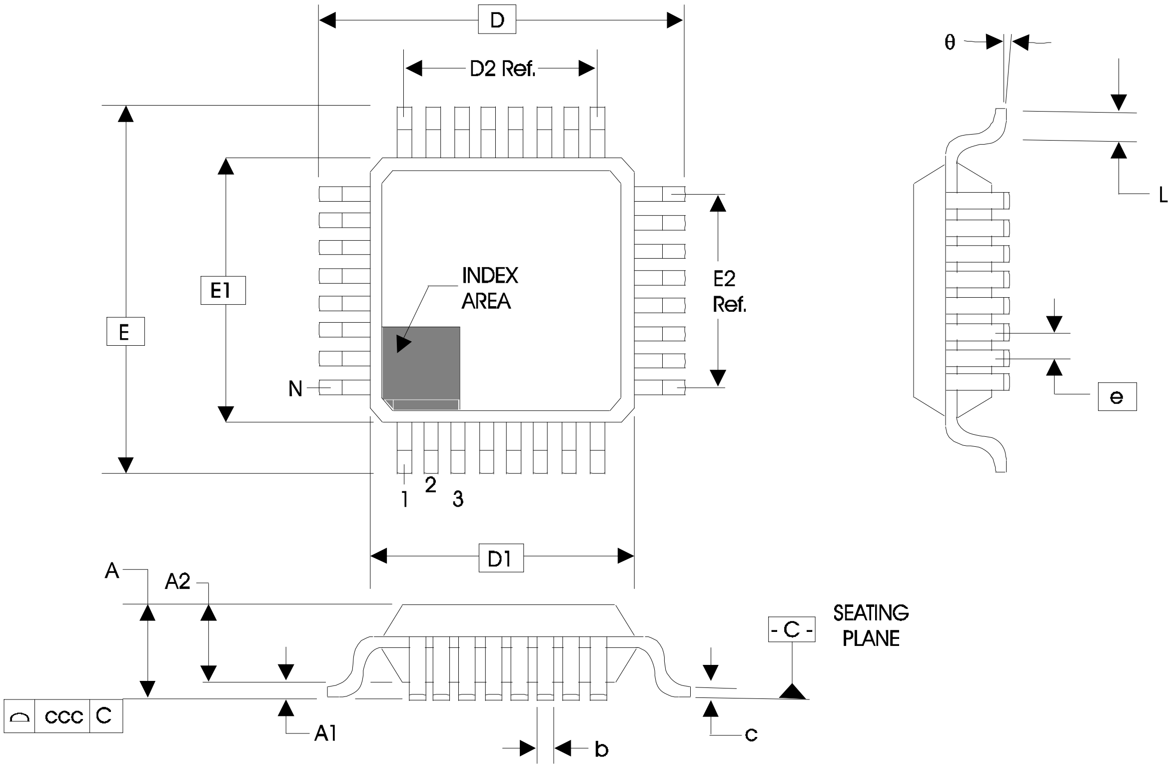


Table 9. Package Dimensions for 32-Lead LQFP

JEDEC Variation: BBC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10

Reference Document: JEDEC Publication 95, MS-026

32-Lead VFQFN Package Outline and Package Dimensions

Package Outline - NL Suffix for 32 Lead VFQFN

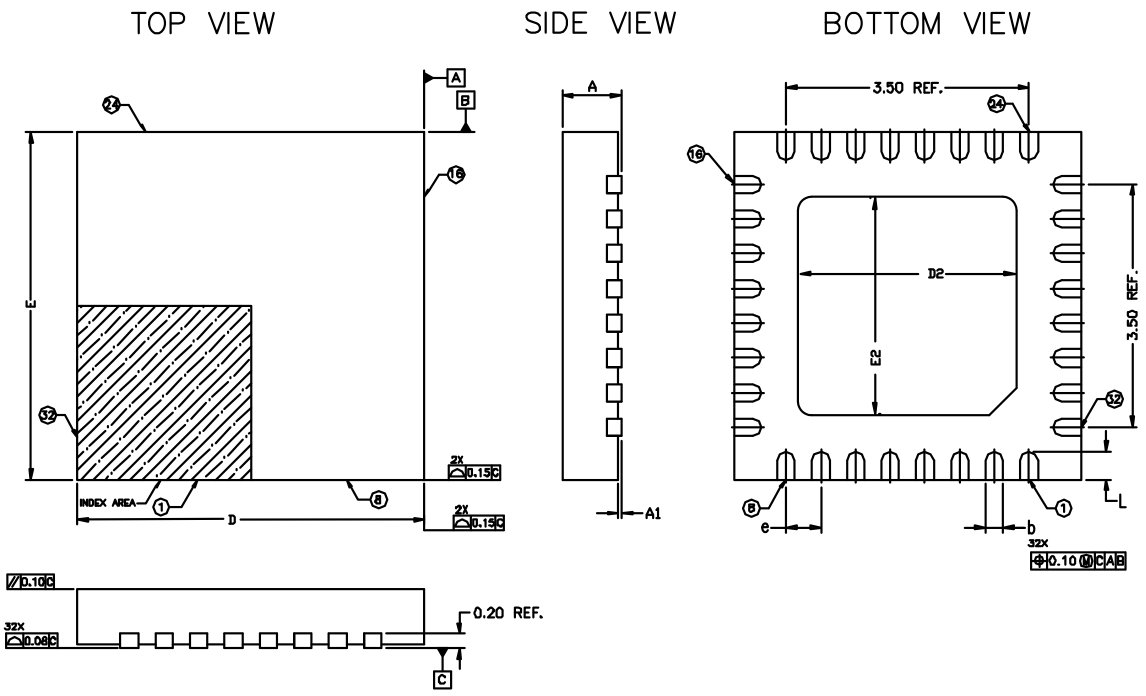


Table 9. Package Dimensions

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 Ref.	
b	0.18	0.25	0.30
D & E		5.00 Basic	
D2 & E2	3.00	3.15	3.30
e		0.50 Basic	
L	0.30	0.40	0.50

NOTE: The drawing and dimension data originates from IDT package outline drawing PSC-4171, Rev. 05.

1. All dimensions are in millimeters. All angles are in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals.
   Coplanarity shall not exceed 0.08mm.
3. Warpage should not exceed 0.10mm.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8735BYI-01LF	ICS8735BI01L	32-Lead LQFP, Lead-Free	Tray	-40°C to 85°C
8735BYI-01LFT	ICS8735BI01L	32-Lead LQFP, Lead-Free	Tape & Reel	-40°C to 85°C
8735BKI-01LF	ICS735BI01L	32-Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
8735BKI-01LFT	ICS735BI01L	32-Lead VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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