Description

The 8P791208 is a low additive jitter 2:8 buffer with CMOS/ differential outputs The device takes one or two reference clocks, selects between them using a pin selection, and generates up to eight outputs that are the same as the reference frequency.

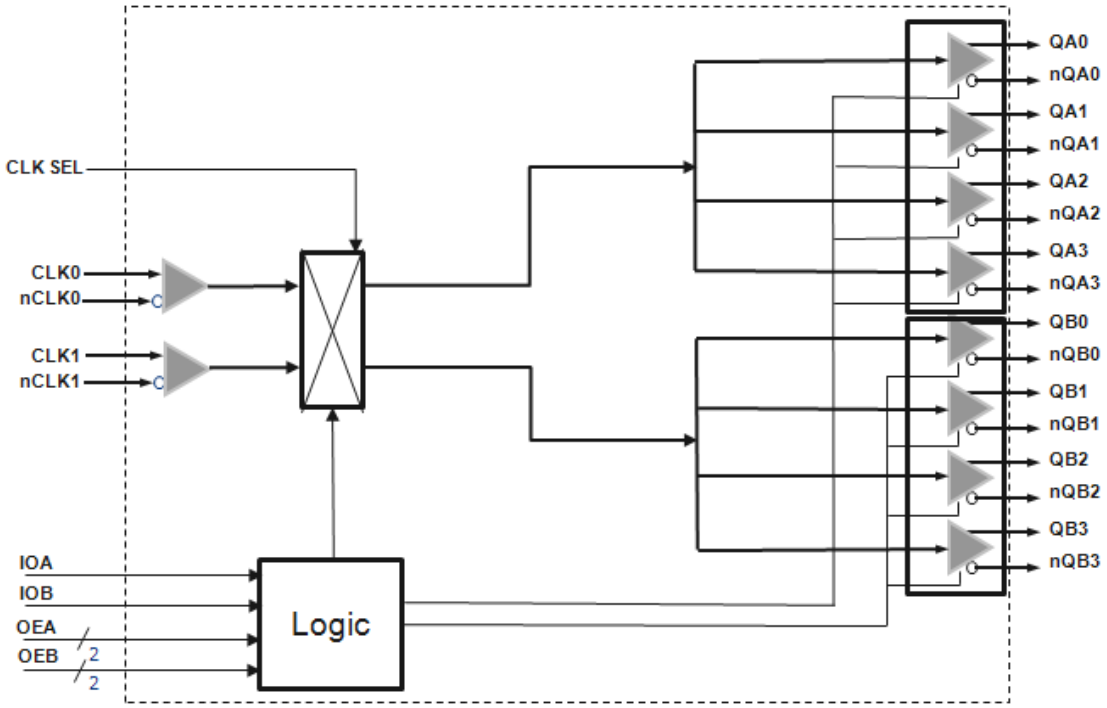
The 8P791208 supports two output banks, each with its own power supply. All outputs in one bank would generate the same output frequency, but each output can be individually controlled for output type or output enable.

The device can operate over the -40°C to 85°C temperature range.

Features

- Accepts input frequencies ranging from 1PPS (1Hz) to 700MHz
- Two differential inputs support LVPECL, LVDS, LVHSTL, HCSL, or LVCMOS reference clocks
- Generates 8 differential or 16 LVCMOS outputs
- Outputs arranged in two banks of four outputs each
- Select pins control which input drives which of two output banks
- Controlled by 3-level input pins that are 3.3V tolerant for all core voltages
- Output type may be selected from LVPEC, LVDS or 2xLVCMOS
- Each bank supports a separate power supply of 3.3V, 2.5V, or 1.8V
- LVCMOS outputs are limited to 125MHz maximum and support swings of 3.3V, 2.5V, 1.8V, and 1.5V
- Individual output enables and output type selection supported
- Output noise floor of –158dBc/Hz at 156.25MHz
- Core voltage supply of 3.3V, 2.5V, or 1.8V
- –40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) QFN-32 (5 × 5mm) packaging

Block Diagram



8P791208 transistor count: 9,703

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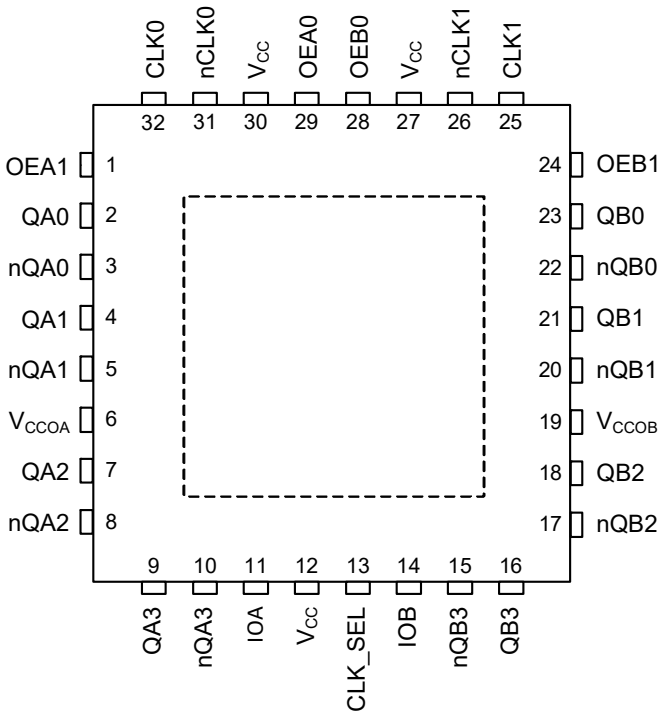
Pin Assignments

Figure 1. Pin Assignment for 5mm × 5mm VFQFN Package – Top View



Pin Descriptions

Table 1. Pin Description

Number	Name	Type[a]	Description
1	OEA1	Input (PU)	Controls output enable functions for Bank A. LVCMOS/LVTTL input levels.
2	QA0	Output	Positive differential clock output. Included in Bank A. Refer to Output Drivers for additional details.
3	nQA0	Output	Negative differential clock output. Included in Bank A. Refer to Output Drivers for additional details.
4	QA1	Output	Positive differential clock output. Included in Bank A. Refer to Output Drivers for additional details.
5	nQA1	Output	Negative differential clock output. Included in Bank A. Refer to Output Drivers for additional details.
6	V_{CCOA}	Power	Output voltage supply for output Bank A.
7	QA2	Output	Positive differential clock output. Included in Bank A. Refer to Output Drivers for additional details.
8	nQA2	Output	Negative differential clock output. Included in Bank A. Refer to Output Drivers for additional details.
9	QA3	Output	Positive differential clock output. Included in Bank A. Refer to Output Drivers for additional details.
10	nQA3	Output	Negative differential clock output. Included in Bank A. Refer to Output Drivers for additional details.

Table 1. Pin Description (Cont.)

Number	Name	Type[a]	Description
11	IOA	Input (PU/PD)	Controls output mode functions for Bank A. 3-level input.
12	V_{CC}	Power	Core Logic voltage supply.
13	CLK_SEL	Input (PU/PD)	Input Clock Selection Control pin. 3-level input. This pin's function is described in the Input Selection section.
14	IOB	Input (PU/PD)	Controls output mode functions for Bank B. 3-level input.
15	nQB3	Output	Negative differential clock output. Included in Bank B. Refer to Output Drivers for additional details.
16	QB3	Output	Positive differential clock output. Included in Bank B. Refer to Output Drivers for additional details.
17	nQB2	Output	Negative differential clock output. Included in Bank B. Refer to Output Drivers for additional details.
18	QB2	Output	Positive differential clock output. Included in Bank B. Refer to Output Drivers for additional details.
19	V_{CCOB}	Power	Output voltage supply for Output Bank B.
20	nQB1	Output	Negative differential clock output. Included in Bank B. Refer to Output Drivers for additional details.
21	QB1	Output	Positive differential clock output. Included in Bank B. Refer to Output Drivers for additional details.
22	nQB0	Output	Negative differential clock output. Included in Bank B. Refer to Output Drivers for additional details.
23	QB0	Output	Positive differential clock output. Included in Bank B. Refer to Output Drivers for additional details.
24	OEB1	Input (PU)	Controls output enable functions for Bank B. LVCMOS/LVTTL input levels.
25	CLK1	Input (PD)	Non-inverting differential clock input.
26	nCLK1	Input (PU/PD)	Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pull-up and pulldown resistors).
27	V_{CC}	Power	Core Logic voltage supply.
28	OEB0	Input (PU)	Controls output enable functions for Bank B. LVCMOS/LVTTL input levels.
29	OEA0	Input (PU)	Controls output enable functions for Bank A. LVCMOS/LVTTL input levels.
30	V_{CC}	Power	Core Logic voltage supply.
31	nCLK0	Input (PU/PD)	Inverting differential clock input. $V_{CC}/2$ when left floating (set by the internal pull-up and pull-down resistors).
32	CLK0	Input (PD)	Non-inverting differential clock input.
EP	Exposed Pad	Ground	Must be connected to GND.

[a] Pull-up (PU) and pull-down (PD) resistors are indicated in parentheses. *Pull-up* and *pull-down* refers to internal input resistors. See Table 10, *DC Input Characteristics,* for typical values.

Principles of Operation

Input Selection

The 8P791208 supports two input references: CLK0 and CLK1 that may be driven with differential or single-ended clock signals. Either may be used as the source frequency for either or both output banks under control of the CLK_SEL input pin.

Table 2. Input Selection Control

CLK_SEL	Description
High	Banks A and B both driven from CLK1
Middle[a]	Bank A driven from CLK0 & Bank B driven from CLK1
Low	Banks A and B both driven from CLK0

[a] A 'middle' voltage level is defined in Table 11. Leaving the input pin open will also generate this level via a weak internal resistor network.

Output Drivers

The QA[0:3] and QB[0:3] clock outputs are provided with pin-controlled output drivers. The following table shows how each bank can be controlled. Each bank is separately controlled and all outputs within a single bank will behave the same way.

Table 3. Output Mode Control

IOx	Output Bank Mode Function
High	All outputs in the bank are LVDS
Middle	All outputs in the bank are LVPECL
Low	All outputs in the bank are LVCMOS

The operating voltage ranges of each output is determined by its independent output power pin (V_{CCOA} or V_{CCOB}) and thus each can have different output voltage levels. Output voltage levels of 1.8V, 2.5V or 3.3V are supported for differential operation and LVCMOS operation. In addition, LVCMOS output operation supports 1.5V V_{CCO}.

LVCMOS Operation

When a given output is configured to provide LVCMOS levels, then both the Q and nQ outputs will toggle at the selected output frequency. All the previously described configuration and control apply equally to both outputs. Frequency, voltage levels and enable / disable status apply to both the Q and nQ pins. When configured as LVCMOS, the Q & nQ outputs are in-phase relative to one another.

Output Enable Control

The 8P791208 has separate pins that control the output enable behavior for each bank as shown in the following table.

Table 4. Output Enable Control

OEx1	OEx0	Output Enable Function			
		Qx3	Qx2	Qx1	Qx0
High	High	On	On	On	On
High	Low	Hi-Z	Hi-Z	On	On
Low	High	On	On	Hi-Z	Hi-Z
Low	Low	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Absolute Maximum Ratings

NOTE: The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8P79208 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{CCX}[a] to GND	3.63V
Inputs OEA[1:0], OEB[1:0], IOA, IOB, CLK_SEL, CLK0, nCLK0, CLK1, nCLK1	–0.5V to V_{CC} + 0.5V
Outputs, I_O QA[0:3], nQA[0:3]; QB[0:3], nQB[0:3] Continuous Current Surge Current	 40mA 60mA
Outputs, V_O QA[0:3], nQA[0:3]; QB[0:3], nQB[0:3]	–0.5V to V_{CCOx}[b] + 0.5V
Maximum Junction Temperature	125°C
Storage Temperature, T_{STG}	–65°C to 150°C
Lead Temperature (Soldering, 10s)	+260°C

[a] V_{CCX} denotes V_{CC}, V_{CCOA}, or V_{CCOB}.

[b] V_{CCOX} denotes V_{CCOA} or V_{CCOB}.

Supply Voltage Characteristics

Table 6. Power Supply Characteristics, V_{CC} = V_{CCOA} = V_{CCOB} = 3.3V ±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core supply voltage		3.135	3.3	3.465	V
V_{CCOA}, V_{CCOB}	Output supply voltage		3.135	3.3	V_{CC}	V
I_{CC}	Core supply current	Device configured for LVDS logic levels		22	25	mA
I_{CCOX}	Output supply current[a]	All outputs configured for LVDS logic levels; outputs unloaded		136	153	mA

[a] Internal dynamic switching current at maximum f_{OUT} is included.

Table 7. Power Supply Characteristics, V_{CC} = V_{CCOA} = V_{CCOB} = 2.5V ±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core supply voltage		2.375	2.5	2.625	V
V_{CCOA}, V_{CCOB}	Output supply voltage		2.375	2.5	V_{CC}	V
I_{CC}	Core supply current	Device configured for LVDS logic levels		21	24	mA
I_{CCOX}	Output supply current[a]	All outputs configured for LVDS logic levels; outputs unloaded		135	151	mA

[a] Internal dynamic switching current at maximum f_{OUT} is included.

Table 8. Power Supply Characteristics, V_{CC} = V_{CCOA} = V_{CCOB} = 1.8V ±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core supply voltage		1.71	1.8	1.89	V
V_{CCOA}, V_{CCOB}	Output supply voltage		1.71	1.8	V_{CC}	V
I_{CC}	Core supply current	Device configured for LVDS logic levels		18	20	mA
I_{CCOX}	Output supply current[a]	All outputs configured for LVDS logic levels; outputs unloaded		122	137	mA

[a] Internal dynamic switching current at maximum f_{OUT} is included.

Table 9. Typical Output Supply Current, V_{CCOA} = V_{CCOB} = 3.3V±5%, 2.5V±5% or 1.8V±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter[a]	Test Conditions[b]	V_{CCOx}[c] = 3.3V ±5%			V_{CCOx}[c] = 2.5V ±5%			V_{CCOx}[c] = 1.8V ±5%			V_{CCOx}[c] = 1.5V ±5%	Units
			LVDS	LVPECL	LVCMOS	LVDS	LVPECL	LVCMOS	LVDS	LVPECL	LVCMOS	LVCMOS	
I_{CCOB}	Bank B output supply current	All outputs enabled	77	52	46	76	51	27	69	46	25	21	mA
		2 outputs enabled	49	37	41	49	34	25	49	32	20	17	mA
		No outputs enabled	42	23	40	36	19	21	28	32	20	17	mA
I_{CCOA}	Bank A output supply current	All outputs enabled	77	52	46	76	51	27	69	46	25	21	mA
		2 outputs enabled	49	37	41	49	34	25	49	32	20	17	mA
		No outputs enabled	42	23	40	36	19	21	28	32	20	17	mA

[a] Internal dynamic switching current at maximum f_{OUT} is included.

[b] Tested with outputs unloaded.

[c] V_{CCOx} denotes V_{CCOA}, V_{CCOB}.

DC Electrical Characteristics

Table 10. Pin Characteristics

Symbol	Parameter		Test Conditions[a]	Minimum	Typical	Maximum	Units
C_{IN}	Input capacitance				2		pF
R_{PULLUP}	Input pull-up resistor				51		kΩ
$R_{PULLDOWN}$	Input pull-down resistor				51		kΩ
R_{OUT}	Output impedance	QA[3:0], nQA[3:0], QB[3:0], nQB[3:0]	LVCMOS output type selected V_{CCOx} = 3.3V ±5%		24		Ω
			LVCMOS output type selected V_{CCOx} = 2.5V ±5%		15		Ω
			LVCMOS output type selected V_{CCOx} = 1.8V ±5%		25		Ω
			LVCMOS output type selected V_{CCOx} = 1.5V ±5%		48		Ω
C_{PD}	Power dissipation capacitance (per output pair) QA[3:0], nQA[3:0], QB[3:0], nQB[3:0]	LVPECL	V_{CCOx} = 3.465V or 2.625V		4.2		pF
		LVDS					
		LVCMOS			5.8		pF
		LVPECL	V_{CCOx} = 1.89V		4.7		pF
		LVDS					
		LVCMOS	V_{CCOx} = 1.89V or 1.545V		5.2		pF

[a] V_{CCOx} refers to V_{CCOA} for QA[3:0], nQA[3:0], or V_{CCOB} for QB[3:0], nQB[3:0].

Table 11. LVCMOS/LVTTL Control / Status Signals DC Characteristics for 3-level Pins, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter	Signals	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input high voltage	IOA, IOB, CLK_SEL	V_{CC} = 3.3V	0.85 * V_{CC}		3.63	V
			V_{CC} = 2.5V	0.85 * V_{CC}		2.625	V
			V_{CC} = 1.8V	0.85 * V_{CC}		1.89	V
V_{IM}	Input middle voltage[a]	IOA, IOB, CLK_SEL	V_{CC} = 3.3V	0.45 * V_{CC}		0.55 * V_{CC}	V
			V_{CC} = 2.5V	0.45 * V_{CC}		0.55 * V_{CC}	V
			V_{CC} = 1.8V	0.45 * V_{CC}		0.55 * V_{CC}	V
V_{IL}	Input low voltage	OEA[1:0], OEB[1:0] IOA, IOB, CLK_SEL	V_{CC} = 3.3V	–0.3		0.15 * V_{CC}	V
			V_{CC} = 2.5V	–0.3		0.15 * V_{CC}	V
			V_{CC} = 1.8V	–0.3		0.15 * V_{CC}	V

Table 11. LVCMOS/LVTTL Control / Status Signals DC Characteristics for 3-level Pins, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter	Signals	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input high current	IOA, IOB, CLK_SEL	V_{CC} = V_{IN} = 3.465V or 2.625V or 1.89V			150	µA
I_{IM}	Input middle current	IOA, IOB, CLK_SEL	V_{CC} = 3.465V or 2.625V or 1.89V, V_{IN} = V_{CC} /2				µA
I_{IL}	Input low current	OEA[1:0], OEB[1:0] IOA, IOB, CLK_SEL	V_{CC} = 3.465V or 2.625V or 1.89V, V_{IN} = 0V	–150			µA

[a] For 3-level input pins, a mid-level voltage is used to select the 3rd state. This voltage will be maintained by a weak internal pull-up / pull-down network for each pin to select this state if the pin is left open. It is recommended that any external resistor networks used to select a middle-level input voltage be terminated to the device's core V_{CC} voltage level.

Table 12. LVCMOS/LVTTL Control / Status Signals DC Characteristics for 2-Level Pins, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter	Signals	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input high voltage	OEA[1:0], OEB[1:0]	V_{CC} = 3.3V	2		3.63	V
			V_{CC} = 2.5V	1.7		2.625	V
			V_{CC} = 1.8V	0.65 ∗ V_{CC}		1.89	V
V_{IL}	Input low voltage	OEA[1:0], OEB[1:0]	V_{CC} = 3.3V	–0.3		0.8	V
			V_{CC} = 2.5V	–0.3		0.7	V
			V_{CC} = 1.8V	–0.3		0.35 ∗ V_{CC}	V
I_{IH}	Input high current	OEA[1:0], OEB[1:0]	V_{CC} = V_{IN} = 3.465V or 2.625V or 1.89V			150	µA
I_{IL}	Input low current	OEA[1:0], OEB[1:0]	V_{CC} = V_{IN} = 3.465V or 2.625V or 1.89V	–150			µA

Table 13. Differential Input DC Characteristics, V_{CC} = 3.3V±5%, 2.5V±5% or 1.8V±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input high current	CLKx, nCLKx[a]	V_{CC} = V_{IN} = 3.465V or 2.625V			150	µA
I_{IL}	Input low current	CLKx[a]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	–5			µA
		nCLKx[a]	V_{CC} = 3.465V or 2.625V, V_{IN} = 0V	–150			µA
V_{PP}	Peak-to-peak voltage[b]			0.15		1.3	V
V_{CMR}	Common mode input voltage[b], [c]			V_{EE}		V_{CC} – 1.2	V

[a] CLKx denotes CLK0, CLK1. nCLKx denotes nCLK0, nCLK1.

[b] V_{IL} should not be less than –0.3V. V_{IH} should not be higher than V_{CC}.

[c] Common mode voltage is defined as the cross-point.

Table 14. LVPECL DC Characteristics, V_{CC} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, V_{EE} = 0V, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	Qx, nQx		V_{CCOX} - 1.3		V_{CCOX} - 0.8	mV
V_{OL}	Output Low Voltage	Qx, nQx		V_{CCOX} - 2.05		V_{CCOX} - 1.75	mV

Table 15. LVDS DC Characteristics, V_{CC} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, V_{CCOx}[a] = 3.3V ±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential output voltage	Qx, nQx[b]	Terminated 100Ω across Qx and nQx	247		465	mV
ΔV_{OD}	V_{OD} magnitude change	Qx, nQx[b]				50	mV
V_{OS}	Offset voltage	Qx, nQx[b]		1.1		1.375	V
ΔV_{OS}	V_{OS} magnitude change	Qx, nQx[b]				50	mV

[a] V_{CCOx} denotes V_{CCOA}, V_{CCOB}.

[b] Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.
nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Table 16. LVDS DC Characteristics, V_{CC} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, V_{CCOx}[a] = 2.5V ±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential output voltage	Qx, nQx[b]	Terminated 100Ω across Qx and nQx	247		465	mV
ΔV_{OD}	V_{OD} magnitude change	Qx, nQx[b]				50	mV
V_{OS}	Offset voltage	Qx, nQx[b]		1.1		1.375	V
ΔV_{OS}	V_{OS} magnitude change	Qx, nQx[b]				50	mV

[a] V_{CCOx} denotes V_{CCOA}, V_{CCOB}.

[b] Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.
nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Table 17. LVDS DC Characteristics, V_{CC} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, V_{CCOx}[a] = 1.8V ±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential output voltage	Qx, nQx[b]	Terminated 100Ω across Qx and nQx	247		454	mV
ΔV_{OD}	V_{OD} magnitude change	Qx, nQx[b]				50	mV
V_{OS}	Offset voltage	Qx, nQx[b]		1.1		1.375	V
ΔV_{OS}	V_{OS} magnitude change	Qx, nQx[b]				50	mV

[a] V_{CCOx} denotes V_{CCOA}, V_{CCOB}.

[b] Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3.
nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Table 18. LVCMOS Clock Outputs DC Characteristics, V_{CCOx}[a] = 3.3V±5%, 2.5V±5% or 1.8V±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter	Test Conditions	V_{CCOx}[a] = 3.3V ±5%			V_{CCOx}[a] = 2.5V ±5%			V_{CCOx}[a] = 1.8V ±5%			V_{CCOx}[a] = 1.5V ±5%			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output high voltage Qx, nQx[b]	I_{OH} = –8mA	2.4			1.8			V_{CC} – 0.45			V_{CC} – 0.38			V
V_{OL}	Output low voltage Qx, nQx[b]	I_{OL} = 8mA			0.8			0.6			0.45			0.38	V

[a] V_{CCOx} denotes V_{CCOA}, V_{CCOB}.

[b] Qx denotes QA0, QA1, QA2, QA3, QB0, QB1, QB2, QB3. nQx denotes nQA0, nQA1, nQA2, nQA3, nQB0, nQB1, nQB2, nQB3.

Table 19. Input Frequency Characteristics, V_{CC} = 3.3V±5%, 2.5V±5% or 1.8V±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	CLKx, nCLKx[a]		1Hz		700MHz	
idc	Input duty cycle[b]				50		%

[a] CLKx denotes CLK0, CLK1. nCLKx denotes nCLK0, nCLK1.

[b] Any deviation from a 50% / 50% duty cycle on the input may be reflected in the output duty cycle.

AC Electrical Characteristics

Table 20. AC Characteristics, V_{CC} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, V_{CCOx}[a] = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter[b]		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output frequency	LVDS, LVPECL		1PPS		700MHz	
f_{OUT}	Output frequency	LVCMOS		1PPS		125MHz	
t_{PD}	Propagation delay	LVCMOS	V_{DDOx} = 3.3V ±5%	1.25		2.25	ns
		LVDS		0.85		2.0	ns
		LVPECL		0.85		2.0	ns
t_R / t_F	Output rise and fall times	LVPECL	20% to 80%	125		700	ps
		LVDS	20% to 80%, V_{CCOx} = 3.3V	150		550	ps
			20% to 80%, V_{CCOx} = 2.5V	175		575	ps
			20% to 80%, V_{CCOx} = 1.8V	200		600	ps
		LVCMOS	20% to 80%, V_{CCOx} = 3.3V	250		775	ps
			20% to 80%, V_{CCOx} = 2.5V	200		915	ps
			20% to 80%, V_{CCOx} = 1.8V	300		950	ps
			20% to 80%, V_{CCOx} = 1.5V	200		1400	ps
t_{sk}(b)	Bank skew[c], [d], [e]	LVPECL, LVDS[f]				60	ps
		LVCMOS[g]				100	ps
t_{sk}(out)	Output Skew[c], [d], [j]	LVPECL[f]	V_{CCOx} = 3.3V ± 5%			65	ps
			V_{CCOx} = 2.5V ± 5%			62	ps
			V_{CCOx} = 1.8V ± 5%			62	ps
		LVDS[f]	V_{CCOx} = 3.3V ± 5%			45	ps
			V_{CCOx} = 2.5V ± 5%			45	ps
			V_{CCOx} = 1.8V ± 5%			35	ps
		LVCMOS[g]	V_{CCOx} = 3.3V ± 5%			90	ps
			V_{CCOx} = 2.5V ± 5%			100	ps
			V_{CCOx} = 1.8V ± 5%			95	ps
t_{sk}(pp)	Part-to-Part Skew[c]	LVPECL[k]	V_{CCOx} = 3.3V ± 5%			380	ps
			V_{CCOx} = 2.5V ± 5%				
			V_{CCOx} = 1.8V ± 5%				
		LVDS[k]	V_{CCOx} = 3.3V ± 5%			325	ps
			V_{CCOx} = 2.5V ± 5%				
			V_{CCOx} = 1.8V ± 5%				
		LVCMOS[l]	V_{CCOx} = 3.3V ± 5%			590	ps
			V_{CCOx} = 2.5V ± 5%				
			V_{CCOx} = 1.8V ± 5%				

Table 20. AC Characteristics, V_{CC} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, V_{CCOx}[a] = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter[b]		Test Conditions	Minimum	Typical	Maximum	Units
odc	Output duty cycle[h], [i]	LVPECL, LVDS	V_{CCOx} = 3.3V or 2.5V	45		55	%
		LVPECL, LVDS	V_{CCOx} = 1.8V	43		57	%
		LVCMOS	V_{CCOx} = 3.3V or 2.5V	45		55	
			V_{CCOx} = 1.8V	43		57	%
			V_{CCOx} = 1.5V	40		60	
MUX_{ISOL}	Mux Isolation				70		dB
	Noise Floor	LVPECL, LVDS	Offset >10MHz from156.25MHz carrier		157		dBc/Hz

[a] V_{CCOx} denotes V_{CCOA}, V_{CCOB}.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] This parameter is guaranteed by characterization. Not tested in production.

[d] This parameter is defined in accordance with JEDEC Standard 65.

[e] Defined as skew within a bank of outputs at the same supply voltage and with equal load conditions.

[f] Measured at the output differential crosspoint.

[g] Measured at V_{CCOx}/2 of the rising edge.

[h] Measured using 50% /50% duty cycle on input reference.

[i] Measurements taken for the following output frequencies:
LVDS and LVPECL: 50MHz, 100MHz, 156.25MHz, 250MHz, 312.5MHz, 491.52MHz, 700MHz
LVCMOS: 25MHz, 50MHz, 100MHz, 125MHz.

[j] Defined as skew between outputs at the same supply voltage and with equal load conditions.

[k] Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

[l] Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at $V_{CCOx / 2}$.

Table 21. Typical Additive Jitter, V_{CC} = 3.3V ±5%, 2.5V ±5% or 1.8V ±5%, V_{CCOx}[a] = 3.3V ±5%, 2.5V ±5%, 1.8V ±5% or 1.5V ±5% (1.5V only supported for LVCMOS outputs), V_{EE} = 0V, T_A = –40°C to 85°C

Symbol	Parameter		Test Conditions[b]		Minimum	Typical	Maximum	Units
$t_{jit}(f)$	RMS Additive Jitter (Random)	LVPECL	f_{OUT} = 156.25MHz, Integration Range: 12kHz to 20MHz	V_{CCOx} = 3.3V or 2.5V		64		fs
				V_{CCOx} = 1.8V		81		fs
		LVDS	f_{OUT} = 156.25MHz, Integration Range: 12kHz to 20MHz	V_{CCOx} = 3.3V or 2.5V		70		fs
				V_{CCOx} = 1.8V		114		fs
		LVCMOS	f_{OUT} = 125MHz, Integration Range: 12kHz to 20MHz	V_{CCOx} = 3.3V or 2.5V		105		fs
				V_{CCOx} = 1.8V		140		fs
				V_{CCOx} = 1.5V		192		fs

[a] V_{CCOx} denotes V_{CCOA}, V_{CCOB}.

[b] All outputs configured for the specific output type, as shown in the table.

Applications Information

Recommendations for Unused Input and Output Pins

Inputs

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS LVTTL Level Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

LVCMOS 3-level I/O Control Pins

These pins are 3-level pins and if left unconnected this is interpreted as a valid input selection option (Middle).

Outputs

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. It is recommended that there is no trace attached.

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

LVDS Outputs

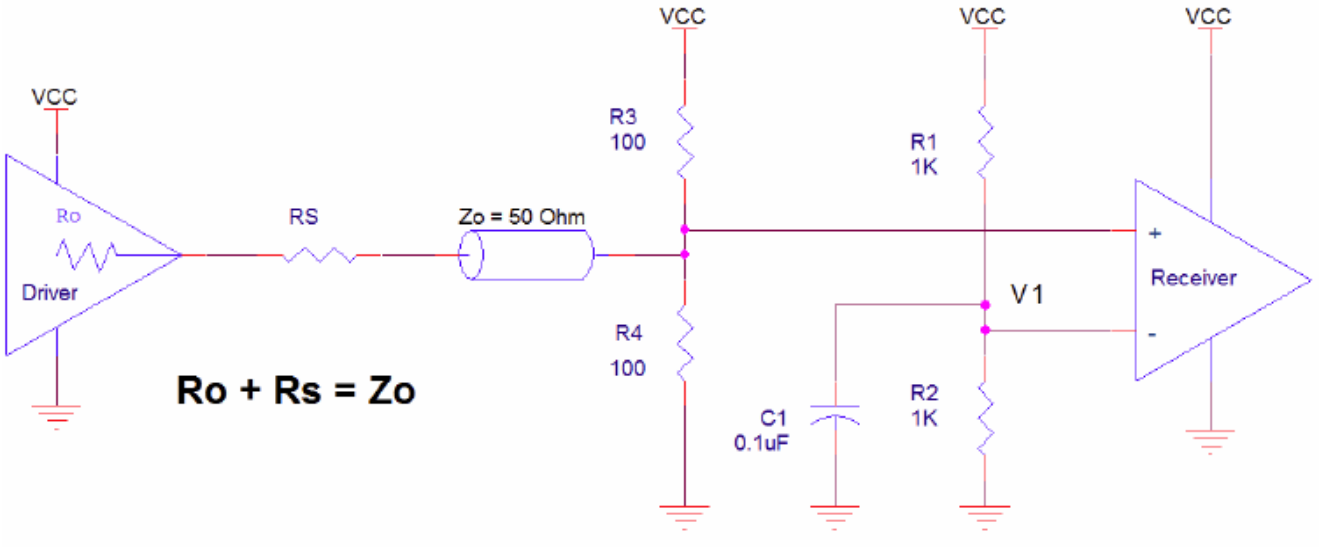
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Wiring the Differential Input to Accept Single-ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half.

This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than –0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figure 3 *to* Figure 7 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3, the input termination applies for Renesas open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

Figure 3. CLKx/nCLKx Input Driven by a Renesas Open Emitter LVHSTL Driver

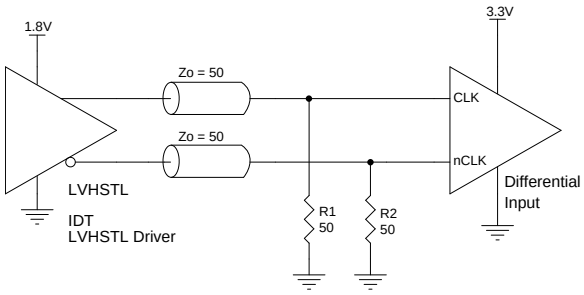


Figure 4. CLKx/nCLKx Input Driven by a 3.3V LVPECL Driver

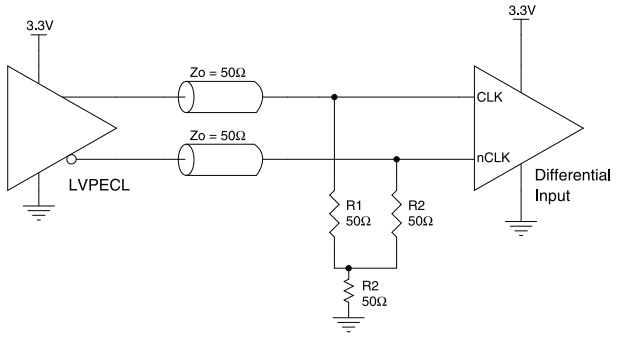


Figure 5. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

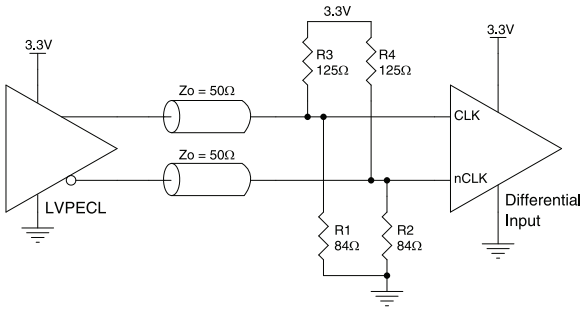


Figure 6. CLK/nCLK Input Driven by a 3.3V HCSL Driver

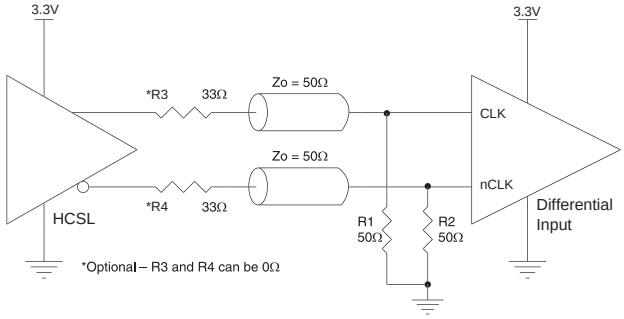
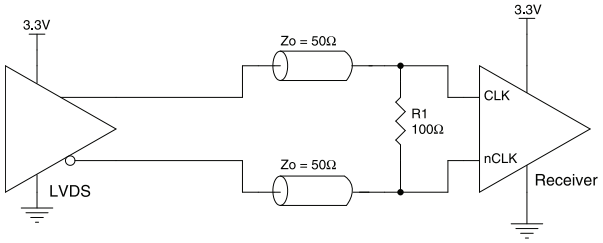


Figure 7. CLK/nCLK Input Driven by a 3.3V LVDS Driver



2.5V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figure 8 *to* Figure 12 show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 8, the input termination applies for Renesas open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

Figure 8. CLKx/nCLKx Input Driven by a Renesas Open Emitter LVHSTL Driver

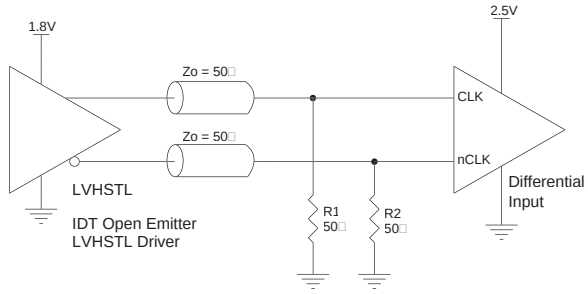


Figure 9. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

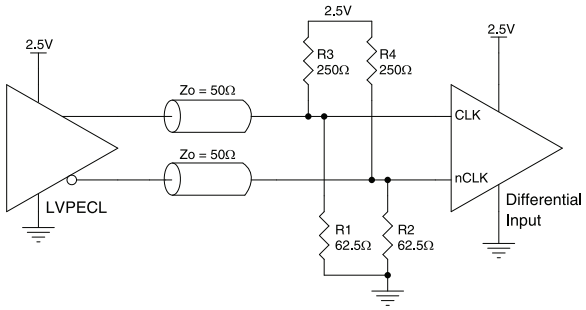


Figure 10. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

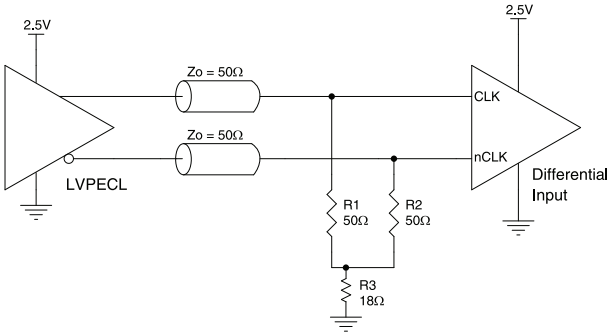


Figure 11. CLK/nCLK Input Driven by a 2.5V LVDS Driver

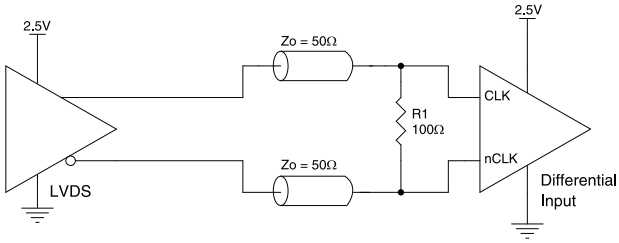
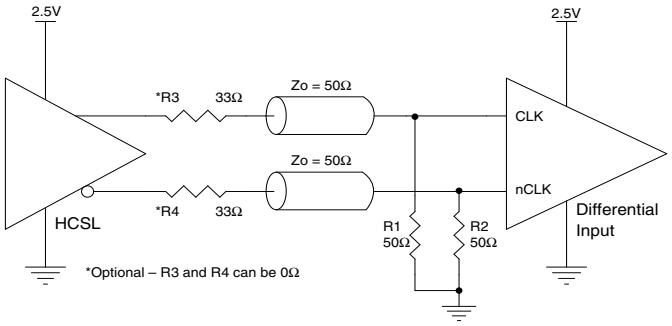


Figure 12. CLK/nCLK Input Driven by a 2.5V HCSL Driver



LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source.

The standard termination schematic as shown in Figure 13 can be used with either type of output structure. Figure 14, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 13. Standard LVDS Termination

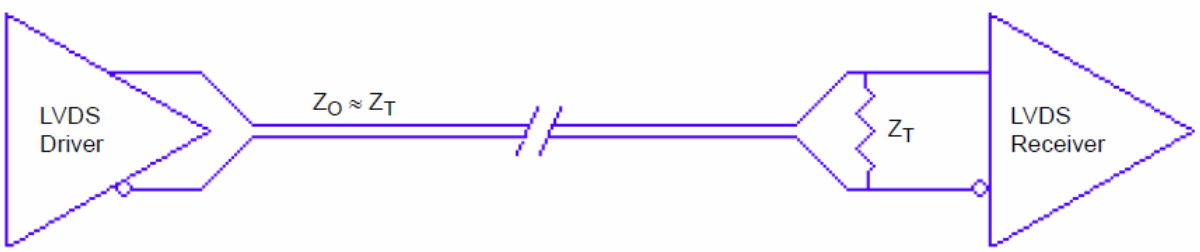
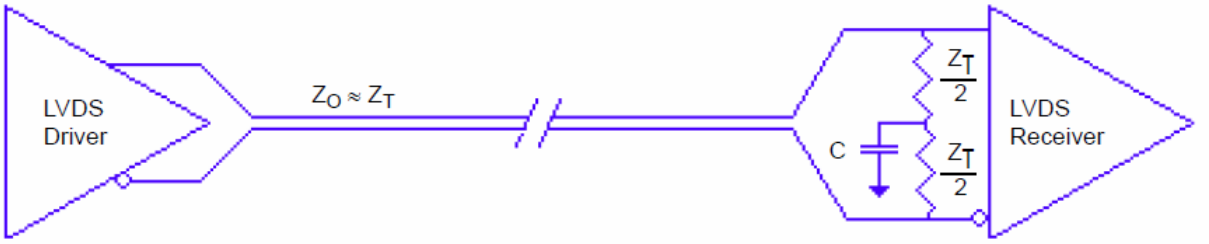


Figure 14. Optional LVDS Termination



Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figure 15 and Figure 16 show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

Figure 15. 3.3V LVPECL Output Termination

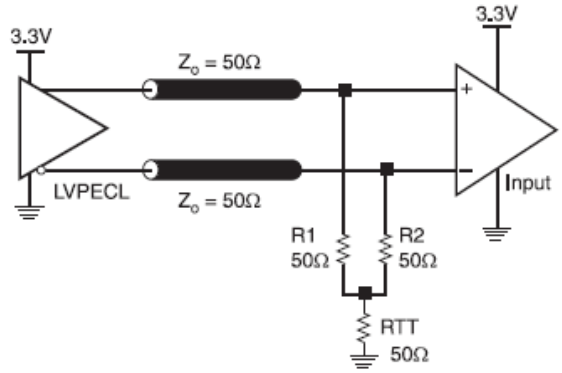
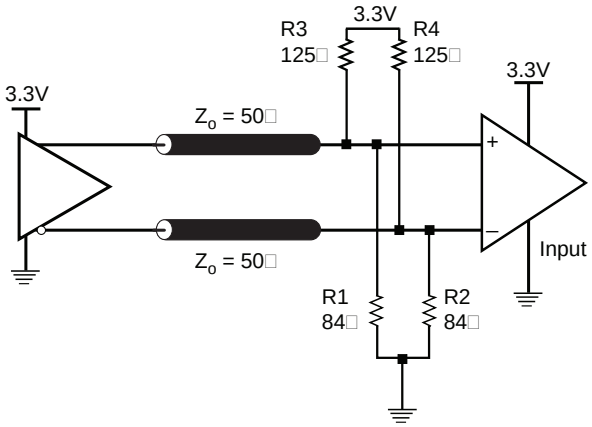


Figure 16. 3.3V LVPECL Output Termination



Termination for 2.5V LVPECL Outputs

Figure 17 and Figure 18 show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 18 can be eliminated and the termination is shown in Figure 19.

Figure 17. 2.5V LVPECL Driver Termination Example

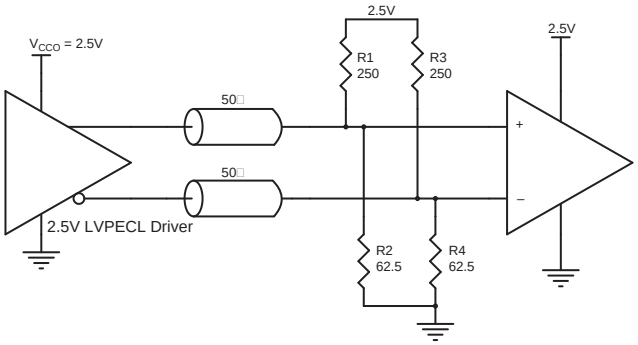


Figure 18. 2.5V LVPECL Driver Termination Example

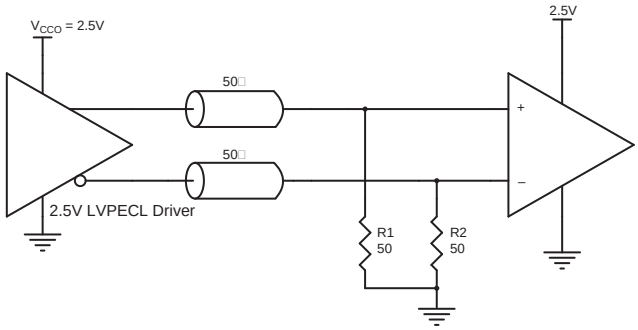
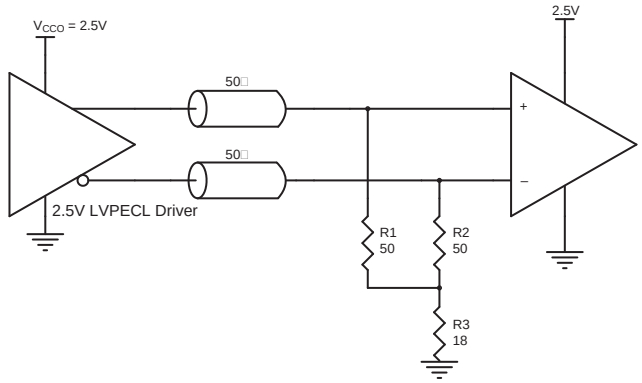


Figure 19. 2.5V LVPECL Driver Termination Example



Power Dissipation and Thermal Considerations

The 8P791208 is a multi-functional, high speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled.

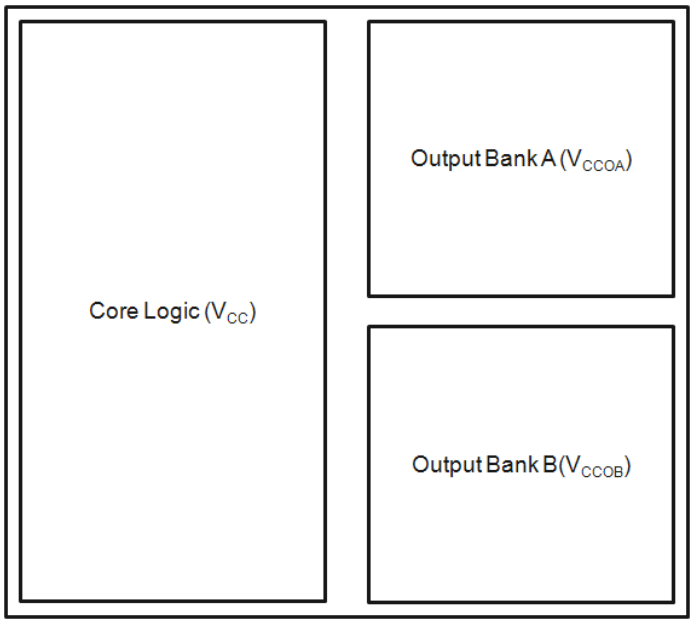
The 8P791208 device was designed and characterized to operate within the ambient industrial temperature range of T_A = -40°C to 85°C. The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature.

The power calculation examples below were generated using a maximum ambient temperature and supply voltage. For many applications, the power consumption will be much lower. Please contact Renesas technical support for any concerns on calculating the power dissipation for your own specific configuration.

Power Domains

The 8P791208 device has a number of separate power domains that can be independently enabled and disabled via register accesses (all power supply pins must still be connected to a valid supply voltage). Figure 20 indicates the individual domains and the associated power pins.

Figure 20. 8P791208 Power Domains



Power Consumption Calculation

Determining total power consumption involves several steps:

1. Determine the power consumption using maximum current values for core voltage from Table 6 to Table 9 for the appropriate case of how many banks or outputs are enabled.
2. Determine the nominal power consumption of each enabled output path.
   a. This consists of a base amount of power that is independent of operating frequency, as shown in Table 22 to Table 28 (depending on the chosen output protocol).
   b. Then there is a variable amount of power that is related to the output frequency. This can be determined by multiplying the output frequency by the FQ_Factor shown in Table 22 to Table 28.
3. All of the above totals are then summed.

Thermal Considerations

Once the total power consumption has been determined, it is necessary to calculate the maximum operating junction temperature for the device under the environmental conditions it will operate in. Thermal conduction paths, air flow rate and ambient air temperature are factors that can affect this. The thermal conduction path refers to whether heat is to be conducted away via a heat-sink, via airflow or via conduction into the PCB through the device pads (including the ePAD). Thermal conduction data is provided for typical scenarios in Table 30. Please contact Renesas for assistance in calculating results under other scenarios.

Current Consumption Data and Equations

Table 22. 3.3V LVDS Output Calculation Table

LVDS	FQ_Factor (mA/MHz)	Base_Current (mA)
Bank A	0.08	25.309
Bank B	0.08	25.309

Table 23. 2.5V LVDS Output Calculation Table

LVDS	FQ_Factor (mA/MHz)	Base_Current (mA)
Bank A	0.05	35.476
Bank B	0.05	35.476

Table 24. 1.8V LVDS Output Calculation Table

LVDS	FQ_Factor (mA/MHz)	Base_Current (mA)
Bank A	0.05	35.330
Bank B	0.05	35.330

Table 25. 3.3V LVCMOS Output Calculation Table

LVCMOS	Base_Current (mA)
Bank A	31.522
Bank B	31.522

Table 26. 2.5V LVCMOS Output Calculation Table

LVCMOS	Base_Current (mA)
Bank A	18.665
Bank B	18.665

Table 27. 1.8V LVCMOS Output Calculation Table

LVCMOS	Base_Current (mA)
Bank A	14.704
Bank B	14.704

Table 28. 1.5V LVCMOS Output Calculation Table

LVCMOS	Base_Current (mA)
Bank A	12.522
Bank B	12.522

Applying the values to the following equation will yield output current by frequency:

Qx Current (mA) = FQ_Factor * Frequency (MHz) + Base_Current

where:
Qx Current is the specific output current according to output type and frequency
FQ_Factor is used for calculating current increase due to output frequency
Base_Current is the base current for each output path independent of output frequency

The second step is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient, using the following equation:

$T_J = T_A + (\theta_{JA} * Pd_{total})$

where:
T_J is the junction temperature (°C)
T_A is the ambient temperature (°C)
θ_{JA} is the thermal resistance value from Table 30, dependent on ambient airflow (°C/W).

Pd_{total} is the total power dissipation of the 8P791208 under usage conditions, including power dissipated due to loading (W).

Note: For LVPECL outputs the power dissipation through the load is assumed to be 27.95mW. When selecting LVCMOS outputs, power dissipation through the load will vary based on a variety of factors including termination type and trace length. For these examples, power dissipation through loading will be calculated using C_{PD} (located in Table 10) and output frequency:

$Pd_{OUT} = C_{PD} * f_{OUT} * V_{CCO}^2$

where:
Pd_{out} is the power dissipation of the output (W)
C_{PD} is the power dissipation capacitance (pF)
f_{OUT} is the output frequency of the selected output (MHz)
V_{CCO} is the voltage supplied to the appropriate output (V)

Example Calculations

Table 29. Example 1 – Common Customer Configuration (3.3V Core Voltage)

Circuit	Configuration	Frequency (MHz)	V_{CCO}
Bank A	LVDS	125	3.3V
Bank B	LVDS		3.3V

Core supply current, I_{CC} = 25mA (maximum)

- Output supply current, Bank A current = 0.08mA x 125MHz + 30mA = 40mA
- Output supply current, Bank B current = 0.08mA x 125MHz + 30mA = 40mA

Total device current = 25mA + 40mA + 40mA = 105mA

Total device power = 3.465V * 105mA = 363.825mW or 0.364W

With an ambient temperature of 85°C and no airflow, the junction temperature is:

- T_J = 85°C + 35.23°C/W * 0.364W = 97.82°C

LVPECL Power Considerations (700MHz)

This section provides information on power dissipation and junction temperature for the 8P791208.
Equations and example calculations are also provided.

4. Power Dissipation.

The total power dissipation for the 8P791208 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

Note: I_{EE_MAX} @ 85°C is 124mA

For information on calculating power dissipated in the load, see Calculations and Equations.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 124mA = **429.66mW**
- Power $(outputs)_{MAX}$ = **27.95mW/Loaded Output pair**
  If all outputs are loaded, the total power is 8 * 27.95mW = **223.6mW**
- **Total Power**$_{MAX}$ = 429.66W + 223.6mW = **653.26mW**

5. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 35.23°C/W per Table 30.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.653W * 35.23°C/W = 108°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

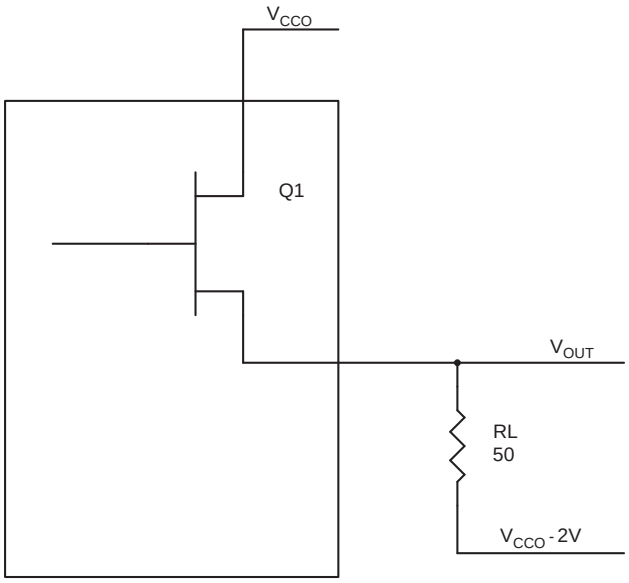
Table 30. Thermal Resistance θ_{JA} for 32-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	35.23°C/W	31.6°C/W	30.0°C/W

6. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair. LVPECL output driver circuit and termination are shown in Figure 21.

Figure 21. LVPECL Driver Circuit and Termination



To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX}} - \mathbf{0.8V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.8V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX}} - \mathbf{1.75V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.75V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OH\_MAX}) = [(2V – 0.8V)/50Ω] * 0.8V =$ **19.2mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} – 2V))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CCO\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} – V_{OL\_MAX}) = [(2V – 1.75V)/50Ω] * 1.75V =$ **8.75mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **27.95mW**

LVDS Power Considerations (700MHz)

This section provides information on power dissipation and junction temperature for the 8P791208.
Equations and example calculations are also provided.

7. Power Dissipation.

The total power dissipation for the 8P791208 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{CC\_MAX}$ = 3.465V * 25mA = **86.625mW**
- Power $(outputs)_{MAX} = V_{CCOx\_MAX} * I_{CCO\_MAX}$ = 3.465V * 153mA = **530.145mW**
- **Total Power**$_{\_MAX}$ = 86.625W + 530.145mW = **616.77mW**

8. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 35.23°C/W per Table 30.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.617W * 35.23°C/W = 107°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

LVCMOS Power Considerations (125MHz)

This section provides information on power dissipation and junction temperature for the 8P791208.
Equations and example calculations are also provided.

9. Power Dissipation.

The total power dissipation for the 8P791208 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{CC\_MAX}$ = 3.465V * 63mA = **217.81mW**

Dynamic Power Dissipation at $f_{OUT(max)}$

Total Power:

Total Power (F_{OUT_MAX}) = [(C_{PD} * N) * Frequency * $(V_{CCO})^2$] = [(0.58pF * 2) * 125MHz * $(3.456V)^2$] = 13.92722mW per output

N = number of outputs

Dynamic Power Dissipation:

= Static Power + Dynamic Power Dissipation

= 217.81mW + 13.927mW

= 231.737mW

10. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 35.23°C/W per Table 30.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.232W * 35.23°C/W = 93.27°C. This is below the limit of 125°C.

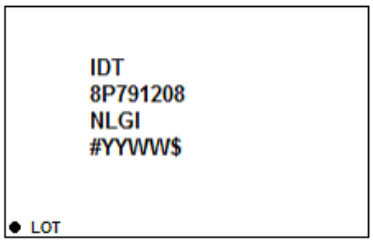
This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.renesas.com/us/en/document/psc/package-outline-drawing-package-code-nlg32p1-32-vfqfpn-50-x-50-x-09-mm-body-05-mm-pitch

Marking Diagram

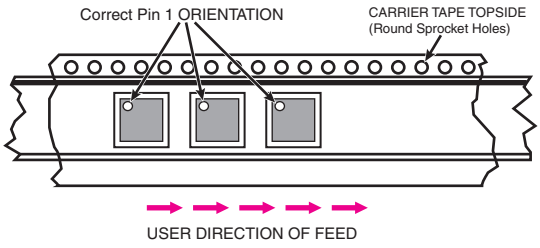
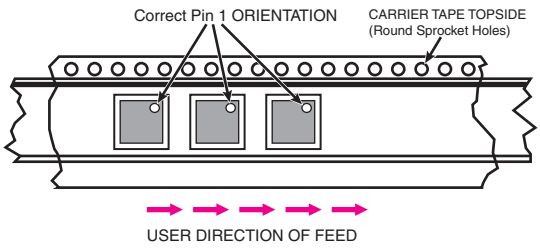


1. IDT
2. Line 2 and line 3 indicates the part number.
3. Line 3:
   - "#" indicates stepping.
   - "YYWW" indicates the date code (YY are the last two digits of the year, and "WW" is a work week number that the part was assembled.
   - "$" indicates the mark code.

Ordering Information

Orderable Part Number	Marking	Package	Carrier Type	Temperature
8P791208NLGI	IDT8P791208NLGI	32-lead VFQFN, Lead Free	Tray	-40°C to 85°C
8P791208NLGI8	IDT8P791208NLGI	32-lead VFQFN, Lead Free	Tape and Reel, Pin 1 Orientation: EIA-481-C	-40°C to 85°C
8P791208NLGI/W	IDT8P791208NLGI	32-lead VFQFN, Lead Free	Tape and Reel, Pin 1 Orientation: EIA-481-D	-40°C to 85°C

Table 31. Pin 1 Orientation in Tape and Reel Packaging

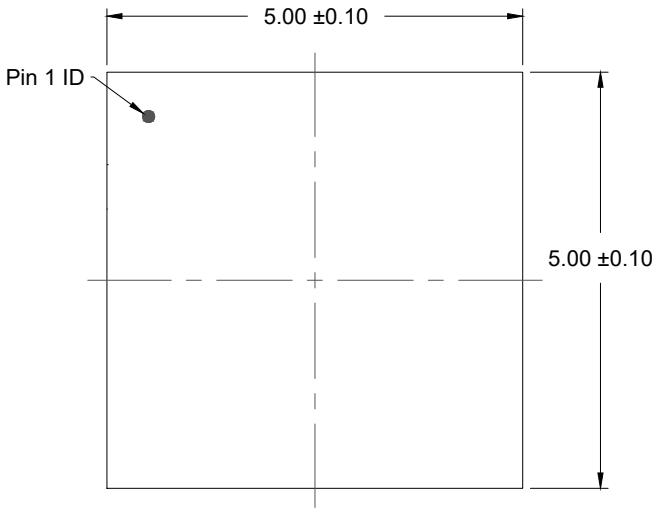
Part Number Suffix	Pin 1 Orientation	Illustration
NLGI8	Quadrant 1 (EIA-481-C)	
NLGI/W	Quadrant 2 (EIA-481-D)	

Revision History

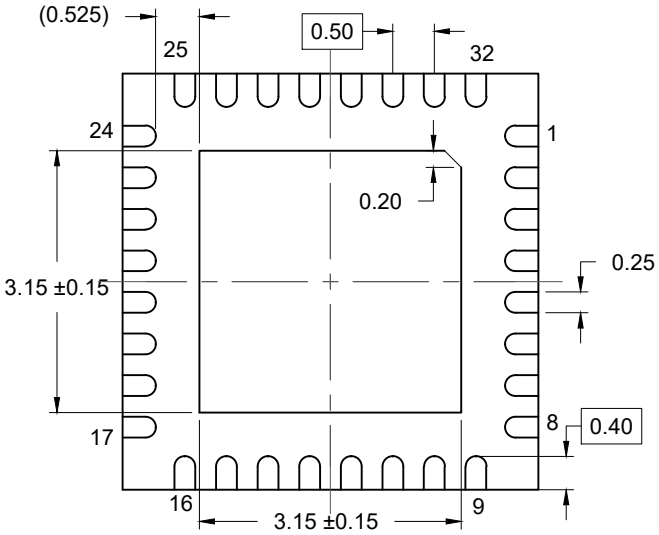
Date	Description of Change
January 31, 2023	Updated POD link in Package Outline Drawings.
September 21, 2020	▪ Corrected description typos in Figure 6 and Figure 7 titles.
June 2, 2020	▪ Reformatted document headers and footers. ▪ Updated AC Electrical Characteristics table with Output Skew and Part-to-Part Skew parameters.
May 8, 2018	▪ Updated the propagation delay minimum and maximum numbers for LVCMOS in Table 20 ▪ Updated the Package Outline Drawings; however, no technical changes
November 5, 2017	▪ Added t_{PD} symbol to Table 20
August 23, 2017	▪ Added Table 14 ▪ Updated the package outline drawings. No mechanical changes.
November 28, 2016	Initial release.

Package Outline Drawing

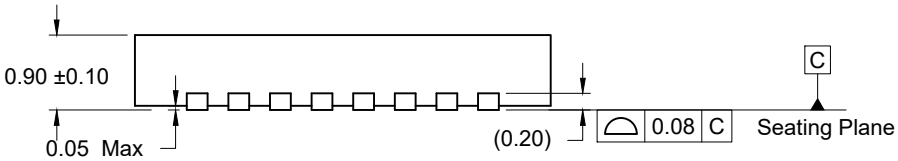
Package Code:NLG32P1
32-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4171-01, Revision: 04, Date Created: Aug 15, 2022



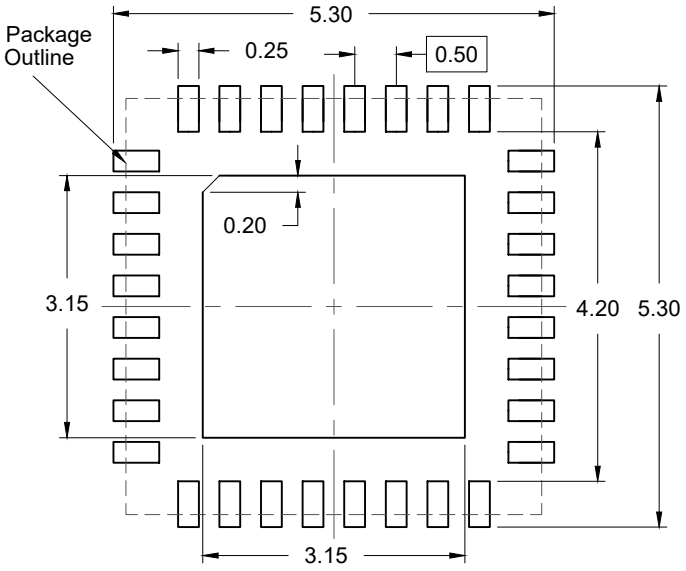
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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