Description

The 8V19N472 is a fully integrated FemtoClock NG Jitter Attenuator and Clock Synthesizer designed as a high-performance clock solution for conditioning and frequency/phase management of wireless base station radio equipment boards. The device is optimized to deliver excellent phase noise performance as required in GSM, WCDMA, LTE, and LTE-A radio board implementations.

A two-stage PLL architecture supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator and uses an external VCXO for best possible phase noise characteristics. The second stage PLL locks on the VCXO-PLL output signal and synthesizes the target frequency. This PLL has two VCO circuits at 2949.12MHz and 2400–2500MHz, respectively, for enhanced frequency flexibility.

The device generates the output clock signals from the selected VCO by frequency division. Five independent frequency dividers are available, four support integer-divider ratios and one integer as well as fractional-divider ratios. Delay circuits can be used for achieving alignment and controlled phase delay between clock signals. The two redundant inputs are monitored for activity. Four selectable clock switching modes are provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers, and phase adjustment capabilities are added for flexibility.

The 8V19N472 is configured through an SPI interface and reports lock and signal loss status in internal registers and via a lock detect (LOCK) output. Internal status bit changes can also be reported via the nINT output. The device is ideal for driving converter circuits in wireless infrastructure, radar/imaging, and instrumentation/medical applications. The device is a member of the high-performance clock family from IDT.

Typical Applications

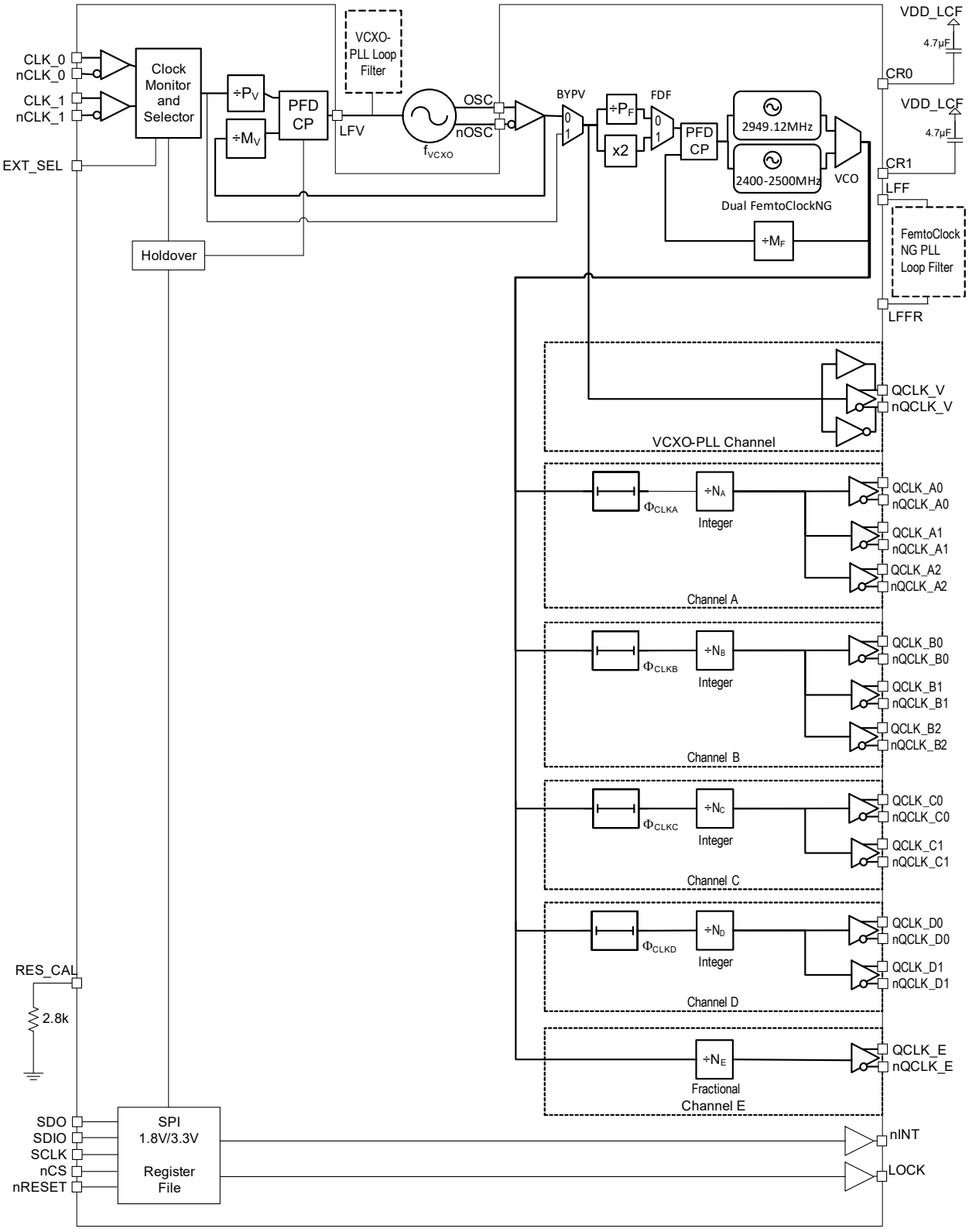
- Low-phase noise clock generation, specifically for jitter-sensitive ADC and DAC circuits
- Wireless infrastructure applications: GSM, WCDMA, LTE, LTE-A
- Ethernet

Features

- High-performance clock RF-PLL
- Optimized for low phase noise: <-150dBc/Hz (1MHz offset; 245.76MHz clock)
- Dual-PLL architecture
  - 1st-PLL stage with external VCXO for clock jitter attenuation
  - 2nd-PLL stage with internal FemtoClockNG PLL at selectable 2949.12MHz and MHz (2400–2500MHz) VCO frequency
- Six output banks with a total of 12 outputs, organized in:
  - Two clock banks with one integer frequency divider and three differential outputs
  - Two clock banks with one integer frequency divider and two differential outputs
  - One clock bank with one fractional output divider and one differential output
  - One VCXO-PLL output bank with one selectable LVDS/two LVCMOS outputs
- Supported clock output frequencies include:
  - From VCO-0: 2949.12, 1474.56, 983.04, 491.52, 368.64, 122.88MHz
  - From VCO-1: 2457.6, 1228.8, 614.4, 307.2, 153.6, 76.8MHz
  - From the fractional output divider: 80 – 300MHz
- Clock channels with integer output divider contain a phase delay circuit with 512 steps of half of the selected VCO period
- Low-power LVPECL/LVDS outputs support configurable signal amplitude, DC and AC coupling and LVPECL, LVDS line terminations techniques
- Redundant input clock architecture
  - Two inputs with an individual input signal monitor
  - Digital holdover
  - Manual and automatic clock selection
  - Hitless switching
- Status monitoring and fault reporting
  - Input signal status
  - Hold-over and reference loss status
  - Lock status with one status pin
  - Maskable status interrupt pin
- Voltage supply:
  - Device core supply voltage: 3.3V
  - Output supply voltage: 3.3V, 2.5V, or 1.8V
  - SPI control I/O voltage: 1.8V or 3.3V (selectable), 3.3V tolerant inputs when set to 1.8V
- Package: 81-FPBGA (8 × 8mm, 0.8 mm ball pitch)
- Temperature range: -40°C to +85°C

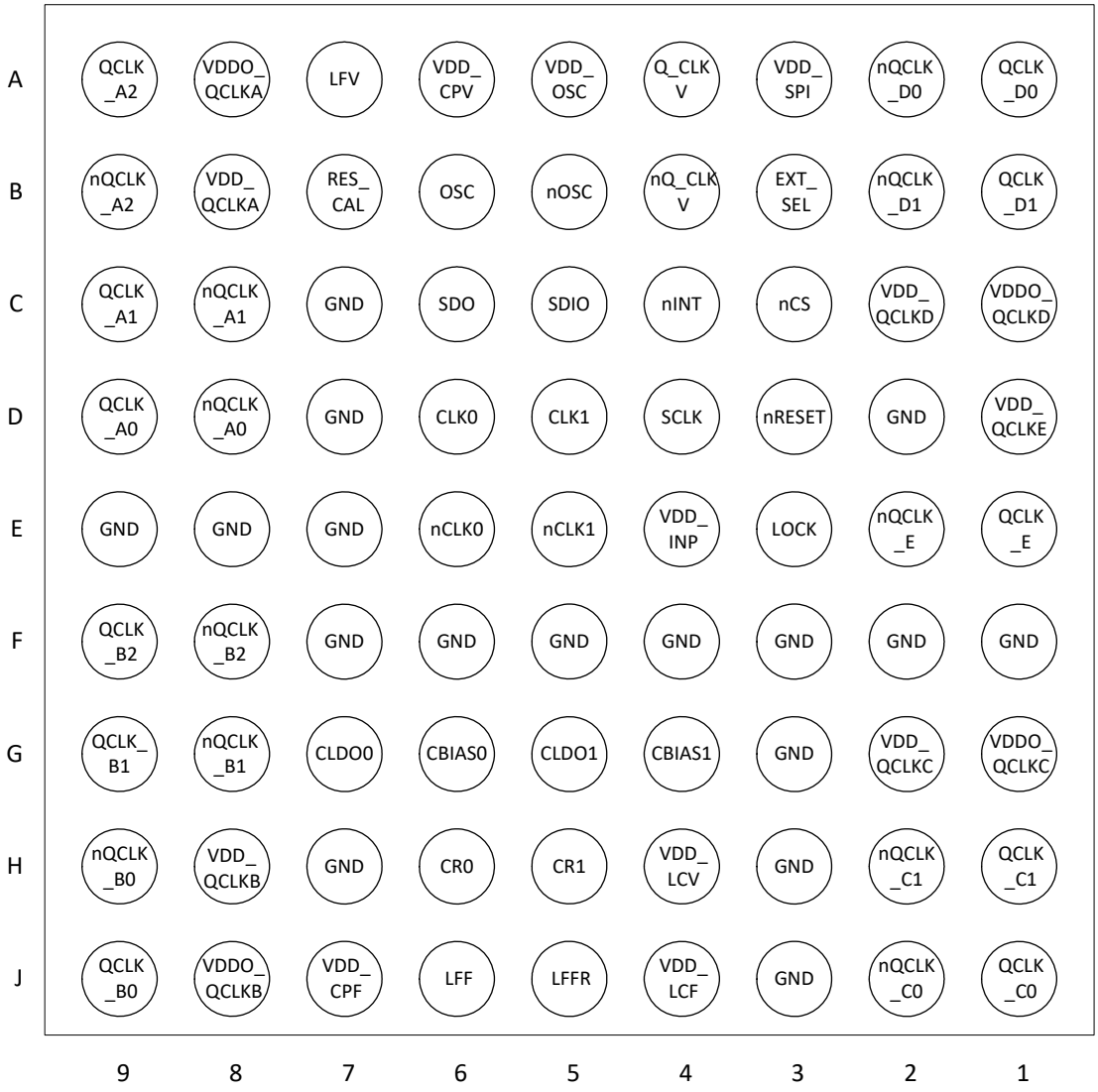
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Ball Map for 8mm × 8mm × 1.35mm, 81-FPBGA Package with 0.8mm Ball Pitch – Bottom View



Pin Descriptions

Table 1. Pin Descriptions[a]

Ball Number	Name	Type[b]		Description
D6	CLK_0	Input	PD	Device clock 0 inverting and non-inverting differential clock input. Inverting input is biased to V_{DD_V}/2 by default when left floating. Compatible with LVPECL, LVDS, and LVCMOS signals.
E6	nCLK_0		PD/PU	
D5	CLK_1	Input	PD	Device clock 1 inverting and non-inverting differential clock input. Inverting input is biased to V_{DD_V}/2 by default when left floating. Compatible with LVPECL, LVDS, and LVCMOS signals.
E5	nCLK_1		PD/PU	
B3	EXT_SEL	Input	PD	Clock reference select. 1.8V LVCMOS interface levels.
D9, D8	QCLK_A0, nQCLK_A0	Output		Differential clock output A0 (Channel A). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKA supply voltage.
C9, C8	QCLK_A1, nQCLK_A1	Output		Differential clock output A1 (Channel A). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKA supply voltage.
A9, B9	QCLK_A2, nQCLK_A2	Output		Differential clock output A2 (Channel A). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKA supply voltage.
J9, H9	QCLK_B0, nQCLK_B0	Output		Differential clock output B0 (Channel B). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKB supply voltage.
G9, G8	QCLK_B1, nQCLK_B1	Output		Differential clock output B1 (Channel B). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKB supply voltage.
F9, F8	QCLK_B2, nQCLK_B2	Output		Differential clock output B2 (Channel B). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKB supply voltage.
J1, J2	QCLK_C0, nQCLK_C0	Output		Differential clock output C0 (Channel C). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKC supply voltage.
H1, H2	QCLK_C1, nQCLK_C1	Output		Differential clock output C1 (Channel C). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKC supply voltage.
A1, A2	QCLK_D0, nQCLK_D0	Output		Differential clock output D0 (Channel D). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKD supply voltage.
B1, B2	QCLK_D1, nQCLK_D1	Output		Differential clock output D1 (Channel D). Configurable LVPECL/LVDS style and amplitude. Output levels are determined by the VDDO_QCLKD supply voltage.
E1, E2	QCLK_E, nQCLK_E	Output		Differential clock output E (Channel E). Configurable LVPECL/LVDS style and amplitude. Output is supplied by 3.3V (VDD_QCLKE)

Table 1. Pin Descriptions[a] (Cont.)

Ball Number	Name	Type[b]		Description
A4, B4	QCLK_V, nQCLK_V	Output		Differential VCXO-PLL clock outputs. Selectable LVPECL/LVDS/(2x LVCMOS 1.8V) style.
C4	nINT	Output		Status output pin for signaling internal changed conditions. Selectable 1.8V/3.3V LVCMOS interface levels.
E3	LOCK	Output		PLL lock detect status output for both PLLs. Selectable 1.8V/3.3V LVCMOS interface levels.
C5	SDIO	Input/Output		Serial Control Port SPI Mode Clock Input/Output. Selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.
C6	SDO	Output		Serial Control Port SPI Mode Output. Selectable 1.8V/3.3V LVCMOS interface levels.
D4	SCLK	Input	PD	Serial Control Port SPI Clock. Selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.
C3	nCS	Input	PU	Serial Control Port SPI Chip Select Input. 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.
D3	nRESET	Input	PU	SPI interface reset. Selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.
H6	CR0	Analog		Internal VCO (0) regulator bypass capacitor. Use a 4.7 µF capacitor between the CR0 and the VDD_LCF terminals.
H5	CR1	Analog		Internal VCO (1) regulator bypass capacitor. Use a 4.7 µF capacitor between the CR1 and the VDD_LCF terminals.
A7	LFV	Output		VCXO-PLL charge pump output. Connect to the loop filter for the external VCXO.
B6	OSC	Input	PD	VCXO non-inverting and inverting differential clock input. Compatible with LVPECL, LVDS, and LVCMOS signals.
B5	nOSC		PD/PU	
J6	LFF	Output		Loop filter/charge pump output for the FemtoClock NG PLL. Connect to the external loop filter.
J5	LFFR	Analog		Ground return path pin for the VCO loop filter.
B7	RES_CAL	Analog		Connect a 2.8kW (1%) resistor to GND for output current calibration.
C7, D2, D7, E7, E8, E9, F1, F2, F3, F4, F5, F6, F7, G3, H3, H7, J3	GND	Power		Ground supply voltage (GND) and ground return path. Connect to board GND (0V).
G4	CBIAS1	Analog		Internal bias circuit for VCO-1. Connect a 4.7µF capacitor to GND.
G5	CLDO1	Analog		Internal LDO bypass for VCO-1. Connect a 10µF capacitor to GND.
G6	CBIAS0	Analog		Internal bias circuit for VCO-0. Connect a 4.7µF capacitor to GND.
G7	CLDO0	Analog		Internal LDO bypass for VCO-0. Connect a 10µF capacitor to GND.
A8	VDDO_QCLKA	Power		Positive supply voltage (3.3V, 2.5V, or 1.8V) for the QCLK_A[2:0] outputs.
B8	VDD_QCLKA	Power		Positive supply voltage (3.3V) for channel A.

Table 1. Pin Descriptions[a] (Cont.)

Ball Number	Name	Type[b]		Description
J8	VDDO_QCLKB	Power		Positive supply voltage (3.3V, 2.5V, or 1.8V) for the QCLK_B[2:0] outputs.
H8	VDD_QCLKB	Power		Positive supply voltage (3.3V) for channel B.
G1	VDDO_QCLKC	Power		Positive supply voltage (3.3V, 2.5V, or 1.8V) for the QCLK_C[1:0] outputs.
G2	VDD_QCLKC	Power		Positive supply voltage (3.3V) for channel C.
C1	VDDO_QCLKD	Power		Positive supply voltage (3.3V, 2.5V, or 1.8V) for the QCLK_D[1:0] outputs.
C2	VDD_QCLKD	Power		Positive supply voltage (3.3V) for channel D.
D1	VDD_QCLKE	Power		Positive supply voltage (3.3V) for the QCLK_E output and channel.
A3	VDD_SPI	Power		Positive supply voltage (3.3V) for the SPI interface.
E4	VDD_INP	Power		Positive supply voltage (3.3V) for the differential inputs (CLK[1:0]).
H4	VDD_LCV	Power		Positive supply voltage (3.3V) for the VCXO-PLL.
J4	VDD_LCF	Power		Positive supply voltage (3.3V) for the internal oscillator of the FemtoClockNG PLL. For more information on power supply filtering, see Power Supply Filtering.
A6	VDD_CPV	Power		Positive supply voltage (3.3V) for internal VCXO_PLL circuits.
J7	VDD_CPF	Power		Positive supply voltage (3.3V) for internal FemtoClockNG circuits.
A5	VDD_OSC	Power		Positive supply voltage (3.3V) for the VCXO input.

[a] For essential information on power supply filtering. See Section "Power Supply Filtering" on page 72.

[b] PU (pull-up) and PD (pull-down) indicate internal input resistors. See Figure 37 for values.

Principles Of Operation

Overview

The 8V19N472 generates low-phase noise, synchronized clock output signals locked to an input reference frequency. The device contains two PLLs with configurable frequency dividers. The first PLL (VCXO-PLL, suffix V) uses an external VCXO as the oscillator and provides jitter attenuation. The external loop filter is used to set the VCXO-PLL bandwidth frequency in conjunction with internal parameters. The second, low-phase noise PLL (FemtoClockNG, suffix F) multiplies the VCXO-PLL frequency to one of its two selectable VCO frequencies of 2949.12MHz or 2457.6MHz.

The FemtoClockNG PLL is completely internal and provides a central reference timing reference point for all output signals. From this point, fully synchronous dividers generate the output frequencies. The device has five output channels (A to E), four channel with one integer output divider (A to D), and one channel with a fractional output divider (E). The clock outputs are configurable with support for LVPECL and LVDS formats, and a variable output amplitude. In channels A to D, the clock phase can be adjusted in phase. Individual outputs and channels, and unused circuit blocks support powered-down states for operation at reduced power consumption. The Register Map, accessible through a selectable 3/4-wire SPI interface with read-back capability, controls the main device settings and delivers device status information. For redundancy purpose, there are two selectable reference frequency inputs and a configurable switch logic with manual, auto-selection, and holdover support.

Phase-Locked Loop Operation

Frequency Generation

Table 2 displays the available frequency dividers for clock generation. The dividers must be set by the user to match input, VCXO and VCO frequency, and to achieve frequency and phase lock on both PLLs. The frequency of the external VCXO is chosen by the user. The internal VCO frequency can be selected at frequencies of 2949.12MHz or 2457.6MHz. Table 10 shows example divider configurations for typical wireless infrastructure applications.

Table 2. PLL Divider Values

Divider	Range	Operation	
		Jitter Attenuation (Dual PLL, BYPV = 0)	Frequency Synthesis (VCXO-PLL bypassed, BYPV = 1)
VCXO-PLL Pre-Divider P_V	÷1…÷32767: (15-bit)	Input clock frequency: $f_{CLK} = P_V \times \frac{f_{VCXO}}{M_V}$	No external VCXO required
VCXO-PLL Feedback Divider M_V	÷1…÷32767: (15-bit)		
FemtoClock NG Pre-Divider P_F	÷1…÷63: (6-bit)	VCXO frequency: $f_{VCXO} = \frac{P_F}{M_F} \times f_{VCO}$	Input clock frequency: $f_{CLK} = \frac{P_F}{M_F} \times f_{VCO}$
FemtoClock NG Feedback Dividers M_F	÷8 …÷511 (9-bit)	f_{VCO} = 2949.12MHz or 2457.6MHz P_F: Set P_F to 0.5 in above equation if the frequency doubler is engaged by setting FDF = 1	f_{VCO} = 2949.12MHz or 2457.6MHz P_F: Set P_F to 0.5 in above equation if the frequency doubler is engaged by setting FDF = 1
Output Divider N*x* (x=A-D)	÷1…÷160	Output frequency $f_{OUT} = \frac{f_{VCO}}{N_X}$	
Output Divider N*E*	Fractional Mode[a]: ▪ N: Integer part (4…2^4-1) ▪ F: Fractional part (1…2^{24}-1)	Output frequency $f_{OUT} = \frac{f_{VCO}}{N_E}$ $N_E = 2 \cdot \left(N_{INT} + \frac{N_{FRAC}}{2^{24}}\right)$	

[a] Greatest N*E* fractional divider is $2 \times (14 + [2^{24}\text{-}1] / 2^{24}) \approx 29.99999988$

VCXO-PLL

The prescaler P_V and the VCXO-PLLs feedback divider M_V require configuration to match the input frequency to the VCXO-frequency. With a divider value range of 15-bit the dividers M_V and P_V, the device support is very flexible and supports a wide range of input and VCXO-frequencies. In addition, the range of available input and feedback dividers allows the adjustment of the phase detector frequency independent of the used input and VCXO frequencies as shown in Table 3 and Table 4. The VCXO-PLL charge pump current is controlled via internal registers, and can be set in 50µA steps from 50µA to 1.6mA. The VCXO-PLL can be bypassed (BYPV): when in bypass, the FemtoClockNG PLL locks to the pre-divided input frequency.

Table 3. Example Configurations for f_{VCXO}=30.72MHz

Input Frequency (MHz)	VCXO-PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
122.88	4	1	30.72
	16	4	7.68
	64	16	1.92
	256	64	0.48
156.25	15625	3072	0.01

Table 4. Example Configurations for f_{VCXO}=122.88MHz

Input Frequency (MHz)	VCXO- PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
122.88	4	4	30.72
	16	16	7.68
	64	64	1.92
	256	256	0.48

Table 5. Example Configurations for f_{VCXO}=153.6MHz

Input Frequency (MHz)	VCXO- PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
122.88	4	5	30.72
	16	20	7.68
	64	80	1.92
	256	320	0.48
156.25	3125	3072	0.05

Table 6. Example Configurations for f_{VCXO}=125MHz

Input Frequency (MHz)	VCXO-PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
25	1	5	25
	4	20	6.25
	16	80	1.5625
	64	320	0.390625
19.44	486	3125	0.04
125	1	1	125
	5	5	25
	25	25	5
	125	125	1
156.25	5	4	31.25
	50	40	3.125
	500	400	0.3125

Table 7. Example Configurations for f_{VCXO}=156.25MHz

Input Frequency (MHz)	VCXO- PLL Divider Settings		f_{PFD} (MHz)
	PV	MV	
19.44	1944	15625	0.01
25	4	25	6.25
	40	250	0.625
	400	2500	0.0625
125	4	5	31.25
	40	50	3.125
	400	500	0.3125
156.25	1	1	156.25
	10	10	15.625
	100	100	1.5625

Table 8. VCXO-PLL Bypass Settings

BYPV	Operation
0	VCXO-PLL operation.
1	VCXO-PLL bypassed and disabled. The reference clock for the FemtoClockNG PLL is the selected input clock. The input clock selection must be set to manual by the user. Clock switching and holdover are not defined. Device synthesizes an output frequency but will not attenuate input jitter. No external VCXO component and loop filter required.

FemtoClockNG PLL

The FemtoClockNG PLL is the second stage PLL and locks to the output signal of the VCXO-PLL (BYPV=0). It requires configuration of the frequency doubler FDF or the pre-divider PF and the feedback divider MF to match the VCXO-PLL frequency to the selected VCO frequency of 2949.12MHz or 2457.6MHz. The best phase noise is typically achieved by engaging the internal frequency doubler (FDF= 1, x2). If engaged, the signal from the first PLL stage is doubled in frequency, increasing the phase detector frequency of the FemtoClockNG PLL. Enabling the frequency doubler disables the frequency pre-divider PF. If the frequency doubler is not used (FDF=0), the PF pre-divider has to be configured. Typically, PF is set to ÷1 to keep the phase detector frequency as high as possible. Set PF to other divider values to achieve specific frequency ratios between first and second PLL stage. This PLL is internally configured to high-bandwidth.

Table 9. Frequency Doubler

FDF	Operation
0	Frequency doubler off. PF divides clock signal from VCXO-PLL or input (in bypass)
1	Frequency doubler on (x2). Signal from VCXO-PLL or input (in bypass) is doubled in frequency. PF divider has no effect.

Table 10. Example PLL Configurations

VCXO-Frequency (MHz)	FemtoClock NG Divider Settings for VCO					
	2949.12MHz			2457.6MHz		
	FDF	PF	MF	FDF	PF	MF
153.6	–	5	96	–	1	16
				x2	–	8
122.88	–	1	24	–	1	20
	x2	–	12	x2	–	10
30.72	–	1	96	–	1	80
	x2	–	48	x2	–	40

Channel Frequency Divider

The device supports five independent output channels, A to E. Channels A to D have one configurable integer frequency divider N*x* (*x*=A to D) that divides the VCO frequency to the desired output frequency with very low phase noise. The integer divider values can be selected from the range of ÷1 to ÷160 as shown in Table 11. Channel E supports fractional divider ratios (see Table 12).

Table 11. Integer Frequency Divider Settings

Channel Divider Nx[a]	Output Clock Frequency (MHz) for VCO (MHz)	
	2949.12	2457.6
÷1	2949.12	2457.6
÷2	1474.56	1228.8
÷3	312.5	819.2
÷4	737.28	614.4
÷5	589.82	491.52
÷6	491.52	409.6
÷8	368.64	307.2
÷10	294.912	245.76
÷12	245.76	204.8
÷16	184.32	153.6
÷18	163.84	136.533
÷20	147.456	122.88
÷24	122.88	102.4
÷30	98.304	81.92
÷32	92.16	76.8
÷36	81.92	68.266
÷40	73.728	61.44
÷48	61.44	51.2
÷50	58.9824	49.152
÷60	49.152	40.96
÷64	46.08	38.4
÷72	40.96	34.133
÷80	36.864	30.72
÷96	30.72	25.6
÷100	29.4912	24.576
÷120	24.576	20.48
÷128	23.04	10.2
÷160	18.432	15.36

[a] *x*=A to D

Table 12. Typical Fractional Frequency Divider Settings

Channel Divider N*E* [a]		Output Clock Frequency (MHz)
f_{VCO} = 2949.12MHz		
18.874368	294912 ÷ 15625	156.25
23.59296	73728 ÷ 3125	125
f_{VCO} = 2457.6MHz		
15.72864	49152 ÷ 3125	156.25
19.6608	12288 ÷ 625	125

[a] Greatest N*E* fractional divider is $2 \times (14 + [2^{24}-1] / 2^{24}) \approx 29.99999988$

Redundant Inputs

The two inputs are compatible with LVDS and LVPECL signal formats, and also support single-ended signals (LVCMOS, see Applications Information for applicable input interface circuits).

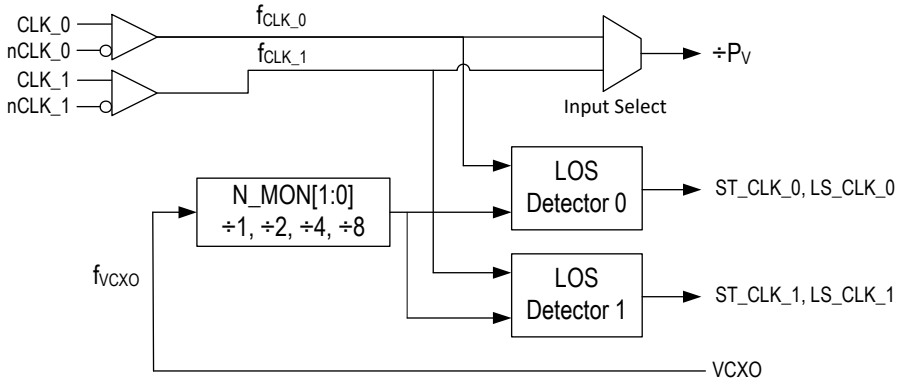
Monitoring

The two clock inputs of the device are individually and permanently monitored for activity. Inactivity is defined by a static input signal. Input frequency changes are not monitored.

Loss of Input Signal (LOS)

In operation, a clock input is declared invalid (LOS) with the corresponding ST_CLK_*n* and LS_CLK_*n* indicator bits set after a specified number of consecutive clock edges. If differential input signals are applied, the input will also detect an LOS condition in case of a zero differential input voltage.The device supports LOS detect circuits, one for each input. The signal detect circuits compare the signals at the CLK_0 and CLK_1 inputs to internally frequency-divided signals from the VCXO-PLL (for information, see Figure 3). The loss-of-signal fault condition is declared upon three or more missing clock input edges. LOS requires configuration of the N_MON[1:0] frequency divider setting to individually match the input frequencies CLK_*n* to the VCXO frequency: $f_{VCXO} \div$ N_MON[1:0] = f_{CLK_n}. For instance, if one of the input frequencies is 15.36MHz and a 30.72MHz VCXO is used, set N_MON[1:0] =÷2 (for configuration details, see Table 28. Then, LOS is declared after three consecutive missing clock edges. LOS is signaled through the ST_CLK_*n* (momentary) and LS_CLK_*n* (sticky, resettable) status bits, and can reported as an interrupt signal on the nINT output. The LOS circuit requires the jitter attenuation mode of device (BYPV=0). LOS does not detect frequency errors.

Figure 3. LOS Detect Circuit



Input Re-Validation

A clock input is declared valid and the corresponding ST_CLK_*n* bit is reset after the clock input signal returns for an user-configurable number of consecutive input periods. This re-validation of the selected input clock is controlled by the CNTV setting (verification pulse counter).

Input Clock Selection

The 8V19N472 supports external, pin-controlled clock selection and internal, register controlled clock selection. The EXT_SEL pin controls the input selection mode. In internal mode, automatic clock selection and manual register-controlled clock selection is available.

Definitions for Input Clock Selection

- Manual input selection – The CLK_n input is selected by the user by pin (external) or register control (internal).
- Automatic input selection – The CLK_n input is selected by an internal state machine based on internal priorities, as response to the clock input status.
- Primary clock – The CLK_n input is selected by the selection logic.
- Secondary clock – The CLK_n input is not selected by the selection logic.
- PLL reference clock – The CLK_n input is selected as the PLL reference signal by the selection logic. In automatic switching mode, the selection can be overwritten by a state machine.

Clock Selection

The device supports five input selection modes: manual with and without holdover, short-term holdover, and two automatic switch modes.

Table 13. Clock Selection Settings

Mode			Name	Description	Flags				Application
nHO_EN	nMA1	nMA0			ST_CLKn	nST_HOLD	ST_SEL	ST_REF	
0	X	X	Manual holdover control (default)	Input selection follows user-configuration of the EXT_SEL pin or INT_SEL register bit as set by nEXT_INT with holdover. Input selection is *never* changed by the internal state machine.					
				LOS on the primary reference clock: Active reference stays selected and the PLLs may stall. Device will not go into holdover.	LOS status	1	Selected input	0[a]	Startup and external selection control with holdover
				Manual change of the reference clock: The device *will go into holdover* and the hold-off down-counter (CNTH) starts. The device initiates a clock switch *after* expiration of the hold-off counter. Duration of holdover is set by CNTH × CNTR / f_{VCXO}. Holdover is terminated even if the secondary clock input is bad (LOS). See "Manual Holdover Control (nHO_EN = 0)"		0[b]	Selected input[c]	LOS status of *selected* input	

Table 13. Clock Selection Settings (Cont.)

Mode			Name	Description	Flags				Application
nHO_EN	nMA1	nMA0			ST_CLKn	nST_HOLD	ST_SEL	ST_REF	
1	0	0	Manual control	Input selection follows user-configuration of the EXT_SEL pin or INT_SEL register bit as set by nEXT_INT. Input selection is *never* changed by the internal state machine.					
				LOS on the primary reference clock: Active reference stays selected and the PLLs may stall. Device will not go into holdover.	LOS status	1	Selected input	0	External selection control
				Manual change of the reference clock: The device will not go into holdover and will attempt to lock to the newly selected reference.		1	Selected input	Actual LOS status of selected input	
1	0	1	Automatic	Input selection follows LOS status. A failing input clock will cause an LOS event for that clock input. If the selected clock has an LOS event, the device will immediately initiate a clock failover switch.					
				LOS on the primary reference clock: The device will switch to the secondary clock without holdover. Input selection is determined by a state machine and may differ from the user's clock selection No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will not enter the holdover state. The PLL is not locked. Re-validation of all input clocks will result in the PLL to attempt to lock on that input clock. See "Revertive Switching".	LOS status	1	Selected input determined by state machine	Actual LOS status of selected input determined by state machine	Multiple inputs with qualified clock signals
				Manual change of the reference clock: The device will switch to the newly selected clock without holdover. If the newly selected clock is not valid, the PLL may stall.		1	Selected Input	Actual LOS status of selected input	

Table 13. Clock Selection Settings (Cont.)

Mode			Name	Description	Flags				Application
nHO_EN	nMA1	nMA0			ST_CLKn	nST_HOLD	ST_SEL	ST_REF	
1	1	0	Short-term Holdover	Input selection follows user-configuration of EXT_SEL pin or INT_SEL register bit as set by nEXT_INT. Selection is never changed by the internal state machine.					
				LOS on the primary reference clock: A failing reference clock will cause an LOS event. If the selected reference fails, the device will enter holdover *immediately*. Re-validation of the selected input clock is controlled by the CNTV setting. A successful re-validation will result in the PLL to re-lock on that input clock.	LOS status	0 for hold over duration	Selected Input	LOS status for duration of LOS until revalidation	Use if a single reference is occasionally interrupted
1	1	1	Automatic with holdover	Input selection follows LOS status. A failing input clock will cause an LOS event for that clock input. If the *selected* clock has an LOS event, the device will go into holdover and switches input clocks after the hold-off counter expires.					
				LOS on the primary reference clock or Manual change of the reference clock: the device will go into holdover and the hold-off down-counter (CNTH) starts. The device initiates a clock failover switch to a valid secondary clock input *after* expiration of the hold-off counter. Duration of holdover is set by CNTH*CNTR*f_{VCXO}. The holdover is terminated prior hold-off count-down if the primary clock revalidates or is terminated by a manual change of the reference clock (for more information, see Automatic with Holdover (nHO_EN = 1, nM/A[1:0]=11) and Revertive Switching). No valid clock scenario: The device remains in holdover if the secondary input clock is invalid.	LOS status	0 for hold over duration	Selected input determined by state machine	Actual LOS status of selected input	Multiple inputs

[a] For the duration of an invalid input signal (LOS).

[b] For the duration of holdover.

[c] Delayed by holdover period.

Holdover

In holdover state, the output frequency and phase is derived from an internal, digital value based on previous frequency and phase information. Holdover characteristics are defined in Table 43.

Manual Holdover Control (nHO_EN = 0)

This is the default switching mode of the device. The switch control is manual. The EXT_SEL pin or the INT_SEL bit as set by nEXT_INT determines the selected reference clock input. If the selection is changed by the user, the device will enter holdover until the CNTH[7:0] counter expires, then the new reference is selected (input switch). Application for this mode is startup and external selection control.

- ST_REF – Status of selected reference clock
- ST_CLK_n will both reflect the status of the corresponding input
- ST_SEL – The new selection
- nST_HOLD = 0 for the duration of holdover

Automatic with Holdover (nHO_EN = 1, nM/A[1:0]=11)

If an LOS event is detected on the active reference clock:

- Holdover begins immediately
- Corresponding ST_REF and LS_REF go low immediately
- Hold-off countdown begins immediately

During this time, both input clocks continue to be monitored and their respective ST_CLK and LS_CLK flags are active. LOS events are indicated on ST_CLK and LS_CLK when they occur.

If the active reference clock resumes and is validated during the hold-off countdown:

- Its ST_CLK status flag will return high and the LS_CLK is available to be cleared by an SPI write of 1 to that register bit
- No transitions will occur of the active REF clock; ST_SEL does not change
- Revertive bit has no effect during this time (whether 0 or 1)

When the hold-off countdown reaches zero:

- If the active reference has resumed and has been validated during the countdown, it will maintain being the active reference clock:
  - ST_SEL does not change
  - ST_REF returns to 1
  - LS_REF can be cleared by an SPI write of 1 to that register
  - Holdover turns off and the VCXO-PLL attempts to lock to the active reference clock
- If the active reference has not resumed but the other clock input CLK_*n* is validated, then:
  - ST_SEL1:0 changes to the new active reference
  - ST_REF returns to 1
  - LS_REF can be cleared by an SPI write of 1 to that register
  - Holdover turns off
- If there is no validated CLK:
  - ST_SEL does not change
  - ST_REF remains low
  - LS_REF cannot be cleared by an SPI write of 1 to that register
  - Holdover remains active

Revertive capability returns if REVS = 1.

Hold-off Counter

A configurable down-counter applicable to the “Automatic with holdover” and “manual with holdover” selection modes. The purpose of this counter is a deferred, user-configurable input switch. The counter expires when a zero-transition occurs; this triggers a new reference clock selection. The counter is clocked by the frequency-divided VCXO-PLL signal. The CNTR setting determines the hold-off counter frequency divider and the CNTH setting the start value of the hold-off counter. For instance, set CNTR to a value of ÷131072 to achieve 937.5Hz (or a period of 1.066ms at f_{VCXO}=122.88MHz): the 8-bit CNTH counter is clocked by 937.5Hz and the user-configurable hold-off period range is 0ms (CNTR = 0x00) to 272ms (CNTR = 0xFF). After the counter expires, it reloads automatically from the CNTH SPI register. After the LOS status bit (LS_CLK_n) for the corresponding input CLK_n is cleared by the user, the input is enabled for generating a new LOS event.
The CNTR counter is only clocked if the device is configured in the clock selection modes “Automatic with holdover” *AND* the *selected* reference clock experiences an *LOS* event or in the “manual with holdover” mode with manual switching. Otherwise, the counter is automatically disabled (not clocked).

Revertive Switching

Revertive switching is only applicable to the two automatic switch modes shown in Table 13:

- Revertive switching enabled – Re-validation of any non-selected input clock(s) will cause a new input selection according to the user-preset input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the currently selected reference clock.
- Revertive switching disabled – Re-validation of a non-selected input clock has no impact on the clock selection. Default setting is revertive switching disabled.

VCXO-PLL Lock Detect

The VCXO-PLL lock detect circuit uses the signal phase difference at the phase detector as loss-of-lock criteria. Loss-of-lock is reported if the actual phase difference is larger than a configurable phase detector window set by the LOCK_TH[14:0] configuration bits. A loss-of-lock state is reported through the nST_LOLV and nLS_LOLV status bits (see Table 17).

FemtoClockNG Loss-of-Lock (LOLF)

FemtoClockNG-PLL loss of lock is signaled through the nST_LOLF (momentary) and nLS_LOLF (sticky, resettable) status bits, and can reported as hardware signal on the LOCK_V output as well as an interrupt signal on the nINT output.

Differential Outputs

Table 14. Output Features

Output	Style	Ampl.[a]	Disable	Power Down	Termination
QCLK_*y*	LVPECL	350–850mV 4 steps	Yes	Yes	50Ω to V_{TT}[b]
	LVDS				100Ω diff.
QCLK_V	LVPECL	350–850mV 4 steps	Yes	Yes	50Ω to V_{TT}
	LVDS				100Ω diff.
	LVCMOS[c]	1.8V	Yes	Yes	–

[a] Amplitudes are measured single-endedly.

[b] See Table 50 for V_{TT} (Termination voltage) values.

[c] LVCMOS style: nQCLK_V and QCLK_V are complementary.

Table 15. Individual Clock Output Settings

PD[a]	Output Power	STYLE	Termination	Enable	State	A[1:0]	Amplitude (mV)[b]
1	Off	X	100Ω diff. or no termination	X	Off	X	X
0	On	0	100Ω diff. (LVDS)	0	Disable[c]	XX	X
				1	Enable	00	350
						01	500
						10	700
						11	850
		1	50Ω to V_{TT}[d] (LVPECL)	0	Disable	XX	X
				1	Enable	00	350
						01	500
						10	700
						11	850

[a] Power-down modes are available for the individual channels A–D and the outputs QCLK_y (A0–D1). QCLK_*E* is defined: nPD_E = 0: power down and nPE=0.

[b] Output amplitudes of 700mV and 850mV require a 3.3V output supply (V_{DDO_V}). 350mV and 500mV output amplitudes support V_{DDO_V} = 2.5V and 1.8V.

[c] Differential output is disabled in static low/high state

[d] See Table 50 for V_{TT} (Termination voltage) values.

Output Phase-Delay

Output phase delay is supported in each channel. The selected VCO frequency sets the delay unit to $1/f_{VCO}$.

Table 16. Delay Circuit Settings

Delay Circuit	Unit	Steps	Range
Clock Phase Φ_{CLK_x}	$\frac{1}{f_{VCO}}$ f_{VCO}=2949.12MHz: 339ps f_{VCO}=2457.6MHz: 407ps	256	 0-86.46ns 0-103.75ns

Status Conditions and Interrupts

The 8V19N472 has an interrupt output to signal changes in status conditions. Settings for status conditions can be accessed in the Status Registers. The device has several conditions that can indicate faults and status changes in the operation of the device. These are shown in Table 17 and can be monitored directly in the status registers. Status bits (named: ST_status_condition) are read-only and reflect the momentary device status at the time of read-access. Several status bits are also copied into latched bit positions (named: LS_status_condition.

The latched version is controlled by the corresponding fault and status conditions and remains set ("sticky") until reset by the user by writing 1 to the status register bit. The reset of the status condition only has an effect if the corresponding fault condition is removed, otherwise, the status bit will be set again. Setting a status bit on several latched registers can be programmed to generate an interrupt signal (nINT) via settings in the Interrupt Enable bits (named: IE_*condition*). A setting of 0 in any of these bits will mask the corresponding latched status bit from affecting the interrupt status pin. Setting all IE bits to 0 has the effect of disabling interrupts from the device.

Table 17. Status Bit Functions

Status Bit		Function			
			Status if Bit is:		Interrupt Enable Bit
Momentary	Latched	Description	1	0	
ST_CLK_0	LS_CLK_0	CLK 0 input status	Active	LOS	IE_CLK_0
ST_CLK_1	LS_CLK_1	CLK 1 input status	Active	LOS	IE_CLK_1
nST_LOLV	nLS_LOLV	VCXO-PLL loss of lock	Locked	Loss of lock	IE_LOLV
nST_LOLF	nLS_LOLF	FemtoClockNG-PLL loss of lock	Locked	Loss of lock	IE_LOLF
nST_HOLD	nLS_HOLD	Holdover	Not in holdover	Device in holdover	IE_HOLD
ST_VCOF	—	FemtoClockNG VCO calibration	Not completed	Completed	—
ST_SEL	—	Clock input selection	0 = CLK_0 1 = CLK_1		—
ST_REF	LS_REF	PLL reference status	Valid reference[a]	Reference lost	IE_REF

[a] Manual and short-term holdover mode: 0 indicates if the selected reference is lost, 1 if not lost.
Automatic mode: will transition to 0 while the input clock is lost and during input selection by priority. Will transition to 1 once a new reference is selected.
Automatic with holdover mode: 0 indicates the reference is lost and still in holdover

Interrupts are cleared by resetting the appropriate bit(s) in the latched register after the underlying fault condition has been resolved. When all valid interrupt sources have been cleared in this manner, this will release the nINT output until the next unmasked fault.

Table 18. Fault Indicator Functions

Status Bit (PLL)		Status Reported on LOCK[a] Output[b]
nLS_LOLV (VCXO-PLL)	nLS_LOLF (FemtoClockNG)	
Locked	Locked	1
Locked	Not locked	0
Not locked	Locked	0
Not locked	Not locked	0

[a] Hardware interrupts on nINT required to set the IE_LOLV, IE_LOLF bits to "enable interrupt".

[b] SELSV1 controls the logic level 1.8V/3.3V of LOCK and nINT outputs.

Device Startup, Reset, and Synchronization

At startup, an internal POR (power-on reset) resets the 8V19N472 and sets all register bits to their default values. The device forces the VCXO control voltage at the LFV pin to half of the power supply voltage to center the VCXO-frequency. In the default configuration the QCLK_*y* outputs are disabled at startup.

Recommended configuration sequence (in order):

1. (Optional) Set the value of the CPOL register bit to define the SPI read mode supported by the SPI controller. Set LSBIT_1ST, SDO_ACT, ACS_ON, and the corresponding mirrored bits in register 0x00 as appropriate for SPI read access to the device.
2. Configure all PLL and output divider and delay circuits as well as other device configurations, such as the charge pump currents. Set the TRANSFER bit (register 0x0F, bit D0) for PLL registers wider than then 8 bits (see double-buffered registers).
3. Set the initialization bit, INIT_CLK.

   This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear.
4. Set both the RELOCK bit and PB_CAL bit. This step should not be combined with the previous step (setting INIT_CLK) in a multi SPI-byte register access. Both bits will self-clear.
5. Clear the FVCV bit to release the VCXO control voltage and VCXO-PLL will attempt to lock to the input clock signal starting from its center frequency.
6. Clear the status flags.
7. Enable the outputs by accessing the output-enable registers in a separate SPI write access.

Changing Frequency Dividers and Phase Delay Values

If a change must be made to a clock divider or phase delay value N_{A-D}, and Φ_{CLKA-D}, complete the following procedure:

1. (Optional) Set the value of the CPOL register to define the SPI read mode so that SPI settings can be validated by subsequent SPI read accesses.
2. (Optional) Disable the outputs whose frequency divider or delay value is changed.
3. Configure the N_{A-D} dividers and the delay circuits Φ_{CLKA-D} to the desired new values.
4. Set the initialization bit INIT_CLK.

   This will initiate all divider and delay circuits and synchronize them to each other. The INIT_CLK bit will self-clear. During this initialization step, all QCLK_*y* outputs are reset to the logic low state.
5. Set the RELOCK bit. This step should not be combined with the setting INIT_CLK in a multi SPI-byte register access. This bit will self-clear.
6. (Optional) Enable the outputs whose frequency divider was changed.

SPI Interface

The 8V19N472 has a selectable 3/4-wire serial control port capable of responding as a slave in an SPI configuration to allow read and write access to any of the internal registers for device programming or read back. The SPI interface consists of the SCLK (clock), SDIO (serial data input and output in 3-wire mode, input in 4-wire mode), SDO (output in 4-wire mode), nCS (chip select) and nRESET (SPI reset) pins. A data transfer contains 16 bits (direction + 15 bit address) and any integer multiple of 8 bits (input or output data), and is always initiated by the SPI master on the bus. Internal register data is organized in SPI bytes of 8 bits each. The device supports the most-significant bit (MSBit) and least-significant (LSBit) first transfer bit positions, single byte and multi-byte data streaming modes with address auto-increment and auto-decrement. For SPI logic diagrams, see Figure 4 to Figure 7.

Chip select. If the nCS pin is at logic high, the SDIO/SDO data output pin is in high-impedance state and the SPI interface of the device is disabled.

3/4-wire mode. In 3-wire mode, the SDIO pin acts as bidirectional input/output and the SDO pin is in high-impedance state. In 4-wire mode, the SDIO pin is the SPI input and the SDO pin is the SPI output. The SPI interface mode is defined by the SDO_ACT bit in the SPI device configuration register.

Active clock edge. In a write operation, data on SDIO is clocked in on the rising edge of SCLK. In a read operation, data on SDIO/SDO is clocked out on the falling or rising edge of SCLK depending on the CPOL setting (CPOL=0: output data changes on the falling edge, CPOL=1: output data changes on the rising edge).

Reset. By asserting the nRESET pin, the SPI engine is reset and all internal device registers reset to its default values.

Logic levels. The SPI pins nRESET, nCS, SCLK, SDIO, and SDO have selectable 1.8V/3.3V logic levels. The SELSV0 register bit controls the logic level. SELSV0=0: 1.8V logic and SELSV0=1: 3.3V logic.

Least Significant Bit Position. The device supports LSBit (least significant bit first) and MSBit (most significant bit first) transfers between master and slave. If MSBit first is set, data is transferred in this order: transfer direction bit first, then the register address bits A14 to A0, then the data bits of the first data byte D7 to D0. If LSBit first is set, the order is: address bits A0 to A14 first, then the transfer direction bit, then the data bits of the first data byte D0 to D7.

Starting a data transfer requires the nCS pin to set and hold at logic low level during the entire transfer. Setting nCS = 0 will enable the SPI interface with the SDIO pin in data input mode. The master must initiate the first 16-bit transfer containing the transfer direction bit and the SPI register address to access.

Transfer direction bit: Defines if the master reads data from the device or writes data to the device. R/nW (1=Read,0=Write). If MSB first is set, the transfer bit is presented by the master as the first bit in the transfer. If LSB first is set, the transfer bit is the 16th bit presented by the master.

Address: The device supports a 15-bit address A[14:0] pointing to an internal register in the address space 0 to 0x7FFF. The device implements registers at the addresses 0x00–0x63.

Read operation from an internal register: a read operation starts with a 16-bit transfer from the master to the slave: the SDIO signal is clocked on the *rising* edge of SCLK. The transfer direction bit R/nW must be to 1 to indicate a read transfer, the other 15 bits is the address A[14:0] to read from. After the first 16 bits are clocked into the SDIO pin, the SDIO I/O changes to output if 4-wire mode is set by SDO_ACT=0 (in 3-wire mode set by SDO_ACT=1, the pin SDO is the output). The register content addressed by A[14:0] are the presented at the SPI output at the next 8 SCLK *falling* (CPOL=1) or next 8 SCLK *rising* (CPOL=1) clock cycles and transfer these to the master. Transfers must be completed with de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. Read operation transfers multiple bytes in streaming mode with the 15-bit register address auto-increment or decrement. Single byte transfers are supported in streaming mode by de-asserting nCS after the first payload byte.

Write operation to a device register: During a write transfer, an SPI master transfers one or more bytes of data into the internal registers of the device. A write transfer starts by asserting the nCS to pin low logic level. The transfer direction bit R/nW must be set to 0 to indicate a write transfer, the other 15 bits are the address A[14:0] to write to. Bits D[7:0] contain 8 bits of transfer data, which is written into the register specified by A[14:0] at the end of each 8-bit write transfer. Multiple, subsequent register transfers from the master to the slave are supported in streaming mode by holding nCS asserted at logic low level during write transfers. Transfers must be completed with de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. The 15-bit register address will auto-increment or decrement (streaming mode). Single byte transfers are supported in streaming mode by de-asserting nCS after the first payload byte.

Register Streaming Mode. Streaming mode is the transfer of multiple data bytes back to back. The address A[14:0] specifies the register location of the first byte to transfer; for the next transfer, the address is automatically incremented or decremented. nCS must stay at logic low level and SDIO/SDO will present multiple registers (e.g. (A), (A-1), (A-2), etc.) with each 8 SCLK cycles. During SPI Read operations, the user may continue to hold nCS low and provide further bytes. The ASC_ON register defines if registers auto-increment ((A), (A+1), (A+2), etc.), or auto-decrement ((A), (A-1), (A-2), etc.).

Address wrap-around: Applicable to streaming mode: The address will wrap around the address range of 0x00–0x63. The SPI engine auto-increments to address 0x00 after 0x63 and auto-decrements to address 0x63 after 0x00.

End of transfer: After nCS is de-asserted to logic 1, the SPI bus is available to transfers to other slaves on the SPI bus. See the READ diagrams (Figure 5 and Figure 6) and WRITE diagram (Figure 4) displaying the transfer of a single byte of data from and into registers.

Mirrored register bits. The register bits D7–D4 in the device SPI configuration register (0x00) are mirrored with the bits D3–D0 in the same register for a LSBit/MSBit First independent access. Setting a mirrored bit to the 1 state requires to set both bit and its <mirrored_bit> to 1.

Double-buffered registers. PLL divider registers that are wider than 8 bits are double buffered for synchronous access. Synchronous configuration of these registers requires to write the multiple-byte setting into the SPI registers first, and then transfer the contents into the device registers by asserting the TRANSFER bit. The configuration only takes effect after the TRANSFER bit is asserted. Configuration data can be read back from SPI and device registers as specified by the RB_MODE bit.

Internal debug registers. Registers in the address range 0x4E–0x4F and 0x5C to 0xFF should not be used. Do not write into any registers in the 0x4E–0x4F and 0x5C to 0xFF address range.

Default SPI modes: After power-up and reset by the nRESET pin, the SPI interface is in 3-wire mode with SDO in high-impedance, MSB first mode, streaming mode on with address auto-decrement. In read transfer mode, data is output on SDIO/SDO on the falling SCLK edge.

Figure 4. Logic Diagram: Single Byte WRITE Data into Device Registers in SPI 3 or 4-wire Mode for LSB and MSB-First

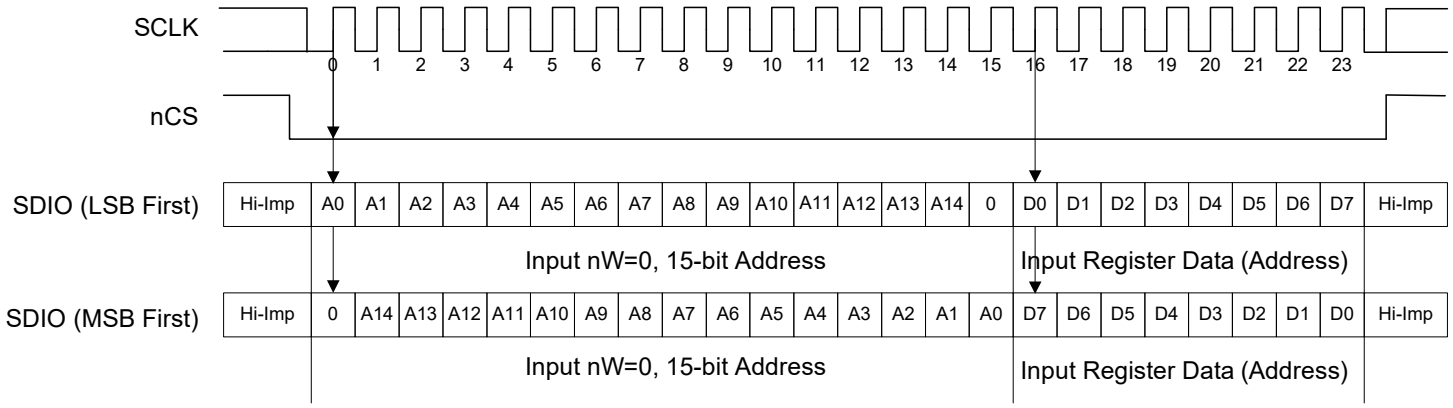


Figure 5. Logic Diagram: Single Byte READ Data from the Device Registers in SPI 3-wire Mode for LSB and MSB-First and CPOL=0, 1

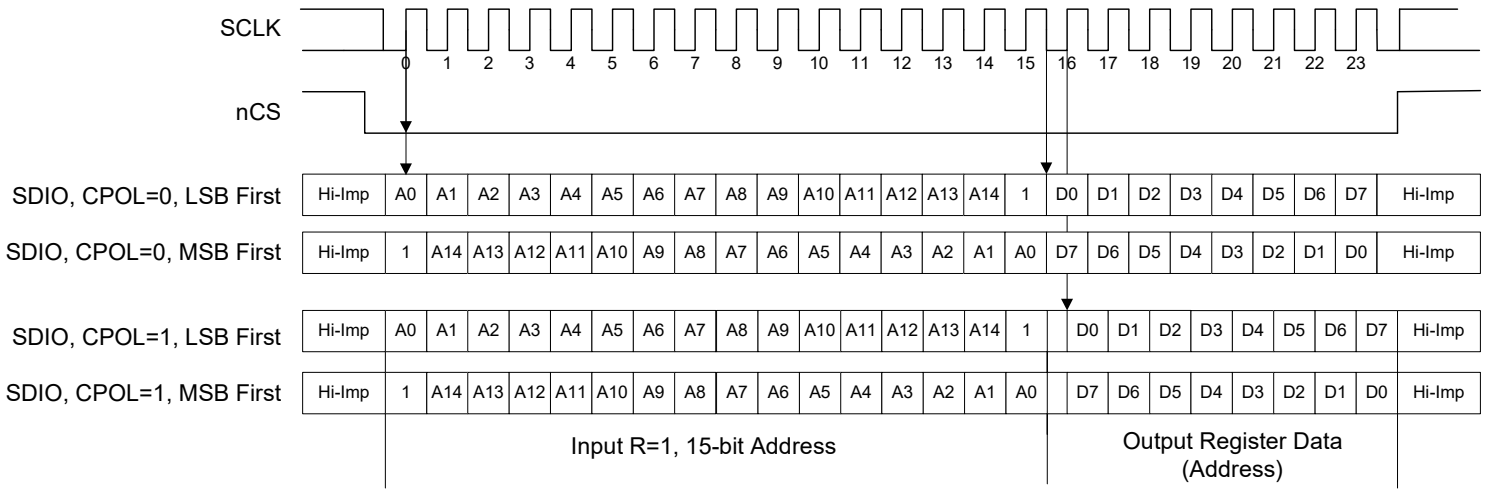


Figure 6. Logic Diagram: Single Byte READ Data from the Device Registers in SPI 4-wire Mode for LSB-First and CPOL=0, 1

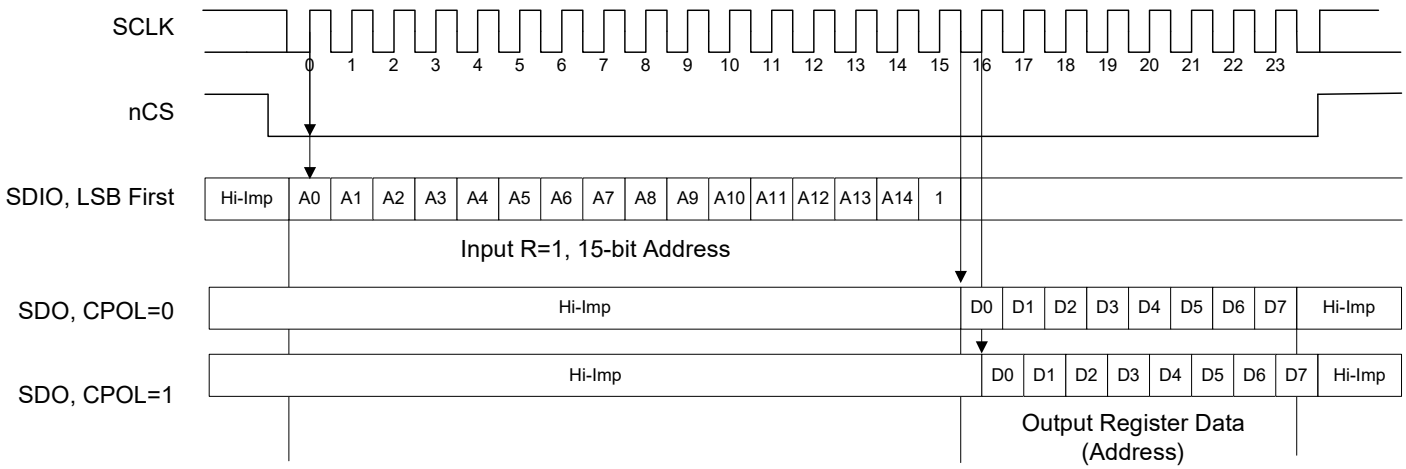


Figure 7. Logic Diagram: Single Byte READ Data from the Device Registers in SPI 4-wire Mode for MSB-First and CPOL=0, 1

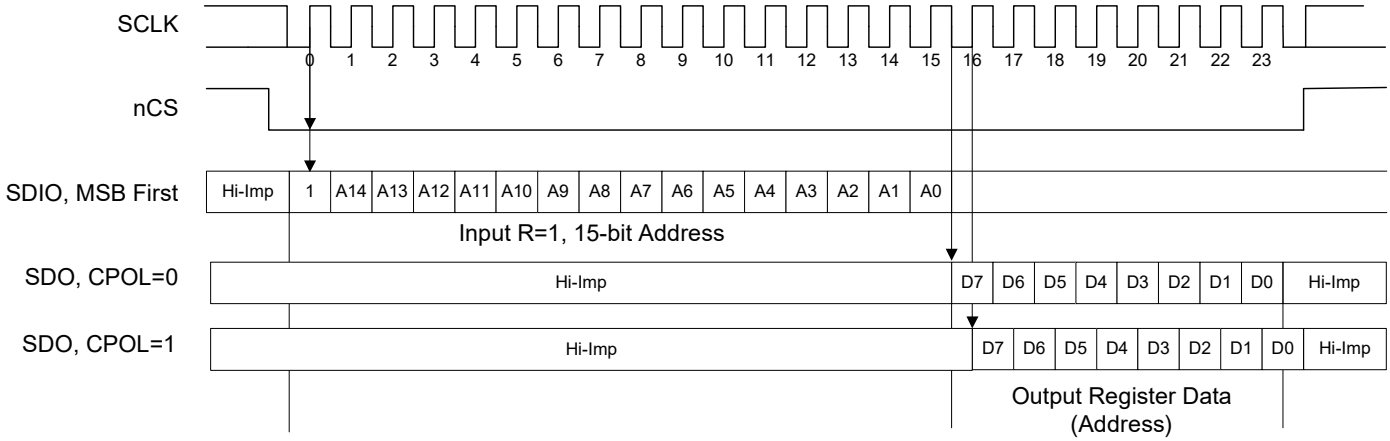


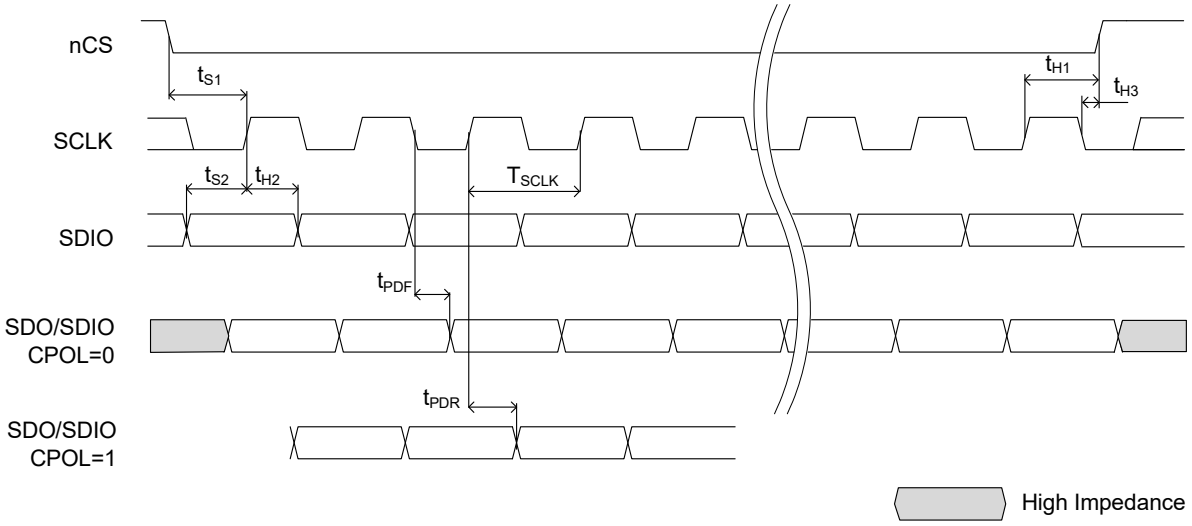
Table 19. SPI Read / Write Cycle Timing Parameters

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
f_{SCLK}	SCLK Frequency			20	MHz
T_{SCLK}	SCLK Clock Period		50		ns
t_{S1}	Setup Time, nCS (falling) to SCLK (rising)		10		ns
t_{S2}	Setup Time, SDIO (input) to SCLK (rising)		8		ns
t_{H1}	Hold Time, SCLK (rising) to nCS (rising)		30		ns
t_{H2}	Hold Time, SCLK (rising) to SDIO (input)		8		ns

Table 19. SPI Read / Write Cycle Timing Parameters (Cont.)

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
t_{H3}	Hold Time, SCLK (falling) to nCS (rising)		8		ns
t_{PDF}	Propagation Delay, SCLK (falling) to SDIO (output in 3-wire mode) or SDO (in 4-wire mode)	CPOL = 0		10	ns
t_{PDR}	Propagation Delay, SCLK (rising) to SDIO (output in 3-wire mode) or SDO (in 4-wire mode)	CPOL = 1		10	ns
t_{WRES}	nRESET Pulse Width		100		ns

Figure 8. SPI Timing Diagram



Device Registers

Register Map

Table 20. Register Map

Register Address	Register Description
0x00–0x02	Device Configuration (SPI)
0x03	Device Type
0x04–0x05	Device ID
0x06	Device Version
0x07–0x0B	Reserved
0x0C–0x0D	Vendor ID
0x0E	Reserved
0x0F	Device Configuration (SPI)
0x10–0x11	PLL Frequency Divider, PV
0x12–0x13	PLL Frequency Divider, MV
0x14	Reserved
0x15–0x16	LOCK_TH
0x17	PLL Control, BYPV
0x18	PLL Control, VCO_SEL
0x19	PLL Frequency Divider, PF, FDF
0x1A	PLL Frequency Divider MF[7:0]
0x1B	PLL Frequency Divider, MF8
0x1C–0x1E	PLL Control
0x1F	I/O Voltage Select
0x20–0x23	Various Control
0x24–0x26	Channel A
0x27	Reserved
0x28–0x2A	Output States QCLK_A0–A2
0x2B	Reserved
0x2C–0x2E	Channel B
0x2F	Reserved
0x30–0x32	Output States QCLK_B0–B2
0x32–0x33	Reserved
0x34–0x36	Channel C
0x37	Reserved
0x38–0x39	Output States QCLK_C0–C1
0x3A–0x3B	Reserved

Table 20. Register Map (Cont.)

Register Address	Register Description
0x3C–0x3E	Channel D
0x3F	Reserved
0x40–0x41	Output States QCLK_D0–D1
0x42–0x43	Reserved
0x44–0x47	Channel E
0x48	Output States QCLK_E
0x49–0x4A	Reserved
0x4B	Output States QCLK_V
0x4C	Interrupt Enable
0x4D	Reserved
0x4E–0x4F	Reserved
0x50	Status (Latched)
0x51	Status (Momentary)
0x52	Reserved
0x53	Status (Momentary)
0x54	Reserved
0x55–0x57	General Control
0x58	Channel, Enable A–E and QCLK_V
0x59–0x5B	Reserved
0x5C–0x5E	Reserved
0x5F–0x60	Reserved
0x61–0x62	Reserved
0x63	Reserved
0x64–0xFF	Reserved

Register Descriptions

This section contains all addressable registers, sorted by function, followed for a detailed description of each bit field for each register. Several functional blocks with multiple instances in this device have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once with an additional table to indicate their addresses and default values. All writable register fields will come up with a default values as indicated in the Factory Defaults column unless altered by values loaded from non-volatile storage during the initialization sequence.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are Reserved. Reserved bit fields can be used for internal debug test and debug functions.

Device Configuration Registers

Table 21. Device Configuration Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x00	Reserved	LSBIT_1ST	ACS_ON	SDO_ACT	<SDO_ACT>	<ACS_ON>	<LSBIT_1ST>	Reserved
0x01	STR_OFF	Reserved	RB_MODE	Reserved	Reserved	Reserved	Reserved	Reserved
0x02	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x03	DEV_TYPE[7:0]							
0x04	DEV_ID[7:0]							
0x05	DEV_ID[15:8]							
0x06	DEV_VER[7:0]							
0x0C	VENDOR_ID[7:0]							
0x0D	VENDOR_ID[15:8]							
0x0F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TRANSFER
0x1F	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SELSV1	SELSV0

Table 22. Device Configuration Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
LSBIT_1ST <LSBIT_1ST>	R/W	0 Value: MSB first	Least Significant Bit Position Defines the bit transmitted first in SPI transfers between slave and master. 0 = The most significant bit (D7) first 1 = The least significant bit (D0) first LSBIT_1ST bit D6 is mirrored with <LSBIT_1ST> in bit position D1. Changing LSBIT_1ST to most significant bit requires to set both LSBIT_1ST and <LSBIT_1ST> bits.

Table 22. Device Configuration Register Descriptions (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
ASC_ON <ASC_ON>	R/W	0 Value: off. Addresses auto-decrement	Address Ascend on 0 = Address ascend is off (Addresses auto-decrement in streaming SPI mode) 1 = Address ascend is on (Addresses auto-increment in streaming SPI mode) The ASC_ON bit specifies whether addresses are incremented or decremented in streaming SPI transfers. The ASC_ON bit D5 is mirrored with <ASC_ON> in bit position D2. Changing ASC_ON to “ON” requires to set both ASC_ON and <ASC_OFF> bits.
SDO_ACT <SDO_ACT>	R/W	0 Value: SPI-3-wire mode	SPI 3/4 Wire Mode Selects the unidirectional or bidirectional data transfer mode for the SDIO pin. 0 = SPI 3-wire mode: – SDIO is the SPI bidirectional data I/O pin – SDO pin is not used and is in high-impedance 1 = SPI 4-wire mode – SDIO is the SPI data input pin – SDO is the SPI data output pin SDO_ACT bit D4 is mirrored with <SDO_ACTIVE> in bit position D3. Changing SDO_ACT to SPI 4-wire mode requires to set both SDO_ACT and <SDO_ACT> bits.
STR_OFF	R/W	0 Value: SPI streaming mode enabled	SPI Streaming Mode 0 = SPI streaming mode enabled 1 = SPI single byte transfer mode In SPI streaming mode, the device transfers SPI data back to back while auto-decrementing (if ASC_ON = 0) or auto-incrementing (if ASC_ON = 1) the SPI register address after a byte access. The device continues to read or write SPI data as long as nCS remains asserted and the SPI streaming mode remains enabled. In SPI streaming mode, single byte data transfers are supported by setting nCS to logic high state after the byte has been transferred. In SPI single byte transfer mode, one byte of SPI data is transferred regardless of nCS being de-asserted after the transfer. If this bit is set and nCS remains asserted, the SPI state machine resets after the data byte is transferred as if nCS was de-asserted and awaits the next transfer. The device does not implement STR_OFF = 1. For implemented SPI single byte transfers, see Figure 4 to Figure 7.
RB_MODE	R/W	0 Value: Read from device registers	Read Back Mode The device implements double-buffered registers for frequency divider registers wider than 8 bits (registers for PV, MV and FRAC). There are SPI registers and device registers. This bit specifies whether a read operation accesses the SPI or the device registers. 0 = Read operation from PV, MV, and FRAC device registers 1 = Read operation from PV, MV, and FRAC SPI registers See the TRANSFER bit to transmit data from the SPI to device registers.

Table 22. Device Configuration Register Descriptions (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
DEV_TYP[7:0]	R only	0000 0110 Value: RF-PLL	Device (Chip) Type Reads 0x06 (RF-PLL) after power-up and reset.
DEV_ID[14:0]	R only	0x04: 0100 0010 0x05: 0000 0000 Value: 0x0042	Device ID Device is composed of registers 0x05 (high byte) and register 0x04 (low byte). Reads 0x0042 after power-up and reset.
DEV_VER[7:0]	R only	0x00 Value: 0	Device Version 0x00. Reads 0x00 (Silicon revision C) after power-up and reset.
VENDOR_ID	R only	0x0C: 0010 0110 0x0D: 0000 0100 Value: 0x0426	Vendor ID 0x0426 (Integrated Device Technology, IDT). Reads 0x0426 (IDT) after power-up and reset.
TRANSFER	R/W Auto-clear	0 Value: No transfer	SPI Transfer The device implements double-buffered registers for frequency divider registers wider than 8 bits (registers for PV, MV, and FRAC). There are SPI registers and device registers. Setting this bit to 1 will copy the content of the PV, MV, MF, LOCK_TH, and FRAC SPI registers synchronously and simultaneously into the device registers where the settings will affect the device operation. For reading from SPI vs. device registers, see the RB_MODE setting. 0 = No transfer 1 = The SPI registers are transferred into the device registers.
SELSV1	Select LOCK/nINT voltage level R/W	0 Value: 1.8V	Selects the voltage level of the LOCK and nINT outputs SELSV1 0 = LOCK, nINT interface pins are 1.8V (default) 1 = LOCK, nINT interface pins are 3.3V
SELSV0	Select SPI voltage level R/W	0 Value: 1.8V	Selects the voltage level of the SPI interface SELSV0 0 = SPI interface pins are 1.8V (default) 1 = SPI interface pins are 3.3V

PLL Frequency Divider Registers

Table 23. PLL Frequency Divider Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x10	PV[7:0]							
0x11	Reserved	PV[14:8]						
0x12	MV[7:0]							
0x13	Reserved	MV[14:8]						
0x15	LOCK_TH[7:0]							
0x16	Reserved	LOCK_TH[14:8]						
0x19	FDF	Reserved	PF[5:0]					
0x1A	MF[7:0]							
0x1B	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MF8

Table 24. PLL Frequency Divider Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
PV[14:0]	R/W	000 0100 0000 0000 Value=÷1024	VCXO-PLL Input Frequency Pre-Divider The value of the frequency divider (binary coding) Range: ÷1 to ÷32767 PV[14:0] is located in double-buffered registers. See the RE_MODE and TRANSFER bit settings.
MV[14:0]	R/W	000 0100 0000 0000 Value=÷1024	VCXO-PLL Feedback-Divider The value of the frequency divider (binary coding) Range: ÷1 to ÷32767 MV[14:0] is located in double-buffered registers. See the RE_MODE and TRANSFER bit settings.

Table 24. PLL Frequency Divider Register Descriptions (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
LOCK_TH[14:0]	R/W	000 0000 1000 0000 Value = 128	PLL lock detect phase window threshold The device reports VCXO-PLL lock when the phase difference between the internal signals f_{REF} and f_{VCXO_REF} are lower than or equal to the phase difference set by LOCK_TH[14:0] for more than 1000 f_{VCXO_DIV} clock cycles. Requires $M_V \geq 4$. Set LOCK_TH[14:0] < M_V. ($f_{REF} = f_{CLK} \div P_V$ is the internal output of the PV divider, $f_{VCXO\_DIV} = f_{VCXO} \div M_V$ is the internal output of the MV divider). LOCK_TH[14:0] is located in double-buffered registers. See the RE_MODE and TRANSFER bit settings.
PF[5:0]	R/W	00 0001 Value = ÷1	FemtoClock NG Pre-Divider The value of the frequency divider (binary coding) Range: ÷1 to ÷63 00 0000: PF is bypassed
FDF	R/W	0 Value = f_{VCXO} ÷ PF	The input frequency of the FemtoClockNG PLL (2nd stage) is: 0 = The output signal of the BYPV multiplexer, divided by the PF divider. 1 = The output signal of the BYPV multiplexer, doubled in frequency. Use this setting to improve phase nose. The PF divider has no effect if FDF=1.
MF[8:0]	R/W	0 0001 1000 Value = ÷24	FemtoClock NG Pre-Divider The value of the frequency divider (binary coding) Range: ÷8 to ÷511

PLL Control Registers

Table 25. PLL Control Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPV
0x18	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VCO_SEL
0x1C	POLV	FVCV	Reserved	CPV[4:0]				
0x1D	Reserved	Reserved	OSVEN	OFFSET[4:0]				
0x1E	Reserved	Reserved	Reserved	CPF[4:0]				

Table 26. PLL Control Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
BYPV	R/W	0 VCXO-PLL enabled	VCXO-PLL Bypass 0 = VCXO-PLL is enabled. 1 = VCXO-PLL is disabled and bypassed.
VCO_SEL	R/W	0 Value = f_{VCO}=2949.12MHz	VCO Select. 0 = Selects VCO-0. f_{VCO}=2949.12MHz 1 = Selects VCO-1. f_{VCO}=2400-2500MHz
POLV	R/W	0 Value = Positive Polarity	VCXO Polarity 0 = Positive polarity. Use for an external VCXO with a positive f(V_C) characteristics. 1 = Negative polarity. Use for an external VCXO with a negative f(V_C) characteristics.
FVCV	R/W	1 Value: Value: LFV = V_{DD_V}/2	VCXO-PLL Force VC control voltage 0 = Normal operation. 1 = Forces the voltage at the LFV control pin (VCXO input) to V_{DD_V}/2. VCXO-PLL unlocks and the VCXO is forced to its mid-point frequency. FVCV=1 is the default setting at startup to center the VCXO frequency. FVCV should be cleared after startup to enable the PLL to lock to the reference frequency.

Table 26. PLL Control Register Descriptions (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
CPV[4:0]	R/W	0 1111 Value: 0.8mA	VCXO-PLL Charge-Pump Current Controls the charge pump current I_{CPV} of the VCXO-PLL. Charge pump current is the binary value of this register plus one multiplied by 50µA. I_{CPV} = 50µA × (CPV[4:0] + 1). CPV[4:0] = 00000 sets ICPV to the minimum current of 50µA. Maximum charge pump current is 1.6 mA. Default setting is 0.8mA: ((15 + 1) × 50µA).
OSVEN	R/W	0	VCXO-PLL Offset Enable 0 = No offset 1 = Offset enabled. A static phase offset of OFFSET[4:0] is applied to the PFD of the VCXO-PLL
OFFSETV[4:0]	R/W	0 0000 Value: 0°	VCXO-PLL Static Phase Offset Controls the static phase detector offset of the VCXO-PLL. Phase offset is the binary value of this register multiplied by 0.9° of the PFD input signal (OFFSET [4:0] × f_{PFD} ÷ 400). Maximum offset is 31 × 0.9° = 27.9°. Setting OFFSET to 0.0° eliminates the thermal noise of an offset current. If the VCXO-PLL input jitter period T_{JIT} exceeds the average input period, set OFFSET to a value larger than f_{PFD} × T_{JIT} × 400 to achieve a better charge pump linearity and lower in-band noise of the PLL.
CPF[4:0]	R/W	0 0110 Value: 1.4mA	FemtoClockNG-PLL Charge-Pump Current Controls the charge pump current I_{CPF} of the FemtoClockNG PLL. Charge pump current is the binary value of this register plus one multiplied by 200µA. I_{CPF} = 200µA × (CPF[4:0] + 1). CPV[4:0] = 00000 sets I_{CPF} to the minimum current of 200µA. Maximum charge pump current is 6.4mA. Default setting is 1.4mA: ((6+1) × 200µA).

Input Selection Mode Registers

Table 27. Input Selection Mode Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x20	Reserved	Reserved	Reserved	N_MON[1:0]		IN_BLOCK	nHO_EN	nEXT_INT
0x21	Reserved	Reserved	Reserved	REVS	nM/A[1:0]		Reserved	INT_SEL
0x22	CNTH[7:0]							
0x23	CNTR[1:0]		Reserved	Reserved	Reserved	Reserved	CNTV[1:0]	

Table 28. Input Selection Mode Registers

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
N_MON[1:0]	R/W	00 Value: ÷1	Clock frequency divider for the input activity monitor The clock activity monitor compares the device input frequency (f_{IN}) to the frequency of the VCXO divided by N_MON. For optimal operation of the activity monitor, the frequency f_{VCXO} ÷ N_MON should match the input frequency. E.g. for f_{IN}=122.88MHz and f_{VCXO}=122.88MHz, set N_MON=÷1. For f_{IN}=30.72MHz and f_{VCXO}=122.88MHz, set N_MON = ÷4. N_MON[1:0] 00 = ÷1 01 = ÷2 10 = ÷4 11 = ÷8
IN_BLOCK	R/W	0 Value: Not blocked	Inactive input clock block 0 = Both input clock signals, CLK0 and CLK1, are routed to the input clock mux. 1 = The input clock that is currently not active is gated off (blocked).
nHO_EN	R/W	0 Value: Enter Holdover	Manual Holdover Control 0 = Enter holdover on a manual input reference switch. Using the EXT_SEL control pin or the INT_SEL control bit, as defined by nEXT_INT for manual reference switching. nMA[1:0] has no meaning. 1 = The device switching and holdover modes are controlled by nMA[1:0].
nEXT_INT	R/W	0 Value: External selection	Input clock selection 0 = The EXT_SEL pin (B3) controls the input clock selection. 1 = The INT_SEL bit (register 0x21, D0) controls the input clock selection.

Table 28. Input Selection Mode Registers (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
REVS	R/W	0 Value: off	Revertive Switching. The revertive input switching setting is only applicable to the two automatic selection modes shown in Table 13. If nM/A[1:0] = X0, the REVS setting has no meaning. 0 = Disabled: Re-validation of the non-selected input clock has no impact on the clock selection. 1 = Enabled: Re-validation of the non-selected input clock will cause a new input selection according to the pre-set input priorities (revertive switch). The default setting is revertive switching turned off.
nM/A[1:0]	R/W	00 Value: Manual Selection	Reference Input Selection Mode. In any of the manual selection modes (nM/A[1:0] = 00 or 10), the VCXO-PLL reference input is selected by INT_SEL. In any of the automatic selection modes, the VCXO-PLL reference input is selected by an internal state machine according to the input LOS states and the priorities in the input priority registers 00 = Manual selection (no holdover) 01 = Automatic selection (no holdover) 10 = Short-term holdover 11 = Automatic selection with holdover
INT_SEL	R/W	0 Value: CLK0 selected	VCXO-PLL Input Reference Selection Controls the selection of the VCXO-PLL reference input in internal (nEXT_INT=1) and in manual selection mode (nHO_EN=1, nM/A[1:0] = 00 or 10). In external (nEXT_INT=0) and in automatic selection modes (nM/A[1:0]=X1), INT_SEL has no meaning. 0 = CLK_0 is the selected VCXO-PLL reference clock 1 = CLK_1 is the selected VCXO-PLL reference clock
CNTH[7:0]	R/W	1000 0000 Value: 136ms)	Short-term holdover: Hold-off counter period. The device initiates a clock failover switch upon counter expiration (zero transition). The counters start to counts backwards after an LOS event is detected. The hold-off counter period is determined by the binary number of VCXO-PLL output pulses divided by CNTR[1:0]. With a VCXO frequency of 122.88MHz and CNTR[1:0]=10, the counter has a period of (1.066ms × binary setting). After each zero-transition, the counter automatically re-loads to the setting in this register. The default setting is 136ms (VCXO=122.88MHz: 1/122.88MHz × 2^{17} × 128).

Table 28. Input Selection Mode Registers (Cont.)

<table>
<tr><th colspan="5">Register Description</th></tr>
<tr><th>Bit Field Name</th><th>Field Type</th><th>Default (Binary)</th><th colspan="2">Description</th></tr>
<tr><td rowspan="5">CNTR[1:0]</td><td rowspan="5">R/W</td><td rowspan="5">10

Value: 2^{17})</td><td colspan="2">Short-term holdover reference divider</td></tr>
<tr><td rowspan="2">CNTR[1:0]</td><td colspan="2">CNTH frequency (period; range)</td></tr>
<tr><td>122.88MHz VCXO</td><td>38.4MHz VCXO</td></tr>
<tr><td>00 = $f_{VCXO} \div 215$</td><td></td><td>1171Hz (0.853ms; 0-217.6ms)</td></tr>
<tr><td>01 = $f_{VCXO} \div 2^{16}$</td><td>1875Hz (0.533ms; 0-136ms)</td><td></td></tr>
<tr><td>10 = $f_{VCXO} \div 2^{17}$</td><td>937.5Hz (1.066ms; 0-272ms)</td><td></td></tr>
<tr><td>CNTV[1:0]</td><td>R/W</td><td>10

Value: 32)</td><td colspan="2">Revalidation counter
Controls the number of required consecutive, valid input reference pulses for clock re-validation on CLK_n in number of input periods. At an LOS event, the re-validation counter loads this setting from the register and counts down by one with every valid, consecutive input signal period. Missing input edges (for one input period) will cause this counter to re-load its setting. An input is re-validated when the counter transitions to zero and the corresponding LOS flag is reset.
00 = 2 (shortest possible)
01 = 16
10 = 32
11 = 64</td></tr>
</table>

Channel Registers

The content of the channel registers set the channel state, the clock divider the clock phase delay, and the power-down state.

Table 29. Channel Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x24: Channel A 0x2C: Channel B 0x34: Channel C 0x3C: Channel D	N_*A*[7:0] N_*B*[7:0] N_*C*[7:0] N_*D*[7:0]							
0x25: Channel A 0x2D: Channel B 0x35: Channel C 0x3D: Channel D	ΦCLK_*A*[7:0] ΦCLK_*B*[7:0] ΦCLK_*C*[7:0] ΦCLK_*D*[7:0]							
0x26: Channel A 0x2E: Channel B 0x36: Channel C 0x3E: Channel D	PD_*A* PD_*B* PD_*C* PD_*D*	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x44: Channel E 0x45: Channel E 0x46: Channel E	N_*E*_FRAC[7:0] N_*E*_FRAC[15:8] N_*E*_FRAC[23:16]							
0x47: Channel E	Reserved	Reserved	Reserved	Reserved	N_*E*_INT[3:0]			
0x58	Reserved	Reserved	EN_QCLK_V	EN_QCLK_A	EN_QCLK_B	EN_QCLK_C	EN_QCLK_D	EN_QCLK_E

Table 30. Channel Register Descriptions[a]

Register Description				
Bit Field Name	Field Type	Default (Binary)	Description	
N_*x*[7:0]	R/W	N_*A*, N_*B*: 0000 0001 Value= ÷3 N_*C*, N_*D*: 0000 0100 Value= ÷6	Output Frequency Divider N N_*x*[7:0]Divider Value	
			1000 0000 0000 0000 0000 0001 0000 0010 0000 0011 0000 0100 0000 0110	÷1 ÷2 ÷3 ÷4 ÷5 ÷6 ÷8
			0100 0011 0100 0100 0100 0110	÷10 ÷12 ÷16
			0100 1011 0100 1100	÷20 ÷24
			0101 0011 0100 1110 0101 0100	÷30 ÷32 ÷36
			0101 1011 0101 0110	÷40 ÷48
			0110 0011	÷50
			0110 0100 0101 1110	÷60 ÷64
			0101 1111	÷72
			0110 0110	÷80
			0110 1110	÷96
			0111 1011	÷100
			0111 1100 0111 0110	÷120 ÷128
			0111 1110	÷160

Table 30. Channel Register Descriptions[a] (Cont.)

Register Description				
Bit Field Name	Field Type	Default (Binary)	Description	
N_*E*_FRAC[23:0]	R/W	0110 1111 1110 1011 0100 1010 Value: 7,334,730	Fractional output divider, fractional part Together with N_E_INT, forms the fractional output divider N*E* value $N_E = 2 \cdot \left(N_{INT} + \frac{N_{FRAC}}{2^{24}}\right)$ The default value is N*E* = 2 × (9 + 0.4371839761732) = 18.8743679523. The default frequency on QCLK_*E* (VCO_SEL=0) is 156.250000395MHz (156.25MHz - 0.0025ppm) Greatest N*E* fractional divider is 2 ×(14 + [2^{24}-1] / 2^{24}) ≈ 29.99999988 N_*E*_FRAC[23:0] is located in double-buffered registers. See the RE_MODE and TRANSFER bit settings.	
N_*E*_INT[3:0]	R/W	1001 Value: 9	Fractional output divider, integer part See N_*E*_FRAC[23:0]	
ΦCLK_*x*[7:0] f_{VCO}=2949.12MHz	R/W	0000 0000	CLK_*x* phase delay ΦCLK_*x*[7:0]	
			f_{VCO}=2949.12MHz: Delay in ps = ΦCLK_*x* × 339 ps (256 steps) ΦCLK_*x*[7:0] Delay (f_{VCO}=2949.12 MHz)	
			0000 0000 0000 0001 … 1111 1111	0ps 339ps … 86.46ns

Table 30. Channel Register Descriptions[a] (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
ΦCLK_*x*[7:0] f_{VCO}=2457.6MHz	R/W	0000 0000	CLK_*x* phase delay ΦCLK_*x*[7:0] f_{VCO}=2457.6MHz: Delay in ps = ΦCLK_*x* × 407ps (256 steps) ΦCLK_*x*[7:0] Delay (f_{VCO}=2457.6MHz) 0000 0000 — 0ps 0000 0001 — 407ps … — … 1111 1111 — 103.75ns
PD_*x*	R/W	0 Value: power up	0 = Channel *x* is powered up 1 = Channel *x* is power down
EN_*x*	R/W	0 Value: disabled	QCLK_*x* channel output enable 0 = All outputs of channel *x* are disabled at the logic low state 1 = All outputs of channel *x* are enabled
EN_QCLK_*V*	R/W	0 Value: disabled	QCLK_*V* output enable 0 = QCLK_*V* is disabled at the logic low state 1 = QCLK_*V* is enabled

[a] *x*=A, B, C, D.

Output Registers

The content of the output registers set the power-down state, the output style and amplitude.

Table 31. Output Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x28: QCLK_A0 0x29: QCLK_A1 0x2A: QCLK_A2	PD_*A0* PD_*A1* PD_*A2*	Reserved	Reserved	STYLE_*A0* STYLE_*A1* STYLE_*A2*	A_*A0*[1:0] A_*A1*[1:0] A_*A2*[1:0]		Reserved	Reserved
0x30: QCLK_B0 0x31: QCLK_B1 0x32: QCLK_B2	PD_*B0* PD_*B1* PD_*B2*	Reserved	Reserved	STYLE_*B0* STYLE_*B1* STYLE_*B2*	A_*B0*[1:0] A_*B1*[1:0] A_*B2*[1:0]		Reserved	Reserved
0x38: QCLK_C0 0x39: QCLK_C1	PD_*C0* PD_*C1*	Reserved	Reserved	STYLE_*C0* STYLE_*C1*	A_*C0*[1:0] A_*C1*[1:0]		Reserved	Reserved
0x40: QCLK_D0 0x41: QCLK_D1	PD_*D0* PD_*D1*	Reserved	Reserved	STYLE_*D0* STYLE_*D1*	A_*D*0[1:0] A_*D*1[1:0]		Reserved	Reserved
0x48: QCLK_E	nPD_*E*	Reserved	Reserved	STYLE_*E*	A_*E*[1:0]		Reserved	Reserved
0x4B: QCLK_V	PD_*V*	Reserved	STYLE_*V*[1:0]		A_*V*[1:0]		Reserved	Reserved

Table 32. Output Register Descriptions[a]

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
PD_*y*	R/W	0 Value: power up	0 = Output QCLK_*y* is powered up 1 = Output QCLK_*y* is power down
PD_*V*	R/W	0: Value: power up	0 = Output QCLK_*V* is powered up 1 = Output QCLK_*V* is power down
nPD_*E*	R/W	0 Value: Power down	0 = Output QCLK_*E* and channel *E* including the fractional divider N_*E* are powered down 1 = Output QCLK_*E* is power up

Table 32. Output Register Descriptions[a]

Register Description				
Bit Field Name	Field Type	Default (Binary)	Description	
A_*y*[1:0] A_*E*[1:0]	R/W	01 Value: 500 mV	QCLK_*y*, QCLK_*E*, QCLK_V Output amplitude	
			Setting for STYLE = 0 (LVDS)	Setting for STYLE = 1 (LVPECL)
A_*V*[1:0]	R/W	01 Value: 350 mV	A[1:0] = 00: 350mV A[1:0] = 01: 500mV A[1:0] = 10: 700mV A[1:0] = 11: 850mV Termination: 100Ω across	A[1:0] = 00: 350mV A[1:0] = 01: 500mV A[1:0] = 10: 700mV A[1:0] = 11: 850mV Termination: 50Ω to V_{TT}[b]
STYLE_*y* STYLE_*E*	R/W	0 Value: LVDS	QCLK_*y* Output format 0 = Output is LVDS (Requires LVDS 100Ω output termination) 1 = Output is LVPECL (Requires LVPECL 50Ω output termination of to the specified recommended termination voltage).	
STYLE_*V*[1:0]	R/W	10 Value: LVCMOS	QCLK_*V* Output format 00 = Output is LVDS (Requires LVDS 100Ω output termination) 01 = Output is LVPECL (Requires LVPECL 50Ω termination to V_{TT}[b]) 1x = Both QCLK_*V* and nQCLK_*V* are single-ended LVCMOS 1.8V outputs. QCLK_V and nQCLK_V are complementary (180° phase difference)	

[a] *y*=A0, A1, A2, B0, B1, B2, C0, C1, D0, D1.

[b] See Table 50 for V_{TT} (Termination voltage) values.

Status Registers

Table 33. Status Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x4C	Reserved	Reserved	IE_LOLF	IE_LOLV	IE_REF	IE_HOLD	IE_CLK_1	IE_CLK_0
0x50	Reserved	Reserved	nLS_LOLF	nLS_LOLV	LS_REF	nLS_HOLD	LS_CLK_1	LS_CLK_0
0x51	Reserved	ST_SEL	nST_LOLF	nST_LOLV	ST_REF	nST_HOLD	ST_CLK_1	ST_CLK_0
0x53	Reserved	Reserved	Reserved	Reserved	Reserved	ST_VCOF	Reserved	Reserved

Table 34. Status Register Descriptions[a]

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
IE_LOLF	R/W	0	Interrupt Enable for FemtoClockNG-PLL loss of lock 0 = Disabled: Setting nLS_LOLF will not cause an interrupt on nINT 1 = Enabled: Setting nLS_LOLF will assert the nINT output (nINT=0, interrupt)
IE_LOLV	R/W	0	Interrupt Enable for VCXO-PLL loss of lock 0 = Disabled: Setting nLS_LOLV will not cause an interrupt on nINT 1 = Enabled: Setting nLS_LOLV will assert the nINT output (nINT=0, interrupt)
IE_CLK_*n*	R/W	0	Interrupt Enable for CLK*n* input loss-of-signal. 0 = Disabled: Setting LS_CLK_*n* will not cause an interrupt on nINT 1 = Enabled: Setting LS_CLK_*n* will assert the nINT output (nINT=0, interrupt)
IE_REF	R/W	0	Interrupt Enable for LS_REF. 0 = Disabled: any changes to LS_REF will not cause an interrupt on nINT 1 = Enabled: any changes to LS_REF will assert the nINT output (nINT=0, interrupt)
IE_HOLD	R/W	0	Interrupt Enable for holdover 0 = Disabled: Setting nLS_HOLD will not cause an interrupt on nINT 1 = Enabled: Setting nLS_HOLD will assert the nINT output (nINT=0, interrupt)
nLS_LOLF	R/W	-	FemtoClockNG-PLL loss of lock (latched status of nST_LOLF) Read 0 = ≥1 loss-of-lock events detected after the last status latch clear Read 1 = No loss-of-lock detected after the last status latch clear Write 1 = Clear status latch (clears pending nLS_LOLF interrupt)
nLS_LOLV	R/W	-	VCXO-PLL loss of lock (latched status of nST_LOLV) Read 0 = ≥1 loss-of-lock events detected after the last status latch clear Read 1 = No loss-of-lock detected after the last nLS_LOLV clear Write 1 = Clear status latch (clears pending nLS_LOLV interrupt)
LS_CLK_*n*	R/W	-	Input CLK_*n* status (latched status of ST_CLK_*n*). Read 0 = ≥1 LOS events detected on CLK_*n* after the last LS_CLK_*n* clear Read 1 = No loss-of-signal detected on CLK_*n* input after the last LS_CLK_*n* clear Write 1 = Clear LS_CLK_*n* status latch (clears pending LS_CLK_*n* interrupts on nINT)
ST_SEL	R	-	Input selection (momentary status) Reference Input Selection Status of the state machine. In any input selection mode, it reflects the input selected by the state machine. 0 = CLK_0 1 = CLK_1
nST_LOLF	R	-	FemtoClockNG-PLL loss of lock (momentary status) Read 0 = ≥1 loss-of-lock events detected Read 1 = No loss-of-lock detected A latched version of these status bit is available (nLS_LOLF).

Table 34. Status Register Descriptions[a] (Cont.)

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
nST_LOLV	R	-	VCXO-PLL loss of lock (momentary status bit) Read 0 = ≥1 loss-of-lock events detected Read 1 = No loss-of-lock detected A latched version of these status bits is available (nLS_LOLV).
ST_CLK_*n*	R	-	Input CLK_*n* status (momentary). 0 = LOS detected on CLK_*n* 1 = No LOS detected, CLK_*n* input is active A latched version of these status bits are available (LS_CLK_*n*).
LS_REF	R/W	-	PLL reference status (latched status of ST_REF). Read 0 = Reference is lost since last reset of this status bit Read 1 = Reference is valid since last reset of this status bit Write 1 = Clear LS_REF status latch (clears pending LS_REF interrupts on nINT)
nLS_HOLD	R/W		Holdover status indicator (latched status of ST_HOLD) Read 0 = VCXO-PLL has entered holdover state ≥1 times after reset of this status bit Read 1 = VCXO-PLL is (or attempts to) lock(ed) to an input clock Write 1 = Clear status latch (clears pending nLS_HOLD interrupt)
ST_VCOF	R	-	FemtoClockNG-PLL calibration status (momentary) Read 0 = FemtoClockNG PLL auto-calibration is completed Read 1 = FemtoClockNG PLL calibration is active (not completed)
ST_REF	R	-	Input reference status. 0 = No input reference present 1 = Input reference is present at the clock selected input clock
nST_HOLD	R	-	Holdover status indicator (momentary) 0 = VCXO-PLL in holdover state, not locked to any input clock 1 = VCXO-PLL is (or attempts to) lock(ed) to input clock A latched version of this status bit is available (nLS_HOLD).

[a] CLK*n* = CLK*0*, CLK*1*

General Control Registers

Table 35. General Control Register Bit Field Locations

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x55	INIT_CLK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x56	RELOCK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x57	PB_CAL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CPOL

Table 36. General Control Register Descriptions

Register Description			
Bit Field Name	Field Type	Default (Binary)	Description
INIT_CLK	W only Auto-Clear	X	Set INIT_CLK = 1 to initialize divider functions. Required as part of the startup procedure.
RELOCK	W only Auto-Clear	X	Setting this bit to 1 will force the FemtoClockNG PLL to re-lock.
PB_CAL	W only Auto-Clear	X	Precision Bias Calibration Setting this bit to 1 will start the calibration of an internal precision bias current source. The bias current is used as reference for outputs configured as LVDS and for as reference for the charge pump currents. This bit will auto-clear after the calibration completed. Set as part of the startup procedure.
CPOL	R/W	0	SPI Read Operation SCLK Polarity 0 = Data bits on SDIO/SDO are output at the falling edge of SCLK edge. 1 = Data bits on SDIO/SDO are output at the rising edge of SCLK edge.

DC Characteristics

Table 37. Pin Characteristics, VDD_v = 3.3V ± 5%, VDDO_v = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	OSC, nOSC		2	4	pF
		other inputs		2	4	pF
R_{PD}	Input Pull-Down Resistor	CLK_*n*, nCLK_*n*, SCLK, EXT_SEL		51		kΩ
R_{PU}	Input Pull-Up Resistor	nCLK_*n*, nCS, nRESET		51		kΩ
R_{OUT}	LVCMOS Output Impedance	nINT, LOCK		25		Ω

Table 38. Power Supply DC Characteristics, VDD_v = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C[a] [b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDD_v	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO_V}	Output Supply Voltage		1.71	1.8, 2.5, 3.3	3.465	V
I_{DD}	Power Supply Current	Note[c]			789	mA

[a] Design Target Specifications.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Configuration for $I_{DD\,(MAX)}$: selected VCO-0; set PV, MV, N[a:D] to their maximum values, all delay settings to maximum, all outputs configured to LVDS, maximum amplitude and turned on. QCLKE set to 156.MHz output frequency.

Table 39. LVCMOS DC Characteristics, VDD_v = 3.3V ± 5%, VDDO_v = (3.3V, 2.5V or 1.8V) ±5%, T_A = -40°C to +85°C)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Control inputs EXT_SEL, nRESET (1.8V logic and 3.3V tolerance)							
V_{IH}	Input High Voltage			1.17		VDD_v	V
V_{IL}	Input Low Voltage			-0.3		0.63	V
I_{IH}	Input High Current	EXT_SEL[1:0] inputs with pull-down resistor	VDD_v = 3.3V, V_{IN} = 3.3V			150	µA
		nRESET input with pull-up resistor				5	
I_{IL}	Input Low Current	EXT_SEL[1:0] inputs with pull-down resistor	VDD_v = 3.465V, V_{IN} = 0V	-5			µA
		nRESET input with pull-up resistor		-150			
Control inputs nCS, SCLK and SDIO (when input) (1.8V logic, hysteresis)							
V_T+	Positive-going Input Threshold Voltage			0.72		1.26	V
V_T-	Negative-going Input Threshold Voltage			0.54		1.08	V
V_H	Hysteresis Voltage		V_T+ – V_T-	0.18		0.72	V

Table 39. LVCMOS DC Characteristics, VDD_v = 3.3V ± 5%, VDDO_v = (3.3V, 2.5V or 1.8V) ±5%, T_A = -40°C to +85°C)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	SCLK input with pull-down resistor	VDD_v = 3.3V, V_{IN} = 1.8V			150	µA
		nCS input with pull-up resistor				5	
		SDIO (when input)				5	
I_{IL}	Input Low Current	SCLK input with pull-down resistor	VDD_v = 3.465V, V_{IN} = 0V	-5			µA
		nCS input with pull-up resistor		-150			
		SDIO (when input)		-5			
Control outputs configured to 3.3V							
V_{OH}	Output High Voltage	SDO, nINT, LOCK_F, LOCK_V, SDIO (when output)	I_{OH} = -4mA	2.0			V
V_{OL}	Output Low Voltage		I_{OL} = 4mA			0.55	V
Control outputs configured to 1.8V							
V_{OH}	Output High Voltage	SDO, nINT, LOCK_F, LOCK_V, SDIO (when output)	I_{OH} = -4mA	1.35		1.8	V
V_{OL}	Output Low Voltage		I_{OL} = 4mA			0.45	V

Table 40. Differential Input DC Characteristics, VDD_v = 3.3V ± 5%, VDDO_v = (3.3V, 2.5V or 1.8V) ±5%, T_A = -40°C to +85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	Input with pull-down resistor[a]	VDD_v = V_{IN} = 3.465V			150	µA
		Input with pull-up/pull-down resistor[b]				150	µA
I_{IL}	Input Low Current	Input with pull-down resistor[a]	VDD_v = 3.465V, V_{IN} = 0V	-150			µA
		Input with [b] pull-up/pull-down resistor[b]		-150			µA

[a] Non-Inverting inputs: CLK_0, CLK_1, OSC.

[b] Inverting inputs: nCLK_0, nCLK_1, nOSC.

Table 41. LVPECL DC Characteristics (QCLK_y, QREF_r, STYLE=1), V_{DD_V} = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C [a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage[b] [c]	350mV Amplitude Setting	V_{DDO_V} - 1.00	V_{DDO_V} - 0.88	V_{DDO_V} - 0.76	V
		500mV Amplitude Setting	V_{DDO_V} - 1.02	V_{DDO_V} - 0.90	V_{DDO_V} - 0.78	V
		700mV Amplitude Setting	V_{DDO_V} - 1.04	V_{DDO_V} - 0.94	V_{DDO_V} - 0.83	V
		850mV Amplitude Setting	V_{DDO_V} - 1.06	V_{DDO_V} - 0.96	V_{DDO_V} - 0.86	V
V_{OL}	Output Low Voltage[b c]	350mV Amplitude Setting	V_{DDO_V} - 1.38	V_{DDO_V} - 1.25	V_{DDO_V} - 1.13	V
		500mV Amplitude Setting	V_{DDO_V} - 1.54	V_{DDO_V} - 1.42	V_{DDO_V} - 1.30	V
		700mV Amplitude Setting	V_{DDO_V} - 1.75	V_{DDO_V} - 1.62	V_{DDO_V} - 1.51	V
		850mV Amplitude Setting	V_{DDO_V} - 1.90	V_{DDO_V} - 1.79	V_{DDO_V} - 1.68	V

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Outputs terminated with 50Ω to V_{TT}. See Table 50 for termination voltage V_{TT} values.

[c] 750mV and 1000mV amplitude settings are only available at V_{DDO_V} ≥ 2.5V

Table 42. LVDS DC Characteristics (QCLK_y, QREF_r, STYLE=0), V_{DD_V} = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C [a]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OS}	Offset Voltage[b] [c]	350mV Amplitude Setting	V_{DDO_V} - 1.146	V_{DDO_V} - 0.982	V_{DDO_V} - 0.809	V
		500mV Amplitude Setting	V_{DDO_V} - 1.249	V_{DDO_V} - 1.084	V_{DDO_V} - 0.928	V
		700mV Amplitude Setting	V_{DDO_V} - 1.351	V_{DDO_V} - 1.198	V_{DDO_V} - 1.026	V
		850mV Amplitude Setting	V_{DDO_V} - 1.460	V_{DDO_V} - 1.296	V_{DDO_V} - 1.131	V
ΔV_{OS}	V_{OS} Magnitude Change			18	50	mV

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] V_{OS} changes with V_{DD}

[c] 750mV and 1000mV amplitude settings are only available at V_{DDO_V} ≥ 2.5V

AC Characteristics

Table 43. AC Characteristics, V_{DD_V} = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C[a] [b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{VCO}	VCO Frequency range		VCO-0	2920	2949.12	3000	MHz
			VCO-1	2400	2457.6	2500	MHz
f_{OUT}	Output Frequency	VCO-0, Integer Divider	QCLK_*y*, N=÷1	2920	2949.12	3000	MHz
			QCLK_*y*, N=÷2	1460	1474.56	1500	MHz
			QCLK_*y*, N=÷3	973.33	983.04	1000	MHz
			QCLK_*y*, N=÷4	720	737.28	750	MHz
			QCLK_*y*, N=÷6	486.66	491.52	500	MHz
			QCLK_*y*, N=÷8	360	368.64	375	MHz
			QCLK_*y*, N=÷12	243.33	245.76	250	MHz
			QCLK_*y*, N=÷24	121.66	122.88	125	MHz
			QCLK_*y*, N=÷96	30.41	30.72	31.25	MHz
		VCO-1, Integer Divider	QCLK_*y*, N=÷1	2400	2457.6	2500	MHz
			QCLK_*y*, N=÷2	1200	1228.8	1250	MHz
			QCLK_*y*, N=÷4	600	614.4	750	MHz
			QCLK_*y*, N=÷8	300	307.2	375	MHz
			QCLK_*y*, N=÷10	240	245.76	250	MHz
			QCLK_*y*, N=÷16	150	153.6	187.5	MHz
			QCLK_*y*, N=÷20	120	122.88	125	MHz
		Fractional Divider	QCLK_E, NE range: $29.\overline{99}$ to $8.\overline{33}$	80		300	MHz
Δf_{OUT}	Output Frequency Accuracy		Integer output divider NA-D			0	pbb
			Fractional output divider NE, f_{OUT}=156.25MHz			10	pbb
f_{IN}	Input Frequency		CLK_*n*	0.008		307.2	MHz
f_{VCXO}	VCXO Frequency			25	122.88	250	MHz
V_{IN}	Input Voltage Amplitude[c]	CLK_*n*		0.15		1.2	V
V_{DIFF_IN}	Differential Input Voltage Amplitude[c, d]	CLK_*n*		0.3		2.4	V
V_{CMR}	Common Mode Input Voltage			1.0		$V_{DD\_V} - (V_{IN\,/\,2})$	V
odc	Output Duty Cycle		QCLK_*y*	45	50	55	%

Table 43. AC Characteristics, V_{DD_V} = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C[a] [b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
t_R / t_F	Output Rise/Fall Time, Differential	QCLK_*y* (LVPECL), 20% to 80%		146	250	ps
		QCLK_*y* (LVDS), 20% to 80%		146	250	ps
	Output Rise/Fall Time	LVCMOS outputs, 20%-80%			1	ns
$V_{O(PP)}$[e]	LVPECL Output Voltage Swing, Peak-to-peak, 1474.56MHz	350mV Amplitude Setting	366	384	402	mV
		500mV Amplitude Setting	498	513	528	mV
		700mV Amplitude Setting	692	714	735	mV
		850mV Amplitude Setting	822	847	872	mV
	LVPECL Differential Output Voltage Swing, Peak-to-peak, 1474.56MHz	350mV Amplitude Setting	731	768	800	mV
		500mV Amplitude Setting	997	1027	1057	mV
		700mV Amplitude Setting	1385	1427	1470	mV
		850mV Amplitude Setting	1643	1694	1745	mV
V_{OD}[f]	LVDS Output Voltage Swing, Peak-to-peak, 1474.56MHz	350mV Amplitude Setting	250	275	301	mV
		500mV Amplitude Setting	362	391	419	mV
		700mV Amplitude Setting	496	571	646	mV
		850mV Amplitude Setting	621	708	794	mV
	LVDS Differential Output Voltage Swing, Peak-to-peak, 1474.56MHz	350mV Amplitude Setting	500	550	601	mV
		500mV Amplitude Setting	724	781	838	mV
		700mV Amplitude Setting	993	1142	1291	mV
		850mV Amplitude Setting	1243	1415	1588	mV
*t*sk(o)	Output Skew; NOTE[g] [h] All delays set to 0	QCLK_*y* (same N divider)		25	50	ps
		QCLK_*y* (any N divider, incident rising edge)		28	50	ps
ΔΦ	Output isolation between any neighboring clock output	f_{OUT} = 1474.56 MHz (0-2949.12MHz)	70.5	74.21		dB
		f_{OUT} = 368.64 MHz (0-737.28MHz)	83	86.9		dB
$t_{D, LOS}$	LOS state detected (measured in input reference periods)	f_{IN} = 122.88MHz f_{IN} = 245.76MHz			2 3	T_{IN}

Table 43. AC Characteristics, V_{DD_V} = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C[a] [b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$t_{D, LOCK}$	PLL lock detect	PLL re-lock time after a short-term holdover scenario[i] VCXO-PLL bandwidth = 20Hz VCXO-PLL bandwidth = 100Hz		 32.5 126.4	300	 ms ms
$t_{D, RES}$	PLL lock residual time error	Refer to PLL lock detect $t_{D,LOCK}$. Reference point: final value of clock output phase after all phase transitions settled.		0.04	20	ns
Δf_{HOLD}	Holdover accuracy	Maximum frequency deviation during a holdover duration of 200ms and after the clock re-validate event. VCXO-PLL bandwidth = 20Hz VCXO-PLL bandwidth = 100Hz		 ±4.11 ±1.02	 ±5 ±5	 ppm ppm
$t_{D, RES-H}$	Holdover residual time error	Measured 50ms after the reference reappeared in a holdover scenario. Reference Point: final value of clock output phase after all phase transitions settled.		±6.6	±8.138	ns

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] VCXO-PLL bandwidth = 100Hz.

[c] V_{IL} should not be less than -0.3V and V_{IH} should not be greater than V_{DD_V}

[d] Common Mode Input Voltage is defined as the cross-point voltage.

[e] Outputs terminated with 50Ω to V_{TT}. See Table 50 for termination voltage V_{TT} values.

[f] LVDS outputs terminated 100Ω across terminals

[g] This parameter is defined in accordance with JEDEC standard 65

[h] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points

[i] Measured from LOS to both PLLs lock-detect asserted; hold-off timer = 200, initial frequency error <200 ppm.

Table 44. Clock Phase Noise Characteristics (f_{VCXO}=30.72MHz), V_{DD_V} = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C[a] [b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
*t*jit(Ø)	Clock RMS Phase Jitter (Random)		Integration Range: 1kHz - 61.44MHz		109	150	fs
			Integration Range: 12kHz - 20MHz		121	132	fs
Φ_N(10)	Clock single-side band phase noise (integer divider)	1474.56 MHz	10Hz offset (determined by VCXO)		-64.3		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-90.7		dBc/Hz
Φ_N(1k)			1kHz offset from Carrier		-109.2	-105	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier		-116.3	-112	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier		-122.5	-118	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier		-138.4	-135	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from Carrier and Noise Floor		-152.0	-147	dBc/Hz
Φ_N(10)	Clock single-side band phase noise (integer divider)	983.04 MHz	10Hz offset (determined by VCXO)		-69		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-94.2		dBc/Hz
Φ_N(1k)			1kHz offset from Carrier		-112	-105	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier		-119.5	-115	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier		-125.7	-120	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier		-141.5	-135	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from Carrier and Noise Floor		-155.2	-150	dBc/Hz
Φ_N(10)	Clock single-side band phase noise (integer divider)	737.28 MHz	10Hz offset (determined by VCXO)		-70.6		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-96.3		dBc/Hz
Φ_N(1k)			1kHz offset from Carrier		-115.7	-110	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier		-122.0	-118	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier		-128.3	-123	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier		-143.9	-138	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from Carrier and Noise Floor		-154.8	-150	dBc/Hz
Φ_N(10)	Clock single-side band phase noise (integer divider)	491.52 MHz	10Hz offset (determined by VCXO)		-74.7		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-99.9		dBc/Hz
Φ_N(1k)			1kHz offset from Carrier		-118.4	-110	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier		-125.2	-120	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier		-131.5	-125	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier		-146.7	-142	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from Carrier and Noise Floor		-154.7	-150	dBc/Hz

Table 44. Clock Phase Noise Characteristics (f_{VCXO}=30.72MHz), V_{DD_V} = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C[a] [b] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$\Phi_N(10)$	Clock single-side band phase noise (integer divider)	368.64 MHz	10Hz offset (determined by VCXO)		-75.37		dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)		-102.3		dBc/Hz
$\Phi_N(1k)$			1kHz offset from Carrier		-120.8	-113	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-128.0	-123	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier		-134.2	-128	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier		-149.5	-146	dBc/Hz
$\Phi_N(\geq 10M)$			≥10MHz offset from Carrier and Noise Floor		-156.6	-153	dBc/Hz
$\Phi_N(10)$	Clock single-side band phase noise (integer divider)	245.76 MHz	10Hz offset (determined by VCXO)		-79.8		dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)		-106.4		dBc/Hz
$\Phi_N(1k)$			1kHz offset from Carrier		-124.4	-120	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-131.9	-130	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier		-138	-135	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier		-152.7	-150	dBc/Hz
$\Phi_N(\geq 10M)$			≥10MHz offset from Carrier and Noise Floor		-158	-155	dBc/Hz
$\Phi_N(10)$	Clock single-side band phase noise (integer divider)	122.88 MHz	10Hz offset (determined by VCXO)		-85.9		dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)		-112.4		dBc/Hz
$\Phi_N(1k)$			1kHz offset from Carrier		-130.9	-120	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-138.1	-130	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier		-144.2	-135	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier		-156.5	-150	dBc/Hz
$\Phi_N(\geq 10M)$			≥10MHz offset from Carrier and Noise Floor		-158.7	-155	dBc/Hz
Φ	Spurious signals	1474.56 MHz	0-2949.12MHz, excluding harmonics, incl. reference and PFD spurious[c]		-74.2	-70.5	dBc
		368.64 MHz	0-737.28MHz, excluding harmonics, incl. reference and PFD spurious[d]		-86.9	-83	dBc

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Phase noise specifications are applicable for all outputs active, Nx not equal. Measured using a VCXO with the following characteristics: 30.72MHz, phase noise -96dBc/Hz at 0.01kHz, -127dBc/Hz at 0.1kHz, -144dBc/Hz at 1kHz,-159dBc/Hz at 10kHz,-162dBc/Hz at 100kHz; input reference frequency: 30.72MHz, VCXO-PLL bandwidth: 30 Hz, VCXO-PLL charge pump current: 1.6mA, FemtoClockNG PLL bandwidth: 139kHz

[c] $N_A = \div 2$, f_{QCLKA} = 1474.56MHz; $N_B = \div 3$, f_{QCLKB} = 983.04MHz; $N_C = \div 4$, f_{QCLKC} = 737.28MHz; $N_D = \div 6$, f_{QCLKD} = 491.52MHz; Bank B delay: Φ_{CLKB} = 0x01. Other divider configurations typically improve spurious. Contact factory for spurious data for other divider configurations.

[d] Output divider configuration: $N_A = \div 6$, f_{QCLKA} = 491.52MHz; $N_B = \div 8$, f_{QCLKB} = 368.64MHz; $N_C = \div 24$, f_{QCLKC} = 122.88MHz; $N_D = \div 12$, f_{QCLKD} = 245.76MHz. Bank A and B delay: Φ_{CLKB} = 0x01.

Table 45. Clock Phase Noise Characteristics (f_{VCXO}=122.88MHz), V_{DD_V} = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C [a] [b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
*t*jit(Ø)	Clock RMS Phase Jitter (Random)		Integration Range: 1kHz - 76.8MHz		102	150	fs
			Integration Range: 12kHz - 20MHz		118	125	fs
Φ_N(10)	Clock single-side band phase noise (integer divider)	1474.56 MHz	10Hz offset (determined by VCXO)		-61.6		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-81.8		dBc/Hz
Φ_N(1k)			1kHz offset from Carrier		-106.3	-105	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier		-119	-112	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier		-124.6	-118	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier		-137	-135	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from Carrier and Noise Floor		-152.8	-147	dBc/Hz
Φ_N(10)	Clock single-side band phase noise (integer divider)	983.04 MHz	10Hz offset (determined by VCXO)		-65		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-85.2		dBc/Hz
Φ_N(1k)			1kHz offset from Carrier		-109.1	-105	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier		-122	-115	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier		-127.7	-120	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier		-140	-135	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from Carrier and Noise Floor		-154.6	-150	dBc/Hz
Φ_N(10)	Clock single-side band phase noise (integer divider)	737.28 MHz	10Hz offset (determined by VCXO)		-67.7		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-87.8		dBc/Hz
Φ_N(1k)			1kHz offset from Carrier		-111.9	-110	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier		-124.6	-118	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier		-130.3	-123	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier		-142.6	-138	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from Carrier and Noise Floor		-155.7	-150	dBc/Hz
Φ_N(10)	Clock single-side band phase noise (integer divider)	491.52 MHz	10Hz offset (determined by VCXO)		-71		dBc/Hz
Φ_N(100)			100Hz offset (determined by VCXO)		-91.2		dBc/Hz
Φ_N(1k)			1kHz offset from Carrier		-115.1	-110	dBc/Hz
Φ_N(10k)			10kHz offset from Carrier		-127.8	-120	dBc/Hz
Φ_N(100k)			100kHz offset from Carrier		-133.6	-125	dBc/Hz
Φ_N(1M)			1MHz offset from Carrier		-145.8	-142	dBc/Hz
Φ_N(≥10M)			≥10MHz offset from Carrier and Noise Floor		-156.5	-150	dBc/Hz

Table 45. Clock Phase Noise Characteristics (f_{VCXO}=122.88MHz), V_{DD_V} = 3.3V ± 5%, V_{DDO_V} = (3.3V, 2.5V or 1.8V) ± 5%, T_A = -40°C to +85°C [a] [b] (Cont.)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$\Phi_N(10)$	Clock single-side band phase noise (integer divider)	368.64 MHz	10Hz offset (determined by VCXO)		-74.1		dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)		-93.8		dBc/Hz
$\Phi_N(1k)$			1kHz offset from Carrier		-117.9	-113	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-130.6	-123	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier		-136.3	-128	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier		-148.4	-146	dBc/Hz
$\Phi_N(\geq 10M)$			≥10MHz offset from Carrier and Noise Floor		-158.1	-153	dBc/Hz
$\Phi_N(10)$	Clock single-side band phase noise (integer divider)	245.76 MHz	10Hz offset (determined by VCXO)		-76.8		dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)		-97.3		dBc/Hz
$\Phi_N(1k)$			1kHz offset from Carrier		-121.7	-115	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-134.5	-130	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier		-140.24	-135	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier		-152	-148	dBc/Hz
$\Phi_N(\geq 10M)$			≥10MHz offset from Carrier and Noise Floor		-159.9	-155	dBc/Hz
$\Phi_N(10)$	Clock single-side band phase noise (integer divider)	122.88 MHz	10Hz offset (determined by VCXO)		-83.6		dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)		-103.6		dBc/Hz
$\Phi_N(1k)$			1kHz offset from Carrier		-128	-120	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-140.7	-130	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier		-146.3	-135	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier		-157	-150	dBc/Hz
$\Phi_N(\geq 10M)$			≥10MHz offset from Carrier and Noise Floor		-161.4	-155	dBc/Hz

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Phase noise specifications are applicable for all outputs active, Nx not equal. Measured using a VCXO with the following characteristics: 122.88MHz, phase noise -75dBc/Hz at 0.01kHz, -105dBc/Hz at 0.1kHz, -129dBc/Hz at 1kHz,-147dBc/Hz at 10kHz,-151dBc/Hz at 100kHz; input reference frequency: 122.88MHz, VCXO-PLL bandwidth: 30 Hz, VCXO-PLL charge pump current: 1.6mA, FemtoClockNG PLL bandwidth: 127kHz

Clock Phase Noise Characteristics

Conditions for Phase Noise Characteristics:

VCXO characteristics: f = 30.72MHz and phase noise: -96dBc/Hz (10Hz), -127dBc/Hz (100Hz), -144dBc/Hz (1kHz), -159dBc/Hz (10kHz), -162dBc/Hz (100kHz)

- Input reference frequency: 30.72MHz
- VCXO-PLL bandwidth: 30Hz
- VCXO-PLL charge pump current: 1.6mA
- FemtoClock-NG PLL bandwidth: 139kHz
- VDD_v = 3.3V, T_A = 25°C

Figure 9. 1474.56MHz Output Phase Noise (f_{VCXO} = 30.72MHz)

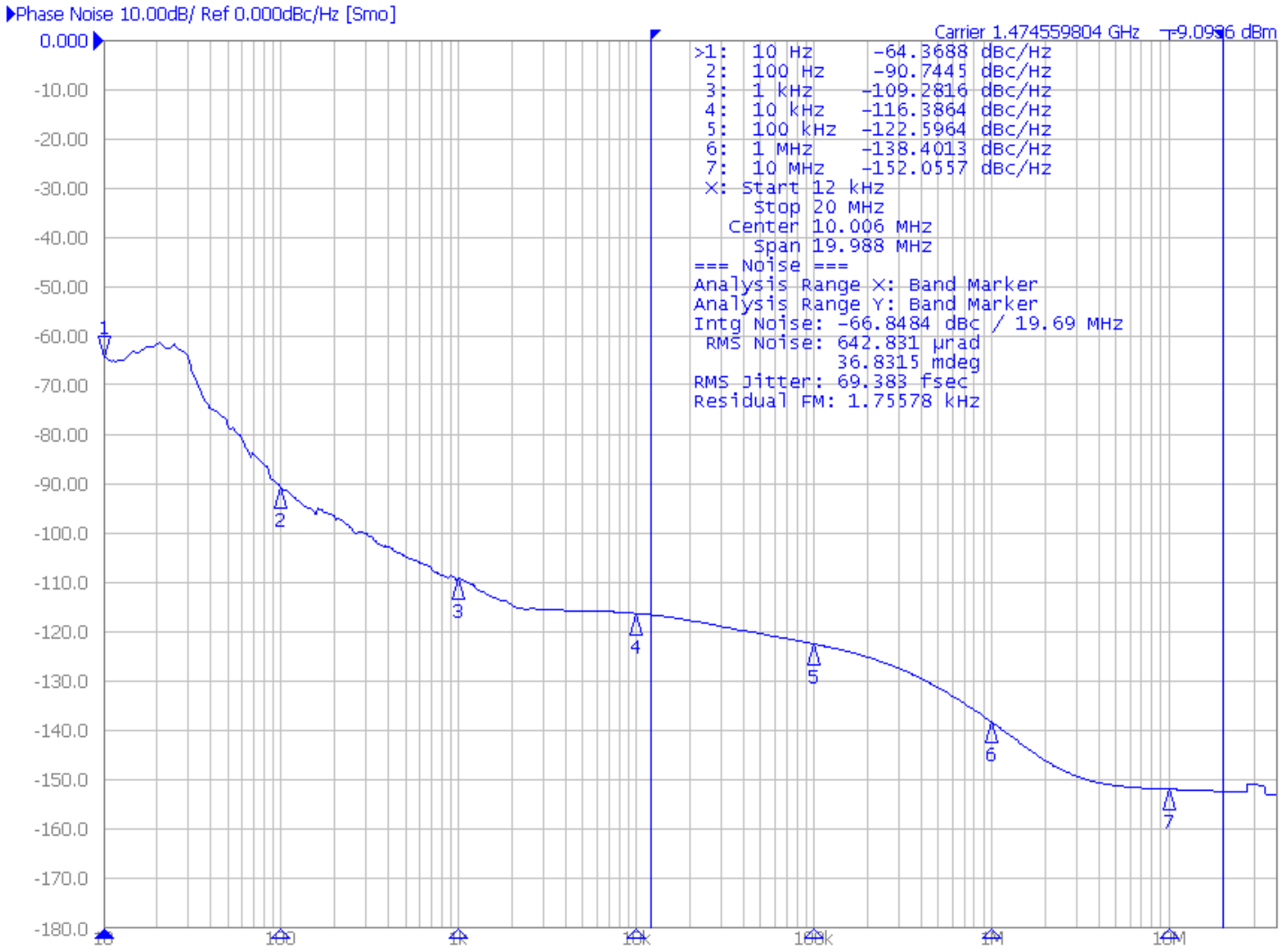


Figure 10. 983.04MHz Output Phase Noise (f_{VCXO} = 30.72MHz)

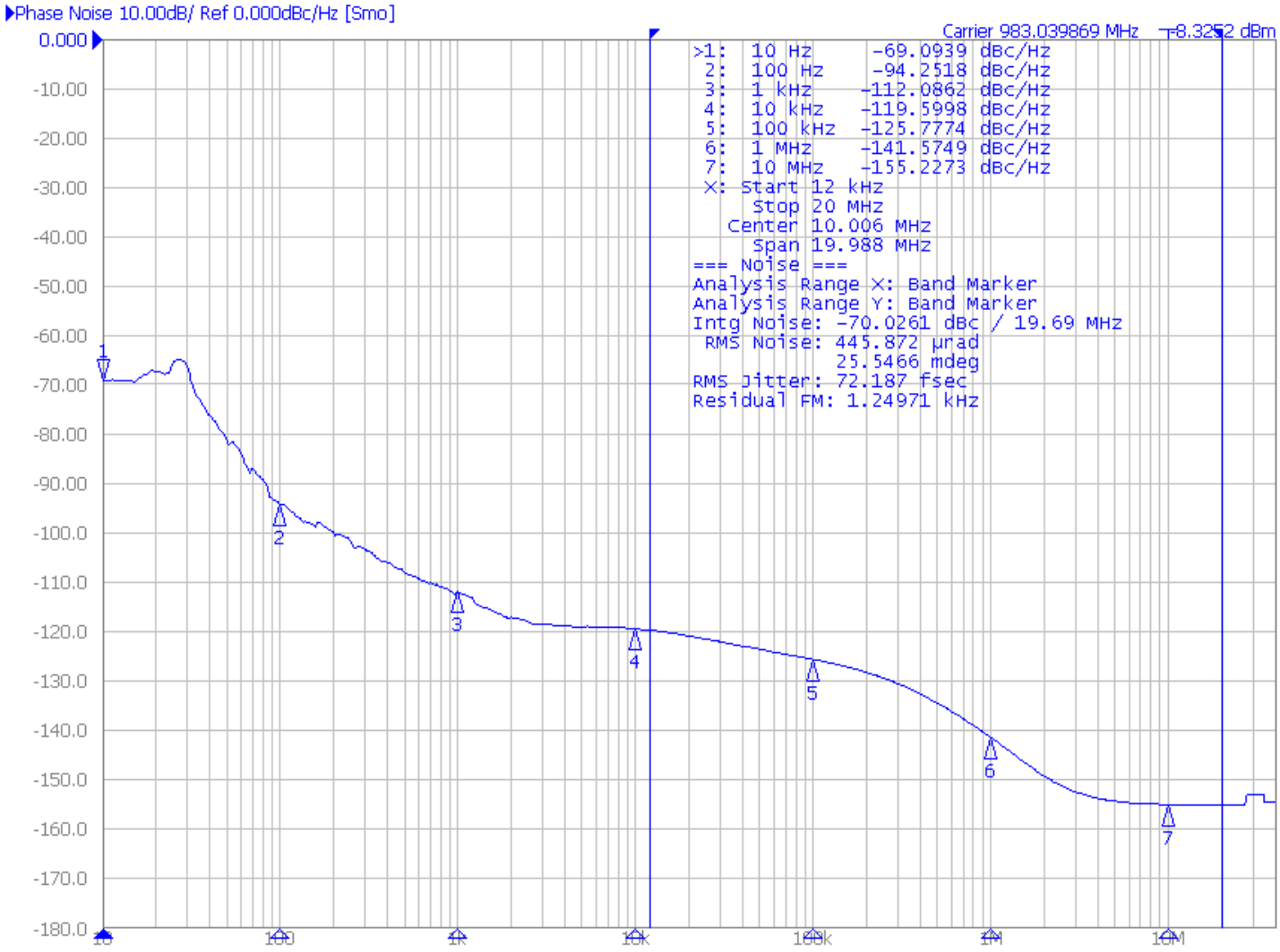


Figure 11. 737.28MHz Output Phase Noise (f_{VCXO} = 30.72MHz)

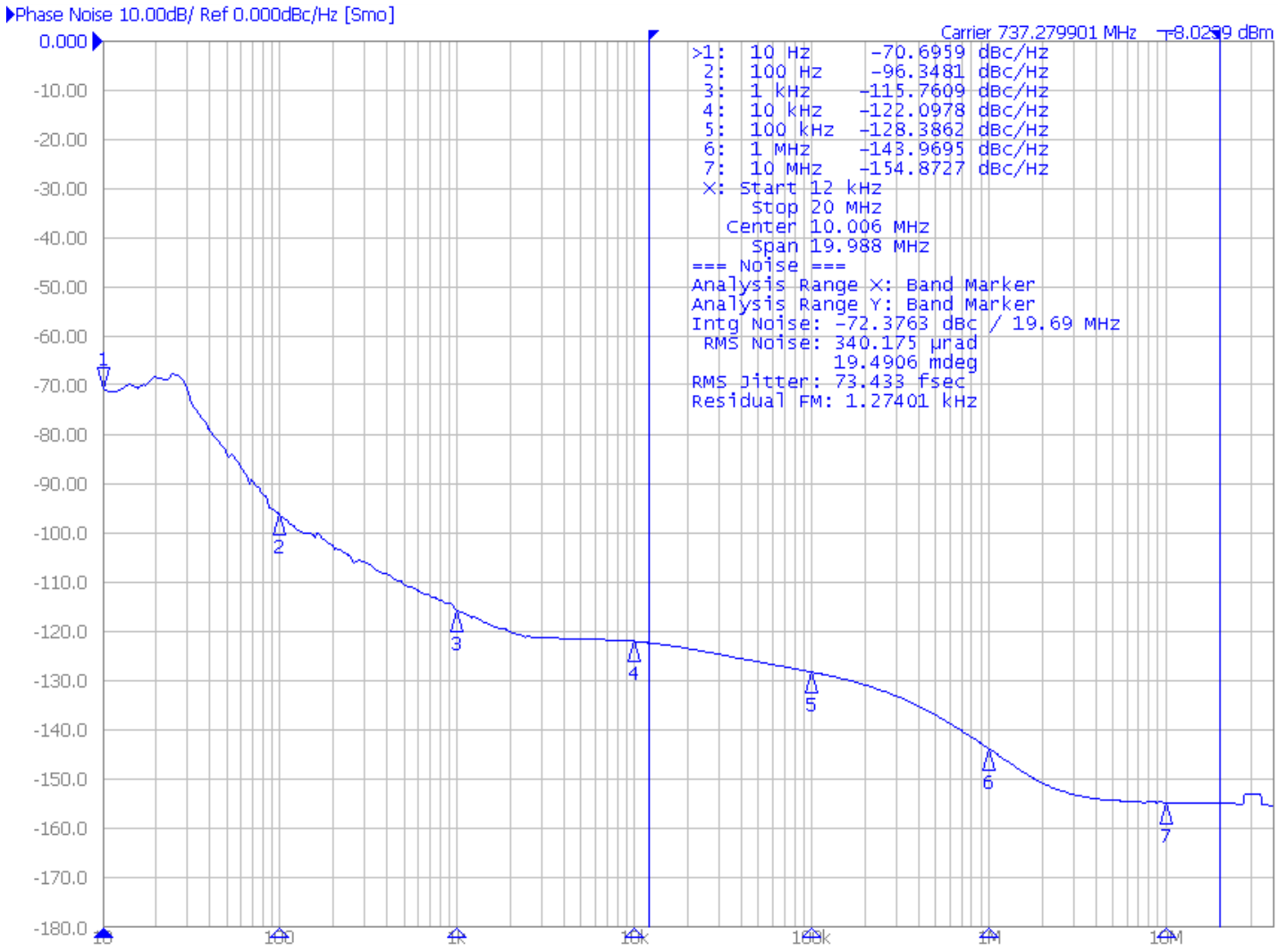


Figure 12. 491.52MHz Output Phase Noise

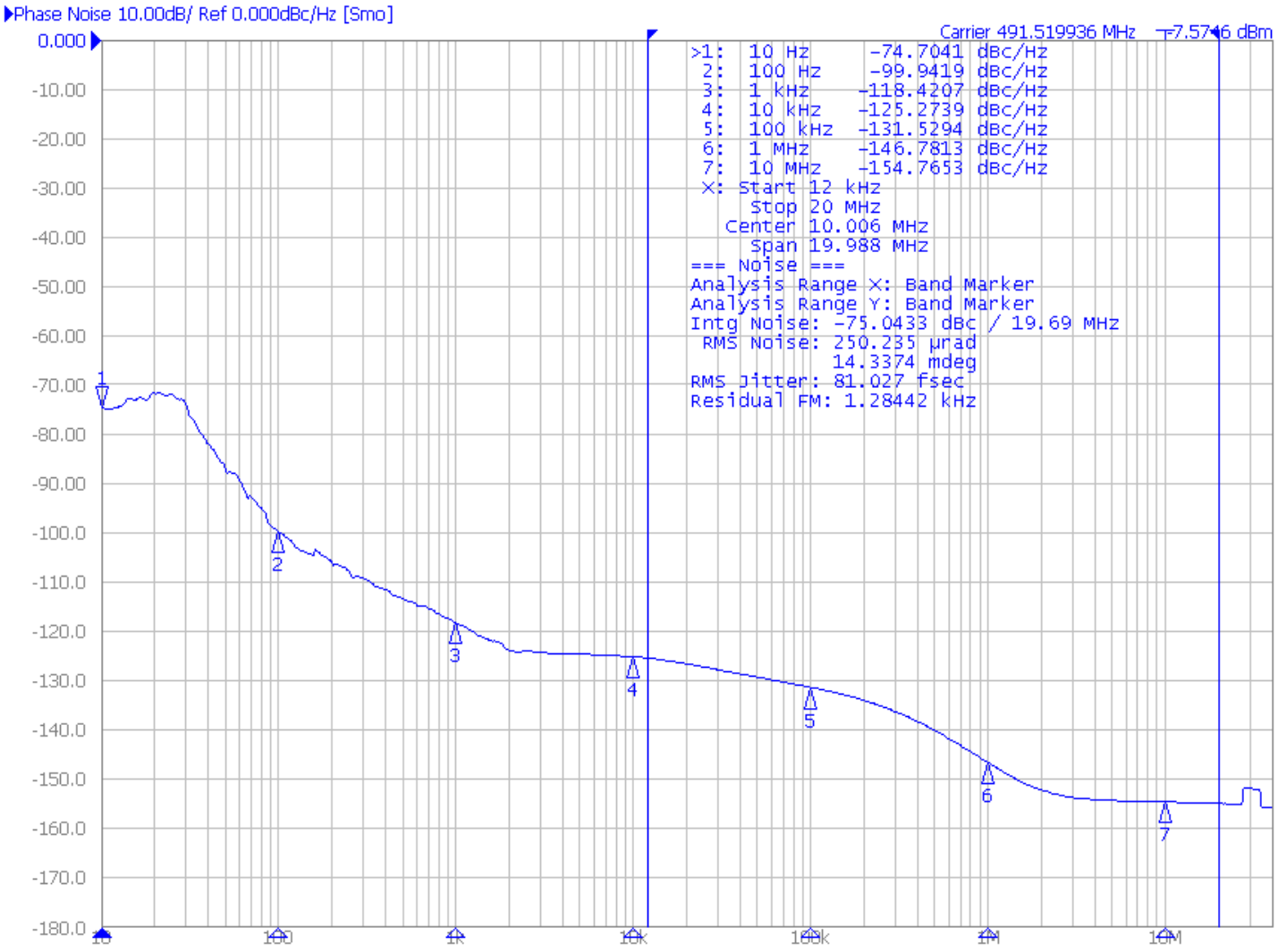


Figure 13. 368.64MHz Output Phase Noise

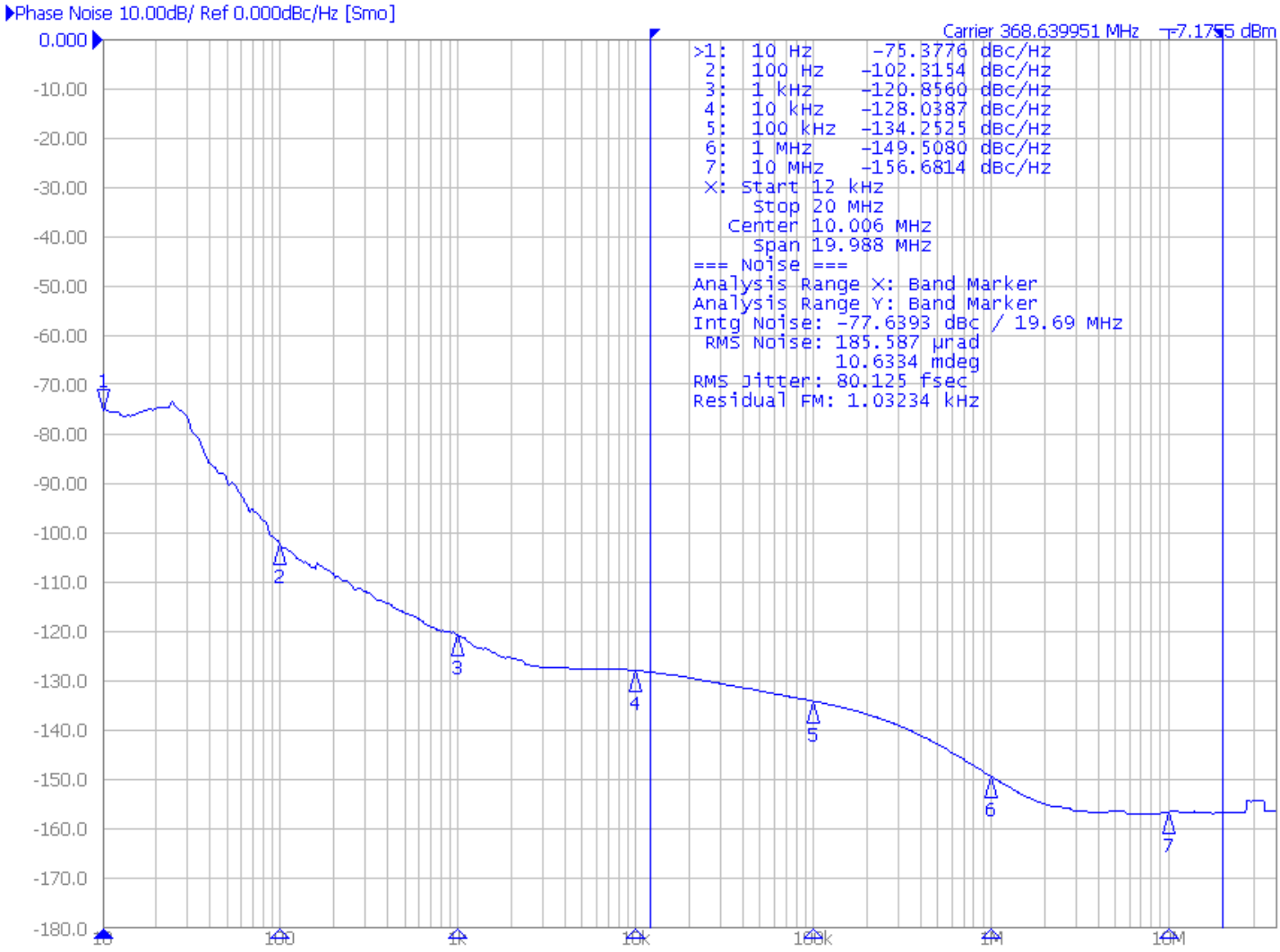


Figure 14. 245.76MHz Output Phase Noise

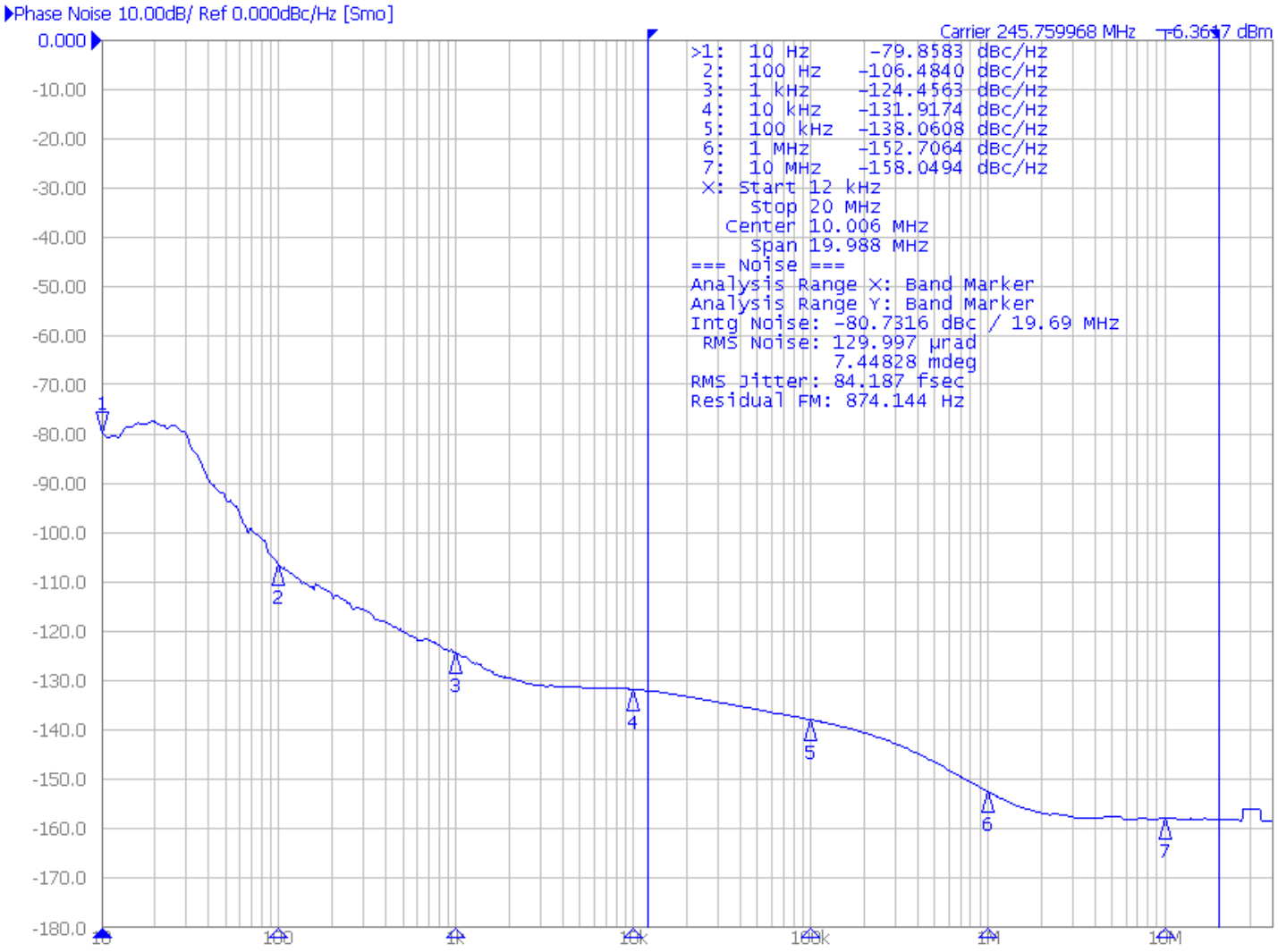


Figure 15. 122.88MHz Output Phase Noise

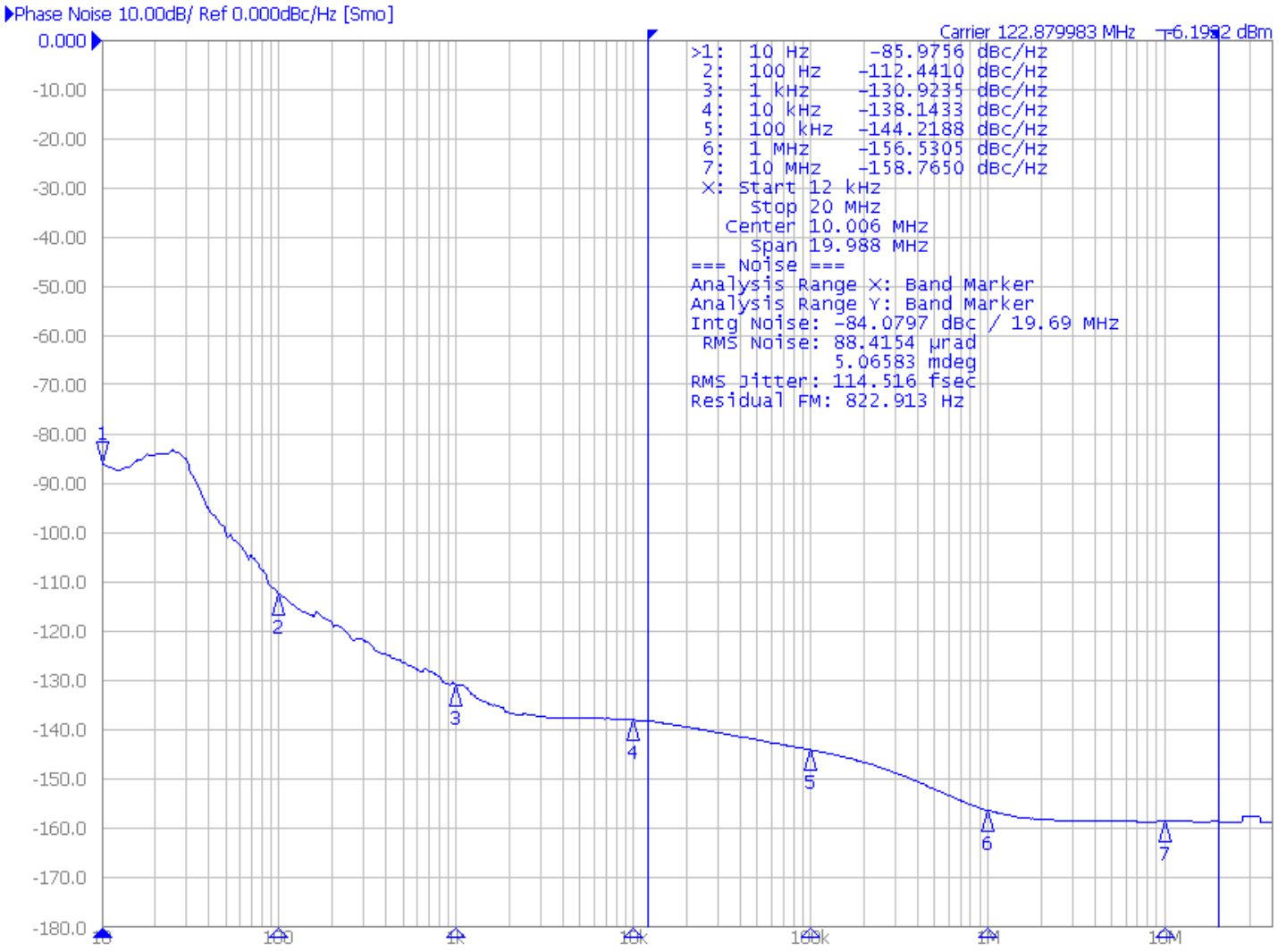


Table 46. Typical QCLK_y Output Amplitude, VDD_v = 3.3V, T_A = 85°C[a]

Symbol	Parameter	Test Conditions	QCLK_y Output Frequency in MHz						Units
			1474.57	1228.8	983.04	737.28	491.52	245.76	
$V_{O(PP)}$[b]	LVPECL Output Voltage Swing, Peak-to-peak	350mV Amplitude Setting	768	715	745	706	736	723	mV
		500mV Amplitude Setting	1027	996	1003	968	1000	994	mV
		700mV Amplitude Setting	1427	1342	1397	1321	1378	1355	mV
		850mV Amplitude Setting	1694	1617	1675	1587	1651	1626	mV
V_{OD}[c]	LVDS Output Voltage Swing, Peak-to-peak	350mV Amplitude Setting	550	581	604	612	627	645	mV
		500mV Amplitude Setting	781	819	851	870	892	909	mV
		700mV Amplitude Setting	1142	1201	1251	1240	1274	1282	mV
		850mV Amplitude Setting	1415	1487	1550	1521	1563	1566	mV

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL outputs terminated 50Ω to V_{TT}. For V_{TT} (Termination voltage) values (see Table 50).

[c] LVDS outputs terminated 100Ω across terminals

Thermal Characteristics

Table 47. Thermal Resistance for 81 FPBGA Package[a]

Multi-Layer PCB, JEDEC Standard Test Board				
Symbol	Thermal Parameter	Condition	Value	Unit
Θ_{JA}	Junction-to-ambient	0 m/s air flow	45.1	°C/W
		2 m/s air flow	39.1	°C/W
Θ_{JC}	Junction-to-case		17.8	°C/W
Θ_{JB}	Junction-to-board[b]		13.2	°C/W

[a] Standard JEDEC 2S2P multilayer PCB.

[b] Thermal model where the heat dissipated in the component is conducted through the board. T_B is measured on or near the component lead.

Temperature Considerations

The device supports applications in a natural convection environment as long as the junction temperature does not exceed the specified junction temperature T_J. In applications where the heat dissipates through the PCB, θ_{JB} is the correct metric to calculate the junction temperature. The following calculation uses the junction-to-board thermal characterization parameter θ_{JB} to calculate the junction temperature (T_J). Care must be taken to not exceed the maximum allowed junction temperature T_J of 125°C.

The junction temperature T_J is calculated using the following equation: $T_J = T_B + P_{TOT} \times \theta_{JB}$

where:

- T_J is the junction temperature at steady state conditions in °C.
- T_B is the board temperature at steady state condition in °C, measured on or near the component lead.
- θ_{JB} is the thermal characterization parameter to report the difference between T_J and T_B.
- P_{TOT} is the total device power dissipation.

Application power dissipation scenarios: Applications may use device settings that result in a lower power dissipation than the maximum power scenario. The 8V19N472 is a multi-functional, high-speed device that targets a variety of applications. Since this device is highly programmable with a broad range of settings and configurations, the power consumption will vary as settings and configurations are changed. Table 38 shows the typical current consumption and total device power consumption along with the junction temperature for the test cases shown in Table 48 and Table 49. The table also displays the maximum board temperature for the Θ_{JB} model.

Reducing power consumption: The output state (on/off) and the output amplitude have the largest impact on the device power consumption and the junction temperature: setting the output amplitude to lower voltages and supplying the outputs by 1.8V reduces power consumption. Unused and periodically unused outputs and inputs should be turned off in phases of inactivity to reduce power. For any given divider setting, the clock frequency has no impact on the device power consumption of the device.

Table 48. Typical Device Power Dissipation and Junction Temperature for LVDS Output Configurations

Test Case[a]	Output Configuration	Device			Θ_{JB} Thermal Model	
		I_{DD_V}	I_{DDO_V}	P_{TOT}	T_J[b]	$T_{B, MAX}$[c]
		mA	mA	W	°C	°C
1	QCLK: LVDS, 350mV, VDDO = 3.3V	314	111	1.390	103.4	106.6
2	QCLK: LVDS, 500mV, VDDO = 3.3V	314	160	1.539	105.3	104.7
3	QCLK: LVDS, 700mV, VDDO = 3.3V	314	202	1.654	106.8	103.2
4	QCLK: LVDS, 850mV, VDDO = 3.3V	315	250	1.792	108.7	101.3
5	QCLK: LVDS, 350mV, VDDO = 1.8V	314	107	1.217	101.1	108.9
6	QCLK: LVDS, 500mV, VDDO = 1.8V	314	149	1.279	101.9	108.1

[a] Configuration: f_{CLK} (input) = 122.88MHz, f_{VCXO} =122.88MHz, 2949.12MHZ VCO selected, PV=÷1000, MV0=÷1000, QA[2:0]=122.88MHz, QB[2:0]=491.52MHz, QC[1:0]=737.28MHz, QD[2:0]=368.64MHz, QE=off, QCLK_V=off. PF=÷1, MF=÷48, FDF=1. I_{CPV}=1.1mA, I_{CPF}=6.4mA, QCLK_y outputs terminated according to amplitude settings.

[b] Junction temperature at board temperature T_B = 85°C.

[c] Maximum board temperature for junction temperature <125°C: $T_{B, MAX} = T_{J, MAX} - \Theta_{JB} \times P_{TOT}$.

Table 49. Typical Device Power Dissipation and Junction Temperature for LVPECL Output Configurations

Test Case[a]	Output Configuration	Device			Θ_{JB} Thermal Model	
		I_{DD_V}	I_{DDO_V}	P_{TOT}	T_J[b]	$T_{B, MAX}$[c]
		mA	mA	W	°C	°C
1	QCLK: LVPECL, 350mV, VDDO = 3.3V	330	233	1.392	103.4	106.6
2	QCLK: LVPECL, 500mV, VDDO = 3.3V	332	261	1.408	103.6	106.4
3	QCLK: LVPECL, 700mV, VDDO = 3.3V	329	301	1.518	105.0	105.0
4	QCLK: LVPECL, 850mV, VDDO = 3.3V	331	332	1.571	105.7	104.3
5	QCLK: LVPECL, 350mV, VDDO = 1.8V	312	231	1.406	103.6	106.4
6	QCLK: LVPECL, 500mV, VDDO = 1.8V	319	263	1.458	104.2	105.8

[a] Configuration: f_{CLK} (input) = 122.88MHz, f_{VCXO} =122.88MHz, 2949.12MHZ VCO selected, PV=÷1000, MV0=÷1000, QA[2:0]=122.88MHz, QB[2:0]=491.52MHz, QC[1:0]=737.28MHz, QD[2:0]=368.64MHz, QE=off, QCLK_V=off. PF=÷1, MF=÷48, FDF=1. I_{CPV}=1.1mA, I_{CPF}=6.4mA, QCLK_y outputs terminated according to amplitude settings.

[b] Junction temperature at board temperature T_B = 85°C.

[c] Maximum board temperature for junction temperature <125°C: $T_{B, MAX} = T_{J, MAX} - \Theta_{JB} \times P_{TOT}$.

Applications Information

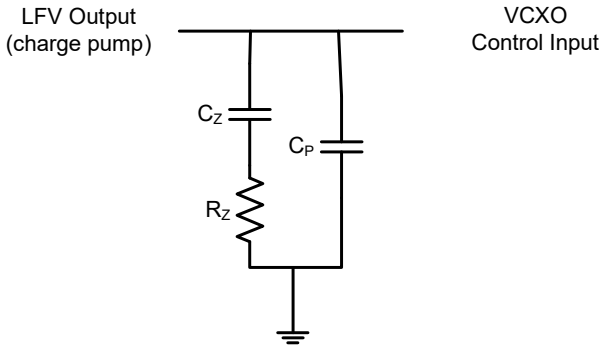
VCXO-PLL Loop Filter

Each of the two PLLs uses a loop filter with external components. The value of the external components depends on the desired loop bandwidth for each PLL, the input clock frequency and in the case of the VCXO-PLL, on the external VCXO component. For the VCXO-PLL (first PLL stage), a 2nd or 3rd order loop filter can be used. The loop filter of the VCXO-PLL is connected to the device through the LFV charge pump input. The filter output is connected to the control voltage input of the external VCXO. The FemtoClock NG PLL (second PLL stage) can use a 2nd order loop filter. The LFF output of the device connects to filter input and LFFR to the filter output.

Typical loop filters are shown in Figure 16 (2nd order) in Figure 17 (3rd order) and are discussed below. Step by step calculations to determine the value of the loop filter components values are shown.

Second-Order Loop Filter

Figure 16. Second-Order Loop Filter



Step-by-step calculation:

Step 1: Determine the desired loop bandwidth f_C. f_C must satisfy the following condition:

$$\frac{f_{PD}}{f_C} \gg 20$$

Where f_{PD} is the input frequency of the VCXO-PLL phase detector frequency.

Step 2: Calculate R_Z by:

$$R_Z = \frac{2\pi \times f_C M_V}{I_{CP} \times K_{VCXO}}$$

Where I_{CP} is the VCXO-PLL charge pump current and K_{VCXO} is the gain of the VCXO component (consult the datasheet of the external VCXO for its gain parameter). M_V is the effective feedback divider:

$$M_V = \frac{f_{VCXO}}{f_{PD}}$$

f_{VCXO} is the frequency of the external VCXO component.

Step 3: Calculate C_Z by:

$$C_Z = \frac{\alpha}{2\pi f_C R_Z}$$

$$\alpha = \frac{f_C}{f_Z}$$

α is ratio between the loop bandwidth and the filter zero. f_Z is the filter zero. α should be greater than 3.

Step 4: Calculate C_P by:

$$C_P = \frac{C_Z}{\alpha\beta}$$

$$\beta = \frac{f_P}{f_C}$$

f_P is the pole and β is ratio between the pole and the loop bandwidth. β should be greater than 3.

Step 4: Verify that the phase margin PM is greater than 50°.

$$PM = \operatorname{atan}\frac{b-1}{2\sqrt{b}}$$

$$b = \frac{C_Z}{C_P} + 1$$

Example calculation: Figure 16 shows a 2nd order loop filter for the VCXO-PLL. In this example, the VCXO-PLL reference frequency is 122.88MHz and an external VCXO component of 122.88MHz is used. The desired VCXO-PLL loop bandwidth f_C is 40Hz. To achieve the desired loop bandwidth with small size loop filter components, set the PLL frequency pre-divider P_V and the PLL feedback divider M_V to 1024. According to the step 1 instruction, f_{PD} is 120kHz. This satisfies the condition $f_{PD}/f_C >> 20$. R_Z is calculated 32.2kΩ.

The VCXO gain K_{VCXO} used for the device reference circuit is 10kHz/V. The charge pump current of the VCXO-PLL is configurable from 50µA to 1200µA. The charge pump current is programmed to $I_{CP} = 800uA$. For $\alpha = 8$, C_Z is calculated to be 0.99µF. C_Z greater than this value assures α > 12. For example, the actual chosen value is the standard capacitor value of 1µF. For $\beta = 5$, C_P is calculated 24.7nF. The standard capacitor value of $C_P = 27ps$ ensures β > 7.

Third-Order Loop Filter

Figure 17. Third Order Loop Filter

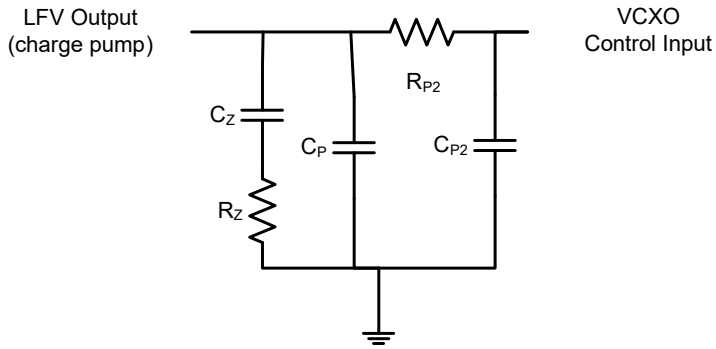


Figure 17 shows a third-order loop filter. The filter is equivalent to the 2nd order filter in Figure 16 with the addition components R_{P2} and C_{P2}. The additional components R_{P2} and C_{P2} should be calculated as shown:

$$C_{P2} = \frac{C_P \times R_Z}{\gamma \times R_{P2}}$$

$$R_{P2} \sim R_Z \times 1.5$$

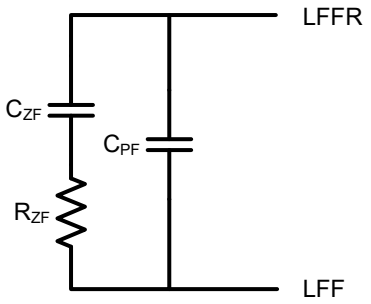
γ is the ratio between the 1st pole and the 2nd pole. γ should be greater than 3.

Example calculation for the 3rd order loop filter shown in Figure 17: Equivalent to the 2nd order loop filter calculation, $R_Z = 33k\Omega$, $C_Z = 1\mu F$, and $C_P = 27nF$. R_{P2} should be in the range of $0.5 \times R_Z < R_{P2} < 2.5 \times R_Z$, for instance $51k\Omega$. With $\gamma = 4$, C_{P2} is 4.37nF (select $4.7\mu F$).

FemtoClock NG PLL Loop Filter

Figure 18 shows a 2nd order loop filter for the FemtoClock NG PLL. This loop filter is equivalent to Figure 16 and uses the loop filter components R_{ZF} (R_Z), C_{ZF} (C_Z) and C_{PZ} (C_P). The VCO frequency of the FemtoClock NG PLL is 2949.12MHz.

Figure 18. 2nd Order Loop Filter for the FemtoClock NG PLL



Example calculation for the 2nd order loop filter shown in Figure 18: the FemtoClock NG receives its reference frequency from the VCXO output. With the P_F pre-divider set to 1, the phase detector frequency is also 122.88MHz. The PLL feedback divider must be set to $M_F = 24$ in order to locate the VCO frequencies in its center range. A target PLL loop bandwidth f_C is 80kHz satisfies the condition in step 1. The gain of the internal VCO is 30MHz/V and the charge pump current I_{CP} is set to 3.6mA. Using the formula for R_Z in step 2, R_{ZF} is calculated 103Ω (chose the standard value of 100Ω); using the formula for C_Z in step 3, C_{ZF} is calculated 88nF for $\alpha = 4$. A capacitor larger than 88nF should be used for C_{ZF} to assure that the α is greater than 4, for instance the standard component capacitor value 100nF.

The recommended C_{PF} value for the loop filter is 40pF (loop filter components are partially integrated). The selected 2nd order loop filter components for this PLL are: $R_{ZF} = 100\Omega$, $C_{ZF} = 100nF$, and $C_{PF} = 40pF$.

Output Termination

LVPECL-style outputs

Differential outputs configured to LVPECL-style are of open-emitter type and require a termination with a DC current path to GND. This section displays parallel and thevenin termination, Y-termination and source termination for various output supply (VDDO_v), and amplitude settings. V_{TT} is the termination voltage.

Figure 19. Parallel Termination 1

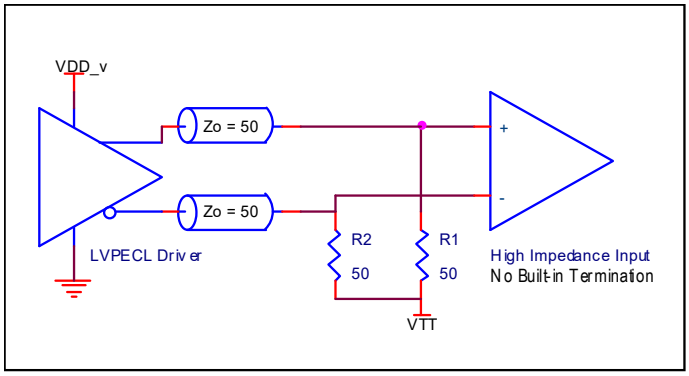


Table 50. Termination Voltage V_{TT} for Figure 19[a]

LVPECL Amplitude (mV)	V_{TT} (V)
350	VDDO_v – 1.60
500	VDDO_v – 1.75
700	VDDO_v – 1.95
850	VDDO_v – 2.10

[a] Output power supplies supporting 3.3V, 2.5V and 1.8V are VDDO_QCLKA, VDDO_QCLKB, VDDO_QCLKC and VDDO_QCLKD.

Figure 20. Parallel Termination 2

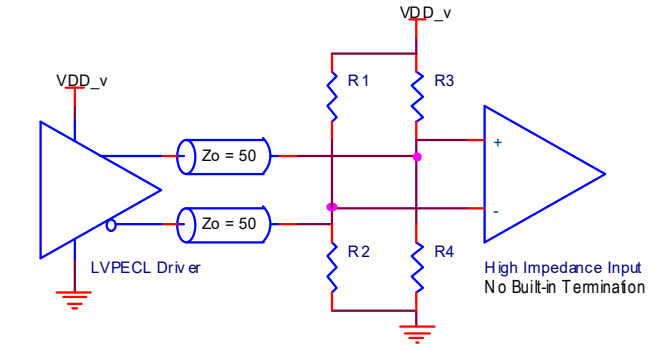


Table 51. Termination Resistor Values for Figure 20

VDDO_v (V)[a]	LVPECL Amplitude (mV)	R1, R3 (Ω)	R2, R4 (Ω)
3.3	350	97.1	103.1
	500	106.5	94.3
	700	122	84.6
	850	137.5	78.6
2.5	350	138.8	78.1
	500	166.7	71.4
	700	227.3	64.1
	850	312.5	59.5
1.8	350	450	56.3
	500	–	50

[a] Output power supplies supporting 3.3V, 2.5V and 1.8V are VDDO_QCLKA, VDDO_QCLKB, VDDO_QCLKC and VDDO_QCLKD.

Figure 21. Y-Termination

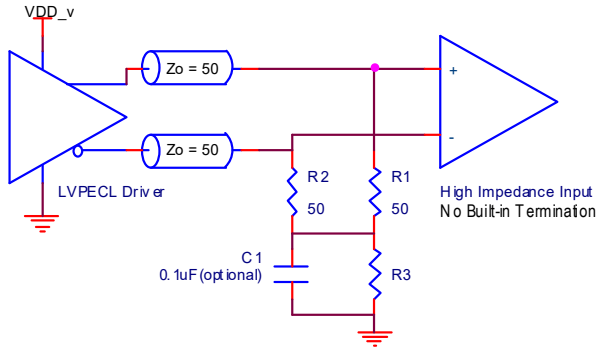


Table 52. Termination Resistor Values for Figure 21

VDDO_v (V)[a]	LVPECL Amplitude (mV)	R3 (Ω)
3.3	350, 500, 700, 850	50
2.5	350, 500, 700, 850	18
1.8	350, 500	0

[a] Output power supplies supporting 3.3V, 2.5V and 1.8V are VDDO_QCLKA, VDDO_QCLKB, VDDO_QCLKC and VDDO_QCLKD.

Figure 22. Source Termination

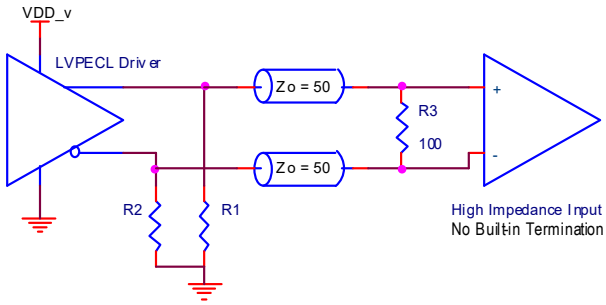


Table 53. Termination Resistor Values for Figure 22

VDDO_v (V)[a]	LVPECL Amplitude (mV)	R1, R2 (Ω)
3.3	350, 500, 700, 850	100 – 200
2.5	350, 500, 700, 850	80 – 150
1.8	350	50 – 100

[a] Output power supplies supporting 3.3V, 2.5V and 1.8V are VDDO_QCLKA, VDDO_QCLKB, VDDO_QCLKC and VDDO_QCLKD.

Figure 23. LVDS-Style Outputs (1)

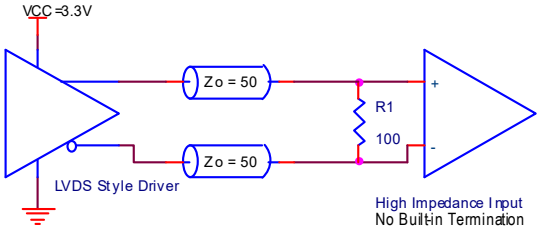
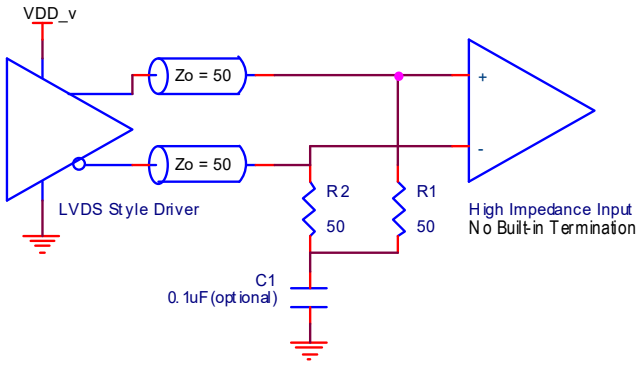


Figure 24. LVDS-Style Outputs (2)



LVDS style outputs support fully differential terminations. LVDS does not require board level pull-down resistors for DC termination. Figure 23 and Figure 24 show typical termination examples with DC coupling for the LVDS style driver. In these examples, the receiver is high input impedance without built-in termination. LVDS-style with a differential termination is preferred for best common-mode rejection and lowest device power consumption.

Power Supply Filtering

Please refer to the document *8V19N470 Hardware Design Guide* for comprehensive information about power supply and isolation, loop filter design for VCXO and VCO, schematics, input and output interfaces/terminations, and an example schematics. This document shows a recommended power supply filter schematic in which the device is operated at VDD_v = 3.3V (The output supply voltages of VDDO_v = 3.3V, 2.5V and 1.8V are supported). This example focuses on power supply connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set for the application.

As with any high-speed analog circuitry, the power supply pins are vulnerable to board supply or device generated noise. This device requires an external voltage regulator for the VDD_v pins for isolation of board supply noise. This regulator (example component: PS7A8300RGT) is indicated in the schematic by the power supply, VREG_3.3V. Consult the voltage regulator specification for details of the required performance. To achieve optimum jitter performance, power supply isolation is required to minimize device generated noise. The VDD_LCF terminal requires the cleanest power supply. The device provides separate power supplies to isolate any high switching noise from coupling into the internal PLLs and into other outputs as shown. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited the 0.1µF and 0.01µF capacitors in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Pull-up and pull-down resistors to set configuration pins can all be placed on the PCB side opposite the device side to free up device side area if necessary.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

Package Outline Drawings

Figure 25. Package Outline Drawings – Sheet 1

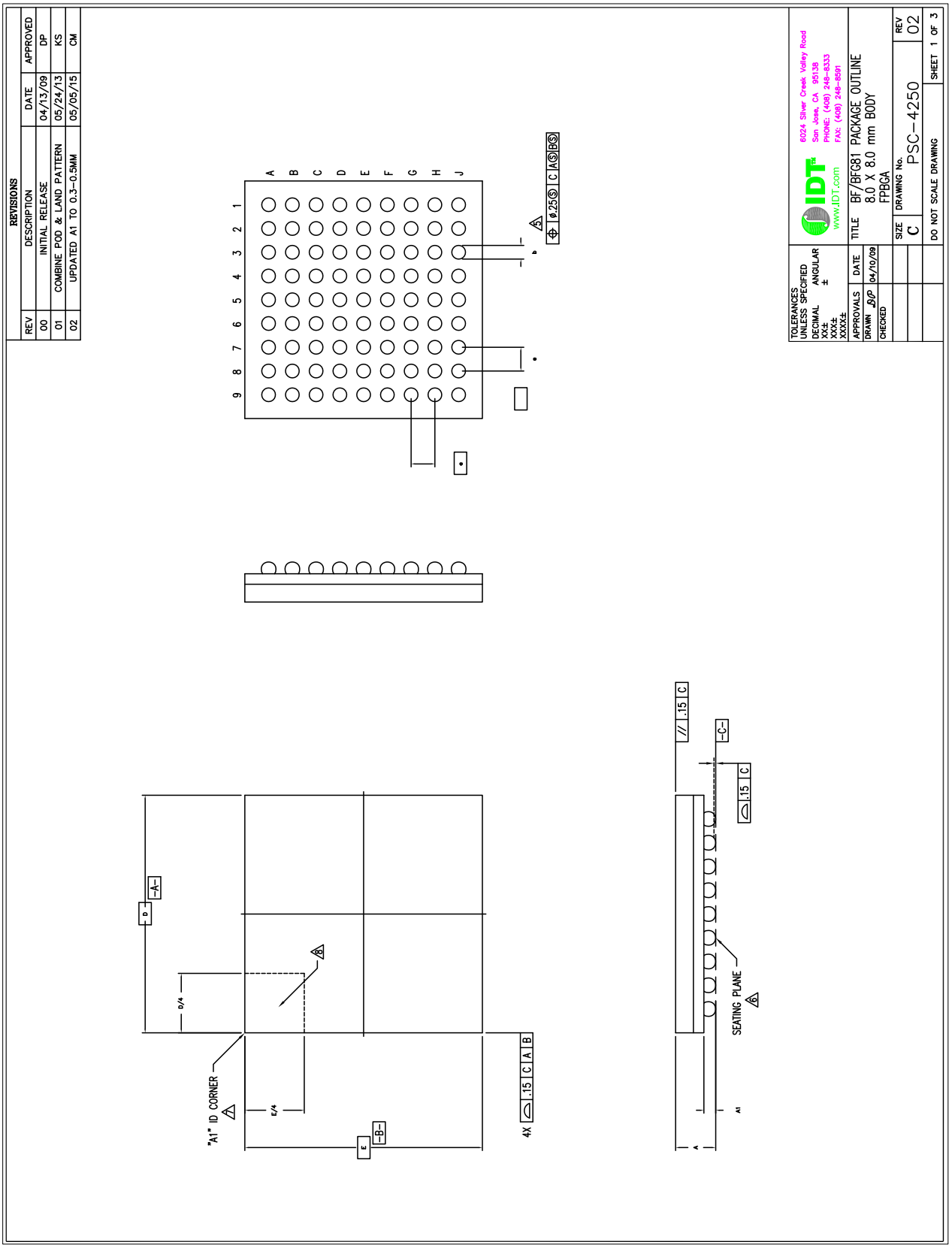


Figure 26. Package Outline Drawings – Sheet 2

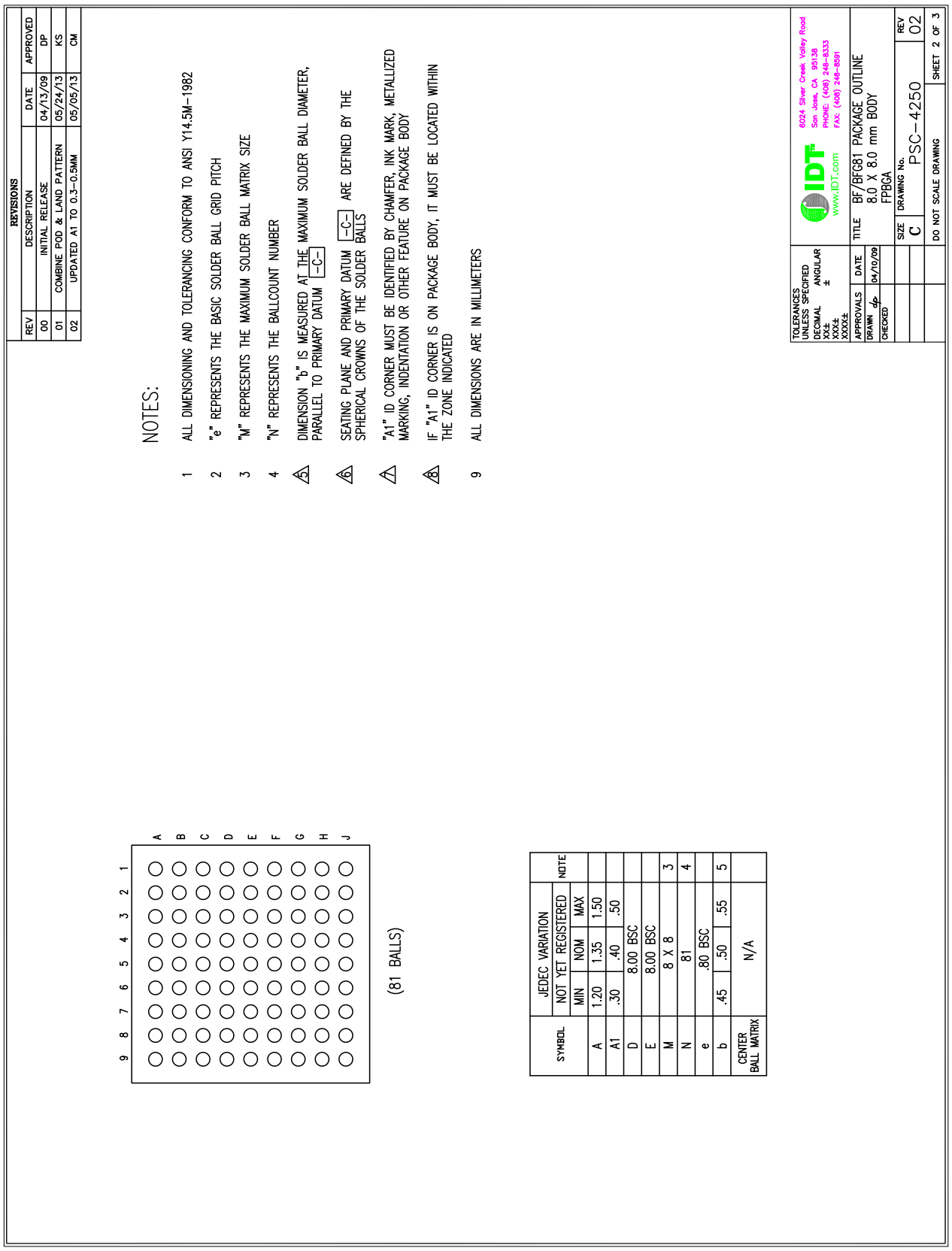
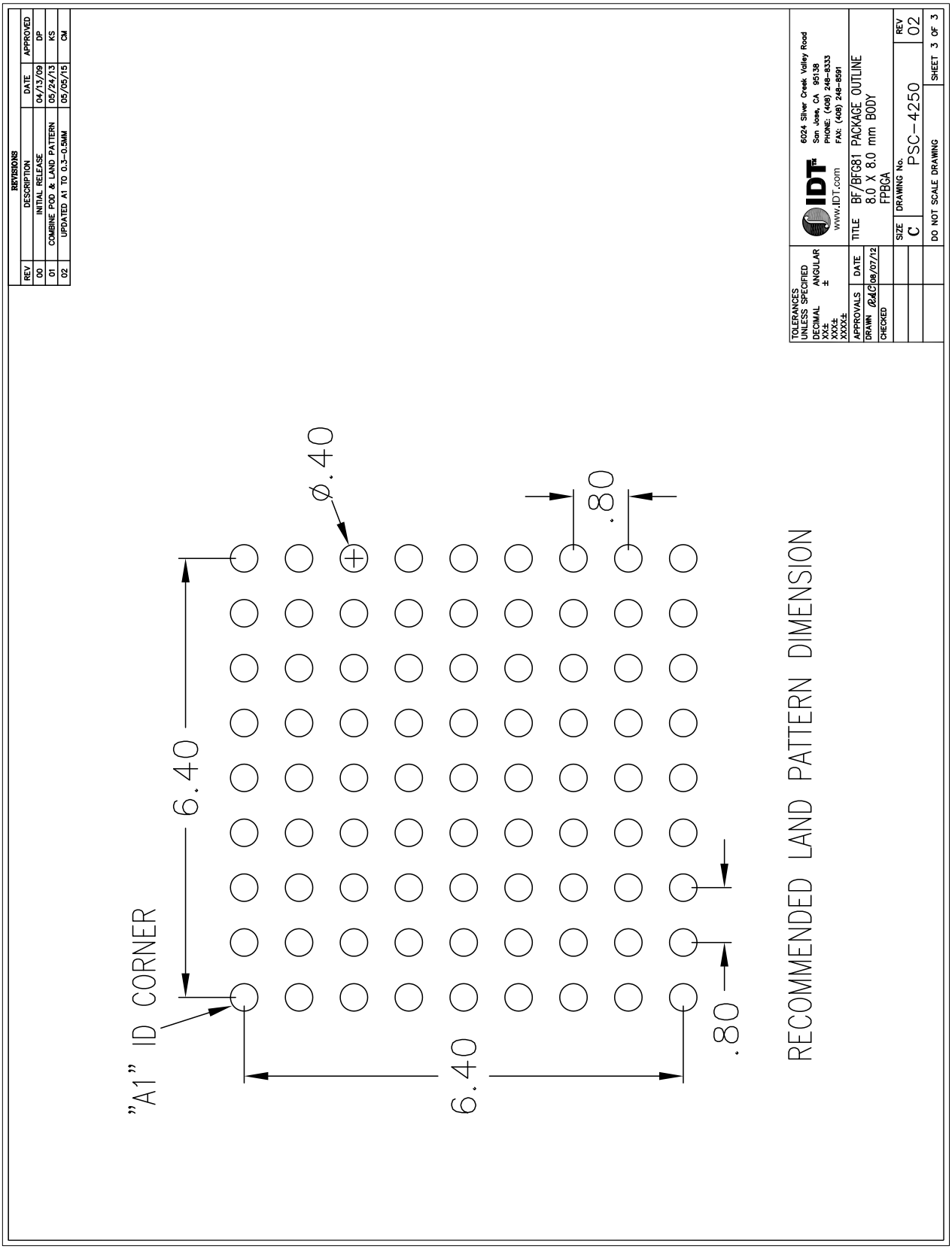


Figure 27. Package Outline Drawings – Sheet 3



Marking Diagram

Figure 28. Marking Diagram

1. Lines 1 and 2 indicate the part number.
2. Line 3 indicates the package part number code.
3. Line 4 indicates the following:
   - "YYWW" is the last digit of the year and week that the part was assembled.
   - #: denotes sequential lot number.
   - $: denotes mark code.

Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V19N472BFGI	IDT8V19N472BFGI	8 × 8 × 1.35 mm, 81-FPBGA	Tray	-40°C to +85°C
8V19N472BFGI8	IDT8V19N472BFGI	8 × 8 × 1.35 mm, 81-FPBGA	Tape & Reel	-40°C to +85°C

Glossary

Table 54. Abbreviations and Nomenclature

Abbreviation	Description
Index *n*	Denominates an clock input. Range: 0 to 1
Index *x*	Denominates a channel, channel frequency divider and the associated configuration bits. Range: A, B, C, D, E
Index y	Denominates a QCLK output and associated configuration bits. Range: A0, A1, A2, B0, B1, B2, C0, C1, D0, D1, E
VDD_v	Denominates core voltage supply pins. Range: VDD_QCLKA, VDD_QCLKB, VDD_QCLKC, VDD_QCLKD, VDD_QCLKE, VDD_SPI, VDD_INP, VDD_LCV, VDD_LCF, VDD_CPV, VDD_CPF and VDD_OSC
VDDO_v	Denominates output voltage supply pins. Range: VDDO_QCLKA, VDDO_QCLKB, VDDO_QCLKC and VDDO_QCLKD
status_condition	Status conditions are: LOLV (Loss of VCXO-PLL lock), LOLF (Loss of FemtoClockNG-PLL lock) and LOS (Loss of input signal)
[...]	Index brackets describe a group associated with a logical function or a bank of outputs.
{…}	List of discrete values
Suffix V	Denominates a function associated with the VCXO-PLL
Suffix F	Denominates a function associated with the 2nd stage PLL (FemtoClock NG)

Revision History

Revision Date	Description of Change
November 7, 2017	Initial release.

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