

## Description

The 8V19N491-24 is a fully integrated FemtoClock NG Jitter Attenuator and Clock Synthesizer that is designed as a high-performance clock solution for conditioning and frequency/phase management of wireless base station radio equipment boards. The device is optimized to deliver excellent phase noise performance as required in GSM, WCDMA, LTE, and LTE-A radio board implementations. The device supports JESD204B subclass 0 and 1 clocks. A two-stage PLL architecture supports both jitter attenuation and frequency multiplication. The first stage PLL is the jitter attenuator and uses an external VCXO for best possible phase noise characteristics. The second stage PLL locks on the VCXO-PLL output signal and synthesizes the target frequency.

The 8V19N491-24 supports the clock generation of high-frequency clocks from the selected VCO and low-frequency synchronization signals (SYSREF). SYSREF signals are internally synchronized to the clock signals. Delay functions exist for achieving alignment and controlled phase delay between system reference and clock signals and to align/delay individual output signals. The four redundant inputs are monitored for activity.

Four selectable clock switching modes are provided to handle clock input failure scenarios. Auto-lock, individually programmable output frequency dividers, and phase adjustment capabilities are added for flexibility. The device is configured through a selectable 3/4-wire SPI interface and reports lock and signal loss status in internal registers and via an lock detect (LOCK) output. Internal status bit changes can also be reported via the nINT output.

The 8V19N491-24 is ideal for driving converter circuits in wireless infrastructure, radar/imaging and instrumentation/medical applications.

## Typical Applications

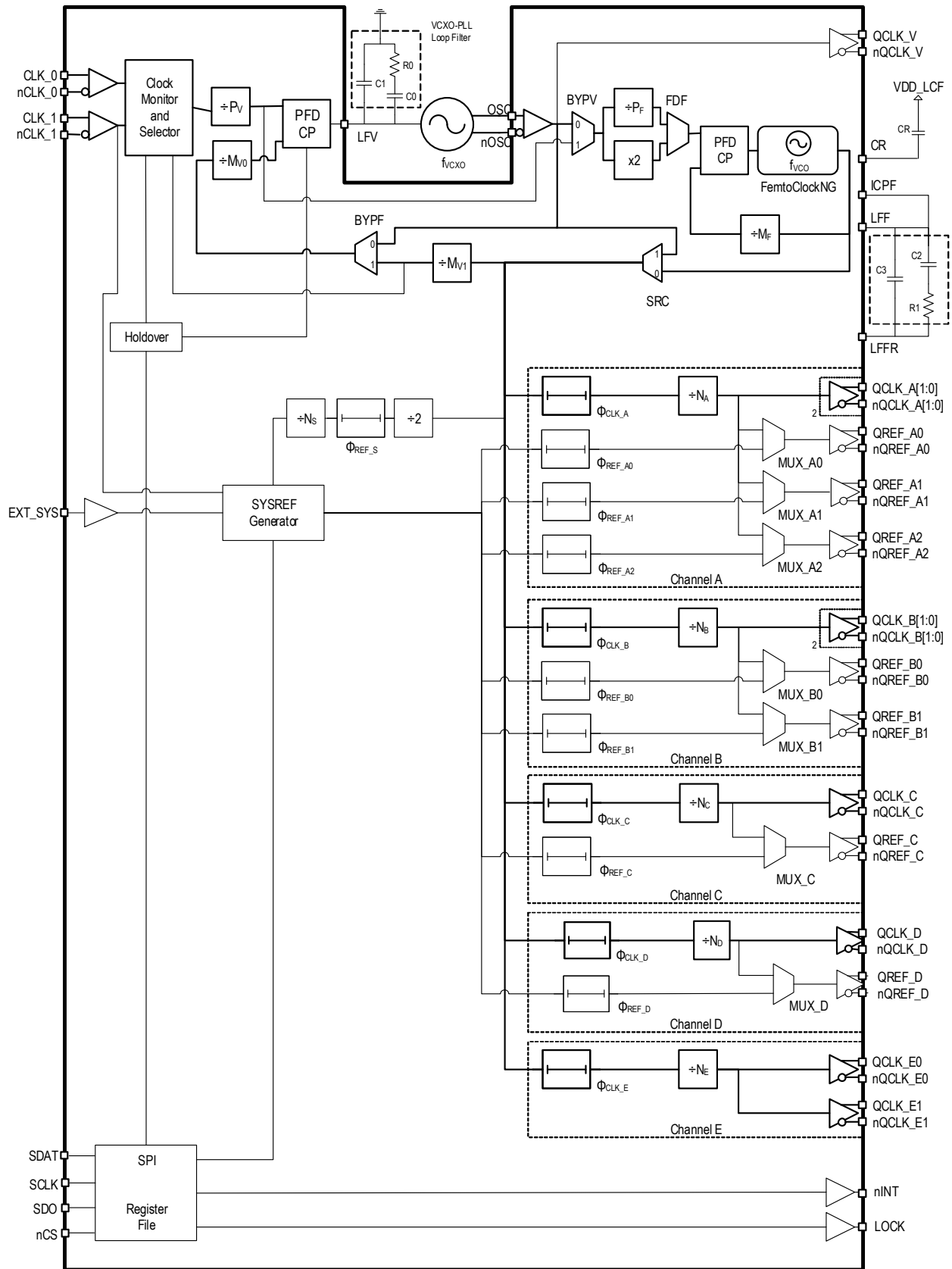
- Wireless infrastructure applications: GSM, WCDMA, LTE, LTE-A, 5G
- Ideal clock driver for jitter-sensitive ADC and DAC circuits
- Low phase noise clock generation
- Ethernet line cards
- Radar and imaging
- Instrumentation and medical

## Features

- High-performance clock RF-PLL with support for JESD204B/C
- Optimized for low phase noise: -155dBc/Hz (1MHz offset; 245.76MHz clock, and 491.52MHz VCXO)
- Integrated phase noise of 80fs RMS typical (12k–20MHz).
- Dual-PLL architecture
- First PLL stage with external VCXO for clock jitter attenuation
- Second PLL with internal FemtoClock NG PLL: 2457.6MHz
- Six output channels with a total of 16 outputs, organized in:
  - Four JESD204B channels (device clock and SYSREF output) with two, four, and five outputs
  - One clock channel with two outputs
  - One VCXO output
- Configurable integer clock frequency dividers
- Supported clock output frequencies include: 2457.6, 1228.8, 614.4, 491.52, 307.2, 245.76, 153.6, and 122.88MHz
- Low-power LVPECL/LVDS outputs support configurable signal amplitude, DC and AC coupling, and LVPECL, LVDS line terminations techniques
- Phase delay circuits
  - Clock phase delay with 256 steps of 407ps and a range of 0 to 103.76 ns
  - Individual SYSREF phase delay with 8 steps of 407ps
  - Additional individual SYSREF fine phase delay with 25ps steps
  - Global SYSREF signal delay with 256 steps of 814ps and a range of 0 to 207.52 ns
- Redundant input clock architecture with two inputs including:
  - Input activity monitoring
  - Manual and automatic, fault-triggered clock selection modes
  - Priority controlled clock selection
  - Digital holdover and hitless switching
  - Differential inputs accept LVDS and LVPECL signals
- SYSREF generation modes include internal and external trigger mode for JESD204B
- Supply voltage: 3.3V
- SPI interface, 3/4 wire configurable
- SPI and control I/O voltage: 1.8V/3.3V (configurable)
- Package: 10 × 10 mm, 88-VFQFPN
- Temperature range: -40°C to +105°C (Case)

# Block Diagram

Figure 1. Block Diagram ( $f_{VCO} = 2457.6\text{MHz}$ )



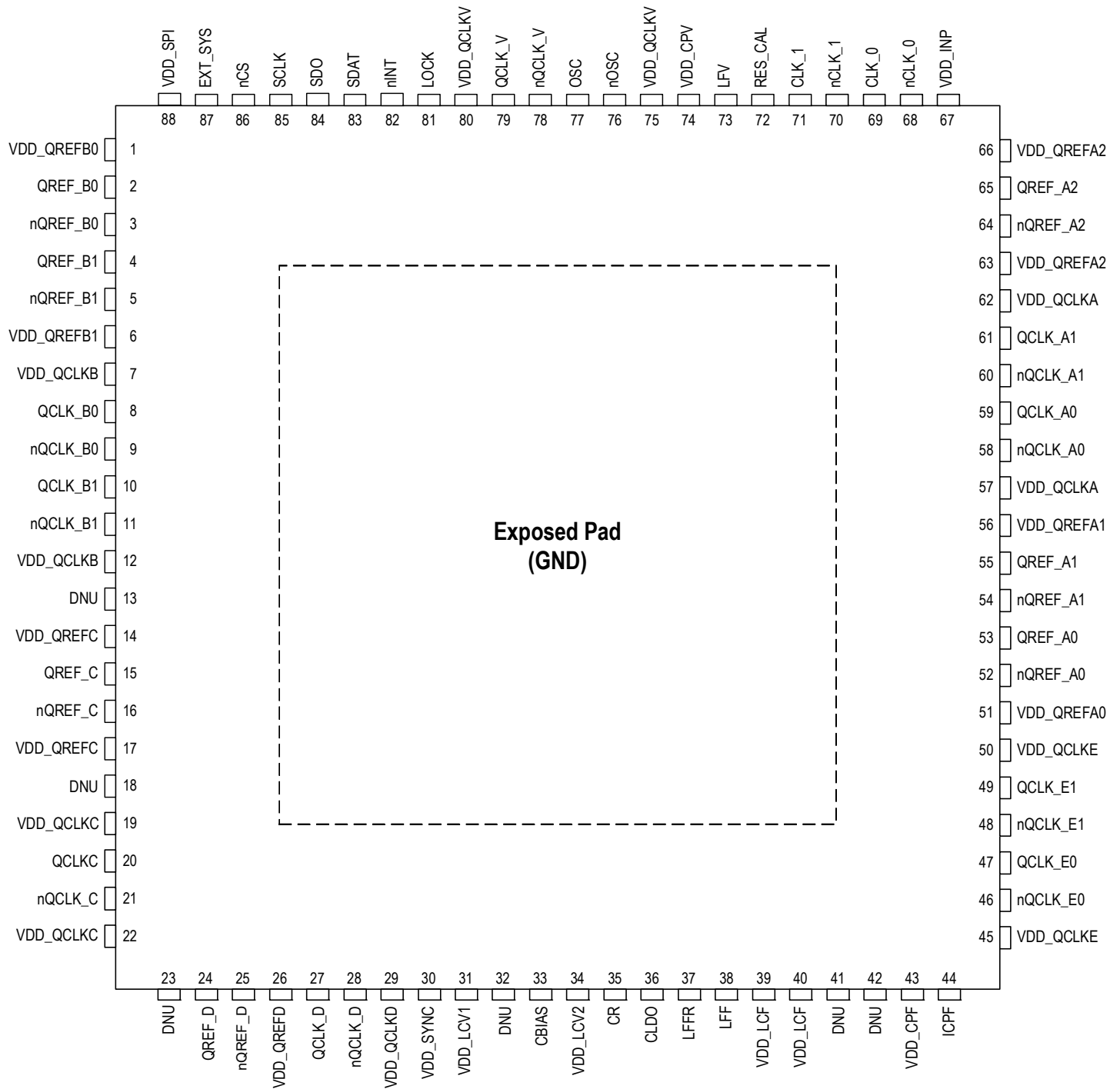
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# Pin Assignments

**Figure 2. Pin Assignments for 10 × 10 mm 88-VFQFPN Package with Exposed Pad (Top View)**



## Pin Descriptions

**Table 1. Pin Descriptions [a]**

Pin	Name	Type <sup>[b]</sup>		Description
69	CLK_0	Input	PD	Device clock 0 non-inverting and inverting differential clock input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
68	nCLK_0		PD/PU	
71	CLK_1	Input	PD	Device clock 1 non-inverting and inverting differential clock input/SYSREF input. Inverting input is biased to $V_{DD\_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals. See SR_INSEL register bit for input selection.
70	nCLK_1		PD/PU	
59, 58	QCLK_A0, nQCLK_A0	Output		Differential clock output A0 (Channel A). Configurable LVPECL/LVDS style and amplitude.
61, 60	QCLK_A1, nQCLK_A1	Output		Differential clock output A1 (Channel A). Configurable LVPECL/LVDS style and amplitude.
53, 52	QREF_A0, nQREF_A0	Output		Differential SYSREF/clock output REF_A0 (Channel A). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
55, 54	QREF_A1, nQREF_A1	Output		Differential SYSREF/clock output REF_A1 (Channel A). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
65, 64	QREF_A2, nQREF_A2	Output		Differential SYSREF/clock output REF_A2 (Channel A). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
8, 9	QCLK_B0, nQCLK_B0	Output		Differential clock output B0 (Channel B). Configurable LVPECL/LVDS style and amplitude.
10, 11	QCLK_B1, nQCLK_B1	Output		Differential clock output B1 (Channel B). Configurable LVPECL/LVDS style and amplitude.
2, 3	QREF_B0, nQREF_B0	Output		Differential SYSREF/clock output REF_B0 (Channel B). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
4, 5	QREF_B1, nQREF_B1	Output		Differential SYSREF/clock output REF_B1 (Channel B). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style, and amplitude for clock operation.
20, 21	QCLK_C, nQCLK_C	Output		Differential clock output C (Channel C). Configurable LVPECL/LVDS style and amplitude.
15, 16	QREF_C, nQREF_C	Output		Differential SYSREF/clock output REF_C (Channel C). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.
27, 28	QCLK_D, nQCLK_D	Output		Differential clock output D (Channel D). Configurable LVPECL/LVDS style and amplitude.
24, 25	QREF_D, nQREF_D	Output		Differential SYSREF/clock output REF_D (Channel D). LVDS, LVPECL style for SYSREF operation, configurable LVPECL/LVDS style and amplitude for clock operation.

**Table 1. Pin Descriptions (Cont.)<sup>[a]</sup>**

Pin	Name	Type <sup>[b]</sup>		Description
47, 46	QCLK_E0, nQCLK_E0	Output		Differential clock output E0. Configurable LVPECL/LVDS style and amplitude.
49, 48	QCLK_E1, nQCLK_E1	Output		Differential clock output E1. Configurable LVPECL/LVDS style and amplitude.
79, 78	QCLK_V, nQCLK_V	Output		Differential VCXO-PLL clock outputs. Configurable LVPECL/LVDS style and amplitude. After power up, this output is powered on and set to LVPECL, 750mV amplitude.
82	nINT	Output		Status output pin for signaling internal changed conditions. Register-selectable 1.8V LVCMOS interface levels.
81	LOCK	Output		PLL lock detect status output for both PLLs. Register-selectable 1.8V/3.3V LVCMOS interface levels.
87	EXT_SYS	Input	PD	External SYSREF pulse trigger input. 1.8V/3.3V LVCMOS interface levels.
83	SDAT	Input/Output	PU	Serial Control Port SPI Mode Data Input and Output. Register selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V and set to input.
84	SDO	Output		Serial Control Port SPI Mode Data Output (4 wire mode). Not used in high-impedance in SPI 3-wire mode. Register-selectable 1.8V/3.3V LVCMOS interface levels.
85	SCLK	Input	PD	Serial Control Port SPI Mode Clock Input. Register-selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.
86	nCS	Input	PU	Serial Control Port SPI Chip Select Input. Register-selectable 1.8V/3.3V LVCMOS interface levels. 3.3V tolerant when set to 1.8V.
35	CR	Analog		Internal VCO regulator bypass capacitor. Use a 1.0μF capacitor between the CR and VDD_LCF.
33	CBIAS	Analog		Internal bias circuit for VCO. Connect a 4.7μF capacitor to GND.
36	CLDO	Analog		Internal LDO bypass for VCO. Connect a 10μF capacitor to GND.
73	LFV	Output		VCXO-PLL charge pump output. Connect to the loop filter for the external VCXO.
77	OSC	Input	PD	VCXO non-inverting and inverting differential clock input. Inverting input is biased to $V_{DD_V}/2$ by default when left floating. Compatible with LVPECL, LVDS and LVCMOS signals.
76	nOSC		PD/PU	
44	ICPF	Analog		Connect to LFF pin (38) and external loop filter.
38	LFF	Output		Loop filter/charge pump output for the FemtoClock NG NG PLL. Connect to the external loop filter.
37	LFFR	Analog		Ground return path pin for the VCO loop filter.
72	RES_CAL	Analog		Connect a 2.8 kΩ (1%) resistor to GND for output current calibration.
13, 18, 23, 32, 41, 42	DNU			Do not use, do not connect.
57, 62	VDD_QCLKA	Power		Positive supply voltage (3.3V) for the QCLK_A[1:0] outputs.
51	VDD_QREFA0	Power		Positive supply voltage (3.3V) for the QREF_A0 outputs.
56	VDD_QREFA1	Power		Positive supply voltage (3.3V) for the QREF_A1 outputs.
63, 66	VDD_QREFA2	Power		Positive supply voltage (3.3V) for the QREF_A2 outputs.

**Table 1. Pin Descriptions (Cont.)<sup>[a]</sup>**

Pin	Name	Type <sup>[b]</sup>	Description
7, 12	VDD_QCLKB	Power	Positive supply voltage (3.3V) for the QCLK_B[1:0] outputs.
1	VDD_QREFB0	Power	Positive supply voltage (3.3V) for the QREF_B0 output.
6	VDD_QREFB1	Power	Positive supply voltage (3.3V) for the QREF_B1 output.
19, 22	VDD_QCLKC	Power	Positive supply voltage (3.3V) for the QCLK_C outputs.
14, 17	VDD_QREFC	Power	Positive supply voltage (3.3V) for the QREF_C outputs.
29	VDD_QCLKD	Power	Positive supply voltage (3.3V) for the QCLK_D outputs.
26	VDD_QREFD	Power	Positive supply voltage (3.3V) for the QREF_D outputs.
45, 50	VDD_QCLKE	Power	Positive supply voltage (3.3V) for the QCLK_E[1:0] outputs.
88	VDD_SPI	Power	Positive supply voltage (3.3V) for the SPI interface.
67	VDD_INP	Power	Positive supply voltage (3.3V) for the differential inputs (CLK0 to CLK1).
31	VDD_LCV1	Power	Positive supply voltage (3.3V) for internal VCXO_PLL circuits.
34	VDD_LCV2	Power	Positive supply voltage (3.3V) for internal VCXO_PLL circuits.
39, 40	VDD_LCF	Power	Positive supply voltage (3.3V) for the internal oscillator of the FemtoClock NG PLL.
43	VDD_CPF	Power	Positive supply voltage (3.3V) for internal FemtoClock NG circuits.
75, 80	VDD_QCLKV	Power	Positive supply voltage (3.3V) for OSC, nOSC input and QCLKV, nQCLKV output.
74	VDD_CPV	Power	Positive supply voltage (3.3V) for internal VCXO_PLL circuits.
30	VDD_SYNC	Power	Positive supply voltage (3.3V).
Exposed Pad (EP)	GND	Power	Ground supply voltage (GND) and ground return path. Connect to board GND (0V).

[a] For essential information on power supply filtering, see [Application Information](#).

[b] PU (pull-up) and PD (pull-down) indicate internal input resistors (for values, see [Table 48](#)).

## Principles of Operation

### Overview

The device generates low-phase noise, synchronized clock and SYSREF output signals locked to an input reference frequency. The device contains two PLLs with configurable frequency dividers. The first PLL (VCXO-PLL, suffix V) uses an external VCXO as the oscillator and provides jitter attenuation. The external loop filter is used to set the VCXO-PLL bandwidth frequency in conjunction with internal parameters. The second, low-phase noise PLL (FemtoClock NG, suffix F) multiplies the VCXO-PLL frequency to 2457.6MHz. The FemtoClock NG PLL is completely internal and provides a central timing reference point for all output signals. From this point, fully synchronous dividers generate the output frequencies and the internal timing references for JESD204B support. The device supports the generation of SYSREF pulses m synchronous to the clock signals.

There are five channels consisting of clock and/or SYSREF outputs. The clock outputs are configurable with support for LVPECL or LVDS formats and a variable output amplitude. Clock and SYSREF offer adjustable phase delay functionality. Individual outputs and channels and unused circuit blocks support powered-down states for operating at lower power consumption. The register map, accessible through SPI interface with read-back capability controls the main device settings and delivers device status information. For redundancy purpose, there are two selectable reference frequency inputs and a configurable switch logic with priority-controlled auto-selection and holdover support.



## Phase-Locked Loop Operation

### Frequency Generation

Table 2 displays the available frequency dividers for clock generation. The dividers must be set by the user to match input, VCXO and VCO frequency and to achieve frequency and phase lock on both PLLs. The frequency of the external VCXO is selected by the user, the internal VCO frequency is set to 2457.6MHz. Table 3 shows example divider configurations for typical wireless infrastructure applications.

**Table 2. PLL Operation and Divider Values**

Divider	Range	Operation for $f_{VCO} = 2457.6\text{MHz}$			Frequency Synthesis FemtoClock NG Bypassed
		Jitter Attenuation, Dual-PLL with deterministic Input-to-Output Delay	Jitter Attenuation, Dual-PLL	Frequency Synthesis VCXO-PLL Bypassed	
SRC	0, 1	0	0	0	1
BYPV	0, 1	0	0	1	0
BYPF	0, 1	1	0	X	X
VCXO-PLL Pre-Divider $P_V$	$\div 1 \dots \div 4095$ : (12 bit)	Input clock frequency $f_{CLK} = P_V \cdot \frac{f_{VCXO}}{P_F} \cdot \frac{M_F}{M_{V0} \cdot M_{V1}}$	Input clock frequency $f_{CLK} = f_{VCXO} \cdot \frac{P_V}{M_{V0}}$  $M_{V1}$ setting is not applicable to PLL operation	Input clock frequency $f_{CLK} = f_{VCO} \cdot \frac{P_V \cdot P_F}{M_F}$  $M_{V0}$ and $M_{V1}$ settings are not applicable to the PLL operation. $P_F$ : Set $P_F$ to 0.5 in above equation if the frequency doubler is engaged by setting $FDF = 1$	Input frequency $f_{CLK} = f_{VCXO} \cdot \frac{P_V}{M_{V0}}$  $M_{V1}$ , $P_F$ and $M_F$ settings are not applicable to VCXO-PLL operation
VCXO-PLL Feedback Divider $M_{V0}$	$\div 1 \dots \div 4095$ : (12 bit)				
PLL Feedback Divider <sup>[a]</sup> $M_{V1}$	$\div 4 \dots \div 511$ : (9 bit)				
FemtoClock NG Pre-Divider $P_F$	$\div 1 \dots \div 63$ : (6 bit)	VCXO frequency: $f_{VCXO} = f_{VCO} \cdot \frac{P_F}{M_F}$  $P_F$ : Set $P_F$ to 0.5 in above equation if the frequency doubler is engaged by setting $FDF = 1$			
FemtoClock NG Feedback Dividers $M_F$	$\div 8 \dots \div 511$ (9 bit)				
Output Divider $N_x$ (x=A, B, C, D, E)	$\div 1 \dots \div 200$ :	Output frequency $f_{OUT} = \frac{f_{VCO}}{N_x}$			Output frequency $f_{OUT} = \frac{f_{VCXO}}{N_x}$
SYSREF Divider <sup>[b]</sup> $N_s$	$\div 64 \dots \div 12,800$ : $2 \times \{2,4,8,16\} \times$ $\{2,3,4,5\} \times \{2,4\}$ $\times \{2,4\} \times$ $\{2,3,4,5\}$	SYSREF frequency/rate $f_{SYSREF} = \frac{f_{VCO}}{2N_s}$			SYSREF frequency/rate $f_{SYSREF} = \frac{f_{VCXO}}{2N_s}$

[a] For input monitoring, configure MV1 as described in [Monitoring and LOS of Input Signal](#).

[b] For SYSREF operation, configure SYNC[5:0] as described in [Status Conditions and Interrupts](#).

### VCXO-PLL

The prescaler  $P_V$  and the VCXO-PLLs feedback divider  $M_{V0}$  and  $M_{V1}$  require configuration to match the input frequency to the VCXO-frequency. The BYPF setting allows to route the VCXO-PLLs feedback path through the  $M_{V0}$  divider. Alternatively, the feedback path is routed through the second PLL and both the  $M_{V0}$  and  $M_{V1}$  feedback divider.  $M_{V0}$  has a divider value range of 12 bit;  $M_{V1}$  has 9 bit. The feedback path through the second PLL, in combination with the divider setting  $P_F=1$ , is the preferred setting for achieving deterministic delay from the clock input to the outputs. Multiple divider settings are available to enable support for input frequencies of 245.76, 122.88, 61.44, and 30.72 MHz and the VCXO-frequencies of 122.88, 61.44, 38.4, 30.72 and 245.76 MHz.

In addition, the range of available input and feedback dividers allows to adjust the phase detector frequency independent on the input and VCXO frequencies. In general, the phase detector may be set into the range from 120kHz to the input reference frequency. The VCXO-PLL charge pump current is controllable via a register and can be set in 50µA steps from 50µA to 1.6mA. The VCXO-PLL may be bypassed: the FemtoClock NG PLL locks to the pre-divider input frequency.

**Table 3. Example Configurations for  $f_{VCXO} = 122.88\text{MHz}^{[a]}$**

Input Frequency (MHz)	VCXO-PLL Divider Settings		$f_{PFD}$ (MHz)
	PV	MV0	
245.76	2	1	122.88
	32	16	7.68
	256	128	0.96
	2048	1024	0.12
122.88	1	1	122.88
	16	16	7.68
	128	128	0.96
	1024	1024	0.12

[a] BYPF = 0

**Table 4. Example Configurations for  $f_{VCXO} = 38.4\text{MHz}^{[a]}$**

Input Frequency (MHz)	VCXO- PLL Divider Settings		$f_{PFD}$ (MHz)
	PV	MV0	
245.76	32	5	7.68
	128	20	1.92
	512	80	0.48
	2048	320	0.12
122.88	16	5	7.68
	64	20	1.92
	256	80	0.48
	1048	320	0.12

[a] BYPF = 0

**Table 5. VCXO-PLL Bypass Settings**

BYPV	Operation
0	VCXO-PLL operation.
1	VCXO-PLL bypassed and disabled. The reference clock for the FemtoClock NG PLL is the input clock divided by the pre-divider PV. The input clock selection must be set to manual by the user. Clock switching and holdover are not defined. Device will not attenuate input jitter. No external VCXO component and loop filter required.

**Table 6. PLL Feedback Path Settings**

BYPF	Operation <sup>[a]</sup>
0	VCXO-PLL feedback path through the $M_{V0}$ divider. FemtoClock NG feedback path uses the $M_F$ divider.
1	VCXO-PLL feedback path through the $M_{V1} \cdot M_{V0}$ dividers. FemtoClock NG feedback path uses the $M_F$ divider. Preferred setting for achieving deterministic delay from input to the outputs.

[a] Regardless of the selected internal feedback path, the MV1 divider should be set to match its internal output frequency to the input reference frequency: the MV1 output signal is the internal reference for input loss-of-signal detect.

**FemtoClock NG PLL**

This PLL locks to the output signal of the VCXO-PLL (BYPV = 0). It requires configuration of the frequency doubler FDF or the pre-divider PF and the feedback divider MF to match the VCXO-PLL frequency to the VCO frequency of 2457.6MHz. This PLL is internally configured to high bandwidth. Best phase noise is typically achieved by engaging the internal frequency doubler (FDF = 1). If engaged, the signal from the first PLL stage is doubled in frequency, increasing the phase detector frequency of the FemtoClock NG PLL. Enabling the frequency doubler disables the frequency pre-divider PF. If the frequency doubler is not used (FDF = 0), the PF pre-divider must be configured. Typically, PF is set to ÷1 to keep the phase detector frequency as high as possible. Set PF to other divider values to achieve specific frequency ratios (1 to 19.2, 1 to 76.8, etc.) between first and second PLL stage.

**Table 7. Frequency Doubler**

FDF	Operation
0	Frequency doubler off. PF divides clock signal from VCXO-PLL or input (in bypass)
1	Frequency doubler on. Signal from VCXO-PLL or input (in bypass) is doubled in frequency. PF divider has no effect.

**Table 8. Output Divider Source Signal**

SRC	Operation
0	The output divider input signal is the FemtoClock NG PLL.
1	The output divider input signal is the VCXO-PLL output signal. The FemtoClock NG PLL is bypassed.

## Channel Frequency Divider

The device supports five independent channels, A to E. Each channel has a frequency divider  $N_x$  ( $x = A$  to  $E$ ) that divides the VCO frequency to the output frequency. Each divider be individually set to a value in the range of  $\div 1$  to  $\div 200$ . See [Table 9](#) for typical divider values and [Table 30](#) for the complete set of supported divider values.

**Table 9. Integer Frequency Divider Settings**

Channel Divider $N_x$ <sup>[a]</sup>	Output Clock Frequency (MHz)
	$f_{VCO} = 2457.6$ (MHz)
$\div 1$	2457.6
$\div 2$	1228.8
$\div 4$	614.4
$\div 5$	491.52
$\div 8$	307.2
$\div 10$	245.76
$\div 16$	153.6
$\div 20$	122.88
$\div 30$	81.92
$\div 32$	76.8
$\div 40$	61.44
$\div 50$	49.152
$\div 60$	40.96
$\div 64$	38.4
$\div 80$	30.72
$\div 100$	24.576
$\div 120$	20.48
$\div 128$	19.2
$\div 160$	15.36
$\div 200$	12.28

[a]  $x = A$  to  $E$

## Redundant Inputs

The two inputs are compatible with LVDS, LVPECL signal formats and also support single-ended signals (for applicable input interface circuits, see [Application Information](#)).

## Monitoring and LOS of Input Signal

The two inputs of the device are individually and permanently monitored for activity. Inactivity is defined by a static input signal.

The clock input monitors compare the device input frequency ( $f_{CLK}$ ) to the frequency of the VCO divided by  $M_{V1}$  (regardless of the internal feedback path using or not using  $M_{V1}$ ). A clock input is declared invalid with the corresponding LOS (Loss-of-input-signal) indicator bit set after three consecutive missing clock edges. For correct operation of the LOS detect circuit,  $M_{V1}$  must be powered-on by setting PD\_MV1 = 0. The MV1 divider must be set so that the LOS detect reference frequency matches the input frequency. For instance, if the input frequency is 245.76MHz,  $M_{V1}$  should be set to ÷10: The VCO frequency of 2457.6MHz divided by 10 equals the input frequency of 245.76MHz. For an input frequency of 122.88MHz, set  $M_{V1}$  to ÷20. Failure to set  $M_{V1}$  to match the input frequency will result in added latency to the LOS circuit (if  $f_{VCO} \div M_{V1} < f_{CLK}$ ) or false LOS indication (if  $f_{VCO} \div M_{V1} > f_{CLK}$ ). The minimum frequency that the circuit can monitor is  $f_{VCO} / MV1(MAX) = 4.809MHz$ . In applications with a lower input frequency than 4.809MHz, disable the monitor to trigger the status flags by setting BLOCK\_LOR = 1.

### Input Re-Validation

A clock input is declared valid and the corresponding LOS bit is reset after the clock input signal returned for user-configurable number of consecutive input periods. This re-validation of the selected input clock is controlled by the CNTV setting (verification pulse counter).

### Clock Selection

The device supports multiple input selection modes: manual, short-term holdover, and two automatic switch modes.

**Table 10. Clock Selection Settings**

Mode	Description	Application
Manual nM/A = 00	Input selection follows user-configuration of SEL[1:0]. Selection is <i>never</i> changed by the internal state machine. A failing reference clock will cause a LOS event and the PLL will unlock if the failing clock is selected. Re-validation of the selected input clock will result in the PLL to re-lock on that input clock.	Startup and external selection control
Automatic nM/A = 01	Input selection follows LOS status by user preset input switch priorities. A failing input clock will cause a LOS event for that clock input. If the selected clock has a LOS event, the device will immediately initiate a clock failover switch. The switch target is determined by pre-set input priorities.  No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will not enter the holdover state. The PLL is not locked. Re-validation of any input clock that is not the selected clock will result in the PLL to attempt to lock on that input clock. See <a href="#">“Revertive Switching”</a>	Multiple inputs with qualified clock signals
Short-term Holdover nM/A = 10	Input selection follows user-configuration of SEL[1:0]. Selection is never changed by the internal state machine. A failing reference clock will cause a LOS event. If the selected reference fails, the device will enter holdover <i>immediately</i> . Re-validation of the selected input clock is controlled by the CNTV setting. A successful re-validation will result in the PLL to re-lock on that input clock. See <a href="#">“Short-Term Holdover”</a>	Single reference
Automatic with holdover nM/A = 11	Input selection follows LOS status by user preset input priorities. Each failing input clock will cause a LOS event for that clock input. If the <i>selected</i> clock detects a LOS event, the device will go into holdover and the hold-off down-counter (CNTH) starts. The device initiates a clock failover switch <i>after</i> expiration of the hold-off counter. The switch target is determined by the preset input priorities.  No valid clock scenario: If no valid input clocks exist, the device will not attempt to switch and will remain in the holdover state. Re-validation of any input clock will result in the PLL to attempt to lock on that input clock. See <a href="#">“Automatic with Holdover (nM/A[1:0] = 11)”</a> and See <a href="#">“Revertive Switching”</a>	Multiple inputs

## Holdover

In holdover state, the output frequency and phase is derived from an internal, digital value based on previous frequency and phase information. Holdover characteristics are defined in [Table 53](#).

## Input priorities

Configurable settings encompass four selectable priorities with the range 0 (lowest priority) to 3 (highest priority). A user may change the input priorities at any time. In the automatic switch modes, input priority changes may cause immediate input selection changes.

## Hold-off Counter

A configurable down-counter applicable to the “Automatic with holdover” selection mode. The purpose of this counter is a deferred, user-configurable, input switch after a LOS event. The counter expires when a zero-transition occurs; this triggers a new reference clock selection. The counter is clocked by the frequency-divided VCXO-PLL signal. The CNTR setting determines the hold-off counter frequency divider and the CNTH setting the start value of the hold-off counter. For instance, set CNTR to a value of  $\neq 131072$  to achieve 937.5 Hz (or a period of 1.066 ms at  $f_{VCXO} = 122.88\text{MHz}$ ): the 8-bit CNTH counter is clocked by 937.5Hz and the user-configurable hold-off period range is 0ms (CNTR = 0x00) to 272ms (CNTR = 0xFF). After the counter expires, it reloads automatically from the CNTH SPI register. After the LOS status bit (LS\_CLK\_n) for the corresponding input CLK\_n has been cleared by the user, the input is enabled for generating a new LOS event.

The CNTR counter is only clocked if the device is configured in the clock selection mode “Automatic with holdover” AND the selected reference clock experiences a LOS event. Otherwise, the counter is automatically disabled (not clocked).

## Revertive Switching

Revertive switching: is only applicable to the two automatic switch modes shown in [Table 10](#). Revertive switching enabled: Re-validation of any non-selected input clock(s) will cause a new input selection according to the user-preset input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the currently selected reference clock.

Revertive switching disabled: Re-validation of a non-selected input clock has no impact on the clock selection. Default setting is revertive switching disabled.

## Short-Term Holdover

If an LOS event is detected on the reference clock designated by the SEL[1:0] bits:

- Holdover begins immediately
- ST\_REF, LS\_REF go low immediately
- No transitions will occur of the active REF clock; ST\_SEL[1:0] does not change
- The hold-off countdown is not active

When the designated reference clock resumes and has met the programmed validation count of consecutive rising edges:

- Holdover turns off
- ST\_SEL[1:0] does not change
- ST\_REF returns to 1

LS\_REF can be cleared by an SPI write of 1 to that register

### Automatic with Holdover (nM/A[1:0] = 11)

If a LOS event is detected on the active reference clock:

- Holdover begins immediately
- Corresponding ST\_REF and LS\_REF go low immediately
- Hold-off countdown begins immediately.

During this time, all clocks continue to be monitored and their respective ST\_CLK, LS\_CLK flags are active. LOS events will be indicated on ST\_CLK, LS\_CLK when they occur.

*If the active reference clock (or any CLK) resumes and is validated during the hold-off countdown:*

- its ST\_CLK status flag will return high and the LS\_CLK is available to be cleared by an SPI write of 1 to that register bit.
- No transitions will occur of the active REF clock; ST\_SEL[1:0] does not change and the ST\_REF, LS\_REF remain low even if active REF clock has been validated and its ST\_CLK status bit returns high
- Revertive bit has no effect during this time (whether 0 or 1)

*When the hold-off countdown reaches zero:*

- If the active reference has resumed and has been validated during the countdown, it will maintain being the active reference clock
  - ST\_SEL1:0 does not change
  - ST\_REF returns to 1
  - LS\_REF can be cleared by an SPI write of 1 to that register
  - Holdover turns off and the VCXO-PLL attempts to lock to the active reference clock
- If the active reference has not resumed, but another (sorted by next priority) clock input CLK<sub>n</sub> is validated, then
  - ST\_SEL1:0 changes to the new active reference
  - ST\_REF returns to 1
  - LS\_REF can be cleared by an SPI write of 1 to that register
  - Holdover turns off
- If there is no validated CLK:
  - ST\_SEL1:0 does not change
  - ST\_REF remains low
  - LS\_REF cannot be cleared by an SPI write of 1 to that register
  - Holdover remains active

Revertive capability returns if REVS = 1.

### **VCXO-PLL Lock Detect**

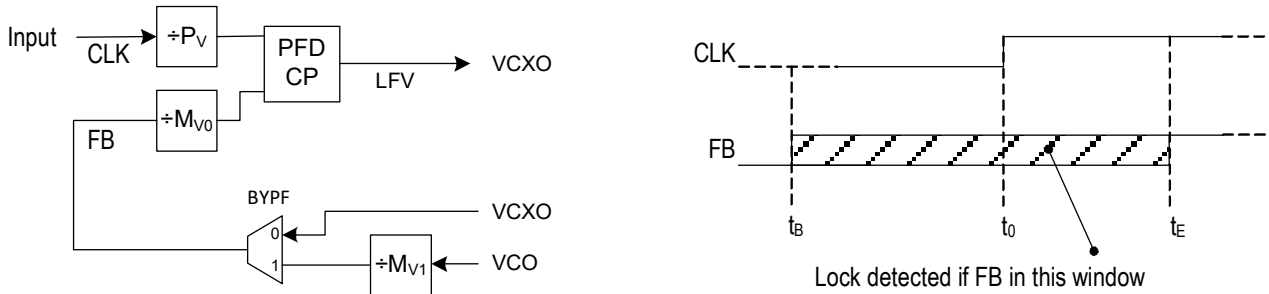
The VCXO-PLL lock detect circuit uses the signal phase difference at the phase detector as loss-of-lock criteria. Loss-of-lock is reported if the actual phase difference is larger than a configurable phase detector window set by the  $\Phi_{MV0}[2:0]$  and  $\Phi_{PV}[2:0]$  configuration bits. A loss-of-lock state is reported through the nST\_LOLV and nLS\_LOLV status bit, see [Table 23](#).

Setting the BLOCK\_LOLV register bit will block the VCXO-PLL lock status from being reported to the LOCK pin (see [Table 24](#)).

### **Loss-of-Lock Window Description**

The selected clock input signal is the reference signal (CLK) for lock detection. The rising edge of CLK defines the reference point  $t_0$ .  $\Phi_{PV}$  configures the start of the lock window  $t_S$  (which occurs before  $t_0$ ) and  $\Phi_{MV0}$  configures the end of the window  $t_E$  (which occurs after  $t_0$ ). The width of the lock window is defined by  $t_E - t_B$ . The VCXO-PLL declares lock when the rising edge of the feedback signal (FB) is within this window, otherwise the PLL reports loss-of-lock.

**Figure 3. Lock Detect Window**



**Table 11.  $t_B$  and  $t_E$  Calculation**

Operation	Jitter Attenuation, Dual-PLL with Deterministic Input-to-Output Delay (BYPV = 0, BYPF = 1)	Jitter Attenuation, Dual-PLL (BYPV = 0, BYPF = 0)
$t_B$	$t_B = -\frac{2^{\Phi_{PV}} - 1}{f_{CLK}}$	
$t_E$	$t_E = \frac{(2^{\Phi_{MV0}} - 1) \cdot M_{V1}}{f_{VCO}}$	$t_E = \frac{2^{\Phi_{MV0}} - 1}{f_{VCXO}}$

Figure 3 shows that  $\Phi_{PV}$  configures the start and  $\Phi_{MV0}$  the end of the window in integer multiples of PLL input and feedback periods. Both  $\Phi_{PV}$  and  $\Phi_{MV0}$  use 3 configuration bits with valid settings from 010 to 111 (2 to 7, decimal). This range allows configuring both  $t_S$  and  $t_E$  from 3 to 127 periods of the input signal ( $T_{IN}$ ) and the feedback signal ( $T_{FB}$ ), respectively, is implied.

**Loss-of-Lock Window Configuration Example**

With given  $P_V$ ,  $M_{V0}$  and  $M_{V1}$  divider values, select the corresponding  $\Phi_{PV}$  and  $\Phi_{MV0}$  settings from Table 12 and apply the  $\Phi_{PV}$  and  $\Phi_{MV0}$  values to the  $\Phi_{PV}[1:0]$  and  $\Phi_{MV0}[1:0]$  registers. Table 12 shows the lock window calculation formulas. For instance, if an input frequency of 245.76MHz and a  $P_V$  divider of 128 is desired, set  $\Phi_{PV}[1:0]$  to a binary value of 100 (decimal 4). This results in  $t_B = -61.035ns$  (15 periods of 4.069ns). With a VCXO-PLL (BYPF = 0) and a VCXO frequency of 122.88MHz and  $M_{V0} = 64$ , select 011 (decimal 3) resulting in  $t_E = 56.96ns$  (7 periods of 8.138 ns) and an overall lock detect window of  $t_E - t_B = 56.96ns + 61.035ns = 118.001ns$ . The user may select a smaller lock detect window. For instance, a  $P_V$  divider of 128 allows to set  $\Phi_{PV}[1:0]$  to 010, 011 or 100 (decimal 2 to 4). Correspondingly, a  $M_{V0}$  divider of 64 allows  $\Phi_{MV0}[1:0]$  settings from 010 to 011 (decimal 2 to 3). With smaller settings, the lock detect window size is reduced exponentially.

$\Phi_{PV}[1:0] = 000$  will set  $t_B$  to  $0.5 \cdot T_{REF}$  and  $\Phi_{PV}[1:0] = 001$  will set  $t_B$  to  $1.5 \cdot T_{REF}$ .  $\Phi_{MV0}[1:0] = 000$  will set  $t_E$  to  $0.5 \cdot T_{REF}$  and  $\Phi_{MV0}[1:0] = 001$  will set  $t_E$  to  $1.5 \cdot T_{REF}$ .



**Table 12. Recommended Lock Detector Phase Window Settings**

$P_V$ Divider Value	$\Phi_{PV}[1:0]$ Setting	$M_{V0}$ Divider Value	$\Phi_{MV0}[1:0]$ Setting
1–31	N/A	1–31	N/A
32–63	010	32–63	010
64–127	$\leq 011$	64–127	$\leq 011$
128–255	$\leq 100$	128–255	$\leq 100$
256–511	$\leq 101$	256–511	$\leq 101$
512–1023	$\leq 110$	512–1023	$\leq 110$
1024 and higher	$\leq 111$	1024 and higher	$\leq 111$

**FemtoClock NG Loss-of-Lock (LOLF)**

FemtoClock NG-PLL loss of lock is signaled through the nST\_LOLF (momentary) and nLS\_LOLF (sticky, resettable) status bits and can be reported as hardware signal on the LOCK output as well as an interrupt signal on the nINT output.

**Channel, Output, and JESD204B Logic**

Each of the four channels A to D consists of one to two clock and associated one to three SYSREF outputs. Each SYSREF output in a channel can be individually configured to generate JESD204B (SYSREF) signals or copy the clock signal of that channel. The fifth channel (E) consists of two clock outputs without SYSREF support in that channel.

If JESD204B/SYSREF operation is assigned to a QREF output, the channel logic controls the outputs: outputs automatically turn on and off in a SYSREF sequence. QREF outputs configured to clock operation can individually configure output states.

**Table 13. Channel Configuration<sup>[a]</sup>**

MUX	0	1
Description	Clock configuration	JESD204B
QCLK_y	Clock signal	Clock signal
QREF_r		SYSREF/JESD204B
Frequency Divider	QCLK_y and QREF_r: $N_x$	QCLK_y: $N_x$ QREF_r: $N_S$ (Global to all QREF_r)
Phase Delay	QCLK_y and QREF_r: $\Phi_{CLK_x}$ $\Phi_{REF_r}$ settings do not apply	QCLK_y: $\Phi_{CLK_x}$ QREF_r: $\Phi_{REF_r}$
Power Down	Per output	Per channel
Output Enable	Per output	Per output

[a] x = A to E. y = A0, A1, B0, B1, C, D, E0, E1; r = A0, A1, A2, B0, B1, C, D

## Differential Outputs

**Table 14. Output Features**

Output	Style	Amplitude <sup>[a]</sup>	Disable	Power Down	Termination
QCLK_y, QREF_r (Clock)	LVPECL	250-1000 mV	Yes	Yes	50Ω to V <sub>T</sub>
	LVDS	4 steps			100Ω differential <sup>[b]</sup>
QREF_r (SYSREF)	LVDS	250-1000 mV 4 steps	Controlled by SYSREF <sup>[c]</sup>		100Ω differential <sup>b</sup>
QCLK_V	LVPECL	250-750 mV	Yes	Yes	50Ω to V <sub>T</sub>
	LVDS	3 steps			100Ω differential <sup>b</sup>

[a] Amplitudes are measured single-endedly. Differential amplitudes supported are 500, 1000, 1500 and 2000mV

[b] AC coupling and DC coupling supported.

[c] State of SYSREF outputs is controlled by an internal SYSREF state machine.

**Table 15. Individual Clock Output Settings<sup>[a]</sup>**

PD <sup>[b]</sup>	STYLE	EN <sup>[c]</sup>	A[1:0] <sup>[d]</sup>	Output Power	Termination	State	Amplitude (mV)
1	X	X	X	Off	100Ω differential or no termination	Off	X
0	0	0	XX	On	100Ω differential (LVDS)	Disable (logic low)	X
			1			00	Enable
		01				500	
		10				750	
		11				1000	
		1	0			XX	50Ω to V <sub>T</sub> (LVPECL)
	00				50Ω to V <sub>T</sub> = V <sub>DD_V</sub> - 1.50V (LVPECL)	250	
	1		01		50Ω to V <sub>T</sub> = V <sub>DD_V</sub> - 1.75V (LVPECL)	500	
			10		50Ω to V <sub>T</sub> = V <sub>DD_V</sub> - 2.00V (LVPECL)	750	
			11		50Ω to V <sub>T</sub> = V <sub>DD_V</sub> - 2.25V (LVPECL)	1000	
					Enable	1000	

[a] Applicable to clock outputs: QCLK\_y and QREF\_r outputs in clock mode (MUX\_r = 0)

[b] Power-down modes are available for the individual channels A-E and the outputs QCLK\_y (A0 to E1).

[c] Output enable is supported on each individual QCLK\_y and QREF\_r output.

[d] Output amplitude control is supported on each individual QCLK\_y and QREF\_r output.

**Table 16. Individual SYSREF Output Settings<sup>[a]</sup>**

PD	STYLE	EN	nBIAS	A[1:0]	Output Power	Termination	State	Amplitude (mV)
1	X	X	X	XX	Off	100Ω differential or no termination	Off	X
0	0	0	0	XX	On <sup>[b]</sup>	100Ω differential (LVDS)	Disable (logic low)	X
		1		00			Enable	250
				01				500
				10				750
				11				1000
				X				Line bias <sup>[c]</sup>
	1	0	0	XX		50Ω to $V_T = V_{DD\_V} - 1.50V$ (LVPECL)	Disable (logic low)	X
		1		00			Enable	250
				01				500
				10				750
				11				1000
				X				Line bias <sup>[c]</sup>

[a] Applicable QREF\_r outputs when configured as SYSREF output (MUX\_r = 1).

[b] Output amplitude should be set to a 500 mV swing (A[1:0] to 01) by SPI. SYSREF output states are controlled by an internal state machine. An internal SYSREF event will automatically turn SYSREF outputs on. After the event, outputs are automatically turned off. Setting nBIAS = 1 will bias powered-off outputs to the LVDS midpoint voltage.

[c] Output (both Q, and nQ) bias the line to the differential signal cross-point voltage. Available if output is AC-coupled and set to LVDS style

**Table 17. QCLK\_V (VCXO-PLL Output) Settings<sup>[a]</sup>**

nPD	STYLE	A[1:0]	Output Power	Termination	Amplitude (mV)
0	X	X	Off	100Ω differential (LVDS) or no termination	X
1	0	00	On	100Ω differential (LVDS)	250
		01			500
		10			750
		11			750
	1	00		50Ω to $V_T = V_{DD\_V} - 1.50V$ (LVPECL)	250
		01		50Ω to $V_T = V_{DD\_V} - 1.75V$ (LVPECL)	500
		10		50Ω to $V_T = V_{DD\_V} - 2.00V$ (LVPECL)	750
		11			750

[a] Changing a QCLK\_V configuration is a two-step process. 1) write the QCLK\_V new configuration value in the register, then step 2) write the EN\_QCLKV\_MOD[7:0] register to the value 0x4B.

**Table 18. QREF\_r Setting for JESD204B Applications**

BIAS_TYPE	nBIAS_r	QREF_r Outputs (LVDS, 500mV Amplitude)			Application
		Initial	During SYSREF Event	SYSREF Completed	
0	0	Static low (QREF = L, nQREF_r = H)	Start switching for the number of configured SYSREF pulses	Released to static low (QREF = L, nQREF_r = H)	QREF_r DC coupled
	1	Static low (QREF = L, nQREF_r = H)			
1	0	Static LVDS crosspoint level (QREF = nQREF_r = VOS)	Start switching for the number of configured SYSREF pulses	Released to static LVDS crosspoint level (QREF = nQREF_r = VOS)	QREF_r AC coupled
	1	Static LVDS crosspoint level (QREF = nQREF_r = VOS)			

### Output Phase Delay

Output phase delay is independently supported on both clock and SYSREF outputs.

The phase delay on clock outputs  $\Phi_{CLK_x}$ , SYSREF outputs coarse delay  $\Phi_{REF_r}$  and global delay  $\Phi_{REF_S}$  is derived from the internal VCO frequency of the second PLL (FemtoClock NG PLL). In configurations bypassing the second PLL by setting SRC = 1, the delay unit is derived from the frequency of the external VCXO: use  $f_{VCXO}$  instead of  $f_{VCO}$  in Table 19.

**Table 19. Delay Circuit Settings**

Delay Circuit	Unit	Steps	Range (ns)	Alignment <sup>[a]</sup>
Clock <sup>[b]</sup> $\Phi_{CLK_x}$	$\frac{1}{f_{VCO}} = 407\text{ps}$	256	0 – 103.76 <sup>[c]</sup>	Incident rising clock edges are aligned, independent on the divider N_x across channels
SYSREF $\Phi_{REF_r}$	Coarse delay: $\frac{1}{f_{VCO}} = 407\text{ps}$	8	0 – 2.848 <sup>[c]</sup>	SYSREF rising edge is aligned to the incident rising clock edge across channels
	Fine delay: 0, 25, 50, 75, 85, 110, 135, 160 ps	8	0 – 0.160 <sup>[d]</sup>	
SYSREF (Global) $\Phi_{REF_S}$	$\frac{2}{f_{VCO}} = 814\text{ps}$	256	0 – 207.52 <sup>[c]</sup>	Global alignment of SYSREF signals

[a] Default configuration (all delay settings = 0)

[b] Clock output inversion supported by setting phase delay to 180° setting.

[c] Exact delay value.

[d] ±20% delay variation over PVT.

## Configuration for JESD204B Operation

### Synchronizing SYSREF and Clock Output Dividers

The SYNC[5:0] divider controls the release of SYSREF pulses at coincident QCLK<sub>y</sub> clock edges. For SYSREF operation, set the SYNC divider value to half of the least common multiple of the clock divider values N<sub>x</sub> (x = A to E). For example, if NA = NB = ÷2, NC = ND = ÷3, NE = ÷4, set the SYNC divider to ÷6.

### SYSREF Generation

A SYSREF event is the generation of one or more consecutive pulses on the QREF outputs. An event can be triggered by SPI commands or by a signal-transition on the EXT\_SYS or CLK\_1 input. The number of SYSREF pulses generated is programmable to 1-255 and to continuous. The SYSREF pulse rate is configurable to the frequencies shown in Table 20. SYSREF output pulses are aligned to coincident rising clock edges of the clock outputs QCLK<sub>y</sub>. If all delay stages are set to the delay value of zero, the phase alignment of all QCLK<sub>y</sub> and QREF<sub>r</sub> outputs is zero. The following SYSREF pulse generation modes are available and configurable by SPI:

- Counted pulse mode – 1 to 255 pulses are generated by the device. SYSREF activity stops automatically after the transmission of the selected number of pulses and the QREF output powers down.
- Continuous mode – The SYSREF signal is a clock signal.

The generation of SYSREF pulses is configured by SPI commands and is available after the initial setup of output clock divider and QREF phase delay stages. A SYSREF event will automatically turn on the SYSREF outputs. After the event, SYSREF outputs are automatically turned-off (power-down). SYSREF outputs with the nBIAS bit set high will bias the outputs at the LVDS crosspoint voltage level (requires BIAS\_TYPE = 1).

**Table 20. SYSREF Generation<sup>[a]</sup>**

N <sub>S</sub>	SYSREF Operation (f <sub>SYSREF</sub> )
	f <sub>VCO</sub> = 2457.6MHz
÷80, ÷160, ÷320, ÷640, ÷1280, ÷2560	15.36, 7.68, 3.84, 1.92, 0.96, 0.48
÷96, ÷192, ÷288, ÷384, ÷480, ÷576, ÷768, ÷1536	12.8, 6.4, 3.2, 1.6, 0.8, 0.4
÷120, ÷240, ÷480, ÷960, ÷1440, ÷1920, ÷2400, ÷2880	10.24, 5.12, 2.56, 1.28, 0.64, 0.32
÷128, ÷256, ÷512, ÷1024, ÷2048	9.6, 4.8, 2.4, 1.2, 0.6, 0.3

[a] Example frequencies

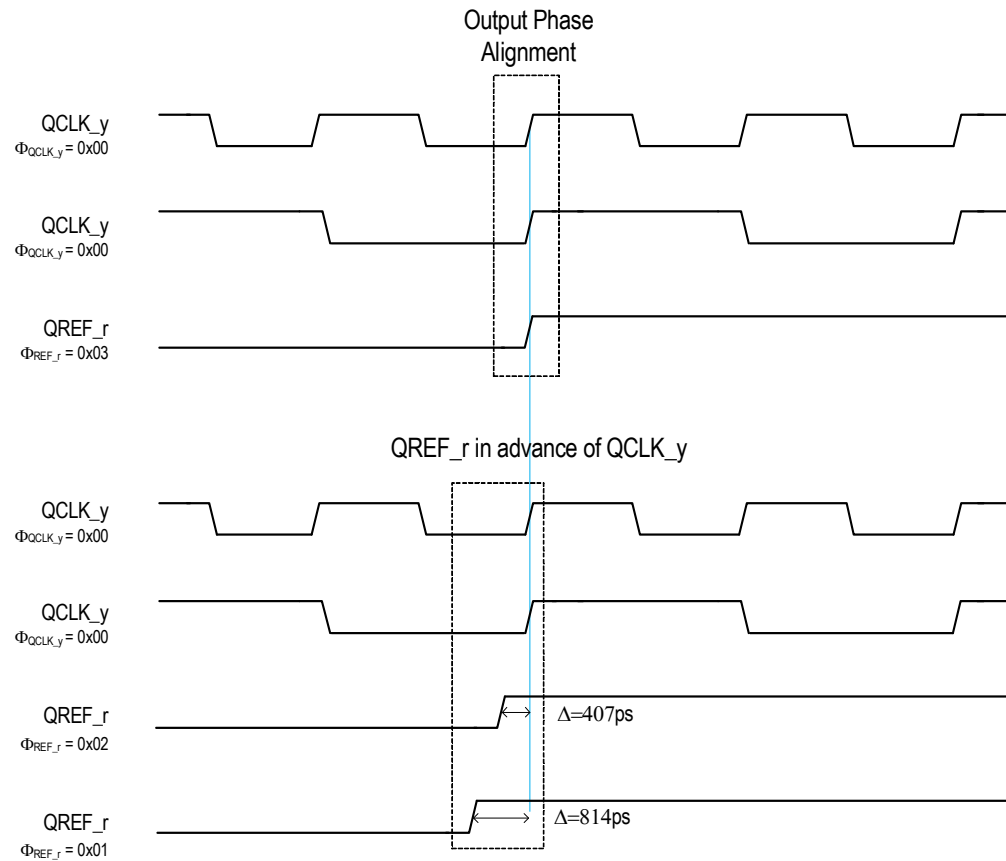
### Internal SYSREF Generation

SYSREF generation is set to internal (SRG = 0). The SRO setting defines if SYSREF pulses are counted or continuous and the NS[7:0] divider sets the frequency. In counted pulse mode, the SRPC register contains the number of pulses to generate. Any number from 1 to 255 pulses can be generated. SYSREF pulses are generated upon completion of the SPI command RS (SYSREF release). Setting RS activates the SYSREF outputs, loads the number of pulses from the SRPC register, and starts the generation of SYSREF pulses synchronized to the incident edge of the clock signals. After the programmed number of pulses are generated, SYSREF outputs will go into logic low state or bias the output voltage to the static LVDS crosspoint level (see Table 18 for settings and details). In continuous mode, SYSREF is a clock signal and the content of the SRPC signal is ignored. For proper operation of this mode, set SR\_INSEL bit to 0.

### QCLK to QREF (SYSREF) Phase Alignment

Figure 4 and Table 21 show how to achieve output phase alignment between the QCLK<sub>y</sub> clock and the QREF<sub>r</sub> SYSREF outputs in internal SYSREF generation mode (SRG=0). The closest (smallest phase error) output alignment is achieved by setting the clock phase delay register  $\Phi_{\text{QCLK}_y}$  to 0x00 (clock), the SYSREF output phase delay registers  $\Phi_{\text{REF}_r}$  to 0x03 (coarse delay),  $\Phi_{\text{REF}_F_r}$  to 111 (160ps, fine delay) and the global  $\Phi_{\text{REF}_S}$  delay register to 0x07. With a SYSREF phase delay setting of 0x02 or less, the QREF<sub>r</sub> output phase is in advance of the QCLK<sub>y</sub> phase, which is applicable in JESD204B application. Phase delay settings and propagation delays are independent on the clock and SYSREF frequencies. Table 21 shows recommended phase delay setting several device configurations.

**Figure 4. QCLK to QREF Phase Alignment**



**Table 21. Recommended Delay Settings for Closest Clock-SYSREF Output Phase Alignment<sup>[a]</sup>**

Divider Configuration	$\Phi_{\text{CLK}_y}$	$\Phi_{\text{REF}_r}$	$\Phi_{\text{REF}_F_r}$	$\Phi_{\text{REF}_S}$
$N_A = \pm 4, N_B = \pm 5, N_C = \pm 8,$ $N_D = N_E = \pm 10$ $N_S = \pm 320$	0x00	0x03	111 (160 ps)	0x07

[a] QCLK and QREF outputs are aligned on the incident edge.

### External SYSREF Generation

SYSREF generation is set to external (SRG = 1): SYSREF pulses are generated in response to the detection of a rising edge at the EXT\_SYS or CLK<sub>1</sub> input (see Table 22 for selection of the active, external SYSREF input). The EXT\_SYS (or CLK<sub>1</sub>) input rising edge releases SYSREF pulses. Both SRO and SRPC register settings apply as in internal SYSREF generation mode for generating single shot and repetitive SYSREF output signals. Set RS = 1 to prepare for SYSREF generation; the generation of SYSREF pulses is triggered by a rising edge at EXT\_SYS or CLK<sub>1</sub> input.

**Table 22. External SYSREF Input**

SR_INSEL	Operation
0 (Default)	EXT_SYS (single-ended) is the external SYSREF input
1	CLK_1 (differential) is the external SYSREF input. CLK_1 is not available as clock input to drive the first-stage PLL.

## Status Conditions and Interrupts

The device has an interrupt output to signal changes in status conditions. Settings for status conditions may be accessed in the Status registers. The device has several conditions that can indicate faults and status changes in the operation of the device. These are shown in Table 23 and can be monitored directly in the status registers. Status bits (named: *ST\_condition*) are read-only and reflect the momentary device status at the time of read-access. Several status bits are also copied into latched bit positions (named: *LS\_condition*). The latched version is controlled by the corresponding fault and status conditions and remains set (“sticky”) until reset by the user by writing 1 to the status register bit.

The reset of the status condition has only an effect if the corresponding fault condition is removed, otherwise, the status bit will set again. Setting a status bit on several latched registers can be programmed to generate an interrupt signal (nINT) via settings in the Interrupt Enable bits (named: *IE\_condition*). A setting of 0 in any of these bits will mask the corresponding latched status bit from affecting the interrupt status pin. Setting all IE bits to 0 has the effect of disabling interrupts from the device. Interrupts are cleared by resetting the appropriate bit(s) in the latched register after the underlying fault condition has been resolved. When all valid interrupt sources have been cleared in this manner, this will release the nINT output until the next unmasked fault

**Table 23. Status Bit Functions**

Status Bit		Function			Interrupt Enable Bit
Momentary	Latched	Description	Status if Bit is:		
			1	0	
ST_CLK_0	LS_CLK_0	CLK 0 input status	Active	LOS	IE_CLK_0
ST_CLK_1	LS_CLK_1	CLK 1 input status	Active	LOS	IE_CLK_1
nST_LOLV <sup>[a]</sup>	nLS_LOLV	VCXO-PLL loss of lock	Locked	Loss of lock	IE_LOLV
nST_LOLF <sup>[b]</sup>	nLS_LOLF	FemtoClock NG-PLL loss of lock	Locked	Loss of lock	IE_LOLF
nST_HOLD	nLS_HOLD	Holdover	Not in holdover	Device in holdover	IE_HOLD
ST_VCOF	—	FemtoClock NG VCO calibration	Not completed	Completed	—
ST_SEL[1:0]	—	Clock input selection in auto-selection mode	00 = CLK_0 01 = CLK_1 10, 11 - not defined		—
ST_REF	LS_REF	PLL reference status	Valid reference <sup>[c]</sup>	Reference lost	IE_REF

[a] Setting the BLOCK\_LOLV register bit will block the LOLV status bit from affecting the LOCK pin.

[b] If the VCXO-PLL is bypassed by setting BYPV = 1, VCXO-PLL lock status is blocked from affecting the LOCK pin.

[c] Manual and short-term holdover mode: 0 indicates if the reference selected by SEL[1:0] is lost, 1 if not lost  
Automatic with holdover mode: 0 indicates the reference is lost and while still in holdover

**Table 24. LOCK Function**

Status Bit (PLL)		Status Reported on LOCK Output
nST_LOLV <sup>[a]</sup> (VCXO-PLL)	nST_LOLF (FemtoClock NG)	
Locked <sup>[b]</sup>	Locked	1
	Not locked	0
Not locked	Locked	0
	Not locked	0

[a] The LOCK pin will only report the FemtoClock NG PLL status on the LOCK pin if BLOCK\_LOLV = 0.

[b] If the VCXO-PLL is bypassed by setting BYPV = 1, VCXO-PLL lock status is blocked from affecting the LOCK pin.

## Device Startup, Reset, and Synchronization

At startup, an internal POR (power-on reset) resets the device and sets all register bits to its default value. The device forces the VCXO control voltage at the LFV pin to half of the power supply voltage to center the VCXO-frequency. In the default configuration the QCLK<sub>y</sub> and QREF<sub>r</sub> outputs are disabled at startup. The QCLK<sub>V</sub> output is enabled and set to 750mV / LVPECL after power-up

### Recommended Configuration Sequence (In Order):

1. (Optional) set the value of the CPOL and (optional) SDO\_ACT register bits to define the SPI read mode and the SPI 3/4-wire mode. If SDO\_ACT is not set, the device will be in 3-wire mode with the SDAT pin as SPI I/O.
2. Configure all PLL settings, output divider and delay circuits as well as other device configurations.
  - BYPF and BYPV for the desired PLL operation mode and configure the PLL dividers P<sub>V</sub>, M<sub>V0</sub>, M<sub>V1</sub>, M<sub>F</sub> and P<sub>F</sub> as required to achieve PLL lock. See [Table 2](#) for details
  - VCXO-PLL lock detect window by configuring the phase settings  $\Phi_{M_{V0}}$  and  $\Phi_{P_V}$
  - Charge pump currents for both PLLs (CPV[4:0] and CPF[4:0]) and POLV for the desired VCXO polarity
  - (optional) OSVEN and OFFSET[4:0] for the VCXO-PLL static phase offset
  - Channel dividers
  - MUX<sub>r</sub> for the desired operation of the QREF<sub>r</sub> outputs
  - QCLK<sub>y</sub>, QREF<sub>r</sub>, and QOSC output features such as desired output power-down state, style, and amplitude. QCLK<sub>y</sub>, QREF<sub>r</sub> and QOSC output features such as desired output power-down state, style and amplitude. Use the EN\_QCLKV\_MOD register to make QOSC register changes effective.
  - Desired input selection and monitoring modes: this involves nM/A[1:0] and SEL[1:0] for input selection. In any of the automatic modes, configure PRIO[1:0]<sub>n</sub>, and REVS. Configure the CNTH[7:0], CNTR[1:0] counters for the desired holdover characteristics and DIV4\_VAL, CNTV[1:0] for input revalidation if applicable to the operation mode.
  - Individual  $\Phi_{CLK_X}$  and  $\Phi_{REF_r}$  registers and the global delay  $\Phi_{REF_S}$  register for the desired phase delay between clock and SYSREF outputs; see [\(link to phase alignment section\)](#).
  - Interrupt enable configuration bits IE<sub>status\_condition</sub>, as desired for fault reporting on the nINT output
3. For SYSREF operation:
  - a. Configure the N<sub>S</sub> and SYNC divider as described in the section [Status Conditions and Interrupts](#)
  - b. Configure the SYSREF registers SRG, SRO and SRPC[7:0] according to the desired SYSREF operation
  - c. Configure the SR\_INSEL register bit if external SYSREF operation is desired.
4. Set the initialization bit INIT\_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT\_CLK bit will self-clear.



5. Set both the RELOCK bit and PB\_CAL bit. This step should not be combined with the previous step (setting INIT\_CLK) in a multi SPI-byte register access. Both bits will self-clear.
6. Clear the FVCV bit to release the VCXO control voltage and VCXO-PLL will attempt to lock to the input clock signal starting from its center frequency
7. Clear the status flags
8. At this point, the basic configuration of the registers 0x00 to 0x73 should be completed and the SPI transfer ended (set nCS to high level)
9. In a separate SPI write access, enable the outputs as desired by accessing the output-enable registers 0x74 and 0x76.
10. For SYSREF operation: set the RS bit to start (or re-start) generating the configured number of SYSREF pulses. The RS bit will auto-clear.
  - In internal SYSREF generation mode (SRG = 0) the SYSREF pulses are generated as a result of setting the RS bit.
  - In external SYSREF mode the SYSREF pulses are generated at the next rising edge of the EXT\_SYS or CLK\_1 input.

Reserved registers and registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

## Changing Frequency Dividers and Phase Delay Values

### *Clock Frequency Divider and Delay*

Following procedure has to be applied for a change of a clock divider and phase delay value  $N_{A-E}$ , and  $\Phi_{CLKA-E}$ :

1. (Optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses
2. (Optional) disable the outputs whose frequency divider or delay value is changed
3. Configure the  $N_{A-E}$  dividers and the delay circuits  $\Phi_{CLKA-E}$  to the desired new values
4. (Optional) configure the SYNC divider if required for synchronization between clock and SYSREF signals
5. Set the initialization bit INIT\_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT\_CLK bit will self-clear. During this initialization step, all QCLK\_y and QREF\_r outputs are reset to the logic low state.
6. Set the RELOCK bit. This step should not be combined with the setting INIT\_CLK in a multi SPI-byte register access. Bit will self-clear.
7. (Optional) enable the outputs whose frequency divider was changed.

### *SYSREF Frequency Divider, Delay and Starting/Re-Starting SYSREF Pulse Sequences*

Following procedure has to be applied for a change of a SYSREF divider and phase delay value  $N_S$  and  $\Phi_{REF_S}$ :

1. (optional) set the value of the CPOL register to define the SPI read mode, so that SPI settings can be validated by subsequent SPI read accesses
2. (optional) disable the outputs whose frequency divider or delay value is changed
3. Configure any  $N_S$  divider and any delay circuits  $\Phi_{REF_S}$  to their desired new values
4. Configure the SYNC divider if required for synchronization between clock and SYSREF signals
5. Set the initialization bit INIT\_CLK. This will initiate all divider and delay circuits and synchronize them to each other. The INIT\_CLK bit will self-clear. During this initialization step, all QCLK\_y and QREF\_r outputs are reset to the logic low state.
6. Set the RELOCK bit. This step should not be combined with the setting INIT\_CLK in a multi SPI-byte register access. Bit will self-clear.
7. Set the SRO bit to counted pulse mode or to continues pulse mode, as desired
8. (Optional) enable the outputs whose frequency divider was changed.
9. For SYSREF operation: set the RS bit to start (or re-start) generating the configured number of SYSREF pulses. The RS bit will auto-clear.
  - In internal SYSREF generation mode (SRG = 0), the SYSREF pulses are generated as a result of setting the RS bit. Set RS for each repeated SYSREF generation (set SR\_INSEL bit to 0 for this mode).
  - In external SYSREF mode the SYSREF pulses are generated at the next rising edge of the EXT\_SYS or CLK\_1 input.

## SPI Interface

The device has a configurable 3-wire/4-wire serial control port capable of responding as a slave in an SPI configuration to allow read and write access to any of the internal registers for device programming or read back. The SPI interface consists of the SCLK (clock), SDAT (serial data input and output in 3-wire mode, input in 4-wire mode), SDO (serial data output in 4-wire mode) and nCS (chip select) pins. After power-up, the SPI interface is in 3-wire mode. The SDO\_ACT register bit controls the SPI 3/4 wire configuration. SDO\_ACT should be set after startup if 4-wire operation is desired. A data transfer consists any integer multiple of 8 bits and is always initiated by the SPI master on the bus. Internal register data is organized in SPI bytes of 8 bit each.

If nCS is at logic high, the SDAT data I/O is in high-impedance state and the SPI interface of the device is disabled.

In a write operation, data on SDAT will be clocked in on the rising edge of SCLK. In a read operation, data on SDAT/SDO will be clocked out on the falling or rising edge of SCLK depending on the CPOL setting (CPOL = 0: output data changes on the falling edge, CPOL = 1: output data changes on the rising edge).

**Starting a data transfer** requires nCS to set and hold at logic low level during the entire transfer. Setting nCS = 0 will enable the SPI interface with SDAT in data input mode. The master must initiate the first 8-bit transfer. The first bit presented by the SPI master in each transfer is the LSB (least significant bit). The first bit presented to the slave is the direction bit R/nW (1 = Read, 0 = Write) and the following seven bits are the address bits A[0:6] pointing to an internal register in the address space 0 to 127.

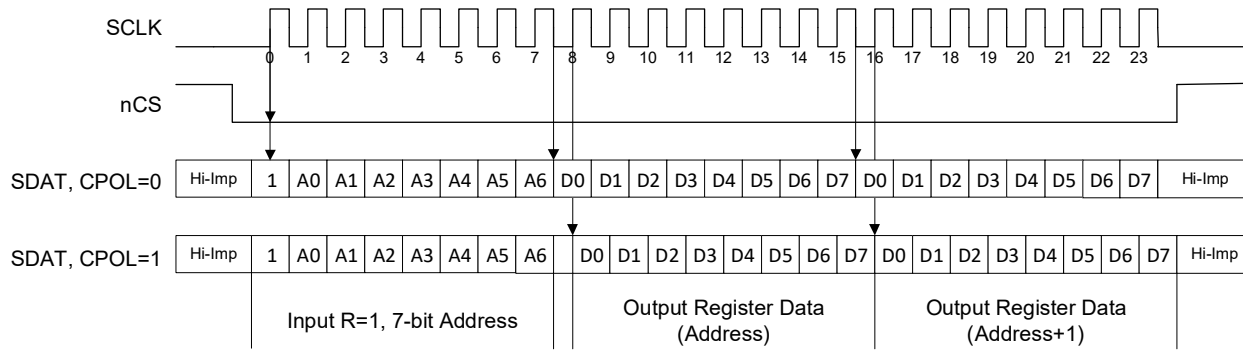
**Read operation** from an internal register: a read operation starts with an 8 bit transfer from the master to the slave: SDAT is clocked on the *rising* edge of SCLK. The first bit is the direction bit R/nW which must be to 1 to indicate a read transfer, followed by 7 address bits A[0:6]. After the first 8 bits are clocked into SDAT (in 3-wire mode), the SDAT I/O changes to output: The register content addressed by A[0:6] are loaded into the shift register and the next 8 SCLK *falling* (CPOL = 1) clock cycles will then present the loaded register data on the SDAT (3-wire mode) / SDO (4-wire-mode) output and transfer these to the master. Transfers must be completed with de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined. SPI byte (8-bit) and back-to-back read transfers of multiple registers are supported with an address auto-increment. During multiple transfers, nCS must stay at logic low level and SDAT (SDO) will present multiple registers (A), (A+1), (A+2), etc. with each 8 SCLK cycles. During SPI Read operations, the user may continue to hold nCS low and provide further bytes of data for up to a total of 127 bytes in a single block read.

**Write operation** to a device register: During a write transfer, a SPI master transfers one or more bytes of data into the internal registers of the device. A write transfer starts by asserting nCS to low logic level. The first bit presented by the master must set the direction bit R/nW to 0 (Write) and the 7 address bits A[0:6] must contain the 7-bit register address. Bits D0 to D7 contain 8 bit of payload data, which is written into the register addressed by A[0:6] at the end of a 8-bit write transfer. Multiple, subsequent register transfers from the master to the slave are supported by holding nCS asserted at logic low level during write transfers. The 7 bit register address will auto-increment. Transfers must be completed with de-asserting nCS after any multiple 8 SCLK cycles. If nCS is de-asserted at any other number of SCLKs, the SPI behavior is undefined.

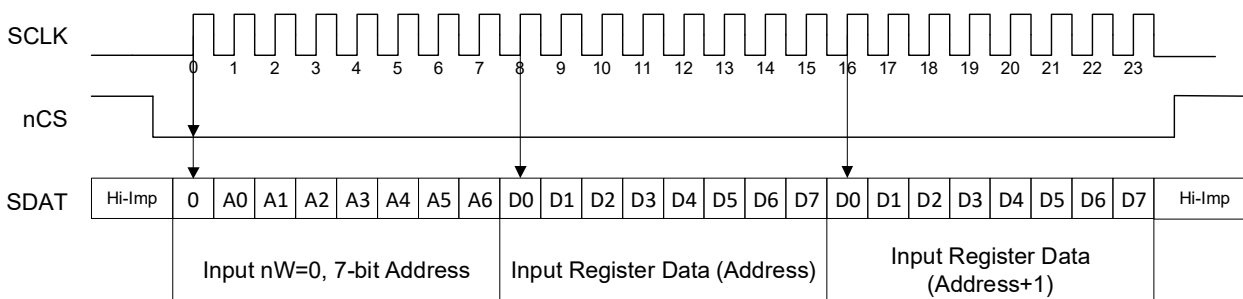
**End of transfer:** After nCS is de-asserted to logic 1, the SPI bus is available to transfers to other slaves on the SPI bus. See also the READ diagram (Figure 5) and WRITE (Figure 6) displaying the transfer of two bytes of data from and into registers.

**Registers 0x78 to 0xFF.** Registers in the address range 0x78 to 0xFF should not be used. Do not write into any registers in the 0x78 to 0xFF range.

**Figure 5. Logic Diagram: Read Data (SPI 3-wire) from Registers for CPOL = 0 and CPOL = 1**



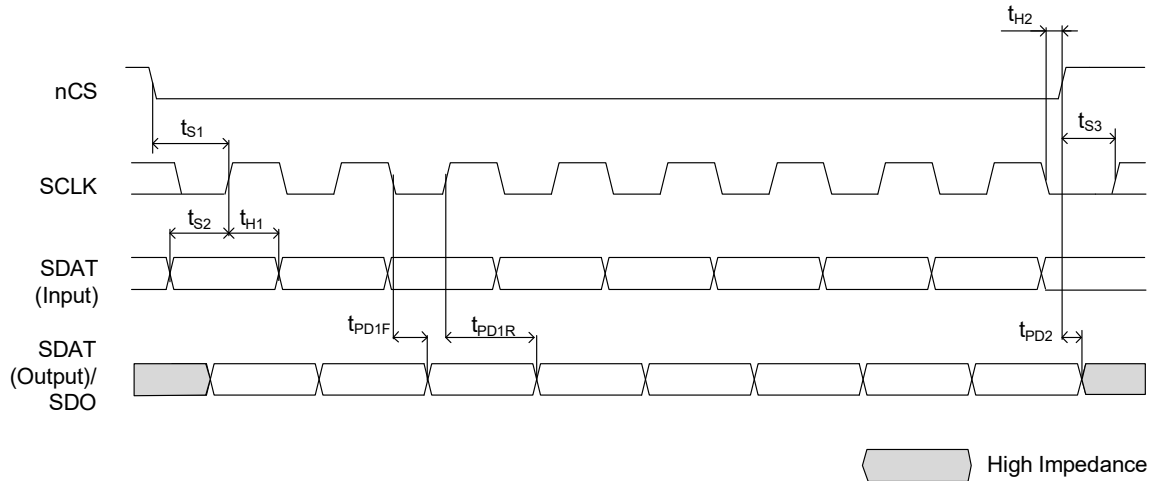
**Figure 6. Logic Diagram: Write Data into Registers**



**Table 25. SPI Read / Write Cycle Timing Parameters**

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
$f_{SCLK}$	SCLK frequency			20	MHz
$t_{S1}$	Setup time, nCS (falling) to SCLK (rising)		5		ns
$t_{S2}$	Setup time, SDAT (input) to SCLK (rising)		5		ns
$t_{S3}$	Setup time, nCS (rising) to SCLK (rising)		5		ns
$t_{H1}$	Hold time, SCLK (rising) to SDAT (input)		5		ns
$t_{H2}$	Hold time, SCLK (falling) to nCS (rising)		5		ns
$t_{PD2F}$	Propagation Delay, SCLK (falling) to SDAT (3-wire) or to SDO (4-wire)	CPOL = 0		5	ns
$t_{PD2R}$	Propagation Delay, SCLK (rising) to SDAT (3-wire) or to SDO (4-wire)	CPOL = 1		5	ns
$t_{PD3}$	Propagation delay, nCS to SDAT disable			5	ns

**Figure 7. SPI Timing Diagram**



**Table 26. Serial Interface Logic Voltage (SPI)<sup>[a]</sup>**

SELSV0	SPI Interface (SDAT, SDO, SCLK, nCS) Logic Voltage
0 (default)	1.8V
1	3.3V

[a] SELV0 is in register 0x1F, bit D4

**Table 27. Serial Interface Logic Voltage (Status Outputs)<sup>[a]</sup>**

SELSV1	Status Output (nINT, LOCK) Logic Voltage
0 (default)	1.8V
1	3.3V

[a] SELV1 is in register 0x1F, bit D5

## Configuration Registers

This section contains all addressable registers, sorted by function, followed for a detailed description of each bit field for each register. Several functional blocks with multiple instances in this device have individual registers controlling their settings, but since the registers have an identical format and bit meaning, they are described only once, with an additional table to indicate their addresses and default values. All writable register fields will come up with a default values as indicated in the Factory Defaults column unless altered by values loaded from non-volatile storage during the initialization sequence.

Fixed read-only bits will have defaults as indicated in their specific register descriptions. Read-only status bits will reflect valid status of the conditions they are designed to monitor once the internal power-up reset has been released. Unused registers and bit positions are Reserved. Reserved bit fields may be used for internal debug test and debug functions.

**Table 28. Configuration Registers**

Register Address	Register Description
0x00–0x01	PLL Frequency Divider: $\Phi$ MV, MV0
0x02–0x03	PLL Frequency Divider: MV1, BYPF
0x04–0x05	VCXO-PLL Control: $\Phi$ PV, PV
0x06–0x07	Reserved
0x08–0x09	PLL Frequency Divider: MF
0x0A	VCXO-PLL Control: BYPV
0x0B	Reserved
0x0C	PLL Frequency Divider: SRC, PF, FDF
0x0D–0x0F	Reserved
0x10–0x12	VCXO-PLL Control, Output state QOSC
0x13	Reserved
0x14	Input Selection Mode: Priority
0x15	Input Selection Mode: Switching
0x16	Input Selection Mode: CNTH
0x17	Input Selection Mode: CNTR, CNTV
0x18	SYSREF Control: Divider
0x19	SYSREF Control: SYNC, PD
0x1A	SYSREF Control: SRPC
0x1B	SYSREF Control: $\Phi$ REF_S
0x1C	SYSREF Control, QCLK_V_EN
0x1D–0x1E	Reserved
0x1F	SYSREF Control, SPI control, SPI/Status output control, QCLK_V_EN
0x20–0x22	Channel A
0x23	Reserved
0x24	Output State QCLK_A0
0x25	Output State QCLK_A1
0x26–0x27	Reserved
0x28	QREF_A0 Delay, MUX

**Table 28. Configuration Registers (Cont.)**

Register Address	Register Description
0x29	QREF_A1 Delay, MUX
0x2A	QREF_A2 Delay, MUX
0x2B	Reserved
0x2C	Output State QREF_A0
0x2D	Output State QREF_A1
0x2E	Output State QREF_A2
0x2F	Reserved
0x30–0x32	Channel B
0x33	Reserved
0x34	Output State QCLK_B0
0x35	Output State QCLK_B1
0x36–0x37	Reserved
0x38	QREF_B0 Delay, MUX
0x39	QREF_B1 Delay, MUX
0x3A–0x3B	Reserved
0x3C	Output State QREF_B0
0x3D	Output State QREF_B1
0x3E–0x3F	Reserved
0x40–0x42	Channel C
0x43–0x44	Reserved
0x45	Output State QCLK_C
0x46–0x48	Reserved
0x49	QREF_C Delay, MUX
0x4A–0x4C	Reserved
0x4D	Output State QREF_C
0x4E–0x4F	Reserved
0x50–0x52	Channel D
0x53	Reserved
0x54	Output State QCLK_D
0x55–0x57	Reserved
0x58	QREF_D Delay, MUX
0x59–0x5B	Reserved
0x5C	Output State QREF_D
0x5D–0x5F	Reserved
0x60–0x62	Channel E
0x63	Reserved

**Table 28. Configuration Registers (Cont.)**

Register Address	Register Description
0x64	Output State QCLK_E0
0x65	Output State QCLK_E1
0x66–0x67	Reserved
0x68–0x69	Interrupt Enable
0x6A–0x6B	Reserved
0x6C	Status (Latched)
0x6D	Status (Momentary)
0x6E	Status (Latched)
0x6F	Status (Momentary)
0x70	SYSREF control: RS
0x71–0x73	General Control
0x74–0x75	Output Enable QCLK
0x76	Output Enable QREF
0x77	Reserved
0x78–0x7A	Reserved
0x7B	Reserved
0x7C–0x7F	Reserved
0x80–0xFF	Reserved

## Channel and Clock Output Registers

The content of the channel register and clock output registers set the channel state, the clock divider, the QCLK output state and clock phase delay.

**Table 29. Channel and Clock Output Register Bit Field Locations**

Bit Field Location									
Register Address	D7	D6	D5	D4	D3	D2	D1	D0	
0x20: Channel A 0x30: Channel B 0x40: Channel C 0x50: Channel D 0x60: Channel E	Reserved					N_A[5:0] N_B[5:0] N_C[5:0] N_D[5:0] N_E[5:0]			
0x21: Channel A 0x31: Channel B 0x41: Channel C 0x51: Channel D 0x61: Channel E				$\Phi$ CLK_A[7:0] $\Phi$ CLK_B[7:0] $\Phi$ CLK_C[7:0] $\Phi$ CLK_D[7:0] $\Phi$ CLK_E[7:0]					
0x22: Channel A 0x32: Channel B 0x42: Channel C 0x52: Channel D 0x62: Channel E	PD_A PD_B PD_C PD_D PD_E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
0x24: QCLK_A0 0x25: QCLK_A1	PD_A0 PD_A1	Reserved	Reserved	STYLE_A0 STYLE_A1	A_A0[1:0] A_A1[1:0]		Reserved		
0x34: QCLK_B0 0x35: QCLK_B1	PD_B0 PD_B1	Reserved	Reserved	STYLE_B0 STYLE_B1	A_B0[1:0] A_B1[1:0]		Reserved		
0x45: QCLK_C	PD_C	Reserved	Reserved	STYLE_C	A_C[1:0]		Reserved		
0x54: QCLK_D	PD_D	Reserved	Reserved	STYLE_D	A_D[1:0]		Reserved		
0x64: QCLK_E0 0x65: QCLK_E1	PD_E0 PD_E1	Reserved	Reserved	STYLE_E0 STYLE_E1	A_E0[1:0] A_E1[1:0]		Reserved		
0x74	EN_QCLK_A0	EN_QCLK_A1	Reserved	EN_QCLK_B0	EN_QCLK_B1	Reserved	EN_QCLK_C	EN_QCLK_D	
0x75	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EN_QCLK_E1	EN_QCLK_E0	



**Table 30. Channel and Clock Output Register Descriptions<sup>[a]</sup>**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
N_x[5:0]	R/W	01 0001 Value = ÷30	Output Frequency Divider N N_x[5:0]Divider Value
			00 0001 ÷1      00 1001 ÷10
			00 0010 ÷2      00 1010 ÷12
			00 0011 ÷3      00 1011 ÷15
			00 0100 ÷4      00 1100 ÷16
			00 0101 ÷5      00 1101 ÷18
			00 0110 ÷6      00 1110 ÷20
			00 0111 ÷8      00 1111 ÷24
			00 1000 ÷9      01 0000 ÷25
			01 0001 ÷30      01 0100 ÷40
			01 0010 ÷32      01 0101 ÷48
			01 0011 ÷36
			01 0110 ÷50      01 1000 ÷60
			01 1010 ÷72      01 1001 ÷64
01 1101 ÷96      01 1011 ÷80			
01 1101 ÷96      01 1110 ÷100			
01 1111 ÷120			
10 0000 ÷128			
10 0001 ÷150			
10 0010 ÷160			
10 0011 ÷200			
PD_x	R/W	0	0 = Channel x is powered up 1 = Channel x is power down
PD_y	R/W	0	0 = Output QCLK_y is powered up 1 = Output QCLK_y is power down
ΦCLK_x[7:0]	R/W	0000 0000	CLK_x phase delay ΦCLK_x[7:0]
			Delay in ps = ΦCLK_x · 407ps (256 steps) 0000 0000 = 0 ps ... 1111 1111 = 103.76ns

**Table 30. Channel and Clock Output Register Descriptions<sup>[a]</sup>**

Bit Field Location				
Bit Field Name	Field Type	Default (Binary)	Description	
A <sub>y</sub> [1:0]	R/W	00	QCLK <sub>y</sub> Output amplitude	
			Setting for STYLE = 0 (LVDS)	Setting for STYLE = 1 (LVPECL)
			A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 750mV A[1:0] = 11:1000mV Termination: 100Ω across	A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 750mV A[1:0] = 11:1000mV Termination: 50Ω to VT
STYLE <sub>y</sub>	R/W	0	QCLK <sub>y</sub> Output format 0 = Output is LVDS (Requires LVDS 100Ω output termination) 1 = Output is LVPECL (Requires LVPECL 50Ω output termination of to the specified recommended termination voltage).	
EN <sub>y</sub>	R/W	0	QCLK <sub>y</sub> Output enable 0 = QCLK <sub>y</sub> Output is disabled at the logic low state 1 = QCLK <sub>y</sub> Output is enabled	

[a] x = A, B, C, D, E; y = A0, A1, B0, B1, C, D, E0, E1

## QREF Output State Registers

The content of the output registers set the output frequency and divider, several output states, the power state, the output style and amplitude.

**Table 31. QREF Output State Register Bit Field Locations**

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x28: QREF_A0 0x29: QREF_A1 0x2A: QREF_A2	Reserved	$\Phi$ REF_F[1:0]_A0 $\Phi$ REF_F[1:0]_A1 $\Phi$ REF_F[1:0]_A2		MUX_A0 MUX_A1 MUX_A2		$\Phi$ REF_A0[2:0] $\Phi$ REF_A1[2:0] $\Phi$ REF_A2[2:0]		$\Phi$ REF_F[2]_A0 $\Phi$ REF_F[2]_A1 $\Phi$ REF_F[2]_A2
0x38: QREF_B0 0x39: QREF_B1	Reserved	$\Phi$ REF_F[1:0]_B0 $\Phi$ REF_F[1:0]_B1		MUX_B0 MUX_B1		$\Phi$ REF_B0[2:0] $\Phi$ REF_B1[2:0]		$\Phi$ REF_F[2]_B0 $\Phi$ REF_F[2]_B1
0x49: QREF_C	Reserved	$\Phi$ REF_F[1:0]_C		MUX_C		$\Phi$ REF_C[2:0]		$\Phi$ REF_F[2]_C
0x58: QREF_D	Reserved	$\Phi$ REF_F[1:0]_D		MUX_D		$\Phi$ REF_D[2:0]		$\Phi$ REF_F[2]_D
0x2C: QREF_A0 0x2D: QREF_A1 0x2E: QREF_A2	PD_A0 PD_A1 PD_A2	Reserved	nBIAS_A0 nBIAS_A1 nBIAS_A2	STYLE_A0 STYLE_A1 STYLE_A2		A_A0[1:0] A_A1[1:0] A_A2[1:0]		Reserved
0x3C: QREF_B0 0x3D: QREF_B1	PD_B0 PD_B1	Reserved	nBIAS_B0 nBIAS_B1	STYLE_B0 STYLE_B1		A_B0[1:0] A_B1[1:0]		Reserved
0x4D: QREF_C	PD_C	Reserved	nBIAS_C	STYLE_C		A_C[1:0]		Reserved
0x5C: QREF_D	PD_D	Reserved	nBIAS_D	STYLE_D		A_D[1:0]		Reserved
0x76	EN_QREF_A0	EN_QREF_A1	EN_QREF_A2	EN_QREF_B0	EN_QREF_B1	Reserved	EN_QREF_C	EN_QCLK_D

**Table 32. QREF Output State Register Descriptions<sup>[a]</sup>**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
MUX_r	R/W	1	0 = QREF_r output signal source is the channel's clock signal 1 = QREF_r output signal source is the centrally generated SYSREF signal
$\Phi$ REF_r[2:0]	R/W	000	SYSREF coarse phase delay $\Phi$ REF_r[2:0] Delay in ps = $\Phi$ REF_r[2:0] · 407 ps (8 steps) 000 = 0 ps ... 111 = 2.848 ns

**Table 32. QREF Output State Register Descriptions<sup>[a]</sup>**

Bit Field Location				
Bit Field Name	Field Type	Default (Binary)	Description	
ΦREF_F[2:0]_r	R/W	000	SYSREF fine phase delay ΦREF_F[2:0]_r	
			Insert a SYSREF fine phase delay in ps (8 steps) in addition to the delay value in ΦREF_r[2:0] 000 = 0ps 001 = 25ps 010 = 50ps 011 = 75ps 100 = 85ps 101 = 110ps 110 = 135ps 111 = 160ps	
nBIAS_r	R/W	0	QREF_r Output Bias Voltage 0 = Output is not voltage biased. 1 = Output is biased to the LVDS cross-point voltage if BIAS_TYPE (register 0x19, bit 7) is set to 1. Bit has no effect if BIAS_TYPE = 0. Output bias = 1 requires AC coupling and LVDS style on the corresponding output.	
A_r[1:0]	R/W	00	QREF_r Output amplitude	
			Setting for STYLE_r = 0 (LVDS)	Setting for STYLE_r = 1 (LVPECL)
			A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 750mV A[1:0] = 11:1000mV Termination: 100Ω across	A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 750mV A[1:0] = 11:1000mV Termination: 50Ω to VT
PD_r	R/W	0	QREF_r Output Power Down 0 = Output is powered up 1 = Output is power down. STYLE, EN and A[1:0] settings have no effect.	
STYLE_r	R/W	0	QREF_r Output format 0 = Output is LVDS (Requires LVDS 100Ω output termination) 1 = Output is LVPECL (Requires LVPECL 50Ω output termination to the specified recommended termination voltage).	
EN_r	R/W	0	QREF_r Output enable 0 = Output is disabled at the logic low state 1 = Output is enabled	

[a] r = A0, A1, A2, B0, B1, C, D

## PLL Frequency Divider and SPI/Status Output Voltage Select Registers

**Table 33. PLL Frequency Divider and SPI/Status Output Voltage Select Register Bit Field Locations**

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x00		ΦMV0[2:0]		PD_MV1			MV0[11:8]	
0x01					MV0[7:0]			
0x02					MV1[7:0]			
0x03	MV[8]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPF
0x04		ΦPV[2:0]		Reserved			PV[11:8]	
0x05					PV[7:0]			
0x08	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MF[8]
0x09					MF[7:0]			
0x0A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPV
0x0C	FDF	SRC				PF[5:0]		
0x1F	BLOCK_LOLV	SDO_ACT	SELSV1	SELSV0			EN_QCLKV_MOD[3:0]	

**Table 34. PLL Frequency Divider and SPI/Status Output Voltage Select Register**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
ΦMV0[2:0]	R/W	101	Phase of the $M_{V0}$ feedback divider. Determines the PLL lock-detect phase window in conjunction with ΦPV[2:0]. Sampling clock phase is relative to the VCXO-PLL phase detector clock edge. Set ΦMV0[2:0] in relationship to $M_{V0}$ :
			$M_{V0}$ Divider Value ΦMV0[2:0] Setting
			1 - 31
			32 - 63
			64-127
			128-255
			256-511
			512-1023
			1024+
			010
			011
			100
			101
			110
			111

**Table 34. PLL Frequency Divider and SPI/Status Output Voltage Select Register**

Bit Field Location																
Bit Field Name	Field Type	Default (Binary)	Description													
MV0[11:0]	R/W	1100 0000 0000 Value = ±3072	VCXO-PLL Feedback-Divider The value of the frequency divider (binary coding) Range: ±1 to ±4095													
MV1[8:0]	R/W	0 0001 1110 Value = ±30	PLL Feedback-Divider. The value of the frequency divider (binary coding) Range: ±4 to ±511													
PD_MV1	R/W	0 Value = MV1 enabled	PLL Feedback-Divider MV1 Power Down/Disabled. 0 = MV1 Divider is enabled 1 = MV1 Divider is powered down and disabled Disabled MV1 to save power consumption in configurations not using the input clock monitors.													
ΦPV[2:0]	R/W	000	Phase of the P <sub>V</sub> input (reference) divider. Determines the PLL lock-detect phase window in conjunction with ΦMV0[2:0]. Sampling clock phase is relative to the VCXO-PLL phase detector clock edge. Set ΦPV[2:0] in relationship to P <sub>V</sub> :													
			<table border="1"> <thead> <tr> <th>P<sub>V</sub> Divider Value</th> <th>ΦPV[2:0] Setting</th> </tr> </thead> <tbody> <tr> <td>1 - 31</td> <td></td> </tr> <tr> <td>32 - 63</td> <td>010</td> </tr> <tr> <td>64-127</td> <td>011</td> </tr> <tr> <td>128-255</td> <td>100</td> </tr> <tr> <td>256-511</td> <td>101</td> </tr> <tr> <td>512-1023</td> <td>110</td> </tr> <tr> <td>1024+</td> <td>111</td> </tr> </tbody> </table>	P <sub>V</sub> Divider Value	ΦPV[2:0] Setting	1 - 31		32 - 63	010	64-127	011	128-255	100	256-511	101	512-1023
P <sub>V</sub> Divider Value	ΦPV[2:0] Setting															
1 - 31																
32 - 63	010															
64-127	011															
128-255	100															
256-511	101															
512-1023	110															
1024+	111															
PV[11:0]	R/W	1100 0000 0000 Value = ±3072	VCXO-PLL Input Frequency Pre-Divider The value of the frequency divider (binary coding) Range: ±1 to ±4095													
MF[8:0]	R/W	0 0001 1000 Value = ±24	FemtoClock NG Pre-Divider The value of the frequency divider (binary coding) Range: ±8 to ±511													
PF[5:0]	R/W	00 0000 Value = Bypass	FemtoClock NG Pre-Divider The value of the frequency divider (binary coding) Range: ±1 to ±63 00 0000: PF is bypassed													
FDF	R/W	0 Value = $f_{VCXO} \div PF$	Frequency Doubler The input frequency of the FemtoClock NG PLL (2nd stage) is: 0 = The output signal of the BYPV multiplexer, divided by the PF divider 1 = The output signal of the BYPV multiplexer, doubled in frequency. Use this setting to improve phase nose. The PF divider has no effect if FDF = 1.													

**Table 34. PLL Frequency Divider and SPI/Status Output Voltage Select Register**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
SRC	R/W	0 PLL enabled	Output Divider Source Signal (FemtoClock NG PLL Bypass) 0 = FemtoClock NG PLL is enabled and feeds the output channel dividers. 1 = FemtoClock NG PLL is disabled and bypassed. The VCXO-PLL output signal is frequency divided by the channel dividers.
BLOCK_LOLV	R/W	0 Not blocked	Blocks the LOLV status condition from reporting to the LOCK pin. 0 = The LOLV (VCXO-PLL lock) condition is reported to the LOCK pin. 1 = The LOLV (VCXO-PLL lock) condition does not affect the LOCK pin.
SDO_ACT	R/W	0 Value: 3-wire SPI	SPI interface select 0 = 3-wire. SDAT is SPI input and output. SDO is in high-impedance state 1 = 4-wire. SDAT is SPI input, SDO pin is the SPI output
SELSV0	R/W	0 Value: 1.8V	SPI (SDO, SDAT, nCS, SCLK) Logic Voltage Select 0 = 1.8V 1 = 3.3V
SELSV1	R/W	0 Value: 1.8V	Status output (nINT, LOCK) Logic Voltage Select 0 = 1.8V 1 = 3.3V

## VCXO-PLL Control Registers

**Table 35. VCXO-PLL Control Bit Field Locations**

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x03	MV1[8]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPF
0x0A	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	BYPV
0x10	POLV	FVCV	Reserved			CPV[4:0]		
0x11	nPD_QCLKV	STYLE_QCLKV	OSVEN			OFFSET[4:0]		
0x12	Reserved	A_QCLKV[1:0]				CPF[4:0]		

**Table 36. VCXO-PLL Control Register Descriptions**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
BYPF	R/W	0	PLL feedback Bypass 0 = VCXO-PLL feedback divider: MV0 1 = VCXO-PLL feedback divider: MV0 · MV1
BYPV	R/W	0	VCXO-PLL Bypass 0 = VCXO-PLL is enabled. 1 = VCXO-PLL is disabled and bypassed.
POLV	R/W	0	VCXO Polarity 0 = Positive polarity. Use for an external VCXO with a positive $f(V_C)$ characteristics 1 = Negative polarity. Use for an external VCXO with a negative $f(V_C)$ characteristics
FVCV	R/W	1	VCXO-PLL Force VC control voltage 0 = Normal operation. 1 = Forces the voltage at the LFV control pin (VCXO input) to $V_{DD\_V}/2$ . VCXO-PLL unlocks and the VCXO is forced to its mid-point frequency. FVCV = 1 is the default setting at startup to center the VCXO frequency. FVCV should be cleared after startup to enable the PLL to lock to the reference frequency.
CPV[4:0]	R/W	1 1000 Value: 1.25mA	VCXO-PLL Charge-Pump Current Controls the charge pump current $I_{CPV}$ of the VCXO-PLL. Charge pump current is the binary value of this register plus one multiplied by $50\mu\text{A}$ . $I_{CPV} = 50\mu\text{A} \cdot (\text{CPV}[4:0] + 1)$ . CPV[4:0] = 00000 sets ICPV to the min. current of $50\mu\text{A}$ . Max. charge pump current is 1.6 mA. Default setting is 1.25mA: $((24 + 1) \cdot 50\mu\text{A})$ .



**Table 36. VCXO-PLL Control Register Descriptions**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
nPD_QCLKV	R/W	0	<p>QCLK_V Power State:                      0 = Output QCLK_V is powered-down.                      1 = Output QCLK_V is powered-up.</p> <p><i>Power up behavior:</i> QCLK_V output is powered up after startup, while nPD_QCLKV remains at 0.</p> <p>To change the QCLK_V power state, first write the desired new nPD_QCLKV value, then write the <a href="#">EN_QCLKV_MOD[7:0]</a> register to make the change effective.</p>
STYLE_QCLKV	R/W	0	<p>QCLK_V Output Format:                      0 = Output is LVDS (requires an LVDS 100Ω output termination).                      1 = Output is LVPECL (requires an LVPECL 50Ω output termination of to the specified recommended termination voltage).</p> <p><i>Power up behavior:</i> QCLK_V output is set to LVPECL after startup, while STYLE_QCLKV remains at 0.</p> <p>To change the QCLK_V output format, first write the desired new STYLE_QCLKV value, then write the <a href="#">EN_QCLKV_MOD[7:0]</a> register to make the change effective.</p>
OSVEN	R/W	0	<p>VCXO-PLL Offset Enable                      0 = No offset                      1 = Offset enabled. A static phase offset of OFFSET[4:0] is applied to the PFD of the VCXO-PLL</p>
OFFSET[4:0]	R/W	0 0000 Value: 0°	<p>VCXO-PLL Static Phase Offset                      Controls the static phase detector offset of the VCXO-PLL. Phase offset is the binary value of this register multiplied by 0.9° of the PFD input signal (OFFSET [4:0] · f<sub>PFD</sub> ÷ 400). Max. offset is 31 · 0.9° = 27.9°. Setting OFFSET to 0.0° eliminates the thermal noise of an offset current. If the VCXO-PLL input jitter period T<sub>JIT</sub> exceeds the average input period: set OFFSET to a value larger than f<sub>PFD</sub> · T<sub>JIT</sub> · 400 to achieve a better charge pump linearity and lower in-band noise of the PLL.</p>
CPF[4:0]	R/W	1 1000 Value: 10mA	<p>FemtoClock NG-PLL Charge-Pump Current                      Controls the charge pump current I<sub>CPF</sub> of the FemtoClock NG PLL. Charge pump current is the binary value of this register plus one multiplied by 400μA.                      I<sub>CPF</sub> = 400μA · (CPF[4:0] + 1).                      CPV[4:0] = 00000 sets I<sub>CPF</sub> to the min. current of 400μA. Maximum charge pump current is 12.8mA. Default setting is 10.0mA: ((24+1) · 400μA)</p>

**Table 36. VCXO-PLL Control Register Descriptions**

Bit Field Location				
Bit Field Name	Field Type	Default (Binary)	Description	
A_QCLKV[1:0]	R/W	00	QCLK_V Output Amplitude	
			Setting for STYLE_r = 0 (LVDS)	Setting for STYLE_r = 1 (LVPECL)
			A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 500mV A[1:0] = 11: 750mV Termination: 100Ω across	A[1:0] = 00: 250mV A[1:0] = 01: 500mV A[1:0] = 10: 500mV A[1:0] = 11: 750mV Termination: 50Ω to VT
			<p><i>Power up behavior:</i> QCLK_V output is set to 750mV amplitude after startup, while A_QCLKV[1:0] remains at 00.</p> <p>To change the QCLK_V amplitude, first write the desired new A_QCLKV value, then write the <a href="#">EN_QCLKV_MOD[7:0]</a> register to make the change effective.</p>	

## Input Selection Mode Registers

**Table 37. Input Selection Mode Bit Field Locations**

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x14	PRIO_0[1:0]		PRIO_1[1:0]		Reserved			
0x15	Reserved	BLOCK_LOR	DIV4_VAL	REVS	nM/A[1:0]		SEL[1:0]	
0x16	CNTH[7:0]							
0x17	CNTR[1:0]		Reserved	Reserved	PD_CLKn		CNTV[1:0]	

**Table 38. Input Selection Mode Register Descriptions**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
PRIO_n[1:0]	R/W	CLK_0: 11 CLK_1: 10	Controls the auto-selection priority of the clock input CLK_n (n = 0...1). If multiple inputs have equal priority, the order within that priority is from CLK0 (highest) to CLK1 (lowest). 00 = Priority 0 (lowest) 01 = Priority 1 10 = Priority 2 11 = Priority 3 (highest)

**Table 38. Input Selection Mode Register Descriptions**

Bit Field Location					
Bit Field Name	Field Type	Default (Binary)	Description		
DIV4_VAL	R/W	0 Value: ÷1	Pre-divider for CNTV[1:0]. Use the ÷4 pre-divider for input frequencies > 250MHz. 0 = ÷1 1 = ÷4		
REVS	R/W	0 (Value: off)	Revertive Switching. The revertive input switching setting is only applicable to the two automatic selection modes shown in Table 10. If nM/A[1:0] = X0, the REVS setting has not meaning. 0 = Disabled: Re-validation of a non-selected input clock has no impact on the clock selection. 1 = Enabled: Re-validation of any non-selected input clock(s) will cause an new input selection according to the pre-set input priorities (revertive switch). An input switch is only done if the re-validated input has a higher priority than the current VCXO-PLL reference clock. Default setting is revertive switching turned off.		
nM/A[1:0]	R/W	00 Value: Manual Selection	Reference Input Selection Mode. In any of the manual selection modes (nM/A[1:0] = 00 or 10), the VCXO-PLL reference input is selected by SEL[1:0]. In any of the automatic selection modes, the VCXO-PLL reference input is selected by an internal state machine according to the input LOS states and the priorities in the input priority registers 00 = Manual selection 01 = Automatic selection (no holdover) 10 = Short-term holdover 11 = Automatic selection with holdover		
SEL[1:0]	R/W	00 Value: CLK0 selected	VCXO-PLL Input Reference Selection Controls the selection of the VCXO-PLL reference input in manual selection mode. In automatic selection modes (nM/A[1:0] = X1), SEL[1:0] has no meaning. 00 = CLK_0 01 = CLK_1		
CNTH[7:0]	R/W	1000 0000 (value: 136ms)	nMA[1:0] = 10 Short-term holdover: Hold-off counter period. The device initiates a clock failover switch upon counter expiration (zero transition). The counters start to counts backwards after a LOS event is detected. The hold-off counter period is determined by the binary number of VCXO-PLL output pulses divided by CNTR[1:0]. With a VCXO frequency of 122.88 MHz and CNTR[1:0] = 10, the counter has a period of (1.066 ms · binary setting). After each zero-transition, the counter automatically re-loads to the setting in this register. The default setting is 136ms (VCXO = 122.88MHz: 1/122.88MHz · 2 <sup>17</sup> · 128)		
CNTR[1:0]	R/W	10 (Value: 2 <sup>17</sup> )	Short-term holdover reference divider		
			CNTR[1:0]	CNTH frequency (period; range)	
				122.88MHz VCXO	38.4MHz VCXO
			00 = f <sub>VCXO</sub> ÷ 2 <sup>15</sup>		1171Hz (0.853ms; 0-217.6ms)
01 = f <sub>VCXO</sub> ÷ 2 <sup>16</sup>	1875Hz (0.533ms; 0-136ms)				
10 = f <sub>VCXO</sub> ÷ 2 <sup>17</sup>	937.5Hz (1.066ms; 0-272ms)				

**Table 38. Input Selection Mode Register Descriptions**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
CNTV[1:0]	R/W	10 (value: 32)	Controls the number of required consecutive, valid input reference pulses for clock re-validation on CLK <sub>n</sub> (n = 0...1), in number of input periods. At a LOS event, the re-validation counter loads this setting from the register and counts down by one with every valid, consecutive input signal period. Missing input edges (for one input period) will cause this counter to re-load its setting. An input is re-validated when the counter transitions to zero and the corresponding LOS flag is reset. DIV4_VAL = 0                      DIV4_VAL = 1
			00 = 2 (shortest possible) 01 = 16 10 = 32 11 = 64
PD_CLK <sub>n</sub>	R/W	0  Power up/Enabled	Input CLK <sub>n</sub> Power Down/Disable. 0 = Input CLK <sub>n</sub> is enabled 1 = Input CLK <sub>n</sub> is power down and disabled Disable individual Input CLK <sub>n</sub> input to save power consumption in configurations not using the respective input and in manual switching or short-term holdover mode. Enable inputs CLK <sub>n</sub> in configurations with automatic switching.
BLOCK_LOR	R/W	0  Value: Not blocked	Block loss-of-reference (input activity) indicator VCXO-PLL loss of lock signals nST_LOLV and nLS_LOLV are triggered by: 0 = VCXO-PLL loss of lock or by inactivity of the selected reference clock 1 = Only VCXO-PLL loss of lock. BLOCK_LOR = 1 will also block loss-of-reference from triggering a failure on the LOCK output pin.

## SYSREF, QCLK\_V Modification Control Registers

**Table 39. SYSREF, QCLK\_V Modification Control Register Bit Field Locations**

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x18								NS[7:0]
0x19	PD_S	BIAS_TYPE						SYNC[5:0]
0x1A								SRPC[7:0]
0x1B								ΦREF_S[7:0]
0x1C			EN_QCLKV_MOD[7:4]			Reserved	SR_INSEL	SRG SRO
0x1F	BLOCK_LOLV	SDO_ACT	SELSV1	SELSV0				EN_QCLKV_MOD[3:0]
0x70	RS	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

**Table 40. SYSREF, QCLK\_V Modification Control Register Descriptions**

Bit Field Location							
Bit Field Name	Field Type	Default (Binary)	Description				
PD_S	R/W	0	SYSREF global power down (incl. global delay ΦS, SYSREF frequency divider NS) 0 = SYSREF functional blocks are powered up. 1 = SYSREF functional blocks are powered down.				
NS[7:0]	R/W	00 00 00 00 Value = ÷64	SYSREF Frequency Divider. The value of the frequency divider is set by the product of 2 × NS[7] × NS[6] × NS[5:4] × NS[3] × NS[2] × NS[1:0]				
			NS[7:6]	NS[5:4]	NS[3]	NS[2]	NS[1:0]
			00 ⇒2 01 ⇒4 10 ⇒8 11 ⇒16	00 ⇒2 01 ⇒3 10 ⇒4 11 ⇒5	0 ⇒2 1 ⇒4	0 ⇒2 1 ⇒4	00 ⇒2 01 ⇒3 10 ⇒4 11 ⇒5
		The SYSREF contains five serial dividers that can be individually controlled by NS[6], NS[5:4], NS[3], NS[2] and NS[1:0], respectively; and an additional divide-by-two. Example: to achieve a SYSREF divider value of ÷3840 = 2 × {16} × {3} × {4} × {2} × {5}; set NS[7:6] = 11, NS[5:4] = 01, NS[3] = 1, NS[2] = 0, and NS[1:0] = 11. If a given output divider can be achieved by multiple NS[7:0] settings, use the highest possible divider in NS[7:6], then in NS[5:4], followed by NS[3], NS[2], and NS[1:0].					

**Table 40. SYSREF, QCLK\_V Modification Control Register Descriptions**

Bit Field Location					
Bit Field Name	Field Type	Default (Binary)	Description		
BIAS_TYPE	R/W	1	SYSREF output voltage bias 0 = QREF_r outputs are in a low/high state when nBIAS_r is set to 1 or during a SYSREF event 1 = QREF_r outputs are in a cross-point biased state when nBIAS_r is set to 1 or during a SYSREF event.		
SYNC[5:0]	R/W	010001 Value = ÷30	SYSREF Synchronizer divider value. This divider controls the release of SYSREF pulses at coincident QCLK clock edges. For SYSREF operation, set this divider value to half of the least common multiple of the clock divider values Nx (x = A to E). For example, if NA = NB = ÷2, NC = ND = ÷3, NE = ÷4, set the SYNC divider to ÷6. SYNC Frequency Divider N SYNC[5:0]    Divider Value                      SYNC[5:0]    Divider Value		
			00 0000    Do not use                      00 1001    ÷10		
			00 0001    Do not use                      00 1010    ÷12		
			00 0010    ÷2                                      00 1011    ÷15		
			00 0011    ÷3                                      00 1100    ÷16		
			00 0100    ÷4                                      00 1101    ÷18		
			00 0101    ÷5                                      00 1110    ÷20		
			00 0110    ÷6                                      00 1111    ÷24		
			00 0111    ÷8                                      01 0000    ÷25		
			00 1000    ÷9		
			01 0001    ÷30                                      01 0100    ÷40		
			01 0010    ÷32                                      01 0101    ÷48		
			01 0011    ÷36		
			01 0110    ÷50                                      01 1000    ÷60		
		01 1001    ÷64			
01 1010    ÷72                                      01 1011    ÷80					
01 1101    ÷96                                      01 1110    ÷100					
		01 1111    ÷120			
10 0000    ÷128                                      10 0010    ÷160					
10 0001    ÷150		10 0011    ÷200			
SRPC[7:0]	R/W	0000 0010 (value: 2)	SYSREF pulse count Binary value of the SYSREF pulses generated and output at all enabled QREF outputs. Allows to generate 1 to 255 pulses after each write access. Requires to set SRG = 0 and SRO = 0.		

**Table 40. SYSREF, QCLK\_V Modification Control Register Descriptions**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
ΦREF_S[7:0]	R/W	0000 0000	ΦREF_S global SYSREF phase delay. This setting affects all QREF_r outputs configured as SYSREF. ΦREF_S[7:0]
			Delay in ps = ΦREF_S · 814ps (256 steps) 0000 0000 = 0 ps ... 1111 1111 = 207.52 ns
SRG	R/W	0	SYSREF pulse generation 0 = Internal, SPI controlled SYSREF generation using the RS bit (set SR_INSEL = 0). 1 = External controlled SYSREF generation using the EXT_SYS or CLK_1 input.
SRO	R/W	0	SYSREF pulse mode 0 = Counted SYSREF pulse generation mode. Number of pulses is controlled by SRPC[7:0]. 1 = Continuous SYSREF pulse generation.
SR_INSEL	R/W	0	SYSREF input select 0 = EXT_SYS is the SYSREF input (single-ended signal support) 1 = CLK_1 is the SYSREF input (differential signal support)
RS	W only Auto-Clear	X	Set RS = 1 to initiate the SYSREF pulse generation of SRPC-number of pulses. Powers up the SYSREF circuitry and releases the SYSREF pulse(s) as configured. Requires SRG = 0 and SRO = 0, otherwise no function. RS = 1 also phase-aligns the QREF outputs to the QCLK outputs and adds the programmed delay values into the QREF paths.
EN_QCLKV_MOD[7:0]	R/W	0000 0000	Enable QCLK_V Configuration Modifications  Set EN_QCLKV_MODE[7:0] to the bit pattern 0100 1011 (0x4B) after QCLK_V configuration bits nPD_QCLKV (0x11, D7), STYLE_QCLKV (0x11, D6) and A_QCLKV[1:0] (0x12, D6:5) have been written. Set EN_QCLKV_MODE[7:4] to any other value, for instance to 0x00, to prevent changes to the nPD_QCLKV, STYLE_QCLKV and A_QCLKV[1:0] bits. If EN_QCLKV_MODE[7:0] is not set to 0x4B, the QCLK_V output is set to its startup configuration (LVPECL, 750mV, power on).

## Status Registers

**Table 41. Status Register Bit Field Locations**

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x68	Reserved	Reserved	IE_LOLF	IE_LOLV	Reserved	Reserved	IE_CLK_1	IE_CLK_0
0x69	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IE_REF	IE_HOLD
0x6C	Reserved	Reserved	nLS_LOLF	nLS_LOLV	Reserved	Reserved	LS_CLK_1	LS_CLK_0
0x6D	ST_SEL[1:0]		nST_LOLF	nST_LOLV	Reserved	Reserved	ST_CLK_1	ST_CLK_0
0x6E	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LS_REF	nLS_HOLD
0x6F	Reserved	Reserved	Reserved	Reserved	Reserved	ST_VCOF	ST_REF	nST_HOLD

**Table 42. Status Register Descriptions<sup>[a]</sup>**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
IE_LOLF	R/W	0	Interrupt Enable for FemtoClock NG-PLL loss of lock 0 = Disabled: Setting LS_LOLF will not cause an interrupt on nINT 1 = Enabled: Setting LS_LOLF will assert the nINT output (nINT = 0, interrupt)
IE_LOLV	R/W	0	Interrupt Enable for VCXO-PLL loss of lock 0 = Disabled: Setting LS_LOLV will not cause an interrupt on nINT 1 = Enabled: Setting LS_LOLV will assert the nINT output (nINT = 0, interrupt)
IE_CLK <sub>n</sub>	R/W	0	Interrupt Enable for CLK <sub>n</sub> input loss-of-signal 0 = Disabled: Setting LS_CLK <sub>n</sub> will not cause an interrupt on nINT 1 = Enabled: Setting LS_CLK <sub>n</sub> will assert the nINT output (nINT = 0, interrupt)
IE_REF	R/W	0	Interrupt Enable for LS_REF 0 = Disabled: any changes to LS_REF will not cause an interrupt on nINT 1 = Enabled: any changes to LS_REF will assert the nINT output (nINT = 0, interrupt)
IE_HOLD	R/W	0	Interrupt Enable for holdover 0 = Disabled: Setting LS_HOLD will not cause an interrupt on nINT 1 = Enabled: Setting LS_HOLD will assert the nINT output (nINT = 0, interrupt)
nLS_LOLF	R/W	-	FemtoClock NG-PLL loss of lock (latched status of nST_LOLF) Read 0 = ≥ 1 loss-of-lock events detected after the last status latch clear Read 1 = No loss-of-lock detected after the last status latch clear Write 1 = Clear status latch (clears pending nLS_LOLF interrupt)



**Table 42. Status Register Descriptions<sup>[a]</sup>**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
nLS_LOLV	R/W	-	VCXO-PLL loss of lock (latched status of nST_LOLV) Read 0 = ≥1 loss-of-lock events detected after the last status latch clear. Read 1 = No loss-of-lock detected after the last nLS_LOLV clear Write 1 = Clear status latch (clears pending nLS_LOLV interrupt)
LS_CLK_n	R/W	-	Input CLK_n status (latched status of ST_CLK_n) Read 0 = ≥1 LOS events detected on CLK_n after the last LS_CLK_n clear Read 1 = No loss-of-signal detected on CLK_n input after the last LS_CLK_n clear Write 1 = Clear LS_CLK_n status latch (clears pending LS_CLK_n interrupts on nINT)
ST_SEL[1:0]	R	-	Input selection (momentary status) Reference Input Selection Status of the state machine. In any input selection mode, reflects the input selected by the state machine. 00 = CLK_0 01 = CLK_1
nST_LOLF	R	-	FemtoClock NG-PLL loss of lock (momentary status) Read 0 = Loss-of-lock events detected Read 1 = No loss-of-lock detected A latched version of these status bit is available (nLS_LOLF)
nST_LOLV	R	-	VCXO-PLL loss of lock (momentary status bit) Read 0 = Loss-of-lock events detected Read 1 = No loss-of-lock detected A latched version of these status bits is available (nLS_LOLV)
ST_CLK_n	R	-	Input CLK_n status (momentary) 0 = LOS detected on CLK_n 1 = No LOS detected, CLK_n input is active A latched version of these status bits are available (LS_CLK_n)
LS_REF	R/W	-	PLL reference status (latched status of ST_REF) Read 0 = Reference is lost since last reset of this status bit. Read 1 = Reference is valid since last reset of this status bit. Write 1 = Clear LS_REF status latch (clears pending IE_REF interrupts on nINT)
nLS_HOLD	R/W	-	Holdover status indicator (latched status of nST_HOLD) Read 0 = VCXO-PLL has entered holdover state ≥1 times after reset of this status bit Read 1 = VCXO-PLL is (or attempts to) lock(ed) to an input clock Write 1 = Clear status latch (clears pending nLS_HOLD interrupt)
ST_VCOF	R	-	FemtoClock NG-PLL calibration status (momentary) Read 0 = FemtoClock NG PLL auto-calibration is completed Read 1 = FemtoClock NG PLL calibration is active (not completed)
ST_REF	R	-	Input reference status 0 = No input reference present 1 = Input reference is present at the clock input that is indicated by ST_SEL[1:0] A latched version of this status bit is available (LS_REF)

**Table 42. Status Register Descriptions<sup>[a]</sup>**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
nST_HOLD	R	-	Holdover status indicator (momentary) 0 = VCXO-PLL in holdover state, not locked to any input clock 1 = VCXO-PLL is (or attempts to) lock(ed) to input clock A latched version of this status bit is available (nLS_HOLD)

[a] CLK<sub>n</sub> = CLK0, CLK1.

## General Control Registers

**Table 43. General Control Register Bit Field Locations**

Bit Field Location								
Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0x71	INIT_CLK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x72	RELOCK	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x73	PB_CAL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	CPOL

**Table 44. General Control Register Descriptions**

Bit Field Location			
Bit Field Name	Field Type	Default (Binary)	Description
INIT_CLK	W only Auto-Clear	X	Set INIT_CLK = 1 to initialize divider functions. Required as part of the startup procedure.
RELOCK	W only Auto-Clear	X	Setting this bit to 1 will force the FemtoClock NG PLL to re-lock.
PB_CAL	W only Auto-Clear	X	Precision Bias Calibration Setting this bit to 1 will start the calibration of an internal precision bias current source. The bias current is used as reference for outputs configured as LVDS and for as reference for the charge pump currents. This bit will auto-clear after the calibration completed. Set as part of the startup procedure.
CPOL	R/W	0	SPI Read Operation SCLK Polarity: 0 = Data bits on SDAT (SPI 3-wire) / SDO (SPI 4-wire) are output at the falling edge of SCLK edge. 1 = Data bits on SDAT (SPI 3-wire) / SDO (SPI 4-wire) are output at the rising edge of SCLK edge.

## Electrical Characteristics

### Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 8V19N491-24 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 45. Absolute Maximum Ratings**

Item	Rating
Supply Voltage, $V_{DD\_V}$	3.6V
Inputs	-0.5V to $V_{DD\_V} + 0.5V$
Outputs, $V_O$ (LVCMOS)	-0.5V to $V_{DD\_V} + 0.5V$
Outputs, $I_O$ (LVPECL) Continuous Current Surge Current	50mA 100mA
Outputs, $I_O$ (LVDS) Continuous Current Surge Current	50mA 100mA
Input termination current, $I_{VT}$	$\pm 35mA$
Operating Junction Temperature, $T_J$	125°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
ESD - Human Body Model <sup>[a]</sup>	2000V
ESD - Charged Device Model <sup>[a]</sup>	500V

[a] According to JEDEC JS-001-2012/JESD22-C101

### Pin Characteristics

**Table 46. Pin Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$  (Case)**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$C_{IN}$ <sup>[a]</sup>	Input Capacitance	OSC, nOSC		2	4	pF
		Other inputs		2	4	pF
$R_{PU}$	Input Pull-Up Resistor	SDAT, nCS, nCLK_0, nCLK_1		51		k $\Omega$
$R_{PD}$	Input Pull-Down Resistor	EXT_SYS, SCLK, CLK_0, OSC, CLK_1		51		k $\Omega$
$R_{OUT}$	LVCMOS Output Impedance	nINT, LOCK		25		$\Omega$

[a] Guaranteed by design

## DC Characteristics

**Table 47. Power Supply DC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$  (Case)<sup>[a]</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{DD\_V}$	Core Supply Voltage		3.135	3.3	3.465	V
$I_{DD\_V}$	Power Supply Current	Test Case 2 in Table 48		902	1020	mA

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**Table 48. Typical Power Supply DC Current Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$  (Case)<sup>[a][b]</sup>**

Symbol	Supply Pin Current		Test Case						Unit
			1	2	3	4	5	6	
	QCLK_y	Style	LVPECL	LVPECL	LVPECL	LVPECL	LVDS	LVDS	-
		State	On	On	On	On	On	On	-
		Amplitude	500	750	1000	250	500	750	mV
	QREF_r	Style	LVDS	LVDS	LVDS	LVDS	LVDS	LVDS	-
		State	On	On	Off	On	Off	Off	-
		Amplitude	500	500	-	250	-	-	mV
$I_{DD\_CA}$	Current through VDD_QCLKA pins		85	101	113	75	69	85	mA
$I_{DD\_CB}$	Current through VDD_QCLKB pins		89	101	112	79	69	85	mA
$I_{DD\_CC}$	Current through VDD_QCLKC pins		64	69	75	58	53	61	mA
$I_{DD\_CD}$	Current through VDD_QCLKD pin		60	66	72	55	49	57	mA
$I_{DD\_CE}$	Current through VDD_QCLKE pins		91	102	113	80	69	85	mA
$I_{DD\_RA}$	Current through VDD_QREFA0-2 pins		77	77	0	56	0	0	mA
$I_{DD\_RB}$	Current through VDD_QREFB0-1 pins		51	51	0	37	0	0	mA
$I_{DD\_RC}$	Current through VDD_QREFC pin		27	25	0	21	0	0	mA
$I_{DD\_RD}$	Current through VDD_QREFD pin		26	26	0	19	0	0	mA
$I_{DD\_INP}$	Current through VDD_INP pin		68	69	69	68	69	69	mA
$I_{DD\_SPI}$	Current through VDD_SPI pin		7	7	7	7	8	8	mA
$I_{DD\_OSC} + I_{DD\_CP}$	Current through VDD_OSC and VDD_CP pins		31	31	31	31	31	31	mA
$I_{DD\_SYNC}$	Current through VDD_SYNC pin		91	91	31	91	31	31	mA
$I_{DD\_CPF}$	Current through VDD_CPF pin		86	86	87	86	85	85	mA
$I_{DD\_LCV}$	Current through VDD_LCV1-2 pins		94	94	94	94	95	94	mA
$I_{DD\_LCF}$	Current through VDD_LCF pin		51	51	51	51	52	52	mA
$P_{TOT}$	Total Device Power Consumption		2.89	2.98	2.28	2.65	2.24	2.45	W
$P_{TOT, SYS}$	Total System Power Consumption <sup>[c]</sup>		3.30	3.46	2.82	2.99	2.24	2.45	W

- [a]  $f_{CLK}$  (input) = 122.88MHz,  $f_{SYSREF}$ =7.68MHz, internal SYSREF generation (continuous). Supply current is independent of the output frequency configuration used for this table: QA[1:0]=2457.6MHz, QB[1:0]=245.76MHz, QC=245.76MHz, QD=491.52MHz, QE[1:0] = 122.88MHz). QCLK\_y outputs terminated according to amplitude settings. QREF\_r outputs unterminated when SYSREF is turned off.
- [b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
- [c] Includes total device power consumption and the power dissipated in external output termination components.

**Table 49. LVC MOS DC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$  (Case)<sup>[a]</sup>**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
<b>SYSREF Trigger Input EXT_SYS (1.8V/3.3V Selectable Logic)</b>							
$V_{IH}$	Input High Voltage			1.17		$V_{DD\_V}$	V
$V_{IL}$	Input Low Voltage			-0.3		0.63	V
$I_{IH}$	Input High Current	Input with pull-down resistor	$V_{DD\_V} = 3.3V, V_{IN} = 1.8V$ or $3.3V$			150	$\mu A$
$I_{IL}$	Input Low Current			$V_{DD\_V} = 3.3V, V_{IN} = 0V$	-5		
<b>SPI Inputs SDAT (when input), SCLK, nCS (1.8V/3.3V selectable logic with input hysteresis)</b>							
$V_I$	Input Voltage			-0.3		$V_{DD\_V}$	V
$V_{T+}$	Positive-going input threshold voltage		1.8V logic (SELSV0 = 0)	0.660		1.350	V
			3.3V logic (SELSV0 = 1)		1.8-2.1		V
$V_{T-}$	Negative-going input threshold voltage		1.8V logic (SELSV0 = 0)	0.495		1.170	V
			3.3V logic (SELSV0 = 1)		0.75-0.97		V
$V_H$	Hysteresis Voltage		$V_{T+} - V_{T-}$	0.165		0.780	V
<b>SPI output DAT (when output), SDO, nINT, LOCK (1.8V/3.3V selectable logic)</b>							
$V_{OH}$	Output High Voltage		1.8V logic (SELSV = 0) $I_{OH} = -4mA$	1.35			V
			3.3V logic (SELSV = 1) $I_{OH} = -4mA$	2.4			V
$V_{OL}$	Output Low Voltage		1.8V logic (SELSV = 0) $I_{OL} = 4mA$			0.45	V
			3.3V logic (SELSV = 1) $I_{OL} = 4mA$			0.4	V

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**Table 50. Differential Input DC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$  (Case)<sup>[a]</sup>**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
$I_{IH}$	Input High Current	Inputs with pull-down resistor <sup>[b]</sup>	$V_{DD\_V} = V_{IN} = 3.465V$			150	$\mu A$
		Pull-down/pull-up inputs <sup>[c]</sup>				150	$\mu A$
$I_{IL}$	Input Low Current	Inputs with pull-down resistor	$V_{DD\_V} = 3.465V, V_{IN} = 0V$	-50			$\mu A$
		Pull-down/pull-up inputs <sup>[c]</sup>		-150			$\mu A$

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Non-Inverting inputs: CLK\_n, OSC

[c] Inverting inputs: nCLK\_n, nOSC

**Table 51. LVPECL DC Characteristics (QCLK\_y, QREF\_r, STYLE = 1),  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$  (Case)<sup>[a]</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{OH}$	Output High Voltage <sup>[b]</sup>	250mV Amplitude Setting	$V_{DD\_V} - 1.027$	$V_{DD\_V} - 0.838$	$V_{DD\_V} - 0.750$	V
		500mV Amplitude Setting	$V_{DD\_V} - 1.041$	$V_{DD\_V} - 0.857$	$V_{DD\_V} - 0.708$	V
		750mV Amplitude Setting	$V_{DD\_V} - 1.054$	$V_{DD\_V} - 0.876$	$V_{DD\_V} - 0.755$	V
		1000mV Amplitude Setting	$V_{DD\_V} - 1.078$	$V_{DD\_V} - 0.898$	$V_{DD\_V} - 0.777$	V
$V_{OL}$	Output Low Voltage	250mV Amplitude Setting	$V_{DD\_V} - 1.311$	$V_{DD\_V} - 1.138$	$V_{DD\_V} - 0.949$	V
		500mV Amplitude Setting	$V_{DD\_V} - 1.575$	$V_{DD\_V} - 1.421$	$V_{DD\_V} - 1.212$	V
		750mV Amplitude Setting	$V_{DD\_V} - 1.842$	$V_{DD\_V} - 1.703$	$V_{DD\_V} - 1.493$	V
		1000mV Amplitude Setting	$V_{DD\_V} - 2.119$	$V_{DD\_V} - 1.983$	$V_{DD\_V} - 1.746$	V

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] Outputs terminated with 50 $\Omega$  to  $V_{DD\_V} - 1.5V$  (250mV amplitude setting),  $V_{DD\_V} - 1.75V$  (500mV amplitude setting),  $V_{DD\_V} - 2.0V$  (750mV amplitude setting),  $V_{DD\_V} - 2.25V$  (1000mV amplitude setting)

**Table 52. LVDS DC Characteristics (QCLK\_y, QREF\_r, STYLE = 0),  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$  (Case)<sup>[a]</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{OS}$	Offset Voltage <sup>[b]</sup>	250mV Amplitude Setting	2.05	2.37	2.70	V
		500mV Amplitude Setting	1.90	2.21	2.55	V
		750mV Amplitude Setting	1.75	2.06	2.39	V
		1000mV Amplitude Setting	1.60	1.91	2.20	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change			50	mV	

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b]  $V_{OS}$  changes with  $V_{DD\_V}$

## AC Characteristics

**Table 53. AC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$  (Case)<sup>[a][b]</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$f_{VCO}$	VCO Frequency		2400	2457.6	2500	MHz
$f_{OUT}$	Output Frequency	QCLK_y, QREF_r (Clock), N=÷1		2457.6		MHz
		QCLK_y, QREF_r (Clock), N=÷2		1228.8		MHz
		QCLK_y, QREF_r (Clock), N=÷4		614.4		MHz
		QCLK_y, QREF_r (Clock), N=÷5		491.52		MHz
		QCLK_y, QREF_r (Clock), N=÷8		307.2		MHz
		QCLK_y, QREF_r (Clock), N=÷10		245.76		MHz
		QCLK_y, QREF_r (Clock), N=÷20		122.88		MHz
		QREF_r (SYSREF)	0.192		38.4	MHz
$f_{CLK}$	Input Frequency	CLK_n	1.92 <sup>[c]</sup>	245.76	2000	MHz
$f_{VCXO}$	VCXO Frequency		30.72	122.88	491.52	MHz
$\Delta_{fp}$	Static Frequency Error	$f_{CLK} = 0$ ppb frequency deviation			0	ppb
$\Delta_{frms}$	Dynamic Frequency Error RMS <sup>[d]</sup>	$f_{CLK} = 0$ ppb frequency deviation			0.5	ppb
$V_{IN}$	Input Voltage Amplitude <sup>[e]</sup>	CLK_n, nCLK_n	0.15		1.2	V
$V_{DIFF\_IN}$	Differential Input Voltage Amplitude <sup>[e],[f]</sup>	CLK_n - nCLK_n	0.3		2.4	V
$V_{CMR}$	Common Mode Input Voltage		1.0		$V_{DD\_V} - (V_{IN} / 2)$	V
odc	Output Duty Cycle	QCLK_y, QREF_r (Clock)	45	50	55	%
$t_R / t_F$	Output Rise/Fall Time, Differential	QCLK_y, QREF_r (LVPECL), 20% to 80%			250	ps
		QCLK_y, QREF_r (LVDS), 20% to 80%			250	ps
		QREF_r (SYSREF, LVDS), 20% to 80%			250	ps
	Output Rise/Fall Time	LVC MOS outputs, 20%-80%			1	ns

**Table 53. AC Characteristics,  $V_{DD\_Y} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$  (Case)<sup>[a][b]</sup> (Cont.)**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$V_{O(PP)}$ <sup>[g]</sup>	LVPECL Output Voltage Swing, Peak-to-peak, 2457.6MHz	250mV Amplitude Setting	187	250	339	mV
		500mV Amplitude Setting	323	425	625	mV
		750mV Amplitude Setting	421	580	821	mV
		1000mV Amplitude Setting	493	710	1032	mV
	LVPECL Differential Output Voltage Swing, Peak-to-peak, 2457.6MHz	250mV Amplitude Setting	374	490	678	mV
		500mV Amplitude Setting	646	850	1250	mV
		750mV Amplitude Setting	842	1160	1641	mV
		1000mV Amplitude Setting	986	1420	2064	mV
$V_{OD}$ <sup>[h]</sup>	LVDS Output Voltage Swing, Peak-to-peak, 2457.6MHz	250mV Amplitude Setting	118	150	224	mV
		500mV Amplitude Setting	241	320	458	mV
		750mV Amplitude Setting	343	470	680	mV
		1000mV Amplitude Setting	415	600	898	mV
	LVDS Differential Output Voltage Swing, Peak-to-peak, 2457.6MHz	250mV Amplitude Setting	236	300	449	mV
		500mV Amplitude Setting	482	635	915	mV
		750mV Amplitude Setting	686	940	1360	mV
		1000mV Amplitude Setting	830	1200	1795	mV
$\Delta t_{PD}$	Propagation delay variation between reference input and any QCLK_y output		-200		+200	ps
$t_{sk(o)}$	Output Skew <sup>[i],[j]</sup> All delays set to 0	QCLK_y (same N divider)			100	ps
		QCLK_y (any N divider, incident rising edge)			100	ps
		QREF_r (Clock)			100	ps
		QREF_r (SYSREF)			100	ps
		QREF_r (Clock) to QCLK_y (any divider, incident rising QCLK edge)			150	ps
		QREF_r (SYSREF) to QCLK_y (any divider, incident rising QCLK edge)			150	ps
$\Delta F$	Output isolation between any neighboring clock output	$f_{OUT} = 1228.8MHz$	71	76		dB
		$f_{OUT} = 491.52MHz$	65	83		dB
		$f_{OUT} = 245.76MHz$	70	83		dB
$\Delta F$	Output isolation between any QCLK_y, QREF_r (SYSREF <sup>[k]</sup> ) output	Both SYSREF and clock signals active	50	60		dB
$t_{D, LOS}$	LOS state detected (measured in input reference periods)	$f_{CLK} = 122.88MHz$			2	$T_{IN}$
		$f_{CLK} = 245.76MHz$			3	



**Table 53. AC Characteristics,  $V_{DD\_V} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$  (Case)<sup>[a][b]</sup> (Cont.)**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$t_{D\_LOCK}$	PLL lock detect	PLL re-lock time after a short-term holdover scenario. Measured from LOS to both PLLs lock-detect asserted; hold-off timer = 200ms, PLL1 bandwidth = 100Hz, initial frequency error <200 ppm.		42	300	ms
$t_{D\_RES}$	PLL lock residual time error	Refer to PLL lock detect $t_{D\_LOCK}$ . Reference point: final value of clock output phase after all phase transitions settled. PLL1 bandwidth = 100Hz		0.0099	20	ns
$\Delta f_{HOLD}$	Holdover accuracy	Max. frequency deviation during a holdover duration of 200ms and after the clock re-validate event. PLL1 bandwidth = 100Hz		1.62	$\pm 5$	ppm
$t_{D\_RES-H}$	Holdover residual error	Measured 50ms after the reference clock re-appeared in a holdover scenario. Reference point: final value of clock output phase after all phase transitions settled. PLL1 bandwidth = 100Hz		4.32	$\pm 8.138$	ns
$t_{H\_E}$	Hold Time	EXT_SYS to CLK_n	-3			ns
$t_{S\_E}$	Setup Time	EXT_SYS to CLK_n	-0.5			ns
$t_{W\_E}$	Pulse Width	EXT_SYS	2			ns
$t_{H\_C}$	Hold Time	CLK_1 to CLK_n	-3			ns
$t_{S\_C}$	Setup Time	CLK_1 to CLK_n	-3			ns
$t_{W\_C}$	Pulse Width	CLK_1	2			ns

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] VCXO-PLL bandwidth = 100Hz.

[c] Minimum input frequency for the loss the input reference detector is  $f_{VCO}/MV1(MAX)$

[d] RMS frequency error, measured at any QCLK\_y output, caused by Gaussian noise. Weighted with a 1ms low pass time window filter.

[e]  $V_{IL}$  should not be less than -0.3V and  $V_{IH}$  should not be greater than  $V_{DD\_V}$

[f] Common Mode Input Voltage is defined as the cross-point voltage.

[g] LVPECL outputs terminated with 50Ω to  $V_{CC0} - 1.5V$  (250mV amplitude setting),  $V_{CC0} - 1.75V$  (500mV amplitude setting),  $V_{CC0} - 2.0V$  (750mV amplitude setting),  $V_{CC0} - 2.25V$  (1000mV amplitude setting)

[h] LVDS outputs terminated 100Ω across terminals

[i] This parameter is defined in accordance with JEDEC standard 65

[j] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential cross points

[k] SYSREF frequencies: 30.72, 15.36, 7.68MHz

**Table 54. Clock Phase Noise Characteristics ( $f_{VCXO} = 122.88\text{MHz}$ ),  $FDF = 1$ ,  $V_{DD_V} = 3.3\text{V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  (Case)<sup>[a][b][c][d]</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
$f_{jit}(\emptyset)$	Clock RMS Phase Jitter (Random)	Integration Range: 1kHz - 76.8MHz		80	120	fs
		Integration Range: 12kHz - 20MHz		66	95	fs
$\Phi_N(10)$	Clock single-side band phase noise	245.76MHz	10Hz offset (determined by VCXO)	-80		dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)	-110		dBc/Hz
$\Phi_N(1k)$			1kHz offset from Carrier	-131	-128	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier	-138	-134	dBc/Hz
$\Phi_N(20k)$			20kHz offset from Carrier	-138	-137	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier	-141	-139	dBc/Hz
$\Phi_N(250k)$			250kHz offset from Carrier	-145	-143	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier	-153	-151	dBc/Hz
$\Phi_N(\geq 10M)$			$\geq 10\text{MHz}$ offset from Carrier and Noise Floor	-158	-157	dBc/Hz
$\Phi_N(10)$	Clock single-side band phase noise	491.52MHz	10Hz offset (determined by VCXO)	-75		dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)	-104		dBc/Hz
$\Phi_N(1k)$			1kHz offset from Carrier	-125	-122	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier	-132	-129	dBc/Hz
$\Phi_N(20k)$			20kHz offset from Carrier	-132	-131	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier	-135	-134	dBc/Hz
$\Phi_N(250k)$			250kHz offset from Carrier	-138	-137	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier	-148	-145	dBc/Hz
$\Phi_N(\geq 10M)$			$\geq 10\text{MHz}$ offset from Carrier and Noise Floor	-154	-153	dBc/Hz
$\Phi_N(10)$	Clock single-side band phase noise	614.4MHz	10Hz offset (determined by VCXO)	-73		dBc/Hz
$\Phi_N(100)$			100Hz offset (determined by VCXO)	-102		dBc/Hz
$\Phi_N(1k)$			1kHz offset from Carrier	-125	-122	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier	-131	-127	dBc/Hz
$\Phi_N(20k)$			20kHz offset from Carrier	-131	-129	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier	-133	-132	dBc/Hz
$\Phi_N(250k)$			250kHz offset from Carrier	-137	-135	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier	-146	-143	dBc/Hz
$\Phi_N(\geq 10M)$			$\geq 10\text{MHz}$ offset from Carrier and Noise Floor	-156	-153	dBc/Hz

**Table 54. Clock Phase Noise Characteristics ( $f_{VCXO} = 122.88\text{MHz}$ ),  $FDF = 1$ ,  $V_{DD_V} = 3.3\text{V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  (Case)<sup>[a][b][c][d]</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit	
$\Phi_N(10)$	Clock single-side band phase noise	1228.8MHz	10Hz offset (determined by VCXO)		-67	dBc/Hz	
$\Phi_N(100)$			100Hz offset (determined by VCXO)		-96	dBc/Hz	
$\Phi_N(1k)$			1kHz offset from Carrier		-120	-119	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-125	-124	dBc/Hz
$\Phi_N(20k)$			20kHz offset from Carrier		-125	-123	dBc/Hz
$\Phi_N(100k)$			100kHz offset from Carrier		-127	-126	dBc/Hz
$\Phi_N(250k)$			250kHz offset from Carrier		-131	-129	dBc/Hz
$\Phi_N(1M)$			1MHz offset from Carrier		-141	-139	dBc/Hz
$\Phi_N(\geq 10M)$			$\geq 10\text{MHz}$ offset from Carrier and Noise Floor		-153	-151	dBc/Hz
$\Phi$	Spurious signals (QCLK, QREF as clock)	491.52MHz	100Hz - 300Hz		-82	-75	dBc
			300Hz - 100kHz		-98	-86	dBc
			100kHz - 100MHz		-93	-85	dBc
			122.88MHz reference spurious <sup>[e]</sup>		-92	-82	dBc
			245.76MHz reference spurious <sup>[f]</sup>		-84	-74	dBc
		245.76MHz	100Hz - 300Hz		-88	-80	dBc
			300Hz - 100kHz		-109	-102	dBc
			100kHz - 100MHz		-91	-88	dBc
			122.88MHz reference spurious <sup>[e]</sup>		-87	-82	dBc

[a] Phase noise characteristics at lower frequency offsets (10Hz ~1kHz) is primarily a function of the VCXO phase noise: VCXO characteristics:  $f = 122.88\text{MHz}$ ; phase noise:  $-87\text{dBc/Hz}(100\text{Hz})$ ,  $-118\text{dBc/Hz}(1\text{kHz})$ ,  $-141\text{dBc/Hz}(10\text{kHz})$ ,  $-152\text{dBc/Hz}$ ,  $-157\text{dBc/Hz}(1\text{MHz})$ .

[b] Phase noise and spurious specifications apply for device operation with QREF\_r outputs inactive (no SYSREF pulses generated).

[c] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[d] Phase noise specifications are applicable for all outputs active,  $N_x$  not equal. Measured without crystal reference noise.

[e] Measured at all offset frequencies except at  $f_{\text{OFFSET}} = 122.88\text{MHz}$ .

[f] Measured at all offset frequencies except at  $f_{\text{OFFSET}} = 245.76\text{MHz}$ .

**Table 55. Clock Phase Noise Characteristics (f<sub>VCXO</sub> = 491.52MHz), FDF = 0, V<sub>DD\_V</sub> = 3.3V ±5%, T<sub>A</sub> = -40°C to +105°C (Case)<sup>[a][b][c][d]</sup>**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
f <sub>jit</sub> (∅)	Clock RMS Phase Jitter (Random)	Integration Range: 1kHz - 76.8MHz		79	120	fs
		Integration Range: 12kHz - 20MHz		61	100	fs
Φ <sub>N</sub> (10)	Clock single-side band phase noise	245.76MHz	10Hz offset (determined by VCXO)	-56		dBc/Hz
Φ <sub>N</sub> (100)			100Hz offset (determined by VCXO)	-89		dBc/Hz
Φ <sub>N</sub> (1k)			1kHz offset from Carrier	-121	-118	dBc/Hz
Φ <sub>N</sub> (10k)			10kHz offset from Carrier	-140	-133	dBc/Hz
Φ <sub>N</sub> (20k)			20kHz offset from Carrier	-141	-137	dBc/Hz
Φ <sub>N</sub> (100k)			100kHz offset from Carrier	-145	-142	dBc/Hz
Φ <sub>N</sub> (250k)			250kHz offset from Carrier	-147	-144	dBc/Hz
Φ <sub>N</sub> (1M)			1MHz offset from Carrier	-153	-151	dBc/Hz
Φ <sub>N</sub> (≥10M)			≥ 10MHz offset from Carrier and Noise Floor	-159	-156	dBc/Hz
Φ <sub>N</sub> (10)	Clock single-side band phase noise	491.52MHz	10Hz offset (determined by VCXO)	-50		dBc/Hz
Φ <sub>N</sub> (100)			100Hz offset (determined by VCXO)	-83		dBc/Hz
Φ <sub>N</sub> (1k)			1kHz offset from Carrier	-115	-112	dBc/Hz
Φ <sub>N</sub> (10k)			10kHz offset from Carrier	-134	-129	dBc/Hz
Φ <sub>N</sub> (20k)			20kHz offset from Carrier	-136	-132	dBc/Hz
Φ <sub>N</sub> (100k)			100kHz offset from Carrier	-139	-137	dBc/Hz
Φ <sub>N</sub> (250k)			250kHz offset from Carrier	-141	-139	dBc/Hz
Φ <sub>N</sub> (1M)			1MHz offset from Carrier	-147	-145	dBc/Hz
Φ <sub>N</sub> (≥10M)			≥ 10MHz offset from Carrier and Noise Floor	-155	-154	dBc/Hz
Φ	Spurious signals (QCLK, QREF as clock)	491.52MHz	100Hz - 300Hz	-81	-73	dBc
			300Hz - 100kHz	-92	-85	dBc
			100kHz - 100MHz	-92	-87	dBc
			122.88MHz reference spurious <sup>[e]</sup>	-84	-79	dBc
			245.76MHz reference spurious <sup>[f]</sup>	-91	-85	dBc
		245.76MHz	100Hz - 300Hz	-86	-79	dBc
			300Hz - 100kHz	-97	-92	dBc
			100kHz - 100MHz	-91	-82	dBc
122.88MHz reference spurious <sup>[e]</sup>	-83		-80	dBc		

[a] Phase noise characteristics at lower frequency offsets (10Hz ~1kHz) is primarily a function of the VCXO phase noise: VCXO characteristics: f = 122.88MHz; phase noise: -87dBc/Hz(100Hz), -118dBc/Hz(1kHz), -141dBc/Hz(10kHz), -152dBc/Hz/, -157dBc/Hz(1MHz).

[b] Phase noise and spurious specifications apply for device operation with QREF\_r outputs inactive (no SYSREF pulses generated).

[c] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[d] Phase noise specifications are applicable for all outputs active, Nx not equal. Measured without crystal reference noise.

[e] Measured at all offset frequencies except at  $f_{\text{OFFSET}} = 122.88\text{MHz}$ .

[f] Measured at all offset frequencies except at  $f_{\text{OFFSET}} = 245.76\text{MHz}$ .

**Table 56. SYSREF Phase Noise Characteristics,  $V_{\text{DD}_V} = 3.3\text{V} \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$  (Case)<sup>[a][b]</sup>**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
$\Phi_N(500)$	SYSREF single-side band phase noise	30.72MHz	500Hz offset		-145	-130	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-155	-130	dBc/Hz
$\Phi_N(60k)$			60kHz offset from Carrier		-155	-140	dBc/Hz
$\Phi_N(800k)$			800kHz offset from Carrier		-158	-145	dBc/Hz
$\Phi_N(\geq 3M)$			$\geq 3\text{MHz}$ offset from Carrier and Noise Floor		-158	-145	dBc/Hz
$\Phi_N(500)$	SYSREF single-side band phase noise	15.36MHz	500Hz offset		-148	-130	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-157	-130	dBc/Hz
$\Phi_N(60k)$			60kHz offset from Carrier		-158	-140	dBc/Hz
$\Phi_N(800k)$			800kHz offset from Carrier		-160	-145	dBc/Hz
$\Phi_N(\geq 3M)$			$\geq 3\text{MHz}$ offset from Carrier and Noise Floor		-160	-145	dBc/Hz
$\Phi_N(500)$	SYSREF single-side band phase noise	7.68MHz	500Hz offset		-138	-130	dBc/Hz
$\Phi_N(10k)$			10kHz offset from Carrier		-149	-130	dBc/Hz
$\Phi_N(60k)$			60kHz offset from Carrier		-158	-140	dBc/Hz
$\Phi_N(800k)$			800kHz offset from Carrier			-145	dBc/Hz
$\Phi_N(\geq 3M)$			$\geq 3\text{MHz}$ offset from Carrier and Noise Floor			-145	dBc/Hz
$\Phi$	Spurious signals <sup>[c]</sup>	30.72MHz	> 500Hz		-60	-56	dBc
		15.36MHz	> 500Hz		-60	-56	dBc
		7.68MHz	> 500Hz		-60	-56	dBc

[a] Phase noise is measured as additive phase noise contribution by the device on all SYSREF outputs, dividers and channel logic. SYSREF signals measured as continued clock signal. Clock signals (QCLK) are turned on.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500fpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Measured as sum of all spurious amplitudes in one side band in the offset frequency range above 500Hz, excluding the harmonics of the fundamental frequency of  $n \cdot f_{\text{SYSREF}}$  (e.g.,  $n \cdot 7.68\text{MHz}$ ).

**Table 57. AC Characteristics: Typical QCLK\_y Output Amplitude,  $V_{DD\_V} = 3.3V$ ,  $T_A = -40^{\circ}C$  to  $+105^{\circ}C$  (Case)<sup>[a]</sup>**

Symbol	Parameter	Test Conditions	QCLK_y Output Frequency in MHz						Unit
			2457.6	1228.8	614.4	491.52	307.2	245.76	
$V_{O(PP)}$ <sup>[b]</sup>	LVPECL Output Voltage Swing, Peak-to-peak	250mV Amplitude Setting	257	281	270	273	278	283	mV
		500mV Amplitude Setting	456	520	508	505	540	528	mV
		750mV Amplitude Setting	620	772	749	744	776	768	mV
		1000mV Amplitude Setting	748	1000	968	984	1000	1016	mV
$V_{OD}$ <sup>[c]</sup>	LVDS Output Voltage Swing, Peak-to-peak	250mV Amplitude Setting	145	200	220	220	230	230	mV
		500mV Amplitude Setting	310	432	450	450	470	478	mV
		750mV Amplitude Setting	455	615	685	680	720	732	mV
		1000mV Amplitude Setting	580	860	931	910	970	990	mV

[a] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[b] LVPECL outputs terminated with 50Ω to  $V_{DD\_V} - 1.5V$  (250mV amplitude setting),  $V_{DD\_V} - 1.75V$  (500mV amplitude setting),  $V_{DD\_V} - 2.0V$  (750mV amplitude setting),  $V_{CC0} - 2.25V$  (1000mV amplitude setting)

[c] LVDS outputs terminated 100Ω across terminals

## Clock Phase Noise Characteristics

Conditions for Phase Noise Characteristics:

VCXO characteristics:  $f = 122.88$  MHz and phase noise:  $-83dBc/Hz(10Hz)$ ,  $-113dBc/Hz(100Hz)$ ,  $-143dBc/Hz(1kHz)$ ,  $-153dBc/Hz(10kHz)$ ,  $-158dBc/Hz(100kHz)$

- Input reference frequency: 122.88MHz
- VCXO-PLL bandwidth: 10Hz
- VCXO-PLL charge pump current: 0.55mA
- FemtoClock NG PLL bandwidth: 59kHz
- $V_{DD\_V} = 3.3V$ ,  $T_A = 25^{\circ}C$

Figure 8. 2457.6MHz Output Phase Noise

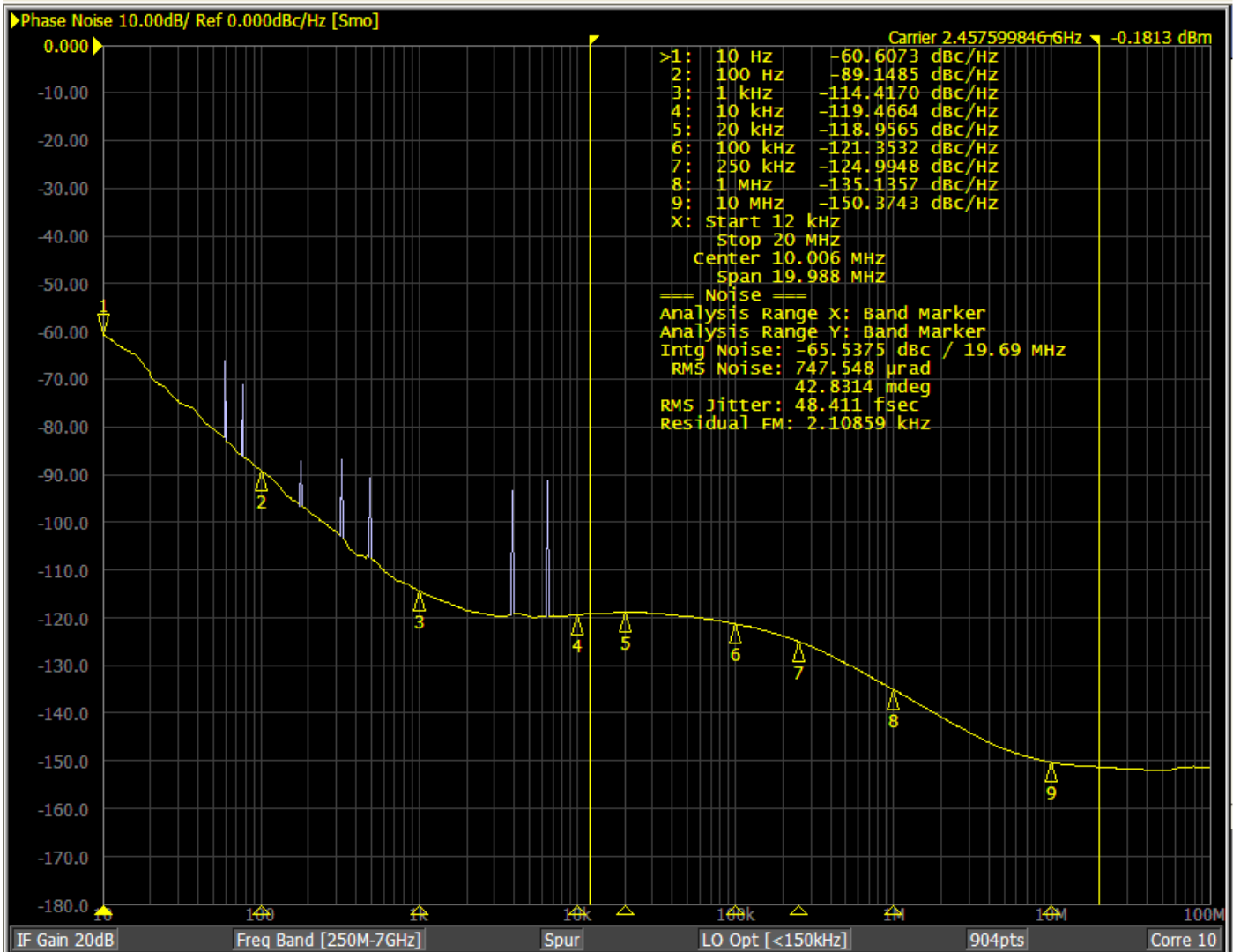


Figure 9. 491.52MHz Output Phase Noise

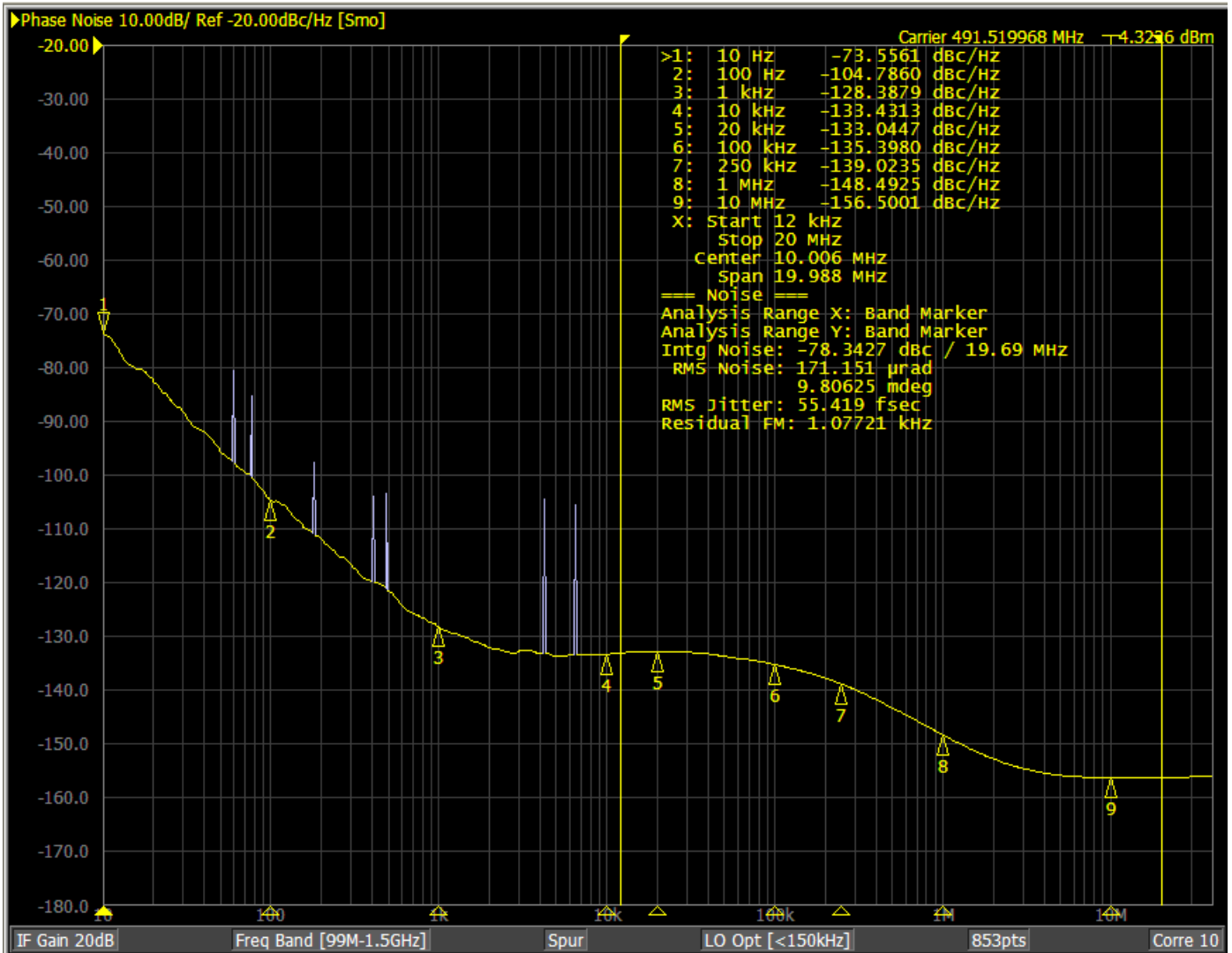
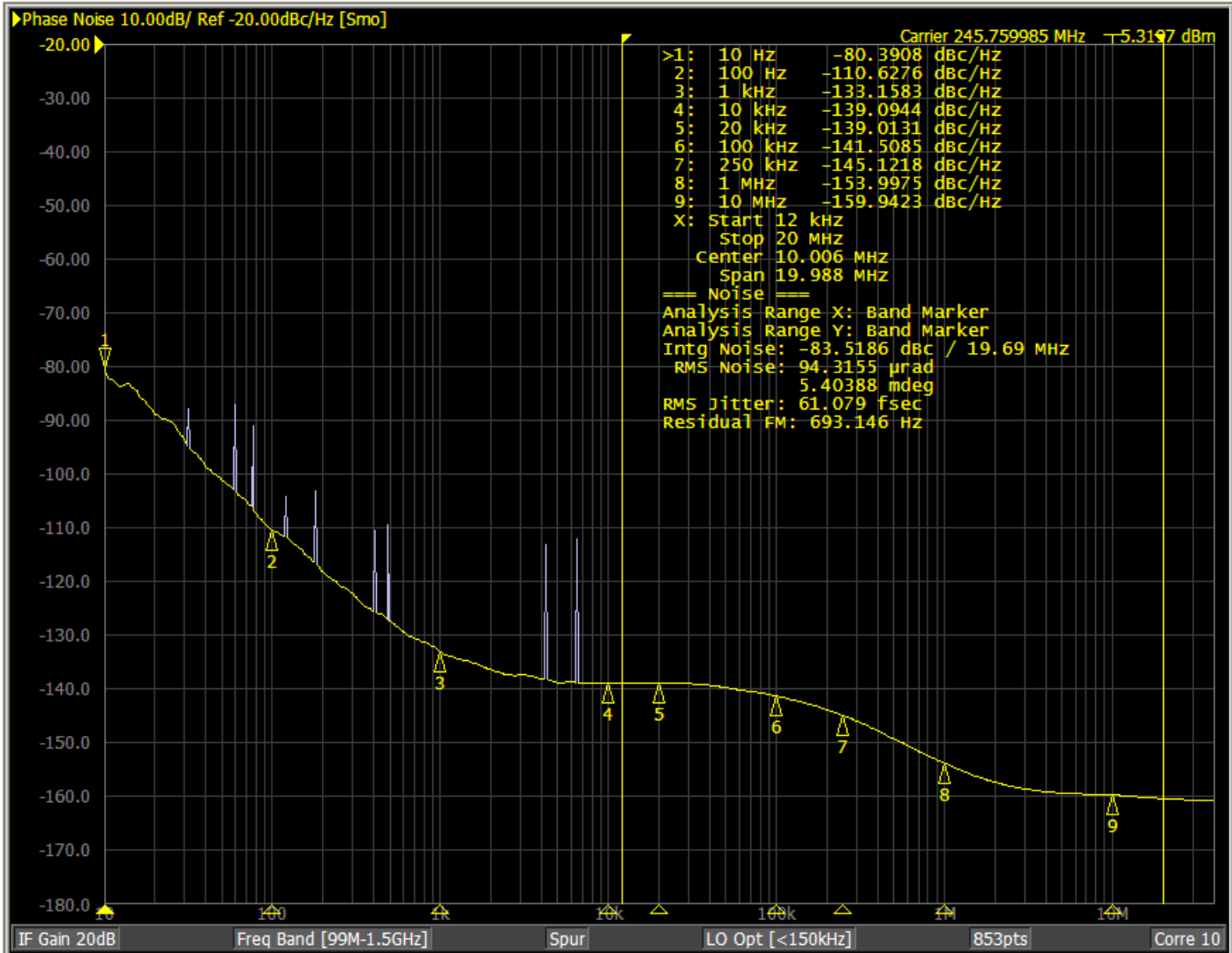




Figure 10. 245.76MHz Output Phase Noise

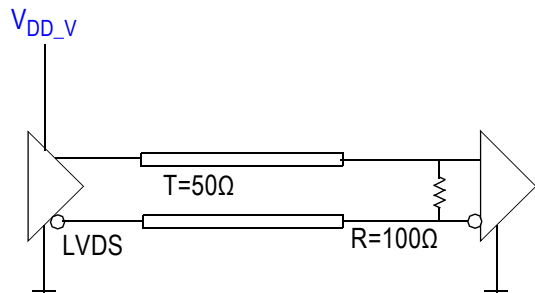


## Application Information

### Termination for QCLK\_y, QREF\_r LVDS Outputs (STYLE = 0)

Figure 11 shows an example termination for the QCLK\_y, QREF\_r LVDS outputs. In this example, the characteristic transmission line impedance is 50Ω. The termination resistor R (100Ω) is matched to the line impedance. The termination resistor must be placed at the line end. No external termination resistor is required if R is an internal part of the receiver circuit. The LVDS termination in Figure 11 is applicable for any output amplitude setting specified in Table 15.

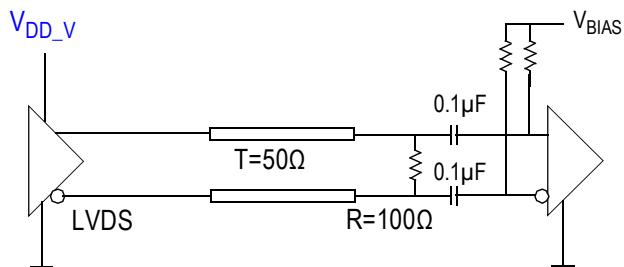
**Figure 11. LVDS (STYLE = 0) Output Termination**



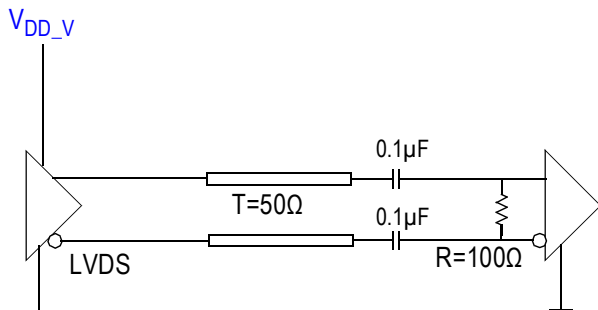
### AC Termination for QCLK\_y, QREF\_r LVDS Outputs (STYLE = 0)

Figure 12 and Figure 13 show example AC terminations for the QCLK\_y, QREF\_r LVDS outputs. In the examples, the characteristic transmission line impedance is 50Ω. In Figure 12, the termination resistor R (100Ω) is placed at the line end. No external termination resistor is required if R is an internal part of the receiver circuit, which is shown in Figure 14. The LVDS terminations in both Figure 12 and Figure 13 are applicable for any output amplitude setting specified in Table 15. The receiver input should be re-biased according to its common mode range specifications.

**Figure 12. LVDS (STYLE = 0) AC Output Termination**



**Figure 13. LVDS (STYLE = 0) AC Output Termination**



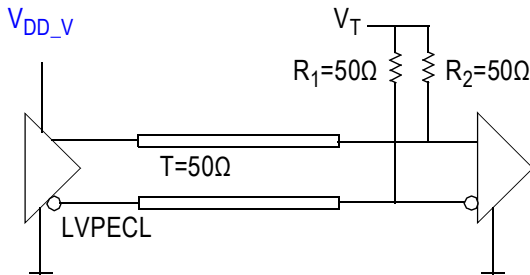
## Termination for QCLK\_y, QREF\_r LVPECL Outputs (STYLE = 1)

Figure 14 shows an example termination for the QCLK\_y, QREF\_r LVPECL outputs. In this example, the characteristic transmission line impedance is 50Ω. The R1 (50Ω) and R2 (50Ω) resistors are matched load terminations. The output is terminated to the termination voltage  $V_T$ . The  $V_T$  must be set according to the output amplitude setting defined in Table 15. The termination resistors must be placed close at the line end.

**Figure 14. LVPECL (STYLE = 1) Output Termination**

$$V_T = V_{DD\_V} - 1.50V \text{ (250 mV Amplitude)}$$

$$V_T = V_{DD\_V} - 1.75V \text{ (500 mV Amplitude)}$$

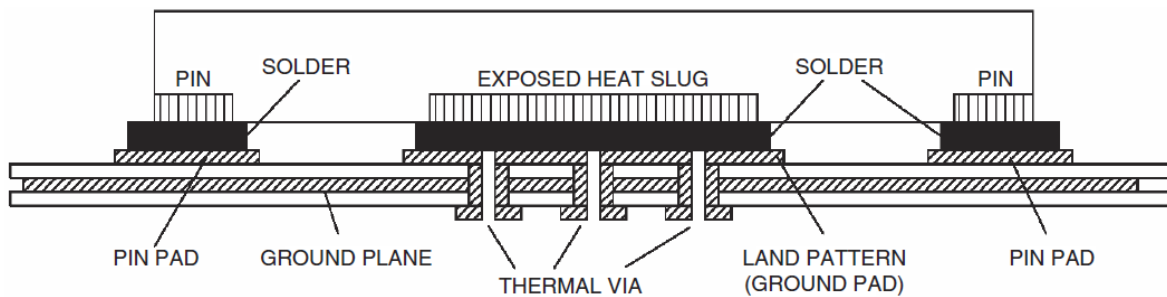


## Thermal Characteristics

### Package Exposed Pad Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 15. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

**Figure 15. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to Scale)**



While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes.” The number of vias (i.e., “heat pipes”) are application-specific and are dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13 mils (0.30 to 0.33 mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern.

Note: These recommendations are to be used as a guideline only. For more information, refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Lead-frame Base Package, Amkor Technology.

### Thermal Characteristics

The 8V19N492 is a multi-functional, high-speed device that targets a wide variety of clock frequencies and applications. Since this device is highly programmable with a broad range of features and functionality, the power consumption will vary as each of these features and functions is enabled. The device was designed and characterized to operate within the industrial temperature range of -40°C to +105°C (Case). The ambient temperature represents the temperature around the device, not the junction temperature. When using the device in extreme cases, such as maximum operating frequency and high ambient temperature, external air flow may be required in order to ensure a safe and reliable junction temperature. Extreme care must be taken to avoid exceeding 125°C junction temperature. For any concerns on calculating the power dissipation for your own specific configuration, please contact IDT technical support.

**Table 58. Thermal Resistance<sup>[a]</sup>**

Symbol	Thermal Parameter	Condition	Value	Unit
$\Theta_{JA}$	Junction to Ambient	0 m/s air flow	17.2	°C/W
		1 m/s air flow	16.1	°C/W
		2 m/s air flow	15.6	°C/W
$\Theta_{JC}$	Junction to Case		22.6	°C/W
$\Theta_{JB}$	Junction to Board		0.9	°C/W

[a] Standard JEDEC 2S2P multilayer PCB.

### Case Temperature Considerations

The 8V19N492 supports applications in a natural convection environment that does not have any thermal conductivity through ambient air. The PCB is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters that is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter  $\Psi_{JB}$  (Psi-JB) to calculate the junction temperature ( $T_J$ ) and ensure it does not exceed the maximum allowed junction temperature in [Absolute Maximum Ratings](#).

The junction-to-board thermal characterization parameter,  $\Psi_{JB}$ , is calculated using the following equation:

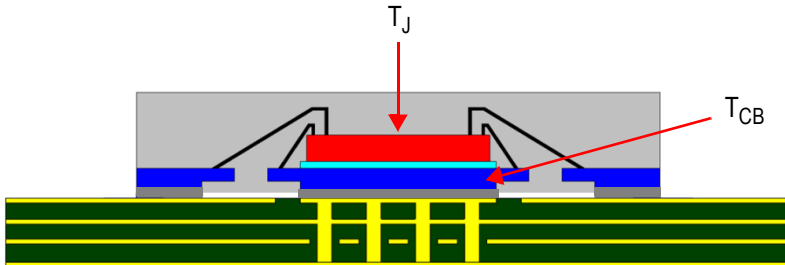
$$T_J = T_{CB} + \Psi_{JB} \times P_D, \text{ where}$$

$T_J$  = Junction temperature at steady state condition in ( $^{\circ}\text{C}$ ).

$T_{CB}$  = Case temperature (Bottom) at steady state condition in ( $^{\circ}\text{C}$ ).

$\Psi_{JB}$  = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

$P_D$  = Power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It is critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature ( $T_{CB}$ ). A good connection ensures that temperature at the exposed pad ( $T_{CB}$ ) and the board temperature ( $T_B$ ) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption, and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

**Example Calculation for Junction Temperature ( $T_J$ ):**  $T_J = T_{CB} + \Psi_{JB} \times P_D$

$P_D = 3.53\text{W}$  ( $P_D$  is calculated from [Table 47](#))

$$T_J = 105^{\circ}\text{C} + 0.7^{\circ}\text{C/W} \times 3.53\text{W} = 107.5^{\circ}\text{C} < 125^{\circ}\text{C}$$

**Table 59. Thermal Resistance for 88-VFQFPN Package**

Package Type	88-VFQFPN
Body size (mm)	10 × 10 mm
ePad size (mm)	8 × 8 mm <sup>2</sup>
Thermal Via	8 × 8 Matrix
$\Psi_{JB}$	0.7 $^{\circ}\text{C/W}$
$T_{CB}$	105 $^{\circ}\text{C}$

## Recommended Application Schematics

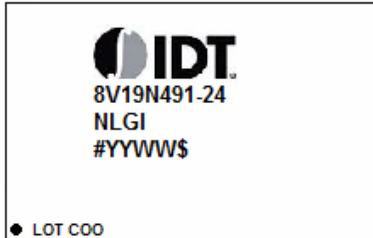
[Figure 16](#) shows an 8V19N492 application schematic example in which the device is operated from a 3.3V power supply. To ensure the logic control inputs are properly set for the application, see [Pin Descriptions](#).



## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

## Marking Diagram



- Line 1 indicates the part number.
- Line 2 indicates the part number suffix.
- Line 3:
  - “#” denotes sequential lot number.
  - “YYWW” is the last digit of the year and week that the part was assembled.
  - “\$” denotes mark code.
- “LOT COO” denotes the lot sequence number and the country of origin.

## Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
8V19N491-24NLGI	10 × 10 mm, <b>88-VFQFPN</b> RoHS 6/6	Tray	-40°C to +105°C (Case)
8V19N491-24NLGI8		Tape and Reel, Pin 1 Orientation: EIA-481-C	
8V19N491-24NLGI/W		Tape and Reel, Pin 1 Orientation: EIA-481-D/E	

**Table 60. Pin 1 Orientation in Tape and Reel Packaging**

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D/E)	

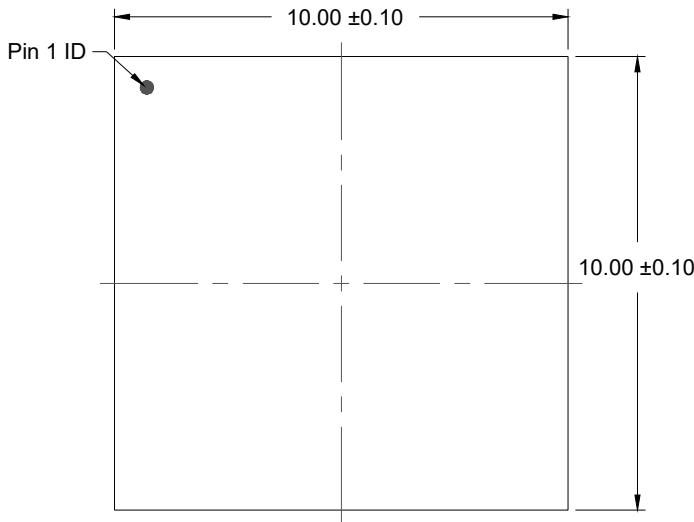
## Glossary

Abbreviation	Description
Index $n$	Denominates a clock input CLK_ $n$ . Range: 0 to 1
Index $x$	Denominates a channel, channel frequency divider and the associated configuration bits. Range: A, B, C, D, E.
Index $y$	Denominates a QCLK output and associated configuration bits. Range: A0, A1, B0, B1, C, D, E0, E1
Index $r$	Denominates a QREF output and associated configuration bits. Range: A0, A1, A2, B0, B1, C, D
ZZ V <sub>DD_V</sub>	Denominates voltage supply pins. Range: VDD_QCLKA, VDD_QCLKB, VDD_QCLKC, VDD_QCLKD, VDD_QCLKE, VDD_QREFA0, VDD_QREFA1, VDD_QREFA2, VDD_QREFB0, VDD_QREFB1, VDD_QREFC, VDD_QREFD, VDD_SPI, VDD_QCLKV, VDD_CPV, VDD_INP, VDD_CPF, VDD_LCF, VDD_LCV1, VDD_LCV2, VDD_SYNC
[...]	Index brackets describe a group associated with a logical function or a bank of outputs.
{...}	List of discrete values
Suffix V	Denominates a function associated with the VCXO-PLL
Suffix F	Denominates a function associated with the 2nd stage PLL (FemtoClock NG)

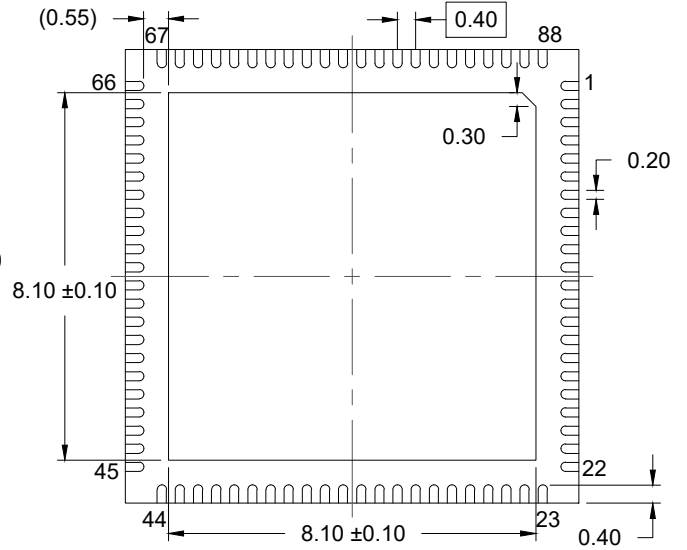
## Revision History

Date	Description of Change
November 20, 2023	Added "LVPECL" in <a href="#">Pin Descriptions</a> for ball numbers 53/52, 55/54, 65/64, 2/3, 4/5, 15/16, and 24/25.
June 11, 2021	<ul style="list-style-type: none"> <li>▪ Updated Package Outline Drawings section; added POD link to Ordering Information.</li> <li>▪ Update pin descriptions for pins 83 and 85.</li> </ul>
November 4, 2020	Updated <a href="#">Output Phase Delay</a>
January 28, 2020	Initial release.

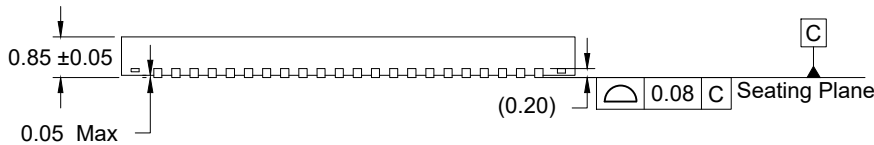




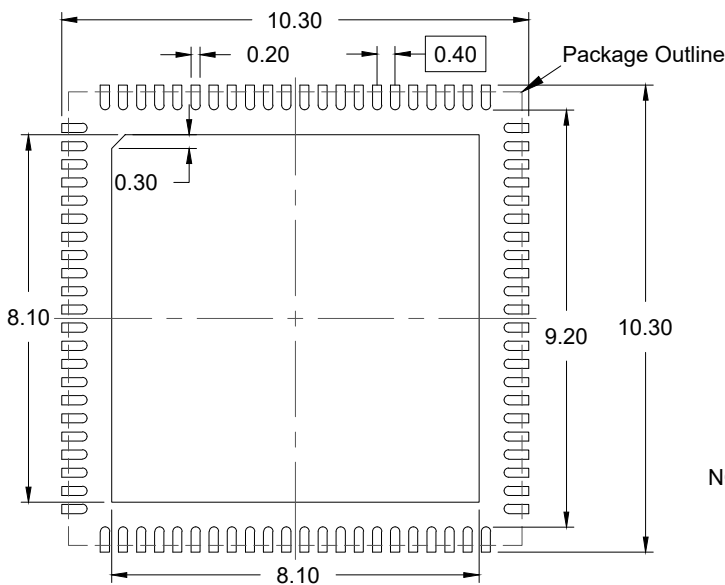
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN  
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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