

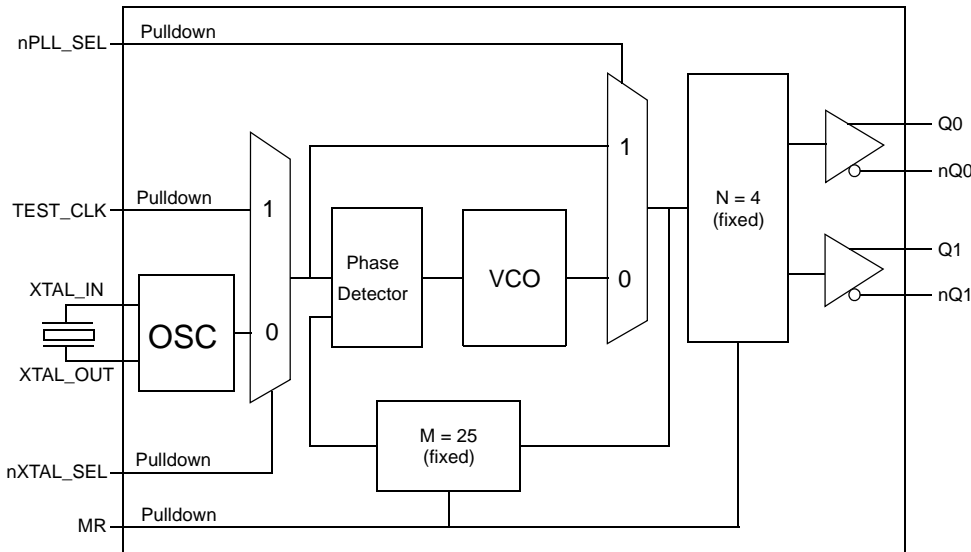
General Description

The 8V43042 is a two output LVPECL synthesizer optimized to generate low jitter reference clock sources. Using a 25MHz or 24MHz, 12pF parallel resonant crystal, it can generate 156.25MHz or 150MHz. The 8V43042 uses 8V43042's 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical RMS phase jitter, easily meeting Ethernet jitter requirements. The 8V43042 is packaged in a small 20-pin TSSOP package.

Features

- Two 3.3V differential LVPECL output pairs
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended clock input
- Supports the following output frequencies: 156.25MHz, 150MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.437ps (typical)
- Full 3.3V supply modes
- 0°C to 70°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment

nc	1	20	V _{CCO}
V _{CCO}	2	19	Q1
Q0	3	18	nQ1
nQ0	4	17	V _{EE}
MR	5	16	V _{CC}
nPLL_SEL	6	15	nXTAL_SEL
nc	7	14	TEST_CLK
V _{CCA}	8	13	XTAL_IN
nc	9	12	XTAL_OUT
V _{CC}	10	11	nc

8V43042

20-Lead 4.4mm x 6.5mm TSSOP

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 7, 9, 11	nc	Unused		No connect
2, 20	V _{CCO}	Power		Output supply pins.
3, 4	Q0, nQ0	Output		Differential output pair. LVPECL interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	nPLL_SEL	Input	Pulldown	Selects either the PLL or the active input reference to be routed to the output dividers. When LOW, selects PLL (PLL Enable). When HIGH, selects the reference clock (PLL Bypass). LVCMOS/LVTTL interface levels.
8	V _{CCA}	Power		Analog supply pin.
10, 16	V _{CC}	Power		Core supply pins.
12, 13	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
17	V _{EE}	Power		Negative supply pins.
14	TEST_CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
15	nXTAL_SEL	Input	Pulldown	Selects between the single-ended TEST_CLK or crystal interface as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL inputs. LVCMOS/LVTTL interface levels.
18, 19	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance	nPLL_SEL, nXTAL_SEL, MR		4		pF
		TEST_CLK		2		pF
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V
Inputs, V_I XTAL_IN Other Inputs	0V to V_{CC} -0.5V to $V_{CC} + 0.5V$
Outputs, I_O (LVPECL) Continuous Current Surge Current	50mA 100mA
Package Thermal Impedance, θ_{JA}	86.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		$V_{CC} - 0.15$	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				135	mA
I_{CCA}	Analog Supply Current	Included in I_{EE}			15	mA

Table 3B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	$V_{CC} = 3.3V \pm 5\%$	2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	$V_{CC} = 3.3V \pm 5\%$	-0.3		0.8	V
I_{IH}	Input High Current	TEST_CLK, MR, nPLL_SEL, nXTAL_SEL $V_{CC} = V_{IN} = 3.465V$			150	μA
I_{IL}	Input Low Current	TEST_CLK, MR, nPLL_SEL, nXTAL_SEL $V_{CC} = 3.465V, V_{IN} = 0V$	-5			μA

Table 3C. LVPECL DC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs termination with 50Ω to $V_{CCO} - 2V$.

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		24		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Load Capacitance (C_L)			12	18	pF

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ to $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range		150		156.25	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2				40	ps
$f_{jit}(\emptyset)$	RMS Phase Jitter, (Random); NOTE 3	156.25MHz, (1.875MHz – 20MHz)		0.437		ps
		150MHz, (1.875MHz – 20MHz)		0.436		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		650	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions

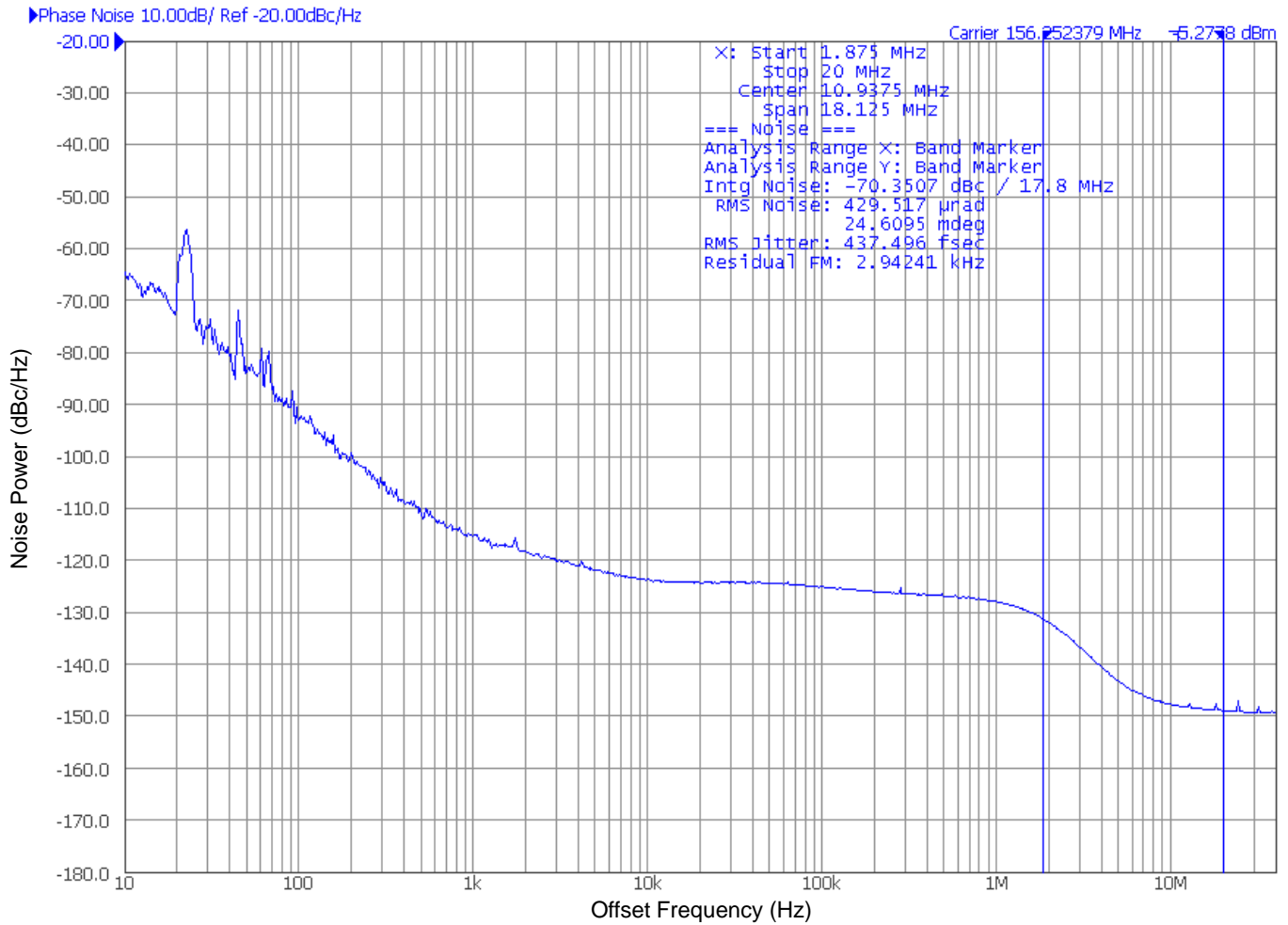
NOTE: Characterized using an 18pF parallel resonant crystal.

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoint.

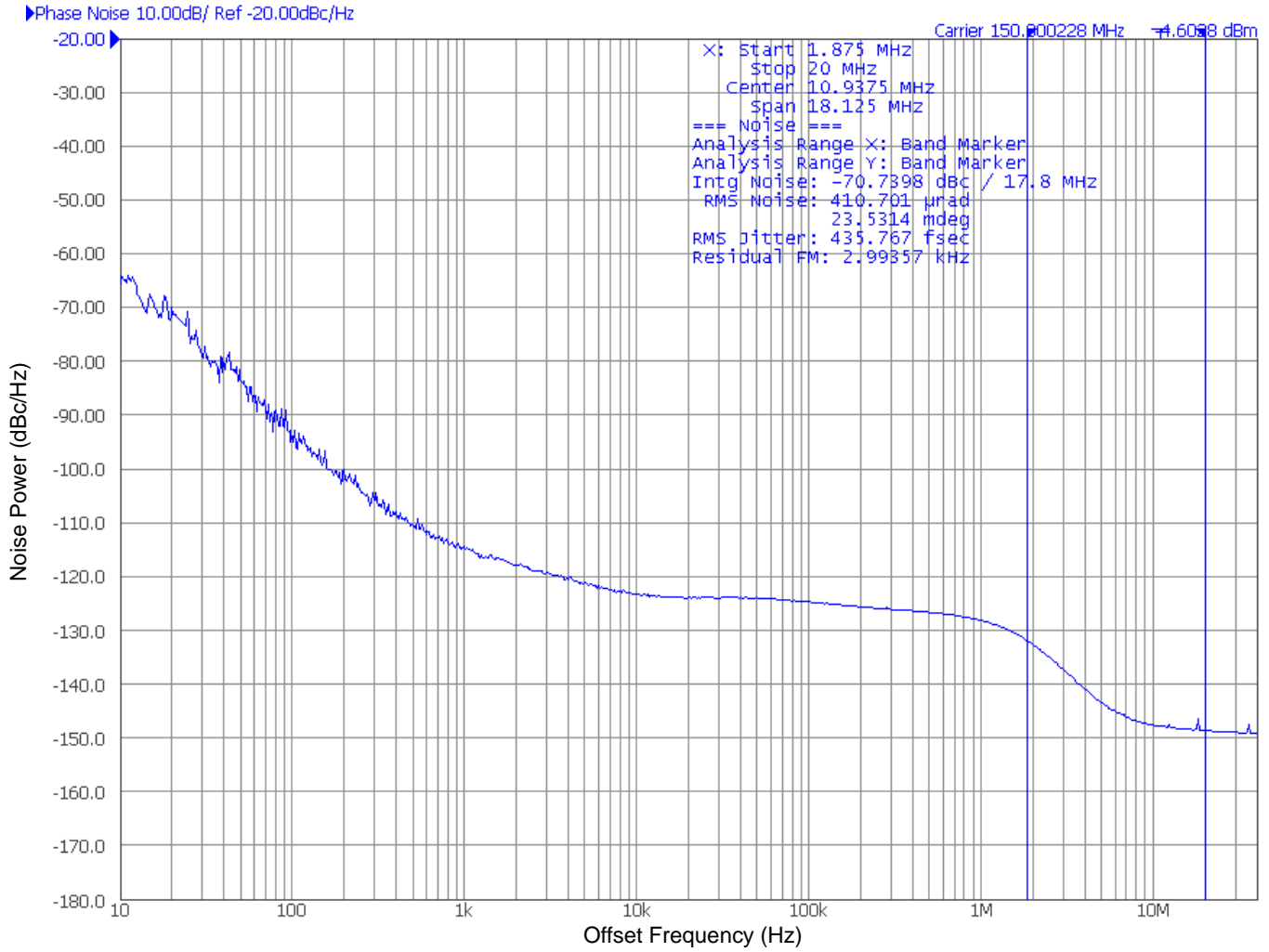
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plots.

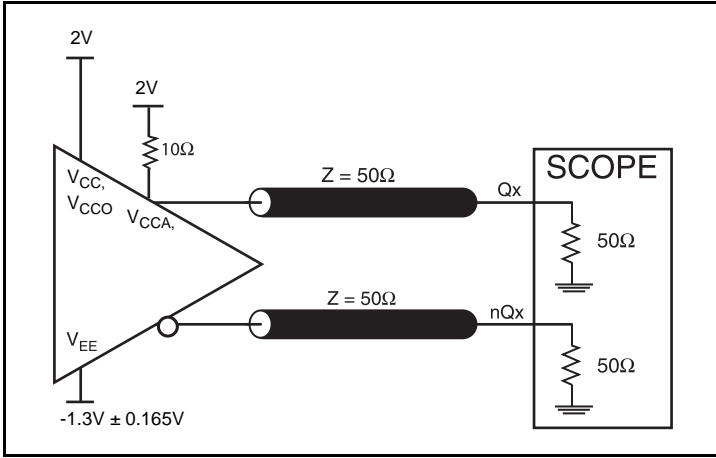
Typical Phase Noise at 156.25MHz



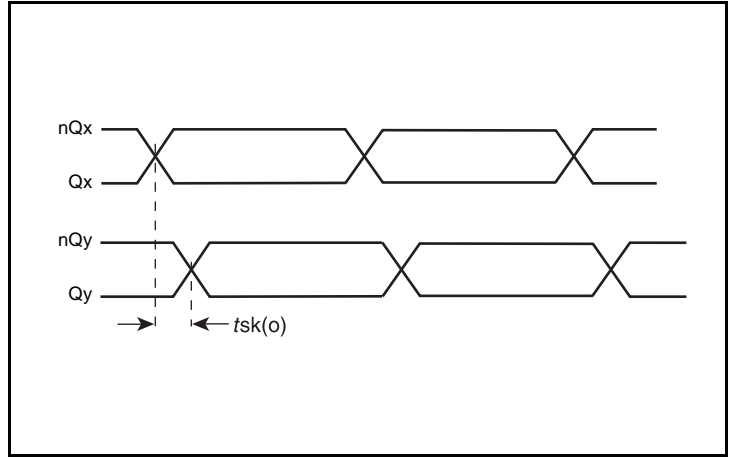
Typical Phase Noise at 150MHz



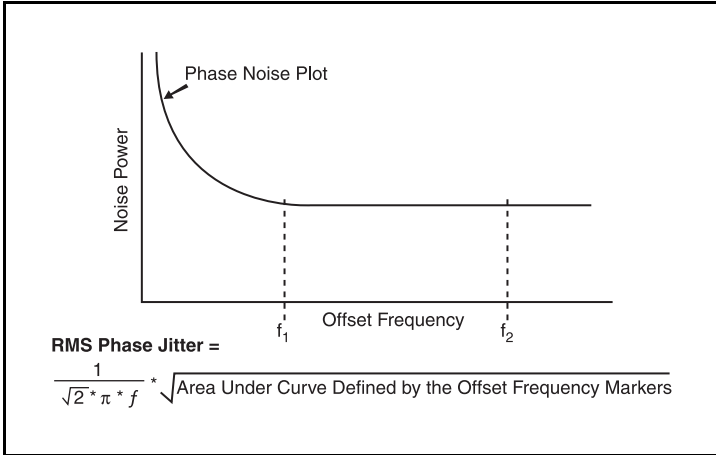
Parameter Measurement Information



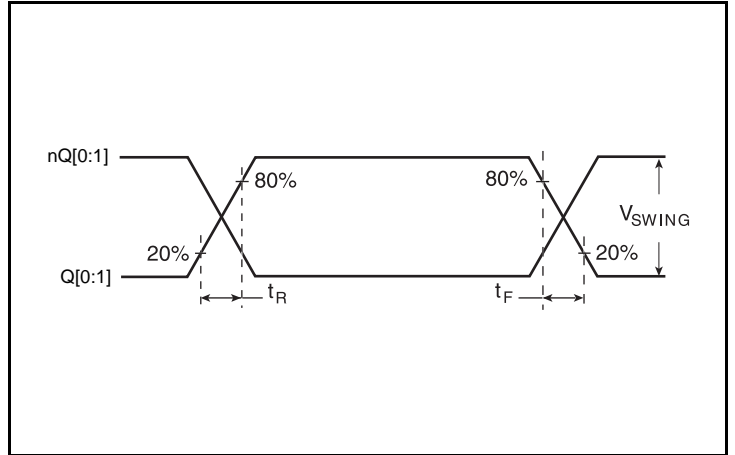
3.3V LVPECL Output Load Test Circuit



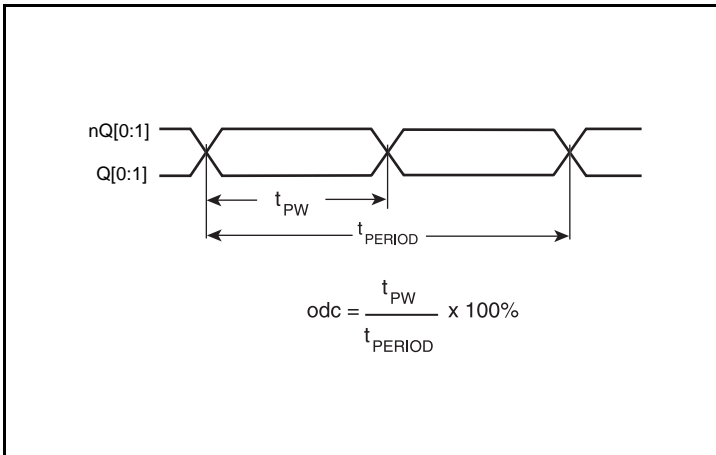
Output Skew



RMS Phase Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

TEST_CLK Input

For applications not requiring the use of the clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the TEST_CLK to ground.

LVC MOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 1A and 1B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

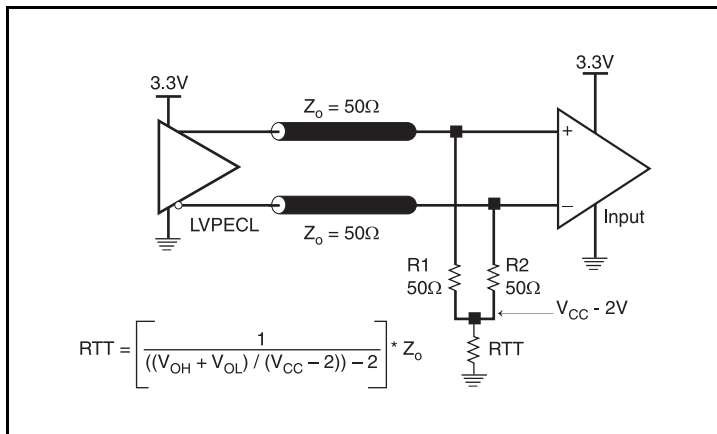


Figure 1A. 3.3V LVPECL Output Termination

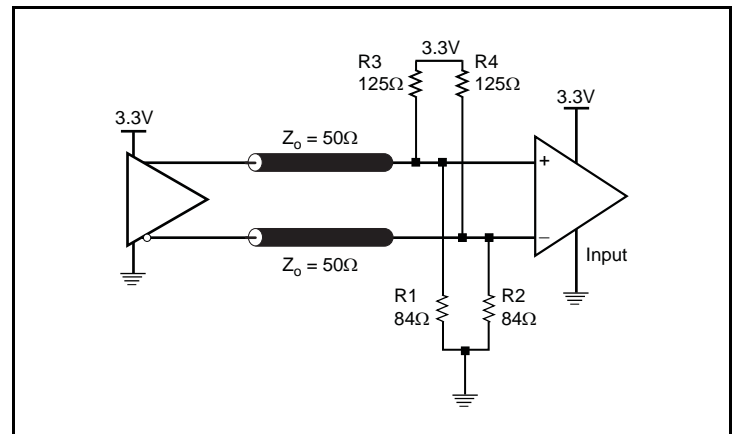


Figure 1B. 3.3V LVPECL Output Termination

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and changing R_2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

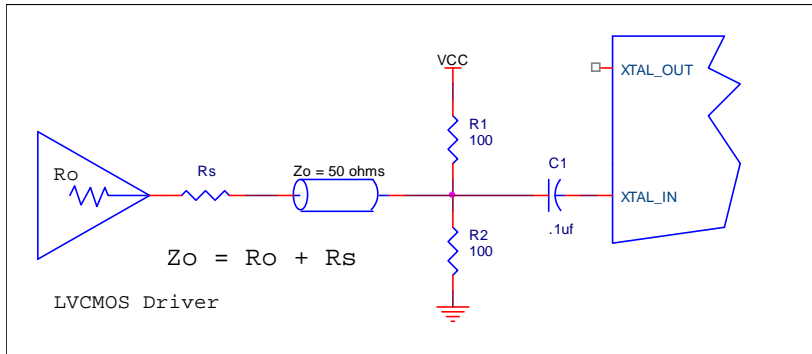


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

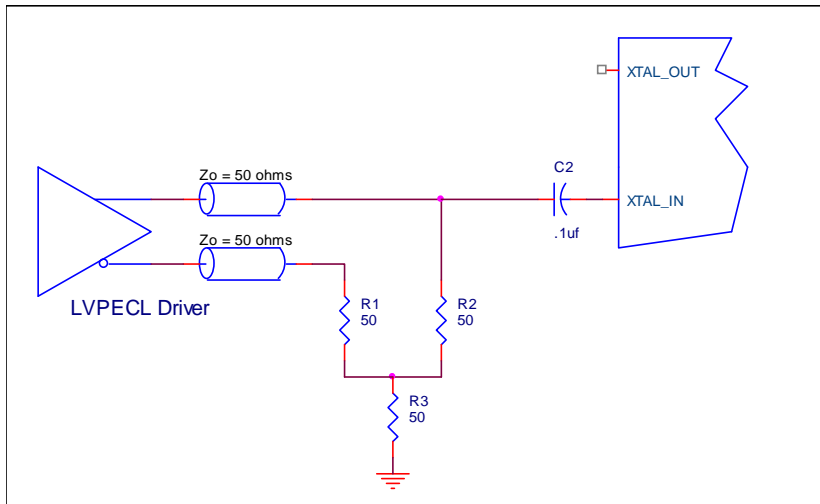


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

Schematic Example

Figure 3 shows an example of 8V43042 application schematic. In this example, the device is operated at $V_{CC} = V_{CCA} = V_{CCO} = 3.3V$. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

A 12pF parallel resonant 25MHz crystal is used. For this device, the crystal load capacitors are required for proper operation. The load capacitance, $C1 = C2 = 10pF$, are recommended for frequency accuracy. Depending on the variation of the parasitic stray capacity of the printed circuit board traces between the crystal and the `XXTAL_IN` and `XXTAL_OUT` pins, the values of C1 and C2 might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used, but this will require adjusting C1 and C2. When designing the circuit board, return the capacitors to ground through a single point contact close to the package. Two Fox crystal options are shown in the schematic for design flexibility.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8V43042 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1 μ F capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

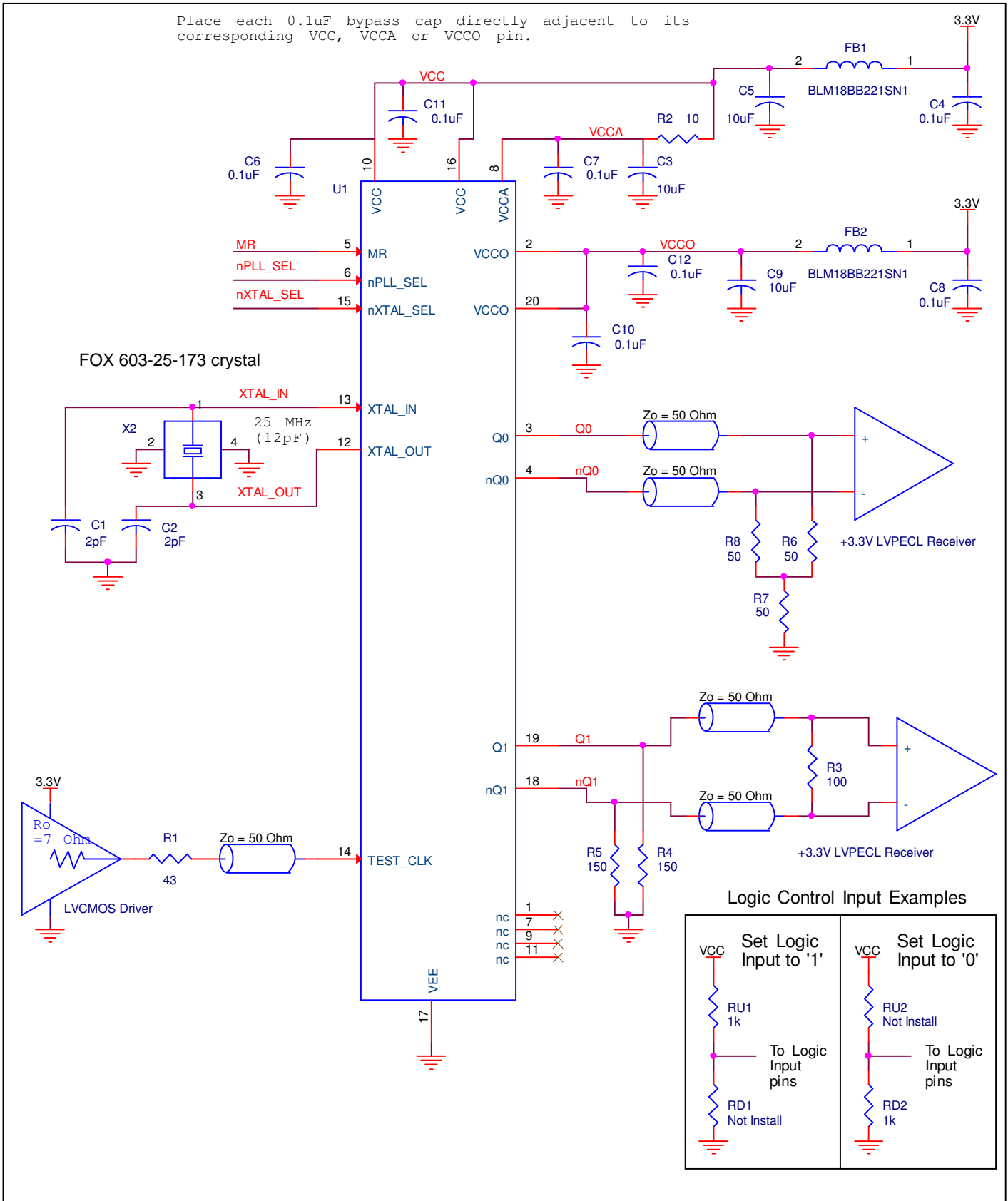


Figure 3. 8V43042 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 8V43042. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8V43042 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 135mA = \mathbf{467.775mW}$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 30mW = \mathbf{60mW}$

Total Power_{MAX} (3.465V, with all outputs switching) = $467.775mW + 60mW = \mathbf{527.775mW}$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_{total} + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 86.7°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.528\text{W} * 86.7^\circ\text{C/W} = 115.8^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 4*.

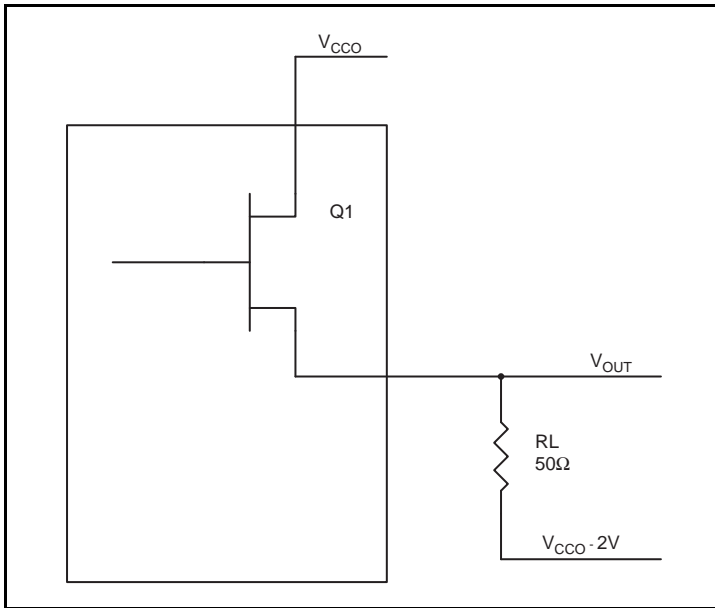


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - **0.9V**
(V_{CCO_MAX} - V_{OH_MAX}) = **0.9V**
- For logic low, V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - **1.7V**
(V_{CCO_MAX} - V_{OL_MAX}) = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX})$$

$$= [(2V - 0.9V)/50\Omega] * 0.9V = \mathbf{19.8mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX})$$

$$= [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

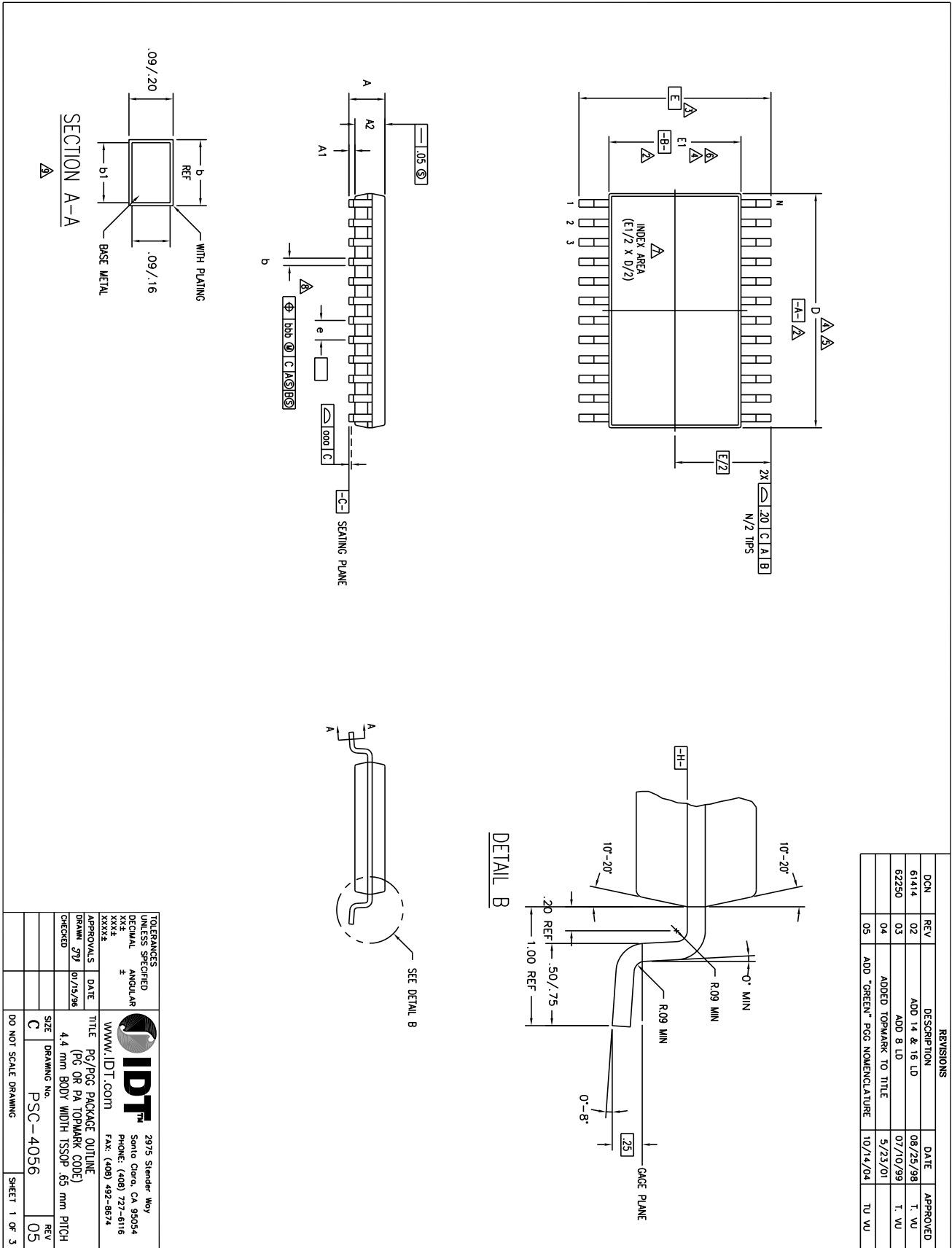
Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	86.7°C/W	82.4°C/W	80.2°C/W

Transistor Count

The transistor count for 8V43042 is: 2,967

20 Lead TSSOP Package Outline and Package Dimensions



20 Lead TSSOP Package Outline and Package Dimensions

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
61414	02	ADD 14 & 16 LD	08/25/98	T. VU
62250	03	ADD 8 LD	07/10/99	T. VU
	04	ADDED TOPMARK TO TITLE	5/23/01	
	05	ADD "GREEN" Pkg NOMENCLATURE	10/14/04	TU VU

SYMBOL	JEDEC VARIATION			N	D	T	E	JEDEC VARIATION			N	D	T	E	JEDEC VARIATION			N	D	T	E	JEDEC VARIATION			N	D	T	E			
	AA	NOM	MAX					AB-1	MIN	NOM					MAX	AB	MIN					NOM	MAX	AC					MIN	NOM	MAX
A	-	-	1.20					-	-	1.20			-	-	1.20			-	-	1.20			-	-	1.20			-	-	1.20	
A1	.05	-	.15					.05	-	.15			.05	-	.15			.05	-	.15			.05	-	.15			.05	-	.15	
A2	.80	1.00	1.05					.80	1.00	1.05			.80	1.00	1.05			.80	1.00	1.05			.80	1.00	1.05			.80	1.00	1.05	
D	2.90	3.00	3.10	4.5				4.90	5.00	5.10	4.5		4.90	5.00	5.10	4.5		4.90	5.00	5.10	4.5		4.90	5.00	5.10	4.5		4.90	5.00	5.10	
E	6.40 BSC			3				6.40 BSC			3		6.40 BSC			3		6.40 BSC			3		6.40 BSC			3		6.40 BSC			3
E1	4.30	4.40	4.50	4.6				4.30	4.40	4.50	4.6		4.30	4.40	4.50	4.6		4.30	4.40	4.50	4.6		4.30	4.40	4.50	4.6		4.30	4.40	4.50	4.6
e	.65 BSC							.65 BSC					.65 BSC					.65 BSC					.65 BSC					.65 BSC			
b	.19	-	.30					.19	-	.30			.19	-	.30			.19	-	.30			.19	-	.30			.19	-	.30	
b1	.19	.22	.25					.19	.22	.25			.19	.22	.25			.19	.22	.25			.19	.22	.25			.19	.22	.25	
000	-	-	.10					-	-	.10			-	-	.10			-	-	.10			-	-	.10			-	-	.10	
bbb	-	-	.10					-	-	.10			-	-	.10			-	-	.10			-	-	.10			-	-	.10	
N			8							14					16					20					24					28	

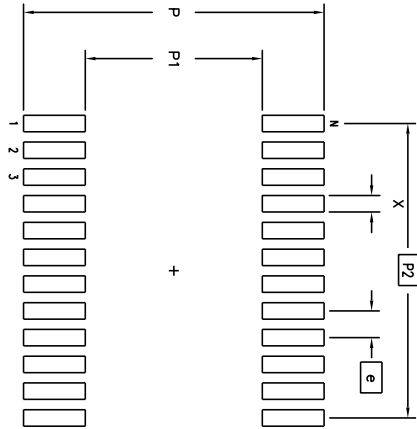
NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
- 2 DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- 3 DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- 4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- 5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS; MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- 6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS; INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- 7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- 8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION; ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION; DAMBAR CANNOT BE LOCATED ON THE LOWER RADII OR THE FOOT
- 9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- 10 ALL DIMENSIONS ARE IN MILLIMETERS
- 11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-153, VARIATION AA, AB-1, AB, AC, AD & AE

TOLERANCES UNLESS SPECIFIED		2975 Slender Way	
ANGULAR	4	San Jose, CA 95054	
XXX		PHONE: (408) 727-6116	
XXXX		FAX: (408) 492-8674	
WWW.IDT.COM		IDT	
APPROVALS	DATE	TITLE	
DRW: J77	01/15/98	PG/PKG PACKAGE OUTLINE (PG OR PA TOPMARK CODE)	
CHECKED		4.4 mm BODY WIDTH TSSOP 65 mm PITCH	
SIZE	DRAWING No.	PSC-4056	
		REV 05	
DO NOT SCALE DRAWING		SHEET 2 OF 3	

20 Lead TSSOP Package Outline and Package Dimensions

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40	7.20	7.40
P1	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40	4.20	4.40
P2	1.95 BSC		3.90 BSC		4.55 BSC		5.85 BSC		7.15 BSC		8.45 BSC	
X	.30	.50	.30	.50	.30	.50	.30	.50	.30	.50	.30	.50
e	.65 BSC		.65 BSC		.65 BSC		.65 BSC		.65 BSC		.65 BSC	
N	8		14		16		20		24		28	

REVISIONS				
DCM	REV	DESCRIPTION	DATE	APPROVED
61414	02	ADD 14 & 16 LD	08/25/98	T. VU
62250	03	ADD 8 LD	07/10/99	T. VU
	04	ADDED TOPMARK TO TITLE	5/23/01	
	05	ADD "GREEN" PGC NOMENCLATURE	10/14/04	TU VU

TOLERANCES UNLESS SPECIFIED:
 ANGULAR 4°
 XXXX
 XXXX
 XXXX

APPROVALS: DATE: 07/15/98
 DRAWN: J77
 CHECKED:

SIZE: C
 DRAWING No. PSC-4056
 REV: 05

DO NOT SCALE DRAWING SHEET 3 OF 3

IDT 2975 Slender Way
 Santa Clara, CA 95054
 PHONE: (408) 727-6116
 FAX: (408) 492-8674
 WWW.IDT.COM

TITLE: PG/PGC PACKAGE OUTLINE
 (PG OR PA TOPMARK CODE)
 4.4 mm BODY WIDTH TSSOP .65 mm PITCH

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8V43042PGG	IDT8V43042PGG	20 Lead TSSOP, Lead-Free	Tube	0°C to 70°C
8V43042PGG8	IDT8V43042PGG	20 Lead TSSOP, Lead-Free	Tape & Reel	0°C to 70°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B		12	Updated schematic with IDT crystal recommendation. Deleted prefix/suffix from part number throughout the datasheet. Updated header/footer.	7/24/15
C		12	Schematic - replaced IDT crystal recommendation with FOX.	11/3/16

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