Low EMI, Spread Modulating, Clock Generator

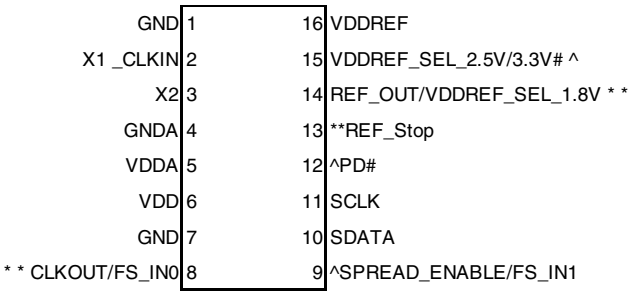
Features:

- ICS91719 is a Spread Spectrum Clock targeted for Mobile PC and LCD panel applications. Generates an EMI optimized clock signal (EMI peak reduction of 7-14 dB on 3rd-19th harmonics) through use of Spread Spectrum techniques.
- ICS91719 focuses on the lower input frequency range of 14.318 to 80.00 MHz with a spread modulation of 20kHz to 40kHz.

Specifications:

- Supply Voltages: VDD = 3.3V ±0.3V
- Frequency range: 14.318 MHz ≤Fin ≥ 80 MHz
- Cyc to Cyc jitter: <150ps
- Output duty cycle 40/60% (worst case)
- Guarantees +85°C operational condition.
- 16-pin TSSOP package 4.4mm body (173mils), 0.65 mm pitch
- 14.318 MHz crystal input or reference clock input
- 27MHz, 48MHz and 66MHz reference clock input

Pin Configuration



16-pin TSSOP

** Internal pull-down
^ Internal pull-up

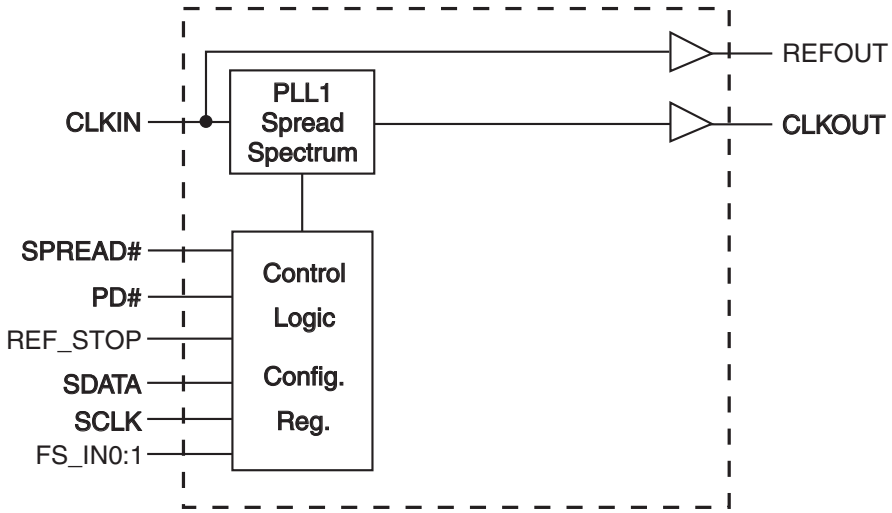
REF Voltage Select Functionality

Pin14	Pin15	REF Voltage
0	0	N/A
0	1	1.8V
1	0	2.5V
1	1	3.3V

Input Select Functionality

FS_IN1	FS_IN0	MHZ	Default Spread %
0	0	14.318 in 27.00 out	-0.8% downspread
0	1	14.318 in/out	-0.8% downspread
1	0	27.00 in/out	-0.8% downspread
1	1	48.00 in/out 66.66 in/out	-0.8% downspread

Block Diagram



Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	GND	POWER	Ground pin for 3V outputs
2	X1 _CLKIN	INPUT	Crystal input or CLOCKIN input
3	X2	OUTPUT	Crystal output
4	GNDA	POWER	Analog ground
5	VDDA	POWER	Analog power supply for 3V
6	VDD	POWER	Power supply for 3V
7	GND	POWER	Ground pin for 3V outputs
8	CLKOUT	OUTPUT	Modulated clock output
	FS_IN0	INPUT	Latched input for input frequency select
9	^SPREAD_ENABLE	INPUT	Spread enable pin
	FS_IN1		Latched input for input frequency select
10	SDATA	INPUT	Data pin for I2C circuitry 5V tolerant
11	SCLK	INPUT	Clock pin for I2C circuitry 5V tolerant
12	^PD#	INPUT	Power down
13	**REF_Stop	INPUT	Stop control for REF_CLOCK output STOP:1, RUNNING:0
14	REF_OUT/VDDREF_SEL_1.8V * *	INPUT/OUTPUT	REF_CLOCK output
15	VDDREF_SEL_2.5V/3.3V# ^	POWER	REF_CLOCK power supply voltage select
16	VDDREF	POWER	Power supply for REF_CLOCK

^internal pull-up
**internal pull-down

Table 1: Frequency Configuration Table (See I2C Byte 0)

	FS4	FS3	FS2	FS1	FS0	Sprd Type	Sprd %
14in/27out	0	0	0	0	0	DOWN SPREAD (-)	0.60
	0	0	0	0	1		0.80
	0	0	0	1	0		1.00
	0	0	0	1	1		1.25
	0	0	1	0	0		1.50
	0	0	1	0	1		2.00
	0	0	1	1	0	Center Spread (+/-)	0.50
	0	0	1	1	1		1.00
14in/14out 27in/27out	0	1	0	0	0	DOWN SPREAD (-)	0.60
	0	1	0	0	1		0.80
	0	1	0	1	0		1.00
	0	1	0	1	1		1.25
	0	1	1	0	0		1.50
	0	1	1	0	1		1.75
	0	1	1	1	0		2.00
	0	1	1	1	1		2.50
	1	0	0	0	0		3.00
	1	0	0	0	1	CENTER SPREAD (+/-)	0.30
	1	0	0	1	0		0.40
	1	0	0	1	1		0.50
	1	0	1	0	0		0.70
	1	0	1	0	1		1.00
	1	0	1	1	0		1.20
	1	0	1	1	1		1.50
48in/48out 66in/66out	1	1	0	0	0	DOWN SPREAD (-)	0.60
	1	1	0	0	1		0.80
	1	1	0	1	0		1.00
	1	1	0	1	1		1.25
	1	1	1	0	0		1.50
	1	1	1	0	1		2.00
	1	1	1	1	0	Center Spread (+/-)	0.50
	1	1	1	1	1		1.00

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D2_{(H)}$	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Byte 7	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 7***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address $D3_{(H)}$	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
	Byte 7
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

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Byte 0:

BYTE	Affected Pin				Bit Control		
0	**Pin #**	**Name**	**Control Function**	**TYPE**	**0**	**1**	**PWD**
Bit 7	-	FS0	Spread/FS0	RW			1
Bit 6	-	FS1	Spread/FS1	RW			0
Bit 5		FS2	Spread/FS2	RW			0
Bit 4		FS3	Spread/FS3	R			0
Bit 3		FS4	FS4	R/RW			0
Bit 2		PD# Tri_Sate	PD# Tri_Sate	RW	Hi-Z	LOW	1
Bit 1		Spread Enable	Spread Enable	RW	OFF	ON	1
Bit 0		HW/SW Control	Spread Spectrum Control FS 3:4 Hard/Software Select	RW	HW	SW	0

Byte 1:

BYTE	Affected Pin				Bit Control		
1	**Pin #**	**Name**	**Control Function**	**TYPE**	**0**	**1**	**PWD**
Bit 7		Reserved	Reserved	R	-	-	1
Bit 6	-	SLEW	Slew Rate REF-OUT	RW	Nominal	Fast	1
Bit 5		FS-IN_1 Readback	FS-IN_1 Readback	RW	Not Freerun	Freerun	1
Bit 4		FS-IN_0 Readback	FS-IN_0 Readback	RW	Nominal	Fast	1
Bit 3		SLEW	Slew Rate CLK-OUT	RW	Nominal	Fast	1
Bit 2		CLK_OUT_Enable	CLK_OUT_Enable	RW	Disable	Enable	1
Bit 1		REF_OUT_Enable	REF_OUT_Enable	RW	Disable	Enable	1
Bit 0		Reserved	Reserved	R	-	-	1

Byte 2:

BYTE	Affected Pin				Bit Control		
2	**Pin #**	**Name**	**Control Function**	**TYPE**	**0**	**1**	**PWD**
Bit 7	x	-	RESERVED	-	-	-	1
Bit 6	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 5	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 4	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 3	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 2	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 1	x	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 0	x	RESERVED	RESERVED	RW	Disable	Enable	1

Byte 3:

BYTE	Affected Pin				Bit Control		
3	**Pin #**	**Name**	**Control Function**	**TYPE**	**0**	**1**	**PWD**
Bit 7	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 6	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 5	X	RESERVED	RESERVED	RW	Freerun	Not Freerun	1
Bit 4	X	RESERVED	RESERVED	RW	Freerun	Not Freerun	1
Bit 3	x	RESERVED	RESERVED	RW	Freerun	Not Freerun	1
Bit 2	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 1	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 0	X	RESERVED	RESERVED	RW	Disable	Enable	1

Byte 4:

BYTE	Affected Pin				Bit Control		
4	**Pin #**	**Name**	**Control Function**	**TYPE**	**0**	**1**	**PWD**
Bit 7	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 6	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 5	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 4	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 3	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 2	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 1	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 0	X	RESERVED	RESERVED	RW	Disable	Enable	1

Byte 5:

BYTE	Affected Pin				Bit Control		
5	**Pin #**	**Name**	**Control Function**	**TYPE**	**0**	**1**	**PWD**
Bit 7	X	RESERVED	RESERVED	-	-	-	1
Bit 6	X	RESERVED	RESERVED	-	-	-	1
Bit 5	X	RESERVED	RESERVED	-	-	-	1
Bit 4	X	RESERVED	RESERVED	-	-	-	1
Bit 3	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 2	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 1	X	RESERVED	RESERVED	RW	Disable	Enable	1
Bit 0	X	RESERVED	RESERVED	RW	Disable	Enable	1

Byte 6:

BYTE	Affected Pin			TYPE	Bit Control		
6	**Pin #**	**Name**	**Control Function**		**0**	**1**	**PWD**
Bit 7	X	Revision ID Bit 3	(Reserved)	R	-	-	1
Bit 6	X	Revision ID Bit 2	(Reserved)	R	-	-	1
Bit 5	X	Revision ID Bit 1	(Reserved)	R	-	-	1
Bit 4	X	Revision ID Bit 0	(Reserved)	R	-	-	1
Bit 3	X	Vendor ID Bit 3	(Reserved)	R	-	-	1
Bit 2	X	Vendor ID Bit 2	(Reserved)	R	-	-	1
Bit 1	X	Vendor ID Bit 1	(Reserved)	R	-	-	1
Bit 0	X	Vendor ID Bit 0	(Reserved)	R	-	-	1

Absolute Maximum Ratings

Supply Voltage . . . . . 3.3 V
Voltage on any pin with respect to GND . . . -0.5 to +7.0 V
Storage Temperature . . . . . –55°C to +125°C
Operating Temperature . . . . . 0°C to +85°C
Ambient Operating Temperature under Bias . -55 to +125 °C
Power Dissipation . . . . . 0.5 W

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 85°C; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Powerdown Current	$I_{DD3.3PD}$			3	5	mA
Input Frequency	Fi	V_{DD} = 3.3 V		14.318		MHz
Input Crystal Frequency	$F_{CY}I$			14.318	Typ + 10%	MHz
Input Clock Frequency	$F_{CLK}I$				80	MHz
Pin Inductance	Lpin				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Transition time[1]	Ttrans	To 1st crossing of target frequency			3	ms
Settling time[1]	Ts	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency		1	3	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 85°C; VDD = 3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL3}	I_{OL} = 1 mA			0.4	
Rise Time	tr3	V_{OL} = 0.41V, V_{OH} = 0.86V	0.5	0.7	1	ns
Fall Time	tf3	V_{OH} = 0.86V V_{OL} = 0.41V	0.5	0.8	1	ns
Duty Cycle	d_{t3}	measurement from differential waveform -0.35V to +035V	45	51	55	%
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = 50%		76	150	ps

[1]Guaranteed by design, not 100% tested in production.

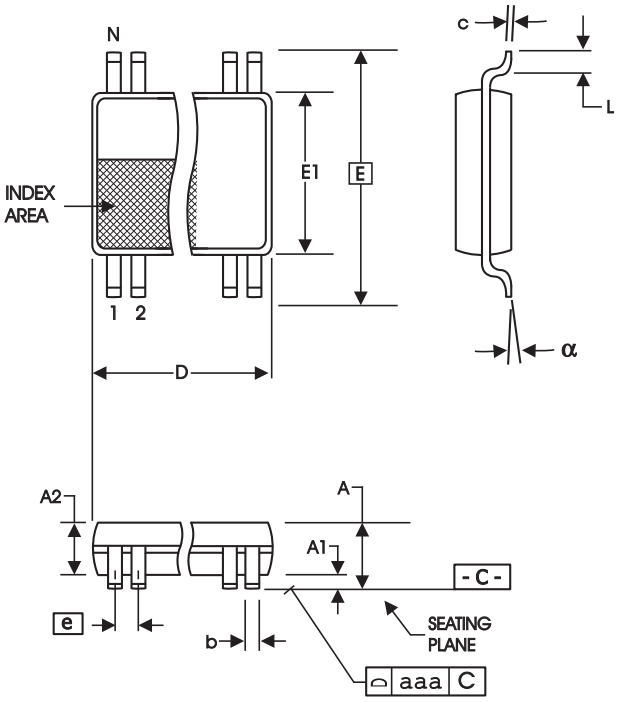
[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - REF

T_A = 0 - 85°C; VDD = 3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}$*(0.5)	20	48	60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.25	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.3	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	53	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		170	300	ps

[1]Guaranteed by design, not 100% tested in production.



4.40mm Body, .65mm pitch

4.40 mm. Body, 0.65 mm. Pitch TSSOP
(173 mil) (25.6 mil)

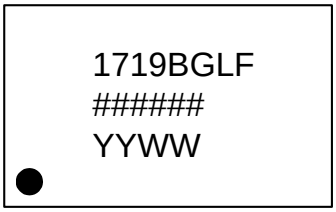
SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
16	4.90	5.10	.193	.201

Reference Doc.: JEDEC Publication 95, MO-153
10-0035

Marking Diagram

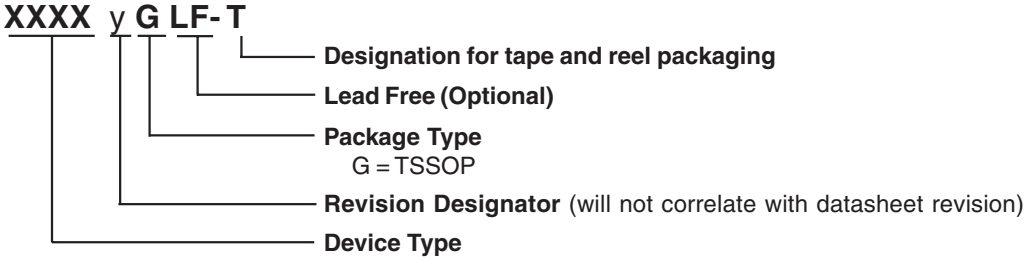


Line 1. Part number.
Line 2. ####### = lot number
Line 3. YYWW = date code

Ordering Information

91719yGLF-T

Example:



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