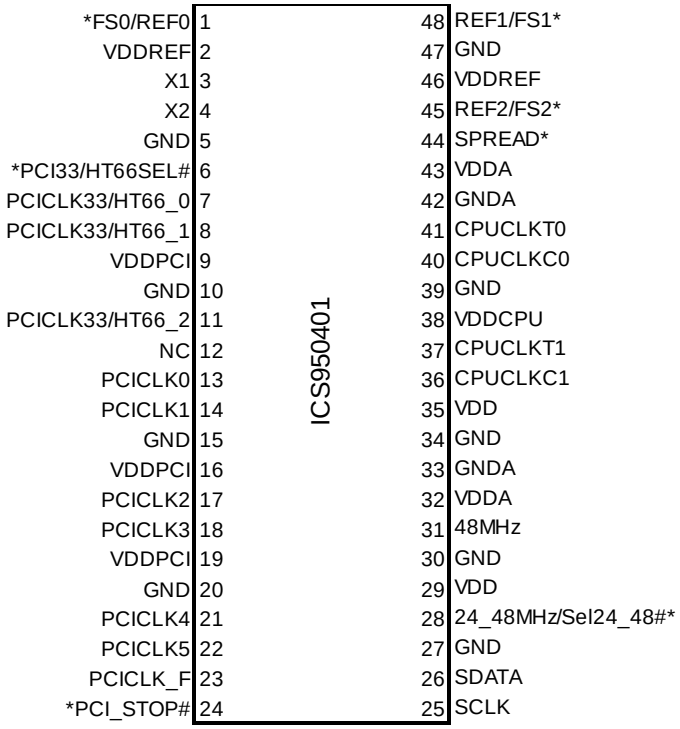
AMD - K8™ System Clock Chip

Recommended Application:
AMD K8 Systems

Output Features:
- 2 - Differential pair push-pull CPU clocks @ 3.3V
- 7 - PCI (Including 1 free running) @3.3V
- 3 - Selectable HT/PCI 66/33MHz @3.3V
- 1 - 48MHz, @3.3V fixed.
- 1 - 24/48MHz @ 3.3V
- 3 - REF @3.3V, 14.318MHz.

Features:
- Up to 220MHz frequency support
- Support power management: PCI stop and stop clocks controlled by I^2C.
- Spread spectrum for EMI reduction
- Uses external 14.318MHz crystal
- I^2C programmability features
- Supports Hypes transport technology (HT66 output).

Pin Configuration

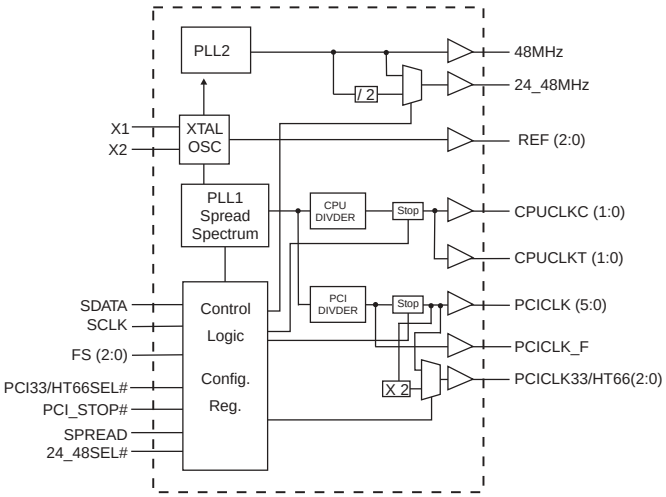


48-SSOP/ TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

Block Diagram



Functionality

FS2	FS1	FS0	PCI33_HT66 SEL#	CPU	PCI33	PCI33_HT66	COMMENTS
0	0	0	X	Hi-Z	Hi-Z	Hi-Z	Tri-State Mode
0	0	1	0	X	X/6	X/3	Bypass Mode
0	0	1	1	X	X/6	X/6	Bypass Mode
0	1	0	X	180.00	30.00	60.00	10% under-clk
0	1	1	X	220.00	36.56	73.12	10% over-clk
1	0	0	X	100.00	33.33	33.33/66.66	Athlon Compatible
1	0	1	X	133.33	33.33	33.33/66.66	Athlon Compatible
1	1	0	X	166.66	33.33	33.33/66.66	Reserved
1	1	1	X	200.00	33.33	33.33/66.66	Hammer Operation

Pin Descriptions

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	*FS0/REF0	I/O	Frequency select latch input pin / 14.318 MHz reference clock.
2	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
3	X1	IN	Crystal input, Nominally 14.318MHz.
4	X2	OUT	Crystal output, Nominally 14.318MHz
5	GND	PWR	Ground pin.
6	*PCI33/HT66SEL#	IN	Input for PCI33/HT66 select. 0= 66.66MHz, 1= 33.33MHz,
7	PCICLK33/HT66_0	IN	PCI clocks at 33.33MHz or HT clocks at 66.66MHz, selected by pin 6 select input.
8	PCICLK33/HT66_1	IN	PCI clocks at 33.33MHz or HT clocks at 66.66MHz, selected by pin 6 select input.
9	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
10	GND	PWR	Ground pin.
11	PCICLK33/HT66_2	IN	PCI clocks at 33.33MHz or HT clocks at 66.66MHz, selected by pin 6 select input.
12	NC	NC	No Connect
13	PCICLK0	OUT	PCI clock output.
14	PCICLK1	OUT	PCI clock output.
15	GND	PWR	Ground pin.
16	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
17	PCICLK2	OUT	PCI clock output.
18	PCICLK3	OUT	PCI clock output.
19	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
20	GND	PWR	Ground pin.
21	PCICLK4	OUT	PCI clock output.
22	PCICLK5	OUT	PCI clock output.
23	PCICLK_F	I/O	Free running PCI clock not affected by PCI_STOP# / Mode selection latch input pin.
24	*PCI_STOP#	I/O	Input select pin, Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low.
25	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.
26	SDATA	I/O	Data pin for SMBus circuitry, 5V tolerant.
27	GND	PWR	Ground pin.
28	24_48MHz/Sel24_48#*	I/O	24/48MHz clock output / Latched select input for 24/48MHz output. 0=48MHz, 1 = 24MHz.
29	VDD	PWR	Power supply, nominal 3.3V
30	GND	PWR	Ground pin.
31	48MHz	OUT	48MHz clock output.
32	VDDA	PWR	3.3V power for the PLL core.
33	GNDA	PWR	Ground pin for the PLL core.
34	GND	PWR	Ground pin.
35	VDD	PWR	Power supply, nominal 3.3V
36	CPUCLKC1	OUT	Complementory clock of differential CPU outputs. Push-pull requires external termination.
37	CPUCLKT1	OUT	True clock of differential CPU outputs. Push-pull requires external termination.
38	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
39	GND	PWR	Ground pin.
40	CPUCLKC0	OUT	Complementory clock of differential CPU outputs. Push-pull requires external termination.
41	CPUCLKT0	OUT	True clock of differential CPU outputs. Push-pull requires external termination.
42	GNDA	PWR	Ground pin for the PLL core.
43	VDDA	PWR	3.3V power for the PLL core.
44	SPREAD*	IN	Asynchronous, active high input, with internal 120Kohm pull-up resistor, to enable spread spectrum functionality.
45	REF2/FS2*	I/O	14.318 MHz reference clock / Frequency select latch input pin.
46	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
47	GND	PWR	Ground pin.
48	REF1/FS1*	I/O	14.318 MHz reference clock / Frequency select latch input pin.

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor ~ This Output has 2X Drive Strength

General Description

The **ICS950401** is a main clock synthesizer chip for AMD-K8. This provides all clocks required for Clawhammer and Sledgehammer systems.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS950401 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I^2C interface allows changing functions, stop clock programming and frequency selection.

Power Groups

VDDA = PLL2 Pin 32
VDDA = VDD for Core PLL Pin 43
VDDREF = REF, Xtal Pin 2

Skew Characteristics

Parameter	Description	Test Conditons	Skew Window	Unit
$T_{sk\_CPU\_CPU}$	time independent skew not dependent on V, T changes	measured at x-ing of CPU,	250	ps
$T_{sk\_CPU\_PCI}$		measured at x-ing of CPU, 1.5V of PCI clock	2000	ps
$T_{sk\_PCI\_PCI}$		measured between rising edge at 1.5V	500	ps
$T_{sk\_PCI33\text{-}HT66}$		measured between rising edge at 1.5V	500	ps
$T_{sk\_CPU\_HT66}$		measured between rising edge at 1.5V	2000	ps
$T_{sk\_CPU\_HT66}$		measured at x-ing of CPU, 1.5V of PCI clock	500	ps
$T_{sk\_CPU\_CPU}$	time variant skew varies over V, T changes	measured at x-ing of CPU,	200	ps
$T_{sk\_CPU\_PCI}$		measured at x-ing of CPU, 1.5V of PCI clock	200	ps
$T_{sk\_PCI\_PCI}$		measured between rising edge at 1.5V	200	ps
$T_{sk\_PCI33\text{-}HT66}$		measured between rising edge at 1.5V	200	ps
$T_{sk\_CPU\_HT66}$		measured between rising edge at 1.5V	200	ps
$T_{sk\_CPU\_HT66}$		measured at x-ing of CPU, 1.5V of PCI clock	200	ps

General I²C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation			
Controller (Host)			**ICS (Slave/Receiver)**
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation			
Controller (Host)			**ICS (Slave/Receiver)**
T	starT bit		
Slave Address D2(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address D3(H)			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

0499C—11/01/04

Byte0: Functionality and Frequency Select

Bit	Pin #	PWD	Description
7		0	Write disable (Write once)[1]
6		0	Spread Spectrum Enable. 0 = Disable; 1 = Enable [2]
5		0	Reserved
4		0	Reserved
3	45	0	FS2
2	48	0	FS1
1	1	0	FS0
0		0	Write Enable [3]

Notes:

1. Write Disable. A '1' written to this bit after a '1' is written to BYTE0/bit 0 will permanently disable writing to I2C until the part is powered off. Once the clock generator has been write disabled, the SMBus controller should still accept and acknowledge subsequent write cycles but it should not modify any of the registers.

2.

Spread Pin	SS Bit	Spread Enable
0	0	Disabled
0	1	Enabled
1	0	Enabled
1	1	Enabled

3. A '1' written to this bit after power-up will enable writing to I2C. Subsequent '0's written to this bit will disable modification of all registers except this single bit. When a '1' is written to Byte 0 Bit 7, all modification is permanently disabled until the device power cycles. Block write transactions to the interface will complete, however unless the interface has been previously unlocked, the writes will have no effect. The effect of writing to this bit does not take effect until the subsequent block write command.

4. Clarification on frequency select on power-up:

i. Upon power-up, Byte0, bits (5:1) [FS(4:0)] are set to default hardware settings.
ii. A '1' is written to Byte0, bit 0 to enable software control.
iii. Every time Byte0 is written, frequency input defaults will be affected.
iv. If a '0' is written to Byte0, bit0, the software control is disabled. Disabling software control does not cause the contents of Byte0 to default back to hardware setting for FS(4:0).

Byte 1: CPU, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	7	1	PCICLK33/66_1
Bit 6	8	1	PCICLK33/66_0
Bit 5	22	1	PCICLK5
Bit 4	21	1	PCICLK4
Bit 3	18	1	PCICLK3
Bit 2	17	1	PCICLK2
Bit 1	14	1	PCICLK1
Bit 0	13	1	PCICLK0

Byte 2: PCI, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	37, 36	1	CPUCLKT/C_1 (Note)
Bit 6	41, 40	1	CPUCLKT/C_0
Bit 5	45	1	REF2
Bit 4	48	1	REF1
Bit 3	1	1	REF0
Bit 2	28	1	24_48MHz
Bit 1	31	1	48MHz
Bit 0	11	1	PCICLK33/66_2

Note: This bit can be optional to disable the CPUCLKT/C1 clock pair; CPUCLKT=L, CPUCLKC=H.

Byte 3: SDRAM, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	(Reserved)
Bit 6	-	0	(Reserved)
Bit 5	22	0	PCICLK5 (Note)
Bit 4	21	0	PCICLK4 (Note)
Bit 3	18	0	PCICLK3 (Note)
Bit 2	17	0	PCICLK2 (Note)
Bit 1	14	0	PCICLK1 (Note)
Bit 0	13	0	PCICLK0 (Note)

Note: The above individual free running enable/disable controls are intended to allow individual clock outputs to be made free running. A clock output that has it's free running bit enabled will not be turned off with the assertion of either PCI_STOP#.

Byte 4: Read-Back Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	23	1	PCICLK_F (Note)
Bit 6	44	1	SPREAD
Bit 5	28	1	24_48SEL
Bit 4	6	1	PCI33/66SEL#
Bit 3	45	1	FS2 power-up latched pin state
Bit 2	48	1	FS1 power-up latched pin state
Bit 1	1	1	FS0 power-up latched pin state
Bit 0	-	0	(Reserved)

Note: Can be optionally used as PCI33_F enable control.

Byte 5: Peripheral , Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	VENDOR ID
Bit 6	-	0	
Bit 5	-	1	
Bit 4	-	0	REVISION ID
Bit 3	-	0	
Bit 2	-	0	
Bit 1	-	0	
Bit 0	-	0	

Notes:

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 6: Byte Count Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Byte7 (Note)
Bit6	-	0	Byte6 (Note)
Bit5	-	0	Byte5 (Note)
Bit4	-	0	Byte4 (Note)
Bit3	-	0	Byte3 (Note)
Bit2	-	1	Byte2 (Note)
Bit1	-	1	Byte1 (Note)
Bit0	-	1	Byte0 (Note)

Note: Writing to this register will configure byte count and how many bytes will be read back. Default state is 07H = 7 bytes.

Byte 7: Reserved, Active/Inactive Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Reserved
Bit6	-	0	Reserved
Bit5	-	0	Reserved
Bit4	-	1	Reserved
Bit3	-	0	Reserved
Bit2	-	0	Reserved
Bit1	-	0	Reserved
Bit0	-	0	Reserved

Byte 8: Single Pulse Mode Control Register (1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit7	-	0	Single Pulse Trigger
Bit6	-	0	Single Pulse Activate
Bit5	-	0	(Reserved)
Bit4	-	0	(Reserved)
Bit3	-	0	(Reserved)
Bit2	-	0	(Reserved)
Bit1	-	0	(Reserved)
Bit0	-	0	(Reserved)

Notes:

ATPG Function: This feature is only used during processor Burn-In and is an optional feature for the clk vendor to implement.
Two SMBus register bits are required to implement this feature:
ATPG Mode Bit: Enables/Disables ATPG mode
ATPG Pulse Bit: Triggers a single CPUclk pulse when set
Assuming that the clock synthesizer is operating either in Normal mode or PLL bypass mode, following sequence may be followed to generate an ATPG pulse.
1. Set the Write Enable Bit (Byte/Bit 0) to program the Clock Synthesizer registers using the SM Bus.
2. Use the ATPG Mode Bit in the clock synthesizer configuration space to enable/disable the ATPG mode. When this bit is set, the ATPG mode is enabled and the differential CPU clock outputs are pulled in differential low state (CPUT = 0 and CPUC = 1). The ATPG mode also requires the USBclk (48MHz) to run as usual. All other clks (PCI, Ref, PCI33_66, SuperIO are not used by the ATPG mode therefore can either be left running or shut off.
3. Use the ATPG Pulse Bit in the clock synthesizer program space to generate the ATPG pulse. When the ATPG Pulse Bit is set, a differential ATPG pulse will be generated on the differential CPU clock pins. The pulse width of the ATPG pulse will be one CPU clock period. The CPU clock period in the ATPG mode is same as the one in Normal mode or PLL bypass mode.
4. Clear the ATPG Pulse Bit, as the clock synthesizer only recognizes 0 to 1 transition of the ATPG pulse bit for next ATPG pulse generation.
5. Use the ATPG Pulse Bit to generate the next ATPG pulse (set to 1).
6. If the ATPG Pulse bit is not set and the ATPG Mode Bit is cleared then the synthesizer should work in normal or PLL bypass mode.

Absolute Maximum Ratings

Supply Voltage 3.8V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +3.8 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

ESD Protection . . . . . Input ESD protection usung human body model > 1KV

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70º C; Supply Voltage V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{DD}$			5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66MHz			180	mA
	$I_{DD3.3OP100}$	C_L = 0 pF; Select @ 100MHz				
	$I_{DD3.3OP133}$	C_L = 0 pF; Select @ 133MHz				
Power Down	PD				600	µA
Input frequency	F_i	V_{DD} = 3.3 V;	10	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Z_O	$V_O = V_X$	15		55	Ω
Output High Voltage	V_{OH2B}		1		1.2	V
Output Low Voltage	V_{OL2B}				0.4	V
Output Low Current	I_{OL2B}	V_{OL} = 0.3 V	18			mA
Rise Edge Rate[1]		Measured from 20-80%	2		7	V/ns
Fall Edge Rate[1]		Measured from 80-20%	2		7	V/ns
V_{DIFF}		Differential Voltage, Measured @ the Hammer test load (single-ended measurement)	0.4		2.3	V
ΔV_{DIFF}		Change in V_{DIFF_DC} magnitude, Measured @ the Hammer test load (single-ended measurement)	-150		150	mV
V_{CM}		Common Mode Voltage, Measured @ the Hammer test load (single-ended measurement)	1.05		1.45	V
ΔV_{CM}		Change in Common Mode Voltage, Measured @ the Hammer test load (single-ended measurement)	-200		200	mV
Duty Cycle[1]	d_{t2B}	V_T = 50%	45		53	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	$V_T = V_X$	0		200	ps

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - V_{DIF} specifies the minimum input differential voltages (V_{TR}-V_{CP}) required for switching, where V_{TR} is the "true" input level and V_{CP} is the "complement" input level.

3 - $Vpullup_{(external)}$ = 1.5V, Min = $Vpullup_{(external)}$/2-150mV; Max=($Vpullup_{(external)}$/2)+150mV

Electrical Characteristics - PCICLK, PCICLK33/HT66 (33MHz)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.0 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-15	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	10			mA
Rise Edge Rate[1]		Measured from 20-60%	1		4	V/ns
Fall Edge Rate[1]		Measured from 60-20%	1		4	V/ns
Duty Cycle[1]	d_{t1}	V_T = 50%	45		55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	Measured on rising edge @ 1.5V			250	ps
Jitter, Accumulated[1]			-1000		1000	ps
Output Impedance	Z_O	$V_O = V_X$	12		55	Ω

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCICLK33/HT66 (66MHz)

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 30 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.0 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-15	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	10			mA
Rise Edge Rate[1]		Measured from 20-60%	1		4	V/ns
Fall Edge Rate[1]		Measured from 60-20%	1		4	V/ns
Duty Cycle[1]	d_{t1}	V_T = 50%	45		55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	Measured on rising edge @ 1.5V			250	ps
Jitter, Accumulated[1]			-1000		1000	ps
Output Impedance	Z_O	$V_O = V_X$	12		55	Ω

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Edge Rate[1]		Measured from 20-80%	0.5		2	V/ns
Fall Edge Rate[1]		Measured from 80-20%	0.5		2	V/ns
Duty Cycle[1]	d_{t5}	V_T = 50%	45		55	%
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	Mesured on rising edge @ 1.5V	0		1000	ps
Jitter, Accumulated[1]			-1000		1000	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz, 48MHz

T_A = 0 - 70º C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Edge Rate[1]		Measured from 20-80%	0.5		2	V/ns
Fall Edge Rate[1]		Measured from 80-20%	0.5		2	V/ns
Duty Cycle[1]	d_{t5}	V_T = 50%	45		55	%
Jitter, Absolute[1]	t_{jabs5}	V_T = 1.5 V	-1		1	ns
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	$V_T = V_X$, for 24_48MHz clock	0		500	ps
Jitter, Cycle-to-cycle[1]	$t_{jcyc-cyc2B}$	$V_T = V_X$, for 48MHz clock	0		200	ps
Output Impedance	Z_O	$V_O = V_X$	20		60	Ω

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the ICS9248-175 serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

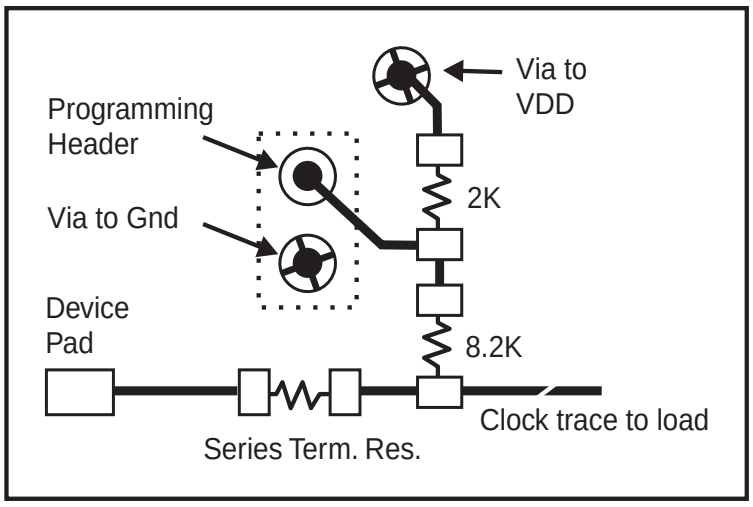
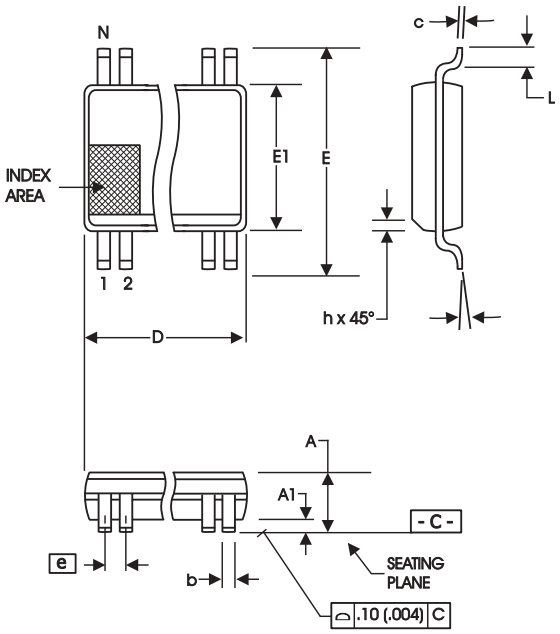


Fig. 1



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

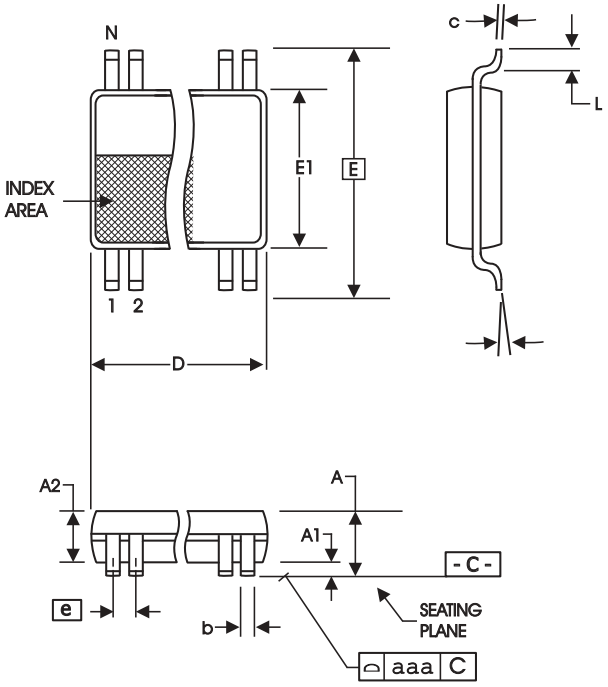
ICS950401yFLF-T

Example:

ICS XXXX y F LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0499C—11/01/04



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

'ARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

Ordering Information

ICS950401yGLF-T

Example:

ICS XXXX y G LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0499C—11/01/04

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