CA91C142D (Universe IID)

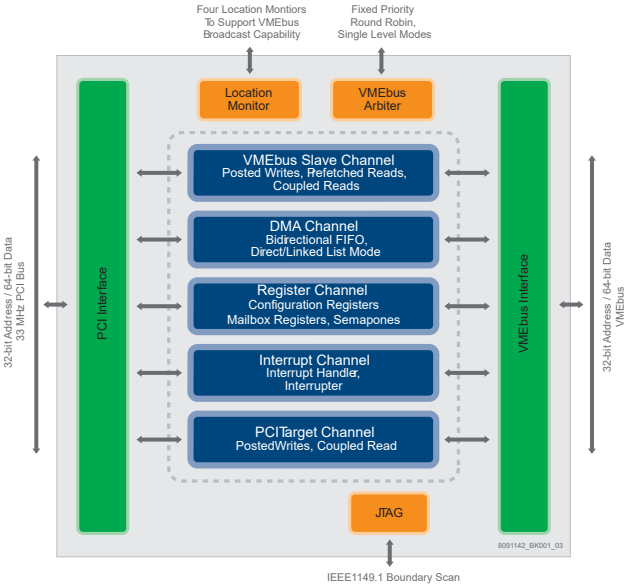
High-Performance PCI-to-VMEbus Interconnect

The CA91C142D is the industry's leading high performance PCI-to-VMEbus interconnect. CA91C142D is fully compliant with the VME64 bus standard, and tailored for the next-generation of advanced PCI processors and peripherals. With a zero-wait state implementation, multi-beat transactions, and support for bus-parking, CA91C142D provides high performance on the PCI bus.

The CA91C142D eases development of multi-master, multi-processor architectures on VMEbus and PCI bus systems. The device is ideally suited for CPU boards functioning as both master and slave in the VMEbus system, and that require access to PCI systems. Bridging is accomplished through a decoupled architecture with independent FIFOs for inbound, outbound, and DMA traffic. With this architecture, throughput is maximized without sacrificing bandwidth on either bus.

With the CA91C142D, you know that as your system becomes more complex, you have proven silicon that continues to provide everything you need in a PCI-to-VME bridge.

Block Diagram



Features

- Industry-proven, high performance 64-bit VMEbus interconnect
- Fully compliant, 32-bit or 64-bit, 33 MHz PCI bus interconnect
- Integral FIFOs for write posting to maximize bandwidth utilization
- Programmable DMA controller with Linked-List mode (Scatter/Gather) support
- Flexible interrupt logic
- Sustained transfer rates up to 60-70 MB/s
- Extensive suite of VMEbus address and data transfer modes
- Automatic initialization for slave-only applications
- Flexible register set, programmable from both the PCI bus and VMEbus ports
- Full VMEbus system controller
- Support for RMWs, ADOH, PCI LOCK_ cycles, and semaphores

Applications

- Single-board computers
- Telecommunications equipment
- Test equipment
- Command and control systems
- Factory automation equipment
- Medical equipment
- Military
- Aerospace

Benefits

- Industry proven device
- Reliable customer support with experience in hundreds of customer designs

Contents

1. Overview

1.1 Typical Application Example: Single Board Computers

The CA91C142D is widely used on VME-based Single Board Computers (SBC) that employ PCI as their local bus and VME as the backplane bus, as shown in the accompanying diagram. These SBC cards support a variety of applications including telecom, datacom, medical, industrial, and military equipment.

The CA91C142D high performance architecture seamlessly bridges the PCI and VME busses, and is the VME industry's standard for single board computer interconnect device.

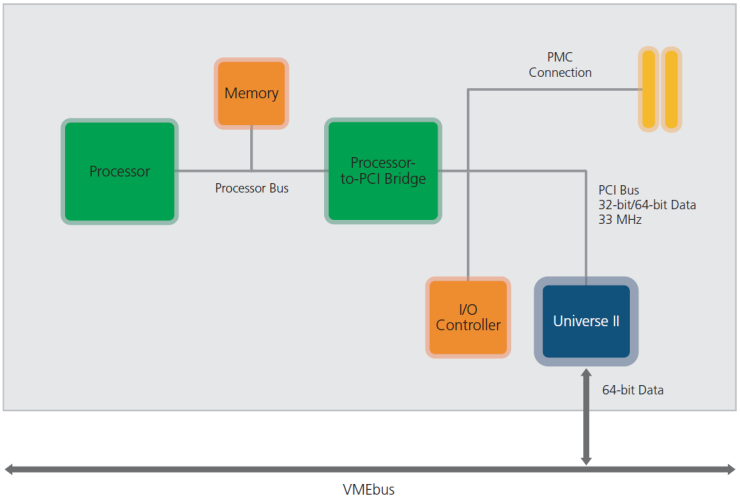


Figure 1. CA91C142D In Single Board Computer Application

1.2 Main Interfaces

The CA91C142D has two main interfaces: the PCI Bus Interface and the VMEbus Interface. Each of the interfaces, VMEbus and PCI bus, there are three functionally distinct modules: master module, slave module, and interrupt module. These modules are connected to the different functional channels operating in the CA91C142D. The device had the following channels:

- VMEbus Slave Channel
- PCI Bus Target Channel
- DMA Channel
- Interrupt Channel
- Register Channel

Figure 2 shows the CA91C142D in terms of the different modules and channels.

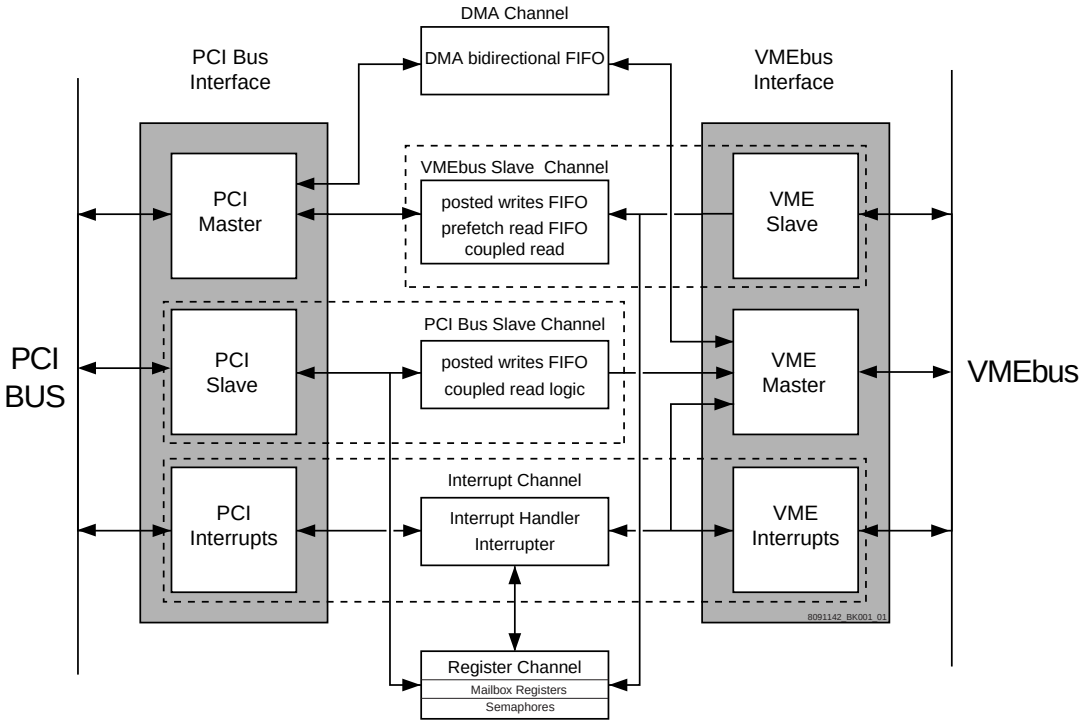


Figure 2. CA91C142D Data Flow Diagram

1.2.1 VMEbus Interface

The VME Interface is a *VME64 Specification* compliant interface.

1.2.1.1 CA91C142D as VMEbus Slave

The CA91C142D VMEbus Slave Channel accepts all of the addressing and data transfer modes documented in the *VME64 Specification* - except A64 and those intended to augment 3U applications. Incoming write transactions from the VMEbus can be treated as either coupled or posted, depending upon the programming of the VMEbus slave image (see “VME Slave Image Programming” in the *Universe IID User Manual*). With posted write transactions, data is written to a Posted Write Receive FIFO (RXFIFO), and the VMEbus master receives data acknowledgment from the CA91C142D. Write data is transferred to the PCI resource from the RXFIFO without the involvement of the initiating VMEbus master (see “Posted Writes” in the *Universe IID User Manual* for a full explanation of this operation). With a coupled cycle, the VMEbus master only receives data acknowledgment when the transaction is complete on the PCI bus. This means that the VMEbus is unavailable to other masters while the PCI bus transaction is executed.

Read transactions may be either prefetched or coupled. A prefetched read is initiated when a VMEbus master requests a block read transaction (BLT or MBLT) and this mode is enabled. When the CA91C142D receives the block read request, it begins to fill its Read Data FIFO (RDFIFO) using burst transactions from the PCI resource. The initiating VMEbus master then acquires its block read data from the RDFIFO instead of directly from the PCI resources.

Note: As VMEbus slave, the CA91C142D does not assert RETRY* as a termination of the transaction.

1.2.1.2 CA91C142D as VMEbus Master

The CA91C142D becomes VMEbus master when the VMEbus Master Interface is internally requested by the PCI Bus Target Channel, the DMA Channel, or the Interrupt Channel. The Interrupt Channel always has priority over the other two channels. Several mechanisms are available to configure the relative priority that the PCI Bus Target Channel and DMA Channel have over ownership of the VMEbus Master Interface.

The CA91C142D's VMEbus Master Interface generates all of the addressing and data transfer modes documented in the *VME64 Specification* - except A64 and those intended to augment 3U applications. The CA91C142D is also compatible with all VMEbus modules conforming to pre-VME64 specifications.

As VMEbus master, the CA91C142D supports Read-Modify-Write (RMW), and Address-Only-with-Handshake (ADOH) but does not accept RETRY* as a termination from the VMEbus slave. The ADOH cycle is used to implement the VMEbus Lock command allowing a PCI master to lock VMEbus resources.

1.2.2 PCI Bus Interface

The PCI Interface is a *PCI 2.1 Specification* compliant interface

1.2.2.1 CA91C142D as PCI Target

Read transactions from the PCI bus are always processed as coupled transactions. Write transactions can be either coupled or posted, depending upon the setting of the PCI bus target image (see "PCI Bus Target Images" in the *Universe IID User Manual*). With a posted write transaction, write data is written to a Posted Write Transmit FIFO (TXFIFO) and the PCI bus master receives data acknowledgment from the CA91C142D with zero wait-states. Meanwhile, the CA91C142D obtains the VMEbus and writes the data to the VMEbus resource independent of the initiating PCI master (see "Posted Writes" in the *Universe IID User Manual* for a full description of this operation).

The CA91C142D has a Special Cycle Generator that enables PCI masters to perform RMW and ADOH cycles. The Special Cycle Generator must be used in combination with a VMEbus ownership function to guarantee PCI masters exclusive access to VMEbus resources over several VMEbus transactions (see "Special Cycle Generator" and "Using the VOWN bit" in the *Universe IID User Manual* for a full description of this functionality).

1.2.2.2 CA91C142D as PCI Master

The CA91C142D becomes PCI master when the PCI Master Interface is internally requested by the VMEbus Slave Channel or the DMA Channel. There are mechanisms provided which allow the user to configure the relative priority of the VMEbus Slave Channel and the DMA Channel.

1.2.3 Interrupter and Interrupt Handler

The Universe II has both interrupt generation and interrupt handling capability.

1.2.3.1 Interrupter

The CA91C142D Interrupt Channel provides a flexible scheme to map interrupts to the PCI bus or VMEbus Interface. Interrupts are generated from hardware or software sources (see "Interrupt Generation" and "Interrupt Handling" in the *Universe IID User Manual* for a full description of hardware and software sources). Interrupt sources can be mapped to any of the PCI bus or VMEbus interrupt output pins. Interrupt sources mapped to VMEbus interrupts are generated on the VMEbus interrupt output pins VIRQ_ [7:1]. When a software and hardware source are assigned to the same VIRQ_ pin, the software source always has higher priority.

Interrupt sources mapped to PCI bus interrupts are generated on one of the INT_ [7:0] pins. To be fully PCI compliant, all interrupt sources must be routed to a single INT_ pin.

For VMEbus interrupt outputs, the CA91C142D interrupter supplies an 8-bit STATUS/ID to a VMEbus interrupt handler during the IACK cycle. The interrupter also generates an internal interrupt in this situation if the SW_IACK bit, in the PCI Interrupt Status (LINT_STAT) register, is set to 1 (see "VMEbus Interrupt Generation" in the *Universe IID User Manual*).

Interrupts mapped to PCI bus outputs are serviced by the PCI interrupt controller. The CPU determines which interrupt sources are active by reading an interrupt status register in the CA91C142D. The source negates its interrupt when it has been serviced by the CPU (see "PCI Interrupt Generation" in the *Universe IID User Manual*).

1.2.3.2 VMEbus Interrupt Handling

A VMEbus interrupt triggers the CA91C142D to generate a normal VMEbus IACK cycle and generate the specified interrupt output. When the IACK cycle is complete, the CA91C142D releases the VMEbus and the interrupt vector is read by the PCI resource servicing the interrupt output. Software interrupts are ROAK, while hardware, and internal interrupts are RORA.

1.2.4 DMA Controller

The CA91C142D has an internal DMA controller for high performance data transfer between the PCI and VMEbus. DMA operations between the source and destination bus are decoupled through the use of a single bidirectional FIFO (DMAFIFO). Parameters for the DMA transfer are software configurable in the CA91C142D registers (see “DMA Controller” in the *Universe IID User Manual*).

The principal mechanism for DMA transfers is the same for operations in either direction (PCI-to-VMEbus, or VMEbus-to-PCI), only the relative identity of the source and destination bus changes. In a DMA transfer, the CA91C142D gains control of the source bus and reads data into its DMAFIFO. Following specific rules of DMAFIFO operation (see “FIFO Operation and Bus Ownership” in the *Universe IID User Manual*), it then acquires the destination bus and writes data from its DMAFIFO.

The DMA controller can be programmed to perform multiple blocks of transfers using linked-list mode. The DMA works through the transfers in the linked-list following pointers at the end of each linked-list entry. Linked-list operation is initiated through a pointer in an internal CA91C142D register, but the linked-list itself resides in PCI bus memory.

2. Pin Information

2.1 Pin Assignments

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	
1	vd[22]		vd[19]		vd[9]		vd[5]		VDD		int_[7]		VSS		lrst_		vrbr_[1]		ad[27]		ad[58]		PLL_ testsel		**AVSS**	1
2		vd[18]		vd[14]		vd[13]		vd[6]		vd[2]		vscon_ DIR		vxbbsy		ad[61]		ad[59]		ad[24]		PLL_ testout		VDD		2
3	vd[23]		vd[21]		vd[20]		vd[12]		vd[3]		int_[5]		vbclr_		vrbr_[2]		VDD		ad[57]		lclk		VDD		vcoctl	3
4		vd[26]		VDD		vd[15]		vd[11]		vd[4]		int_[4]		VSS		pwrrst_		ad[25]		ad[56]		perr_		ad[22]		4
5	vd[30]		vd[24]		VDD		vd[17]		vd[8]		VDD		ad[63]		ad[60]		ad[26]		vrbr_[0]		int_[1]		**AVDD**		par64	5
6		vd[27]		vd[25]		vd[16]		vd[10]		vd[7]		vrbbsy_		ad[30]		VSS		int_[3]		ad[23]		ad[55]		VSS		6
7	vrberr_		vd[28]		viack_		**VDD**		vd[0]		vrbr_[3]		vsysclk		VDD		ad[28]		**VDD**		serr_		devsel_		ad[20]	7
8		vam_DIR		vwrite_		vd[29]		**VDD**		vd[1]		int_[6]		par		ad[29]		**VDD**		ad[21]		ad[54]		trdy_		8
9	vam[5]		VDD		vd[31]		vam[2]		**VDD**		int_[2]		**VSS**		ad[62]		**VDD**		ad[18]		ad[53]		VSS		VDD	9
10		vam[3]		vam[1]		vd_DIR		vam[4]		**VSS**		vxsysfail		ad[31]		**VDD**		ad[51]		VSS		ad[52]		ad[19]		10
11	vds_[1]		tms		vam[0]		VDD		vds_DIR		**VSS**		**VSS**		**VSS**		VSS		ack64_		VDD		ad[50]		ad[16]	11
12		voe_		vxberr		vds_[0]		tck		vas_DIR		**VSS**		**VSS**		cbe[6]		ad[48]		ad[49]		ad[17]		cbe[7]		12
13	tdi		tdo		trst_		va_DIR		**VSS**		**VSS**		**VSS**		**VSS**		**VSS**		cbe[3]		tmode[0]		vrsysfail_		VSS	13
14		vas_		va[5]		va[3]		va[1]		vlword_		**VSS**		**VSS**		cbe[2]		cbe[1]		cbe[0]		VSS		cbe[5]		14
15	va[2]		vslave_D IR		VDD		vdtack_		va[4]		**VSS**		**VSS**		**VSS**		ad[15]		VDD		ad[14]		irdy_		cbe[4]	15
16		va[8]		va[10]		va[13]		va[7]		**VSS**		vbgi_[1]		ad[0]		**VSS**		vrirq_[5]		VSS		idsel		ad[47]		16
17	VDD		va[9]		va[14]		va[6]		**VDD**		ad[32]		**VSS**		vrirq_[7]		**VDD**		frame_		ad[13]		VDD		gnt_	17
18		va[12]		va[17]		va[16]		**VDD**		vxirq[3]		vbgo_[2]		vracfail_		ad[3]		**VDD**		ad[45]		stop_		req64_		18
19	va[11]		va[18]		va[23]		**VDD**		vxirq[1]		VDD		ad[33]		ad[2]		ad[35]		**VDD**		rst_		ad[12]		ad[46]	19
20		va[19]		va[21]		va[22]		vrirq_[2]		int_[0]		vbgo_[0]		vrirq_[6]		ad[5]		ad[39]		ad[43]		ad[11]		ad[44]		20
21	va[15]		vrsysrst_		va[28]		va[27]		vrirq_[4]		viacko_		vbgi_[0]		VDD		ad[38]		ad[41]		tmode[1]		ad[10]		enid	21
22		va[20]		VDD		va[29]		vrirq_[1]		req_		vxirq[6]		ad[1]		ad[4]		vme_res et_		ad[40]		ad[8]		ad[42]		22
23	vxsysrst		clk64		va[25]		vxbr[3]		VDD		vxirq[5]		vbgi_[3]		ad[34]		ad[36]		tmode[2]		lock_		VDD		viacki_	23
24		VDD		va[30]		va[31]		vxbr[1]		vxirq[2]		vbgo_[3]		vxbr[2]		VSS		VSS		VDD		ad[7]		VDD		24
25	va[24]		va[26]		vrirq_[3]		vxbr[0]		vxirq[4]		vbgo_[1]		vbgi_[2]		vxirq[7]		VDD		ad[37]		ad[6]		VSS		ad[9]	25

2.2 Pin Descriptions

Table 1. Pin Descriptions

Pin Name	Pin Type	Description
VMEbus Signals		
CLK64	Input	Reference Clock – this 64MHz clock is used to generate fixed timing parameters. It requires a 50-50 duty cycle (±20%) with a 5ns maximum rise time. CLK64 is required to synchronize the internal state machines of the VME side of the CA91C142D.
VA [31:1]	Bidirectional	VMEbus Address Lines 31 to 01 – during MBLT transfers, VA 31-01 serve as data bits D63-D33. VA03-01 are used to indicate interrupt level on the VMEbus.
VA_DIR	Output	VMEbus Address Transceiver Direction Control – the CA91C142D controls the direction of the address (VA31-01, VLWORD_) transceivers as required for master, slave and bus isolation modes. When the CA91C142D is driving lines on the VMEbus, this signal is driven high; when the VMEbus is driving the CA91C142D, this signal is driven low.

Table 1. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
VAM [5:0]	Bidirectional	VMEbus Address Modifier Codes – these codes indicate the address space being accessed (A16, A24, A32), the privilege level (user, supervisor), the cycle type (standard, BLT, MBLT) and the data type (program, data).
VAM_DIR	Output	VMEbus AM Code Direction Control – controls the direction of the AM code transceivers as required for master, slave and bus isolation modes. When the CA91C142D is driving lines on the VMEbus, this signal is driven high; when the VMEbus is driving the CA91C142D, this signal is driven low.
VAS_	Bidirectional	VMEbus Address Strobe – the falling edge of VAS_ indicates a valid address on the bus. By continuing to assert VAS_, ownership of the bus is maintained during a RMW cycle.
VAS_DIR	Output	VMEbus Address Strobe Direction Control – controls the direction of the address strobe transceiver as required for master, slave and bus isolation modes. When the CA91C142D is driving lines on the VMEbus, this signal is driven high; when the VMEbus is driving the CA91C142D, this signal is driven low.
VBCLR_	Output	VMEbus Bus Clear – requests that the current owner release the bus. Asserted by the CA91C142D when configured as SYSCON and the arbiter detects a higher level pending request.
VBGI[3:0]_	Input	VMEbus Bus Grant Inputs – The VME arbiter awards use of the data transfer bus by driving these bus grant lines low. The signal propagates down the bus grant daisy chain and is either accepted by a requester if it requesting at the appropriate level, or passed on as a VBGO [3:0]_ to the next board in the bus grant daisy chain.
VBGO[3:0]_	Output	VMEbus Bus Grant Outputs – Only one output is asserted at any time, according to the level at which the VMEbus is being granted.
VD[31:0]_	Bidirectional	VMEbus Data Lines – 31 through 0
VD_DIR	Output	VMEbus Data Transceiver Direction Control – the CA91C142D controls the direction of the data (VD [31:0]) transceivers as required for master, slave and bus isolation modes. When the CA91C142D is driving lines on the VMEbus, this signal is driven high; when the VMEbus is driving the CA91C142D, this signal is driven low.
VDS[1:0]_	Bidirectional	VMEbus Data Strobes – the level of these signals are used to indicate active byte lanes During write cycles, the falling edge indicates valid data on the bus. During read cycles, assertion indicates a request to a slave to provide data.
VDS_DIR	Output	VMEbus Data Strobe Direction Control – controls the direction of the data strobe transceivers as required for master, slave and bus isolation modes. When the CA91C142D is driving lines on the VMEbus, this signal is driven high; when the VMEbus is driving the CA91C142D, this signal is driven low.
VDTACK_	Bidirectional	VMEbus Data Transfer Acknowledge – VDTACK_ driven low indicates that the addressed slave has responded to the transfer. The CA91C142D always rescinds DTACK*. It is tristated once the initiating master negates AS*.
VIACK_	Bidirectional	VMEbus Interrupt Acknowledge – Indicates that the cycle just beginning is an interrupt acknowledge cycle.
VIACKI_	Input	VMEbus Interrupt Acknowledge In – Input for IACK daisy chain driver. If interrupt acknowledge is at same level as interrupt currently generated by the CA91C142D, then the cycle is accepted. If interrupt acknowledge is not at same level as current interrupt or CA91C142D is not generating an interrupt, then the CA91C142D propagates VIACKO_.
VIACKO_	Output	VMEbus Interrupt Acknowledge Out – Generated by the CA91C142D if it receives VIACKI_ and is not currently generating an interrupt at the level being acknowledged.
VLWORD_	Bidirectional	VMEbus Longword Data Transfer Size Indicator – This signal is used in conjunction with the two data strobes VDS [1:0]_ and VA 01 to indicate the number of bytes (1 – 4) in the current transfer. During MBLT transfers VLWORD_ serves as data bit D32.

Table 1. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
VOE_	Output	VMEbus Transceiver Output Enable – Used to control transceivers to isolate the CA91C142D from the VMEbus during a reset or BI-mode. On power-up, VOE_ is high (to disable the buffers). VOE_ is negated during some VMEbus Slave Channel read operations.
VRACFAIL_	Input	VMEbus ACFAIL Input signal – Warns the VMEbus system of imminent power failure. This gives the modules in the system time to shut down in an orderly fashion before power-down. ACFAIL is mapped to a PCI interrupt.
VRBBSY_	Input	VMEbus Receive Bus Busy – Allows the CA91C142D to monitor whether the VMEbus is owned by another VMEbus master
VRBERR_	Input	VMEbus Receive Bus Error – A low level signal indicates that the addressed slave has not responded, or is signaling an error.
VRBR[3:0]_	Input	VMEbus Receive Bus Request Lines – If the CA91C142D is the Syscon, the arbiter logic monitors these signals and generates the appropriate Bus Grant signals. Also monitored by requester in ROR mode.
VRIRQ[7:1]_	Input	VMEbus Receive Interrupts 7 through 1 – These interrupts can be mapped to any of the CA91C142D's PCI interrupt outputs. VRIRQ7-1_ are individually maskable, but cannot be read.
VRSYSFAIL_	Input	VMEbus Receive SYSFAIL – Asserted by a VMEbus system to indicate some system failure. VRSYSFAIL_ is mapped to a PCI interrupt.
VRSYSRST_	Input	VMEbus Receive System Reset – Causes assertion of LRST_ on the local bus and resets the CA91C142D.
VSLAVE_DIR	Output	VMEbus Slave Direction Control – Transceiver control that allows the CA91C142D to drive DTACK* on the VMEbus. When the CA91C142D is driving lines on the VMEbus, this signal is driven high; when the VMEbus is driving the CA91C142D, this signal is driven low.
VSYSCLK	Bidirectional	VMEbus System Clock – Generated by the CA91C142D when it is the Syscon and monitored during DY4 Auto ID sequence
VSCON_DIR	Output	Syscon Direction Control – Transceiver control that allows the CA91C142D to drive VBCLR_ and SYSCLK. When the CA91C142D is driving lines on the VMEbus, this signal is driven high; when the VMEbus is driving the CA91C142D, this signal is driven low.
VWRITE_	Bidirectional	VMEbus Write signal – Indicates the direction of data transfer.
VXBBSY	Output	VMEbus Transmit Bus Busy Signal – Generated by the CA91C142D when it is VMEbus master
VXBERR	Output	VMEbus Transmit Bus Error Signal – Generated by the CA91C142D when PCI target generates Target-Abort on coupled PCI access from VMEbus.
VXBR [3:0]	Output	VMEbus Transmit Bus Request – The CA91C142D requests the VMEbus when it needs to become VMEbus master.
VXIRQ [7:1]	Output	VMEbus Transmit Interrupts – The VMEbus interrupt outputs are individually maskable.
VXSYSFAIL	Output	VMEbus System Failure – Asserted by the CA91C142D during reset and plays a role in VME64 Auto ID.
VXSYSRST	Output	VMEbus System Reset – The CA91C142D output for SYSRST*.
PCI Signals		
ACK64_	Bidirectional	Acknowledge 64-bit Transfer – It indicates slave can perform a 64-bit transfer when driven by the PCI slave (target).
AD [31:0]	Bidirectional	PCI Address/Data Bus – Address and data are multiplexed over these pins providing a 32-bit address and 32-bit data bus.
AD [63:32]	Bidirectional	PCI Address/Data Bus – Address and data are multiplexed over these pins providing 64-bit address and data capability.

Table 1. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
C/BE_ [7:0]	Bidirectional	PCI Bus Command and Byte Enable Lines – Command and byte enable information is multiplexed over all eight C/BE lines. C/BE [7:4]_ are only used in a 64-bit PCI bus
DEVSEL_	Bidirectional	PCI Device Select – This signal is driven by the CA91C142D when it is accessed as PCI slave.
ENID	Input	Enable IDD Tests – Required for ASIC manufacturing test, tie to ground for normal operation.
FRAME_	Bidirectional	Cycle Frame – This signal is driven by the CA91C142D when it is PCI initiator, and is monitored by the CA91C142D when it is PCI target.
GNT_	Input	PCI Grant – indicates to the CA91C142D that it has been granted ownership of the PCI bus.
IDSEL	Input	PCI Initialization Device Select – This signal is used as a chip select during configuration read and write transactions.
LINT[7:0]_	Bidirectional (Open Drain)	PCI Interrupt Inputs – These PCI interrupt inputs can be mapped to any PCI bus or VMEbus interrupt output.
IRDY_	Bidirectional	Initiator Ready – Is used by the CA91C142D as PCI master to indicate that is ready to complete a current data phase.
LCLK	Input	PCI Clock – Provides timing for all transactions on the PCI bus. PCI signals are sampled on the rising edge of CLK, and all timing parameters are defined relative to this signal. The PCI clock frequency of the Universe II must be between 25 and 33MHz. Lower frequencies result in invalid VME timing.
LOCK_	Bidirectional	Lock – Used by the CA91C142D to indicate an exclusive operation with a PCI device. While the CA91C142D drives LOCK_, other PCI masters are excluded from accessing that particular PCI device. When the CA91C142D samples LOCK_, it can be excluded from a particular PCI device.
LRST_	Output	PCI Reset Output – Used to reset PCI resources.
PAR	Bidirectional	Parity – Parity is even across AD [31:0] and C/BE [3:0] (the number of 1s summed across these lines and PAR equal an even number).
PAR64	Bidirectional	Parity Upper DWORD – Parity is even across AD [63:32] and C/BE [7:4] (the number of 1s summed across these lines and PAR equal an even number).
PERR_	Bidirectional	Parity Error – Reports parity errors during all transactions. The CA91C142D drives PERR_ high within two clocks of receiving a parity error on incoming data, and holds PERR_ for at least one clock for each errored data phase.
PLL_TESTOUT	Output	Manufacturing Test Output—No connect
PLL_TESTSEL	Input	Manufacturing Test Select—Tie to ground for normal operation
PWRRST_	Input	Power-up Reset – All CA91C142D circuitry is reset by this input.
REQ_	Output	Bus Request – Used by the CA91C142D to indicate that it requires the use of the PCI bus.
REQ64_	Bidirectional	64-Bit Bus Request— Used to request a 64-bit PCI transaction. If the target does not respond with ACK64_, 32-bit operation is assumed.
RST_	Input	PCI Reset Input— Resets the CA91C142D from the PCI bus.
SERR_	Output	System Error – Reports address parity errors or any other system error.
STOP_	Bidirectional	Stop – Used by the CA91C142D as PCI slave when it wishes to signal the PCI master to stop the current transaction. As PCI master, the CA91C142D terminates the transaction if it receives STOP_ from the PCI slave.
TCK	Input	JTAG Test Clock Input – Used to clock the CA91C142D's TAP controller. Tie to any logic level if JTAG is not used in the system.
TDI	Input	JTAG Test Data Input – Used to serially shift test data and test instructions into the CA91C142D. Tie to any logic level if JTAG is not used in the system.

Table 1. Pin Descriptions (Cont.)

Pin Name	Pin Type	Description
TDO	Output	JTAG Test Data Output – Used to serially shift test data and test instructions out of the CA91C142D
TMODE [2:0]	Input	Test Mode Enable – Used for chip testing, tie to ground for normal operation.
TMS	Input	JTAG Test Mode Select – Controls the state of the Test Access Port (TAP) controller in the CA91C142D. Tie to any logic level if JTAG is not used in the system.
TRDY_	Bidirectional	Target Ready – Used by the CA91C142D as PCI slave to indicate that it is ready to complete the current data phase. During a read with CA91C142D as PCI master, the slave asserts TRDY_ to indicate to the CA91C142D that valid data is present on the data bus.
TRST_	Input	JTAG Test Reset – Provides asynchronous initialization of the TAP controller in the CA91C142D. Tie to ground if JTAG is not used in the system.
VCOCTL	Input	Manufacturing testing – Tie to ground for normal operation
VME_RESET_	Input	VMEbus Reset Input — Generates a VME bus system reset.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 2. Absolute Maximum Ratings

Parameter	Range
DC Supply Voltage (VSS to VDD)	-0.3 to 7.0 V
DC Input Voltage (V_{IN})	-0.5 to vdd + 0.5V
DC Current Drain per Pin, Any Single Input or Output	± 50ma
DC Current Drain per Pin, Any Paralleled Outputs	± 100ma
DC Current Drain V_{DD} and V_{SS} Pins	± 75ma
Storage Temperature, (T_{STG})	-40 ºC to 125 ºC

3.2 Recommended Operating Conditions

The following table specifies recommended operating condition for the CA91C142D.

Table 3. Recommended Operating Conditions

Symbols	Parameters	Min	Max	Frequency Operation (MHz)
Vdd	DC Supply Voltage (5V ± 10%)	4.5V	5.5V	
Ta (Commercial)	Ambient Temperature	0ºC	+70ºC	25 - 33
Ta (Industrial)	Ambient Temperature	-40ºC	+85ºC	25 - 33
Ta (Extended)	Ambient Temperature	-55ºC	+125ºC	25

3.3 DC Characteristics

3.3.1 Non-PCI Characteristics

Table 4 specifies the required DC characteristics of all non-PCI signals pins.

Table 4. Non-PCI Electrical Characteristics

Symbols	Parameters	Test conditions	Tested at 0°C to 70°C	
			Min	Max
VIH_TTL	Voltage Input high	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	2.2 V	V_{DD} + 0.3V
VIH_CMOS	Voltage Input high	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	0.7 Vdd	V_{DD} + 0.3V
VIL_TTL	Voltage Input low	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	–0.3 V	0.8V
VIL_CMOS	Voltage Input low	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	–0.3 V	0.3V_{DD}
VT+_TTL	Voltage Input high (Schmitt trigger)	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	-	2.4 V

Table 4. Non-PCI Electrical Characteristics (Cont.)

Symbols	Parameters	Test conditions	Tested at 0°C to 70°C	
			Min	Max
VT+_CMOS	Voltage Input high (Schmitt trigger)	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	-	0.7V_{DD}
VT -_ttl	Voltage Input low (Schmitt trigger)	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	0.8V	-
VT -_CMOS	Voltage Input low (Schmitt trigger)	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	0.25V_{DD}	-
I_{IN}	Input leakage current	With no pull-up or pull-down resistance (Vin = Vss or V_{DD})	-5.0µA	5.0µA
I_{IH}	Input leakage current high	Inputs with pull-down resistance (Vin = Vdd)	10µA	180µA
I_{IL}	Input leakage current low	Inputs with pull-up resistance (Vin = Vss)	-180µA	-10µA
I_{OZ}	Tristate output leakage	Vout = Vdd or Vss	-10.0µA	10.0µA

3.3.2 PCI Characteristics

Table 5 specifies the required AC and DC characteristics of all PCI Universe II signal pins.

Table 5. AC/DC PCI Electrical Characteristics

Symbols	Parameters	Condition	Min	Max	Unit
VIL	Voltage Input low		-0.5	0.8	V
VIH	Voltage Input high		2.0	Vdd + 0.5	V
I_{IN}	Input leakage current	Vin = 2.7V or 0.5V	-10	10	µA
I_{IL}	Input leakage current low (Pin with pull-up)	Vin = 0.5V	-70	-10	µA
VOL	Voltage output low	Iout = 3mA, 6mA	-	0.4	V
VOH	Voltage output high	Iout = -2mA	2.4	-	V
IOH (AC)[1]	Switching current high	0 < Vout²1.4	-44	-	mA
		1.4 < Vout < 2.4	-44 + (Vout -1.4) / 0.024	-	mA
		3.1 < Vout < Vdd	-	Equation A	mA
	(Test point)	Vout = 3.1V	-	-142	mA
IOL (AC)[2]	Switching current high	0 < Vout³1.4	95	-	mA
		0.6Vdd < Vout < 0.1Vdd	Vout / 0.023	-	mA
		0.71 < Vout < 0	-	Equation B	mA
	(Test point)	Vout = 0.71V	-	206	mA
ICL	Low clamp current	-5 Vin²-1	-25 + (Vin +10) / 0.015	-	mA
SLEWR	Output rise slew rate	0.4V to 2.4V load	1	5	V/ns
SLEWR	Output fall slew rate	2.4V to 0.4V load	1	5	V/ns

1. Equation A: Ioh = 11.9 * (Vout - 5.25) * (Vout + 2.45) for Vdd > Vout > 3.1V
2. Equation B: Iol = 78.5 * Vout * (4.4 - Vout) for 0V < Vout < 0.71V

3.3.3 Pin List and DC Characteristics for all Signals

Table 6 specifies the required DC characteristics of all Universe II signal pins

Table 6. Pin List and DC Characteristics for Universe II Signals

Pin Name	Pin Number	Type	Input Type	Output Type	I_{OL} (mA)	I_{OH} (mA)	Signal Description
ack64#	W11	I/O	TTL	3S	6	–2	PCI Acknowledge 64 Bit Transfer
AD [63:0]	Listed in Pin Assignments	I/O	TTL	3S	6	–2	PCI Address/Data Pins
C/BE# [0]	Y14	I/O	TTL	3S	6	–2	PCI Command and Byte Enables
C/BE# [1]	V14						
C/BE# [2]	T14						
C/BE# [3]	W13						
C/BE# [4]	AE15						
C/BE# [5]	AD14						
C/BE# [6]	T12						
C/BE# [7]	AD12						
clk64	C23	I	TTL	–	–	–	VME Clock 64 MHz—60-40 duty, 5 ns rise time
devsel#	AC7	I/O	–	3S	6	–2	PCI Device Select
enid	AE21	I	CMOS	–	–	–	Enable IDD Tests
frame#	W17	I/O	TTL	3S	6	–2	PCI Cycle Frame
gnt#	AE17	I	TTL	–	–	–	PCI Grant
idsel	AB16	I	TTL	–	–	–	PCI Initialization Device Select
lint# [0]	K20	I/O	TTL	OD	12	–12	PCI Interrupt
lint# [1]	AA5	I/O	TTL	OD	4	–4	
lint# [2]	L9						
lint# [3]	V6						
lint# [4]	M4						
lint# [5]	L3						
lint# [6]	M8						
lint# [7]	L1						
irdy#	AC15	I/O	TTL	3S	6	–2	PCI Initiator Ready
lclk	AA3	I	TTL	–	–	–	PCI Clock Signal
lock#	AA23	I/O	TTL	3S	6	–2	PCI Lock
lrst#	R1	O	–	3S	6	–2	PCI Reset Output
par	P8	I/O	TTL	3S	6	–2	PCI parity
par64	AE5	I/O	TTL	3S	6	–2	PCI Parity Upper DWORD
perr#	AB4	I/O	TTL	3S	6	–2	PCI Parity Error
pll_testout	AB2	For factory testing					

Table 6. Pin List and DC Characteristics for Universe II Signals (Cont.)

Pin Name	Pin Number	Type	Input Type	Output Type	I_{OL} (mA)	I_{OH} (mA)	Signal Description
pll_testsel	AC1	For factory testing					
pwrrst#	T4	I	TTL/Schm	–	–	–	Power–up Reset
req#	K22	O	–	3S	6	–2	PCI Request
req64#	AD18	I/O	TTL	3S	6	–2	PCI Request 64 Bit Transfer
rst#	AA19	I	TTL	–	–	–	PCI Reset
serr#	AA7	O	TTL	OD	12	–12	PCI System Error
stop#	AB18	I/O	TTL	3S	6	–2	PCI Stop
tck	H12	I	TTL	–	–	–	JTAG Test Clock Input
tdi	A13	I	TTL (PU)	–	–	–	JTAG Test Data Input
tdo	C13	O	–	3S	–	–	JTAG Test Data OUTput
tmode [0]	AA13	I	TTL	–	–	–	Test Mode Enable
tmode [1]	AA21						
tmode [2]	W23						
tms	C11	I	TTL (PU)	–	–	–	JTAG Test Mode Select
trdy#	AD8	I/O	TTL	3S	6	–2	PCI Target Ready
trst#	E13	I	TTL (PU)	–	–	–	JTAG Test Reset
VA [31:1]	Listed in Pin Assignments	I/O	TTL (PD)	3S	3	–3	VMEbus Address Pins
vam [0]	E11	I/O	TTL	3S	3	–3	VMEbus Address Modifier Signals
vam [1]	D10						
vam [2]	G9						
vam [3]	B10						
vam [4]	H10						
vam [5]	A9						
vam_dir	B8	O	–	3S	6	–6	VMEbus AM Signal Direction Control
vas#	B14	I/O	TTL/Schm (PU)	3S	3	–3	VMEbus Address Strobe
vas_dir	K12	O	–	3S	6	–6	VMEbus AS Direction Control
va_dir	G13	O	–	3S	12	–12	VMEbus Address Direction Control
vbclr#	N3	O	–	3S	3	–3	VMEbus BCLR* Signal

Table 6. Pin List and DC Characteristics for Universe II Signals (Cont.)

Pin Name	Pin Number	Type	Input Type	Output Type	I_{OL} (mA)	I_{OH} (mA)	Signal Description
vbgi# [0]	N21	I	TT	–	–	–	VMEbus Bus Grant In
vbgi# [1]	M16						
vbgi# [2]	N25						
vbgi# [3]	N23		TT (PD)				
vbgo# [0]	M20	O	–	3S	12	–12	VMEbus Bus Grant Out
vbgo# [1]	L25						
vbgo# [2]	M18						
vbgo# [3]	M24						
vcoctl	AE3	I	–	–	–	–	Factory testing
VD [31:0]	Listed in 313 Pin PBGA Package	I/O	TTL	3S	3	–3	VMEbus Data Pins
vd_dir	F10	O	–	3S	12	–12	VMEbus Data Direction Control
vds# [0]	F12	I/O	TTL (PU)	3S	3	–3	VMEbus Data Strobes
vds# [1]	A11						
vds_dir	J11	O	–	3S	6	–6	VMEbus Data Strobe Direction Control
vdtack#	G15	I/O	TTL/Schm (PU)	3S	3	–3	VMEbus DTACK* Signal
viack#	E7	I/O	TTL	3S	3	–3	VMEbus IACK* Signal
viacki#	AE23	I	TTL	–	–	–	VMEbus IACKIN* Signal
viacko#	L21	O	–	3S	12	–12	VMEbus IACKOUT* Signal
vlword#	K14	I/O	TTL (PD)	3S	3	–3	VMEbus LWORD* Signal
VME_RESET#	V22	I	TTL				VMEbus Reset Input
voe#	B12	O	–	3S	24	–24	VMEbus Transceiver Output Enable
vracfail#	P18	I	TTL/Schm	–	–	–	VMEbus ACFAIL* Signal
vrbbsy#	M6	I	TTL/Schm	–	–	–	VMEbus Received BBSY* Signal
vrberr#	A7	I	TTL/Schm	–	–	–	VMEbus Receive Bus Error
vrbr# [0]	W5	I	TTL/Schm	–	–	–	VMEbus Receive Bus Request
vrbr# [1]	U1						
vrbr# [2]	R3						
vrbr# [3]	L7						

Table 6. Pin List and DC Characteristics for Universe II Signals (Cont.)

Pin Name	Pin Number	Type	Input Type	Output Type	I_{OL} (mA)	I_{OH} (mA)	Signal Description
vrirq# [1]	H22	I	TTL/Schm	–	–	–	VMEbus Receive Interrupts
vrirq# [2]	H20						
vrirq# [3]	E25						
vrirq# [4]	J21						
vrirq# [5]	V16						
vrirq# [6]	P20						
vrirq# [7]	R17						
vrsysfail#	AC13	I	TTL	–	–	–	VMEbus Receive SYSFAIL Signal
vrsysrst#	C21	I	TTL/Schm	–	–	–	VMEbus Receive SYSRESET* Signal
vscon_dir	M2	O	–	3S	6	–6	SYSCON signals direction control
vslave_dir	C15	O	–	3S	6	–6	DTACK/BERR direction control
vsysclk	N7	I/O	TTL	3S	3	–3	VMEbus SYSCLK Signal
vwrite#	D8	I/O	TTL	3S	3	–3	VMEbus Write
vxbbsy	P2	O	–	3S	3	–3	VMEbus Transmit BBSY* Signal
vxberr	D12	O	–	3S	3	–3	VMEbus Transmit Bus Error (BERR*)
vxbr [0]	G25	O	–	3S	3	–3	VMEbus Transmit Bus Request
vxbr [1]	H24						
vxbr [2]	P24						
vxbr [3]	G23						
vxirq [1]	J19	O	–	3S	3	–3	VMEbus Transmit Interrupts
vxirq [2]	K24						
vxirq [3]	K18						
vxirq [4]	J25						
vxirq [5]	L23						
vxirq [6]	M22						
vxirq [7]	R25						
vxsysfail	M10	O	–	3S	3	–3	VMEbus Transmit SYSFAIL Signal
vxsysrst	A23	O	–	3S	3	–3	VMEbus Transmit SYSRESET* Signal

3.4 Power Dissipation

Table 7. Power Dissipation

Parameter	Rating
IDLE	
Power Dissipation	1.50 W
Typical	
Power Dissipation (32-bit PCI)	2.00 W
Power Dissipation (64-bit PCI)	2.20 W
Maximum	
Power Dissipation (32-bit PCI)	2.70W
Power Dissipation (64-bit PCI)	3.20W

3.5 Power Sequencing

When designing with the CA91C142D device, care must be taken when powering the device to ensure proper operation. During power-up, no signals must be applied to any CA91C142D signal pins prior to stable power being applied to the device.

Note: In a mixed 3.3V and 5V design, Renesas recommends that 5V power be stable prior to other devices coming out reset. If other devices come out of reset before the 5V power is stable, make certain that no signals are driven to the CA91C142D signal pins - including possible signals from the VME backplane.

4. Design Guidelines

For additional information on designing a product with the CA91C142D device, see the following two sections in the *CA91C142D User Manual*:

- Chapter 9, “Resets, Clocks and Power-up Options”
- Appendix E, “Typical Applications”

5. Package Outline Drawings

5.1 313 Pin PBGA Package

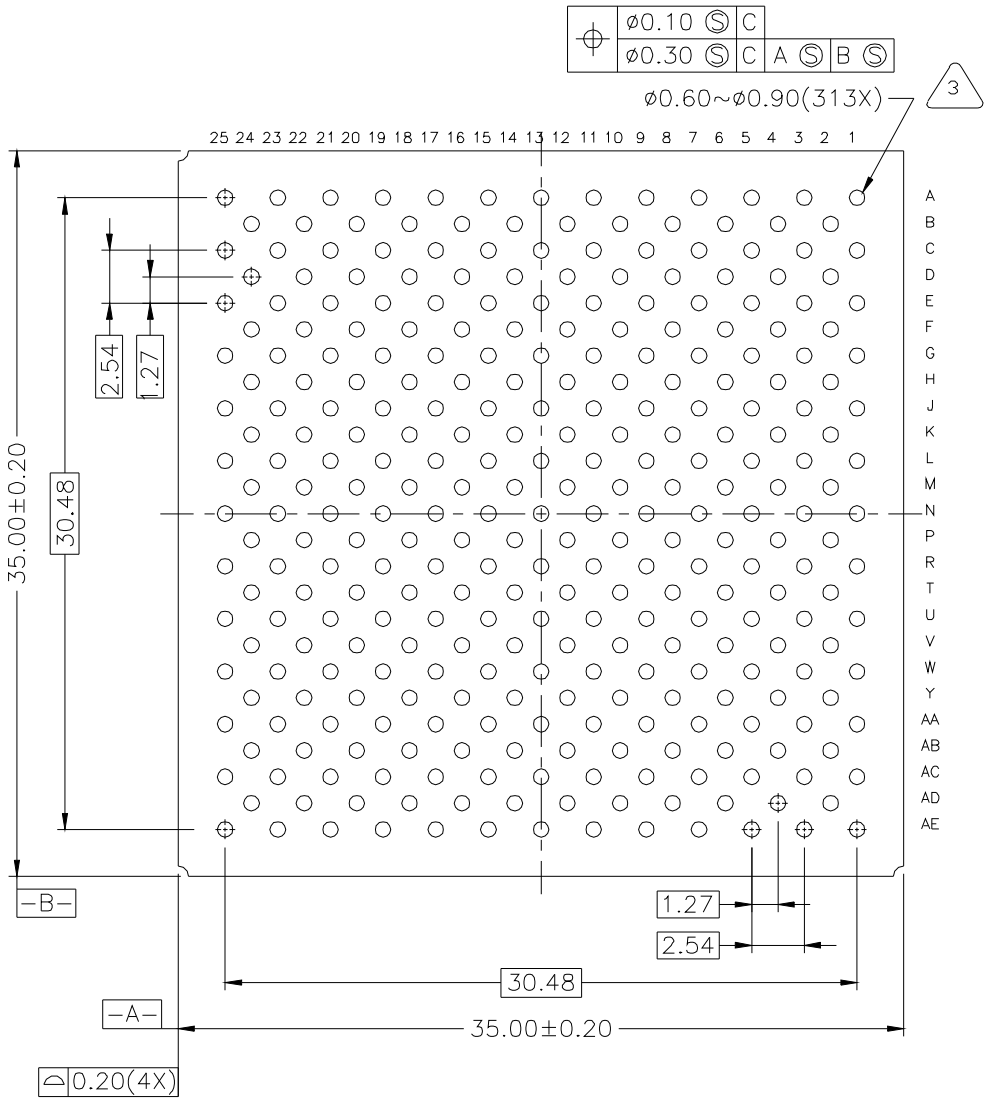


Figure 3. 313 PBGA - Bottom View

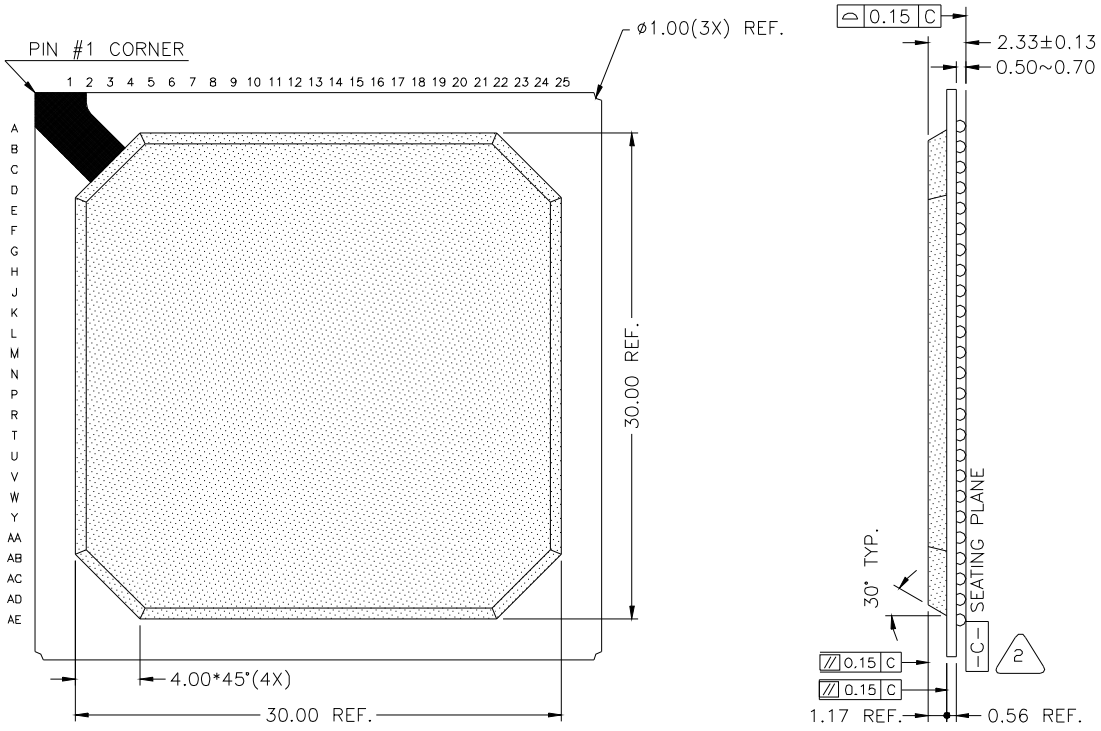


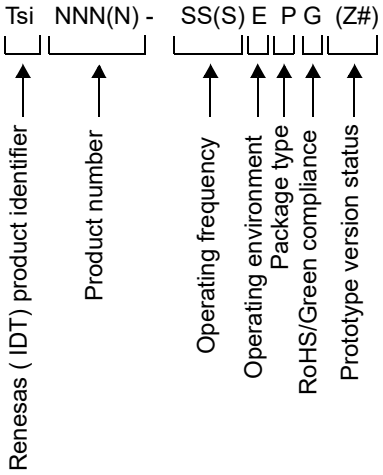
Figure 4. 313 PBGA - Top and Side View

6. Ordering Information

Table 8. Standard Ordering Information

Part Number	PCI Frequency	Voltage	Temperature	Package
CA91C142D-33CE	33 MHz	5 V	Commercial (0° to 70°C)	PBGA
CA91C142D-33CEV	33 MHz	5 V	Commercial (0° to 70°C)	PBGA (RoHS/Green)
CA91C142D-33IE	33 MHz	5 V	Industrial (-40° to 85°C)	PBGA
CA91C142D-33IEV	33 MHz	5 V	Industrial (-40° to 85°C)	PBGA (RoHS/Green)
CA91C142D-25EE	25 MHz	5 V	Extended (-55° to 125°C)	PBGA

The Renesas “Tsi” part numbering system is explained as follows.



- ( ) – Indicates optional characters.
- Tsi – Renesas (IDT) “Tsi” product identifier.
- NNNN – Product number (may be three or four digits).
- SS(S) – Maximum operating frequency or data transfer rate of the fastest interface. For operating frequency numbers, M and G represent MHz and GHz. For transfer rate numbers, M and G represent Mbps and Gbps.
- E – Operating environment in which the product is guaranteed. This code may be one of the following characters:
  - C - Commercial temperature range (0 to +70°C)
  - I - Industrial temperature range (-40 to +85°C)
  - E - Extended temperature range (-55 to +125°C)
- P – The Package type of the product:
  - B - Ceramic ball grid array (CBGA)
  - E, L, J, and K - Plastic ball grid array (PBGA)
  - G - Ceramic pin grid array (CPGA)
  - M - Small outline integrated circuit (SOIC)
  - Q - Plastic quad flatpack (QFP)
- G – Renesas (IDT) “Tsi” products fit into three RoHS-compliance categories:
  - Y - RoHS Compliant (6of6) – These products contain none of the six restricted substances above the limits set in the EU Directive 2002/95/EC.
  - Y - RoHS Compliant (Flip Chip) – These products contain only one of the six restricted substances: Lead (Pb). These flip-chip products are RoHS compliant through the Lead exemption for Flip Chip technology, Commission Decision 2005/747/EC, which allows Lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit Flip Chip packages.
  - V - RoHS Compliant/Green - These products follow the above definitions for RoHS Compliance and meet JIG (Joint Industry Guide) Level B requirements for Brominated Flame Retardants (other than PBBs and PBDEs).
- Z# – Prototype version status (optional). If a product is released as a prototype then a “Z” is added to the end of the part number. Further revisions to the prototype prior to production release would add a sequential numeric digit. For example, the first prototype version of device would have a “Z,” a second version would have “Z1,” and so on. The prototype version code is dropped once the product reaches production status.

7. Revision History

Revision	Date	Description
1.00	Jul 2, 2024	Initial release. ▪ The information in this document used to reside exclusively in the *Universe IID User Manual*. ▪ No technical changes were made in the creation of the datasheet.

A. Reliability Prediction

A.1 Overview

This section is designed to help the user to estimate the inherent reliability of the CA91C142D. The information serves as a guide only; meaningful results will be obtained only through careful consideration of the device, its operating environment, and its application.

A.2 Physical Characteristics

- CMOS gate array
- 120,000 two-input NAND gate equivalence
- 0.5 µm feature size
- 309 mils x 309 mils scribed die size

A.3 Thermal Characteristics

- Idle power consumption: 1.50 Watts
- Typical power consumption* (32-bit PCI): 2.00 Watts
- Maximum power consumption (32-bit PCI): 2.70 Watts
- Typical power consumption (64-bit PCI): 2.20 Watts
- Maximum power consumption (64-bit PCI): 3.20 Watts

Maximum power consumption is worst case consumption when the CA91C142D is performing DMA reads from the VME bus with alternating worst case data patterns ($FFFF_FFFF, $0000_0000 on consecutive cycles), and 100pF loading on the PCI bus

In the majority of system applications, the CA91C142D consumes typical values or less. Typical power consumption numbers are based on the CA91C142D remaining idle 30%-50% of the time, which is significantly less than what is considered likely in most systems. For this reason, it is recommended that typical power consumption numbers be used for power estimation and ambient temperature calculations, as described below.

The HTOL FIT rate is 67 FITs. The HTOL test showed 67 FITs based on the calculation of 60% Confidence Level (C.L.) and Activation Energy Ea=0.7eV for 0.5um process at stress condition 1.1 x Vcc at 125°C ambient temperature This FIT rate is approximately equivalent to 90% C.L. 167 FITs. Calculations were based on a 100 piece sample size for three lots. The test conditions were at 125°C/Bias, 5.5 V at 1 MHz per MIL-STD-883D.M1015.8.

Tip: FIT is the basic reliability rate expressed as failures per billion (1e-9) device hours. Mean Time Between Failures (MTBF) is the reciprocal of FIT. MTBF is the predicted number of device hours before a failure will occur.

A.4 CA91C142D Ambient Operating Calculations

The maximum ambient temperature of the CA91C142D can be calculated as follows:

$$T_a \leq T_j - \theta_{ja} * P$$

Where,

T_a = Ambient temperature (°C)

T_j = Maximum CA91C142D Junction Temperature (°C)

θ_{ja} = Ambient to Junction Thermal Impedance (°C / Watt)

P = CA91C142D power consumption (Watts)

The ambient to junction thermal impedance (θ_{ja}) is dependent on the air flow in linear feet per minute over the CA91C142D. The values for θ_{ja} over different values of air flow are shown in Table 9.

Table 9. Ambient to Junction Thermal Impedance

Air Flow (m/s)	0	1	2
313 PBGA	15.10	13.10	11.70

For example, the maximum ambient temperature of the 313 PBGA, 32-bit PCI environment with 100 LFPM blowing past the CA91C142D is:

$T_a \leq T_j - \theta_{ja} * P$

$T_a \leq 125 - 13.1* 2.0$

$T_a \leq 98.8\ °C$

Therefore the maximum rated ambient temperature for the CA91C142D in this environment is 98.8°C. Further improvements can be made by adding heat sinks to the PBGA package.

T_j values of CA91C142D are calculated as follows ($Tj = \theta ja * P + Ta$)

Table 10. Maximum CA91C142D Junction Temperature

Extended (125 °C Ambient)[1]	Industrial (85 °C Ambient)	Commercial: (70 °C Ambient)
Tj=13.1*2.7+125=160.37°C	Tj=13.1*2.7+85=120.37°C	Tj=13.1*2.7+70=105.37°C

1. Renesas recommends that the maximum junction temperature of the CA91C142D does not exceed 150 °C. This temperature limit can be achieved by using heat dissipation techniques, such as heat sinks and forced airflows.

These values were obtained under the following PCB and environmental conditions:

- PCB conditions:
  - PCB standard: JEDEC JESD51-9
  - PCB layers: 4
  - PCB dimensions: 101.6 mm x 114.3 mm
  - PCB thickness: 1.6 mm
- Environmental conditions:
  - Maximum junction temperature: 125°C
  - Ambient temperature: 70°C
  - Power dissipation: 3 W

A.5 Thermal Vias

The 313-pin plastic BGA package contains thermal vias which directly pipe heat from the die to the solder balls on the underside of the package. The solder balls use the capabilities of the power and ground planes of the printed circuit board to draw heat out of the package.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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