CCE4510

IO-Link Master PHY with integrated Frame Handler

The CCE4510 is a high-voltage interface IC with overvoltage detection as well as high temperature and high current protection, based upon a 0.35 µm HV-CMOS technology.

Typical applications are industrial sensors or actuators, which should support the IO-Link standard. To improve the application performance, an integrated IO-Link frame handler is provided, which automates most of the lower layer communication tasks. This reduces the microcontroller loads significantly, thus gaining more performance for other tasks, even if slower microcontrollers are used.

A variety in fields of application is given by different packaging*[1] and configuration options.

Features

- Two IO-Link compliant channels with 1 A peak CQ driving current
- Wide voltage range 8-32 V
- Transceiver mode (SIO)
- Integrated UART (COM1-3)
- Hardware frame handler (support for all IO-Link v1.1 frame types)
- Fully IO-Link v1.1 compliant
- Possibility to use IO-Link ports as master or device
- Completely automated wake-up procedure for master
- Two status LED drivers
- Synchronization features for IO Link channels and LEDs over multiple chips
- Includes NMOS gate drivers for ext. FETs controlling the power supply of devices with load currents of e.g. 2A (or higher)
- Supports feed through of clock
- Temperature and supply voltage monitoring and protection
- Overload protection for channels and connected devices
- Ideal fit for 2/4/8/16-port IO Link master applications
- Evaluation boards available

[1] Other packaging options are possible upon request

Contents

1. Overview

1.1 Block Diagram

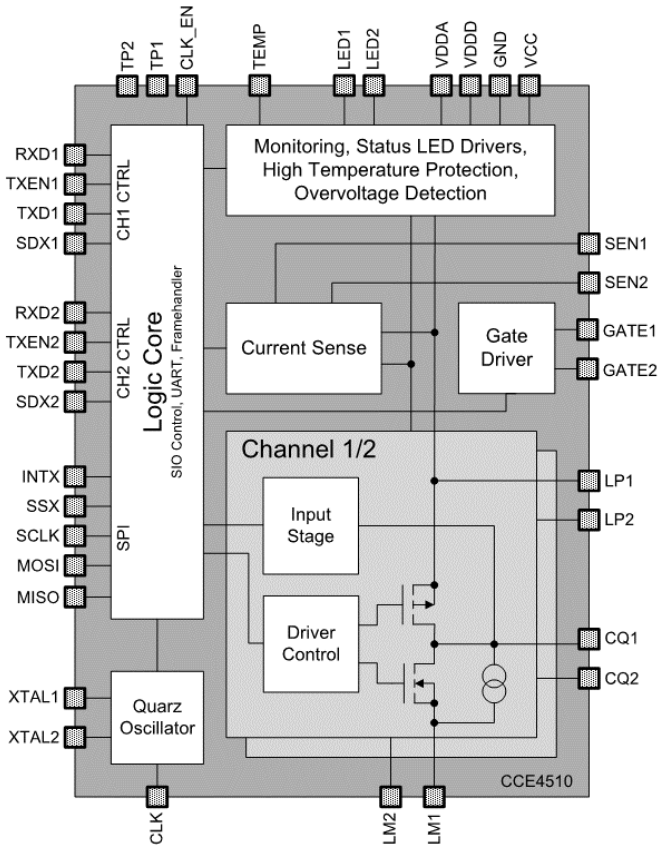


Figure 1. Block Diagram

2. Pin Information

2.1 Package

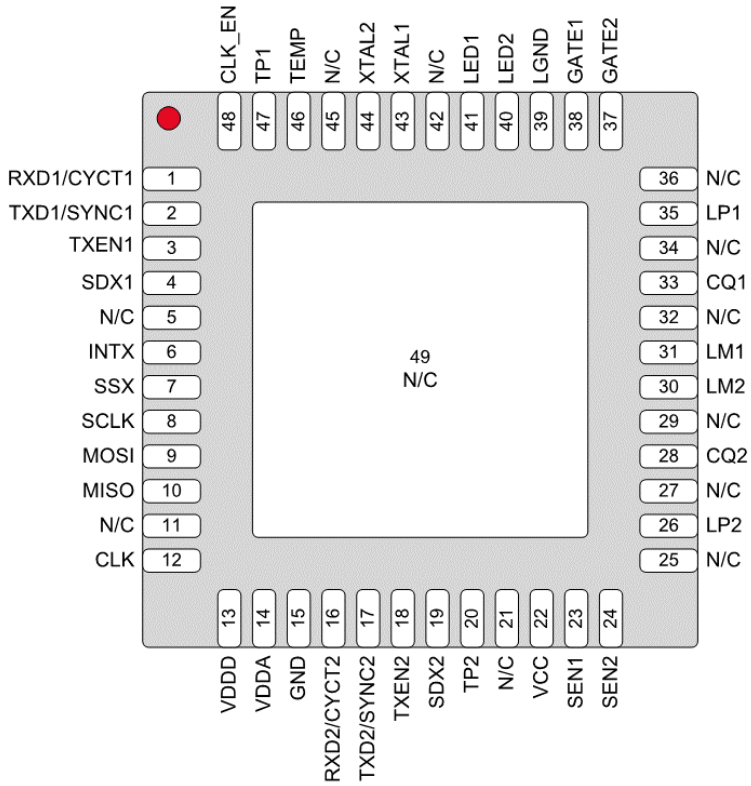


Figure 2. QFN48 Package (7x7 mm)

2.2 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	RXD1/CYCT1	OUT	RXD1: CQ1 input; inverted CYCT1: Cycle time indicator channel 1
2	TXD1/SYNC1	IN	TXD1: CQ1 output; internal pull-down; inverted SYNC1: Channel 1 synchronization trigger
3	TXEN1	IN	CQ1 driver enable; active high, internal pull-down
4	SDX1	OUT	Device 1 short detected; active low
6	INTX	OUT	SPI interrupt signal; active low
7	SSX	IN	SPI slave select; active low; internal pull-up
8	SCLK	IN	SPI clock; internal pull-down
9	MOSI	IN	SPI data in; internal pull-down
10	MISO	OUT	SPI data out; tri-state if SSX is high

12	CLK	OUT	Buffered clock feed through
13	VDDD	PWR	3.3 V digital voltage supply
14	VDDA	PWR	3.3 V analog voltage supply
15	GND	PWR	Ground
16	RXD2/CYCT2	OUT	RXD2: CQ2 input; inverted CYCT2: Cycle time indicator channel 2
17	TXD2/SYNC2	IN	TXD2: CQ2 output; internal pull-down; inverted SYNC2: Channel 2 synchronization trigger
18	TXEN2	IN	CQ2 driver enable; active high, internal pull-down
19	SDX2	OUT	Device 2 short detected; active low
20	TP2	OUT	Test Point 2; leave open
22	VCC	PWR	24 V main voltage supply
23	SEN1	IN	Sense input channel 1
24	SEN2	IN	Sense input channel 2
26	LP2	PWR	Sensor supply channel 1
28	CQ2	IN/OUT	IO-Link channel 2
30	LM2	PWR	Sensor ground 2
31	LM1	PWR	Sensor ground channel 1
33	CQ1	IN/OUT	IO-Link channel 1
35	LP1	PWR	Sensor supply channel 1
37	GATE2	OUT	NMOS gate driver channel 2
38	GATE1	OUT	NMOS gate driver channel 1
39	LGND	PWR	LED ground
40	LED2	OUT	LED driver channel 2
41	LED1	OUT	LED driver channel 1
43	XTAL1	IN	Crystal input; external clock source input
44	XTAL2	OUT	Crystal feedback
46	TEMP	OUT	High temperature indication, active high
47	TP1	IN	Test Point 1; internal pull-down; leave open or tie to ground
48	CLK_EN	IN	Enable buffered clock feed through; internal pull-down

3. Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VCC	static	-0.7		36	V
Power dissipation QFN48	P_{TOT_QFN48}	Multilayer PCB, Exp. Pad soldered, ϑ_{AMB} = 60°C			2	W
Junction Temperature	ϑ_{JUNC}				150	°C
ESD-sensitivity	V_{ESD}	Human Body Model EIA/JESD22-A114-B	2			kV
Storage Temperature	$\vartheta_{STORAGE}$		-55		155	°C
Soldering Temperature	ϑ_{SOLDER}	12 s max			260	°C
FIT Rate		$\vartheta_{JUNC} \leq 55°C$			50	FIT

4. Electrical Characteristics

4.1 General Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Main Supply Voltage	VCC		8	24	32	V
Quiescent Current Main Supply	I_{VCC}				5	mA
Pad Supply Voltage	VDD		3.1	3.3	3.5	V
Quiescent Current Pad Supply	I_{VDD}				5	mA
Operating Temperature	ϑ_{AMB}		-40		85	°C
Thermal Resistance Case	ϑ_{JC_QFN48}	Junction to Case; QFN48		0.5		°C/W
Thermal Resistance Ambient	ϑ_{JA_QFN48}	Junction to Ambient; QFN48		29		°C/W
Thermal Parameter Board	Ψ_{JB_QFN48}	Junction to Board; 4L JEDEC PCB (9 vias); QFN48		6.7		°C/W
Thermal Parameter Case	Ψ_{JC_QFN48}	Junction to Case; 4L JEDEC PCB (9 vias); QFN48		0.2		°C/W

4.2 IO-Link Channels

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LP Supply Voltage	V_{LP}		8	24	32	V
Permissible Voltage Range	V_{CQ}		-0.3		V_{LP}+ 0.3	V
Load or Discharge Current	I_{CQ_LOAD}	can be disabled; see 5.8.17		10	15	mA
CQ DC Driver Current ‘H’	I_{CQH}				300	mA
CQ DC Driver Current ‘L’	I_{CQL}				300	mA
Residual Voltage ‘H’	V_{RESH}	Voltage drop at I_{CQH_MAX}			3	V
Residual Voltage ‘L’	V_{RESL}	Voltage drop at I_{CQL_MAX}			3	V
CQ Output Peak Current ‘H’	I_{PEAKH}	Duration t_{PEAK} = 1 ms	0.5	1		A
CQ Output Peak Current ‘L’	I_{PEAKL}	Duration t_{PEAK} = 1 ms	0.5	1		A
Capacitive Load	C_{LOAD}			1		nF
Output Driver Rise Time	t_{RISE}	C_{NOM}=1 nF			300	ns
Output Driver Fall Time	t_{FALL}	C_{NOM}=1 nF			300	ns
Break Before Make Delay	t_{BBM}				50	ns
Input Detection Time ‘H’	t_{DETH}				300	ns
Input Detection Time ‘L’	t_{DETL}				300	ns
Input Threshold ‘H’	V_{THH_IOL}	IO-Link mode; see 5.8.17	10.5		13	V
Input Threshold ‘L’	V_{THL_IOL}	IO-Link mode; see 5.8.17	8		11.5	V
Hysteresis input threshold	V_{HYS_IOL}	IO-Link mode; see 5.8.17		2		V
Input Threshold ‘H’	V_{THH_RAT}	Ratiometric mode; see 5.8.17	0.55 V_{LP}			V
Input Threshold ‘L’	V_{THL_RAT}	Ratiometric mode; see 5.8.17			0.4 V_{LP}	V
Hysteresis input threshold	V_{HYS_RAT}	Ratiometric mode; see 5.8.17		0.0125 V_{LP}		V

4.3 NMOS Gate Drivers

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
On Switching Time	t_{GATE_ON}	C_{GATE} = 1 nF		1		ms
Off Switching Time	t_{GATE_OFF}	C_{GATE} = 1 nF		10		µs
Output Voltage	V_{GATE}	VCC ≥ 15 V	VCC+4		VCC+8	V
External Capacitance	C_{GATE}			1		nF
Transistor Leakage Current	I_{TGSL}	Gate to Source (external NMOS)			1	µA

4.4 Oscillator

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Frequency	f_{OSC}	External crystal		14.7456		MHz
Startup Time	t_{OSC_START}			30		ms
Rise Time	t_{OSC_RISE}			5		ns
Fall Time	t_{OSC_FALL}			5		ns
CLK Pin Driving Capability	C_{OUT_MAX}				15	pF

4.5 Digital Pads

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage ‘H’	V_{INH}		0.7 VDD			V
Input Voltage ‘L’	V_{INL}				0.3 VDD	V
Input Hysteresis	V_{IHYST}			340		mV
Input Capacitance	C_{IN}			5		pF
Input Leakage Current	I_{ILEAK}	No pull-up/pull-down	-1		1	µA
Output Voltage ‘H’	V_{OUTH}		0.8 VDD			V
Output Voltage ‘L’	V_{OUTL}				0.4	V
Output Leakage Current	I_{OLEAK}	Tri-State active			1	µA
Output Capacitance	C_{OUT}			5		pF
Output Driving Current	I_{OUT}		6			mA
Weak Pull-Up Current	I_{IH}	VIN = 0V		-30		µA
Weak Pull-Down Current	I_{IL}	VIN = VDD		30		µA

4.6 Serial Peripheral Interface

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SPI Clock Frequency	f_{SPI}		1		20	MHz
SPI Clock Period	t_{SPI_CLK}		50		1000	ns
SPI Start Clock after Select	t_{SPI_S}		25			ns
SPI End of Select after Clock	t_{SPI_E}		25			ns
SPI Idle between Access	t_{SPI_I}		100			ns

4.7 Current Sensing

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Ext. Short Detection Thresh.	V_{EXT_SD}		180	205	230	mV
Ext. Short Detection Current	I_{EXT_SD}	RSHUNT = 500 mΩ	380	415	450	mA
Int. Short Detection Current	I_{INT_SD}		300	350	400	mA
Driver Overload Detection Time	$t_{OVLDDET}$	Configurable; see 5.8.3	0.1		6.4	ms
Driver Overload Polling Time	$t_{OVLDDIS}$	Configurable; see 5.8.3	1		6400	ms
Short Circuit Detection Time	$t_{SHORTDET}$	Configurable; see 5.8.4	0.1		336	ms

4.8 Monitoring Thresholds

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Min. Voltage Monitor Thresh.	V_{CCOK_MIN}			7.5		V
Max. Voltage Monitor Thresh.	V_{CCOK_MAX}			34		V
Voltage Monitor Hysteresis	V_{CCOK_HYST}			0.6		V
Temperature Monitor Thresh.	ϑ_{INT}			125	150	°C
Temperature Monitor Hysteresis	ϑ_{INT_HYST}			10		°C

4.9 LEDs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LED Permissible Voltage Range	V_{LED}		-0.3		VDD+ 0.3	V
LED Current 5 mA	I_{LED_5MA}		4.5		5.5	mA
LED Current 10 mA	I_{LED_10MA}		9		11	mA
LED Sequence Bits	$BITS_{LED}$	Configurable; see 5.8.15		8		Bit
Bit high hold time	t_{HLDL}	Configurable; see 5.8.16	50		800	ms
Bit low hold time	t_{HLDH}	Configurable; see 5.8.16	50		800	ms

5. Functional Description

5.1 Power-up Sequence

For proper operation of the IC, VDD must be powered up before VCC. Not respecting the power-up sequence may result in damage to the IC.

5.2 Clocking

The IC is clocked by connecting an external 14.7456 MHz quartz at the XTAL1 and XTAL2 pins.

It is possible to daisy chain or directly connect multiple CCE4510 chips to the CLK pin for clocking. The CLK pin is then connected to the XTAL1 pin of the other chip(s). Clock feed through is enabled by default and can be disabled by pulling the CLK_EN pin high.

References: Oscillator, Pin Descriptions

5.3 Operational Modes

There are three possible operational modes for each CCE4510 IO-Link Channels - Standard I/O, UART and Frame Handler Mode. The channel mode can be configured in the MODE register.

5.3.1. Standard I/O (SIO)

If a channel is configured in the Standard I/O Mode, the mode of the output stage is freely configurable.

The SIO register allows the user to choose between a N, P or Push-Pull driving mode via the DRV bits. The TXEN and TXD bits of this register enable direct control over the output driver. The RXD bit in the MISO Status Nibble reflects the current state of the CQ pin.

In this mode, it is also possible to control and observe the channel using the TXEN, TXD and RXD pins. The corresponding pin and register values get logically ORed. Therefore, either the unused pin or register values should be zero, to allow control via the desired interface.

Since the sense of TXD to CQ is inverted, it is possible to connect a standard microcontroller UART interface with a high idle state to the TXD/RXD pins.

References: SIO1/2 (0x23/0x43), MISO Status Nibble, Pin Descriptions

5.3.2. UART

If a channel is configured in UART Mode, the output stage is set into Push-Pull Mode and the output cannot be controlled via the SIO register or the external pins. It is required to define the used COM speed in the MODE register.

By default, the channel will listen for incoming UART transactions at the CQ pin. If a character is received, an interrupt is triggered, and the data can be read back from the UART register. A transaction is started by writing the data to the UART register.

The received UART data is not buffered. Receiving multiple characters, while not reading them back, causes data loss. This will be indicated by the OFLW bit in the MISO Status Nibble.

References: UART1/2 (0x24/0x44), MODE1/2 (0x20/0x40), MISO Status Nibble

5.3.3. Frame Handler

The Frame Handler Mode extends the UART interface. Like in UART mode, the output stage is set into Push-Pull Mode and the output cannot be controlled via the SIO register or the external pins. It is required to define the used COM speed in the MODE register.

It mostly automates the transaction of frames, defined by the IO-Link protocol. Therefore, an automated CRC check for incoming and an automated CRC computation for outgoing messages is integrated. The frame handler will also monitor the specified timing constraints and takes care to comply with them as well.

5.3.3.1. Configuration

The operational mode as IO-Link Master or Device can be set via the MAS bit in the FHC register. This register also allows the user to relax the timeout detection or to disable the automatic CRC computation.

The master and device message lengths of each frame are influenced by the OD, MPD and DPD registers, but are also depending on the access type, addressed channel and frame type which are defined in the second byte of each IO-Link frame. FT0 frames always use one byte on-request data. FT1 frames use the MPD or DPD lengths, if the address channel is the Process Data Channel, otherwise the OD length is used. FT2 frames always use the MPD, DPD and OD lengths.

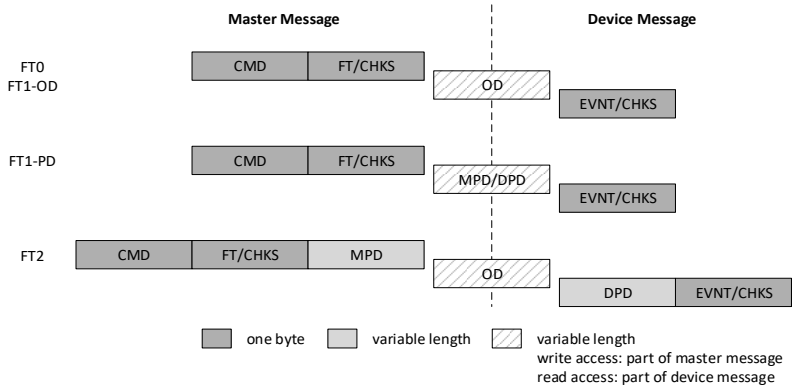


Figure 3: Frame Lengths

References: FHC1/2 (0x25/0x45), OD1/2 (0x26/0x46), MPD1/2 (0x27/0x47), DPD1/2 (0x28/0x48)

5.3.3.2. Master Mode

If configured as master, the frame handler waits for the user to write the complete message data into the frame buffer via the FHD register. This can be done by multiple SPI transactions or by a single bulk SPI transaction. By default, writing the last byte of a message into the buffer will start the transaction and the message CRC is automatically generated. If the automatic CRC feature is disabled, the transaction will start immediately after the first byte is written into the frame buffer. There is also the possibility to start a new frame transaction with respect to the defined cycle time in the CYCT register or even synchronizing various CCE4510 IO-Link channels using the sophisticated synchronization mechanism.

If a frame was transmitted successfully, the frame handler will start listening for any incoming device data and triggers an interrupt after a part or the complete device message is received. The interrupt behavior can be modified using the IMSK and TRSH register. Parity or checksum errors during the transaction will be indicated by the MISO Status Nibble. The received data can be read back via the FHD register by multiple SPI transactions or single/multiple bulk SPI transactions.

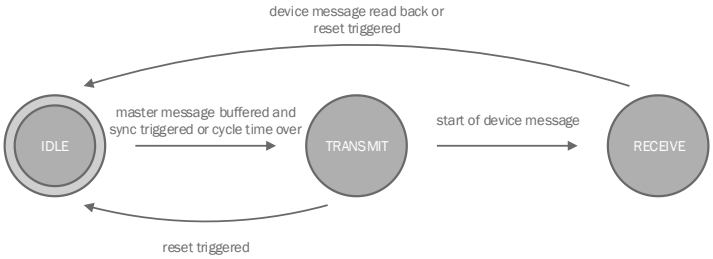


Figure 4: Master Mode Sequence

References: Additional IO-Link Features, Serial Peripheral Interface, Interrupt Masking, FHD1/2 (0x2A/0x4A)

5.3.3.3. Device Mode

Configured as device, the frame handler listens for incoming master transactions and triggers an interrupt, if a part or the complete device message is received. The interrupt behaviour can be modified using the IMSK and TRSH register. Parity or checksum errors during the transaction will be indicated by the MISO status nibble. The received data can be read back via the FHD register by multiple SPI transactions or single/multiple bulk SPI transactions.

After successfully receiving an incoming master message, the frame handler waits for the user to write the complete message data into the frame buffer via the FHD register. This can be done by multiple SPI transactions or by a single bulk SPI transaction. The transaction always starts immediately after the first byte is written into the frame buffer.

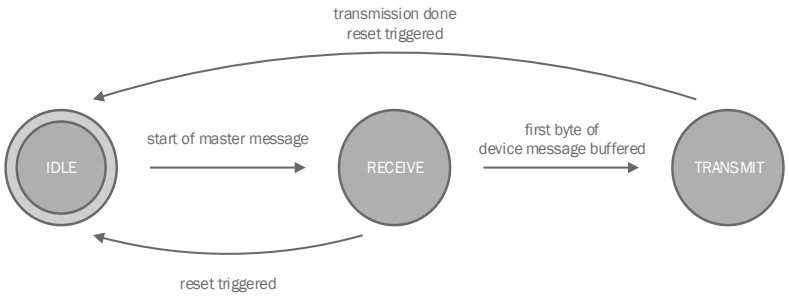


Figure 5: Device Mode Sequence

References: Additional IO-Link Features, Serial Peripheral Interface, FHD1/2 (0x2A/0x4A)

5.3.3.4. Skip and Reset Function

It is possible to reset the frame handler or skip an invalid frame from any state. This can be done by writing one to the RST or the SKIP bit of the FHC register.

Skipping a frame causes the frame handler to ignore the rest of an incoming message, without triggering any additional interrupt. A soft reset is done after receiving the rest of invalid message or if a timeout was detected. Skipping a frame has no effect on the cycle timer.

Resetting a frame will immediately reset the frame handler into its idle state and causes a reset of the cycle timer.

When resetting the frame handler with the RST bit or skipping a frame with the SKIP bit, all other bits written to the FHC1/2 register within the same SPI frame will be ignored.

References: FHC1/2 (0x25/0x45)

5.4 Interrupt Handling

The chip utilizes two modes of interrupt handling. The active mode can be switched with the IMODE bit in the INT register. Interrupt Mode 1 is active by default.

5.4.1. Mode 1

Interrupts are triggered on rising edges of the WURQ, RXRDY, TXRDY or TOUT bits in the SPI Status. If CQ is configured as input in SIO mode, interrupts are also triggered on any edge of the RXD bit.

Changes of the STATE bits in the SPI Status also trigger interrupts depending on the IMSK register settings. Trigger conditions can be the start of frame transmission or reception or reaching a defined fill level of the buffer. An interrupt is always triggered after a frame is completely received.

Another trigger condition is any change of values in the STAT register. Therefore, the microcontroller should always deal with an interrupt by reading back the STAT register.

The interrupt is cleared while reading the status register.

References: MISO Status Nibble, STAT (0x60), IMSK1/2 (0x2C/0x4C)

5.4.2. Mode 2

The interrupt triggering conditions are the same as described in Interrupt Mode 1. Mode 2 differs in the way how interrupts are handled.

First, the interrupt origin can be determined by reading the INT register. The interrupt then needs to be actively cleared by the user. This is done by writing a one to the appropriate bit ISTAT, ICH1 or ICH2 in the INT register.

The INTX pin will remain in its active state until all interrupts are cleared.

References: MISO Status Nibble, STAT (0x60), INT (0x64), IMSK1/2 (0x2C/0x4C)

5.4.3. Interrupt Masking

To reduce the number of triggered interrupts in frame handler mode, the user can deactivate the triggering of interrupts at certain conditions in the IMSK register.

Interrupt	Name	Description
SOT	Start of Transaction Interrupt	Triggers when the chip starts transmitting its message
SOR	Start of Reception Interrupt	Triggers as soon as the chip starts receiving a message
LVL	Message Level Interrupt	Triggers if a defined amount of buffered characters is reached
MSG	End of Message Interrupt	Triggers after the last character of a message was received
CYCT	Cycle Time Interrupt	Triggers when the configured cycle time has passed

The MSG interrupt is always active. By default, all other interrupts are masked. If the LVL interrupt is active, an interrupt will be triggered if the input buffer reaches a defined fill level. The current amount of buffered characters can be queried in the BLVL register. The threshold for buffered characters which triggers the LVL interrupt is configured in the TRSH register.

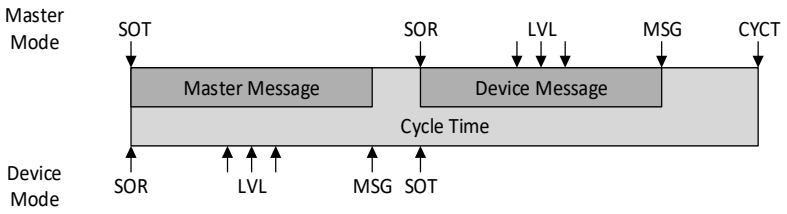


Figure 6: Interrupt Trigger Positions

It is also possible to mask the short detected (SD) interrupt of the STAT register. Otherwise, an interrupt gets triggered as soon as a short is detected.

References: Frame Handler, IMSK1/2 (0x2C/0x4C)

5.5 Protection Features

The CCE4510 IO-Link Master PHY integrates various features to protect the IO-Link master and connected IO-Link devices. Different configuration options allow the user to take individual safety measures and to prevent damage.

5.5.1. Current Sensing

5.5.1.1. Internal / External Mode

There are two possible methods implemented to detect a high load at the IO-Link supply voltage – an internal and an external current sensing mechanism. Both mechanisms cannot be active at the same time. The user must choose, which one should be used for each channel. The current sensing mode is configured by the SDINT bit in the CFG register. The SD bit in the STAT register and the SDX pins always reflect the current sensing state.

The internal current sensing mechanism does not need any external circuitry to work but has the limitation to only detect currents I_{MHS} and I_{MLS} at the CCE4510 CQ pin with a fixed current threshold. High currents I_{DEV} from a connected device cannot be detected. Therefore, the short protection feature for devices is not feasible in this mode. However, the usage of an external NMOS transistor is still possible.

The external current sensing can detect high currents I_{MHS} and I_{MLS} at the CQ pin and IDEV of a connected device. External shunts with a typical resistance of 0.5 Ω need to be applied for a current threshold of 400 mA. It is possible to adjust the high current detection threshold by changing the shunts resistance value. The voltage drop over the shunt is defined with 200 mV. Current sensing over a shunt and an external NMOS transistor allow the usage of the short protection feature.

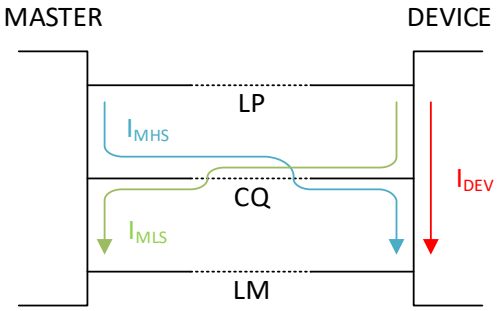


Figure 7: High Current Detection

References: Current Sensing, Application Notes, CFG1/2 (0x2F/0x4F)

5.5.1.2. Overload / Short Protection

The Overload Protection protects master and device from high loads at the channel output CQ. The output driver of a channel is automatically disabled if high currents are detected for a time > $t_{OVLDDET}$. The channel stays disabled and gets re-enabled after a time $t_{OVLDDIS}$. If the high load at CQ still persists, the channel will be disabled again. This high current polling reduces the power dissipation of the chip and reduces the risk of overheating. The feature can be used in conjunction with the internal and external current sensing. Timing is configured in the OVLD register. It is also possible to disable this feature.

The short protection feature detects shorted or defective devices and disables their power supply, if NMOS transistors are used for power supply switching. If a high current is detected for a time > $t_{SHRTDET}$, the gate driver gets disabled, and the device is powered down. The gate driver stays disabled but can be switched on again manually by the user. The feature can only be used in conjunction with the external current sensing. Timing is configured in the SHRT register.

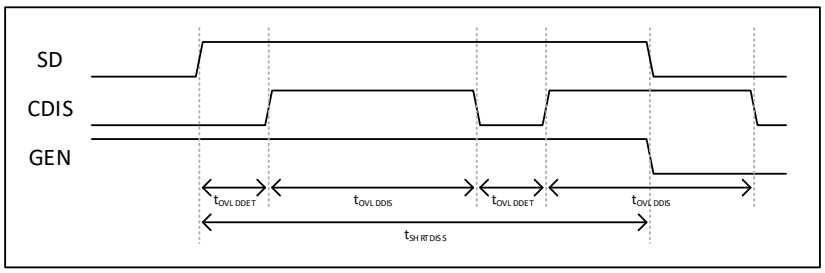


Figure 8: Overload/Short Protection Timing

The current state of the channel (CDIS) and the gate driver (GEN) is always reflected in the STAT register.

The IO-Link specification allows high currents while powering on a device. To avoid automatic disabling of the gate driver during power-on, $t_{SHRTDET}$ should be configured > 50 ms. Time can be reduced again after the power-on phase.

References: OVLD1/2 (0x21/0x41), SHRT1/2 (0x22/0x42), STAT (0x60)

5.5.2. Voltage / Temperature Monitoring

The chip is equipped with a voltage monitor that observes the VCC supply voltage of the chip and a temperature monitor which observes the die temperature. By default, the chip is configured to automatically disable all channels if the die temperature is too high or the VCC supply voltage is out of range.

The monitor states can be read back from the PROT register. The automatic protection feature is also controlled via the PROT register.

References: Monitoring Thresholds, PROT (0x63)

5.6 Additional IO-Link Features

5.6.1. Automated Wake-Up

Before starting the automated wake-up procedure, the following configuration needs to be applied:

- SIO mode selected in the MODE register (default value)
- Output driver enabled (DRV = 11 in the SIO register, default value)
- If external gate driver is used: enable external gate driver (GEN = 1 in the CFG register)
- SYNC and CRC bit of the FHC register configured with default values

Writing a one to the WURQ bit in the SIO register will then start the automated wake-up procedure. If the procedure is active, the WURQ bit is set to one and can be aborted by writing a one to the WURQ bit.

During the procedure, the chip is set into frame Handler mode and runs the wake-up procedure which complies to the IO-Link standard (IO-Link Spec v1.1, 7.3.2.2). After the procedure is finished, an interrupt is triggered and the chip stays in IO-Link mode. If a timeout is indicated, the procedure failed. Otherwise, the chip is configured, and the detected COM mode can be read back using the Mode register.

References: MODE1/2 (0x20/0x40), SIO1/2 (0x23/0x43), FHC1/2 (0x25/0x45), CFG1/2 (0x2F/0x4F)

5.6.2. Cycle Timer

A cycle timer is available for channels configured as frame handler in master mode. It enables the user to comply with the configured IO-Link cycle times without further effort. The cycle time is set up in the CYCT register. The format of this register resembles the defined structure in the IO-Link.

It is possible to configure cycle times that are shorter than 400 µs. Although this is not recommended, since the standard states 400 µs as minimum cycle time (IO-Link Spec v1.1, A.3.7). If the register is zero, the cycle timer gets disabled.

When the cycle timer is active, a new master message transaction will not start until the configured cycle time has passed. If the cycle time is over and no new data is available to start the message transaction, the EOC bit in the MISO Status Nibble will indicate the end of a cycle.

It is possible to reset the frame handler without resetting the cycle timer by triggering a soft reset, using the SKIP bit in the FHC register. The cycle timer will be reset together with the frame handler when a hard reset is triggered using the RST bit in the FHC register (see 5.3.3.4 Skip and Reset Function).

References: CYCT1/2 (0x29/0x49), MISO Status Nibble, FHC1/2 (0x25/0x45)

5.6.3. Channel Synchronization

The CCE4510 provides a synchronization feature that can be enabled by the SYNC bit in the FHC register. If enabled, TXD (SYNC) and RXD (CYCT) pins are used for synchronization purposes and do not have their default behavior in frame handler mode.

The CYCT pins indicate if the cycle time has passed with a high level. It is also possible to enable the cycle time interrupt for a channel over the CYCT bit in the IMSK register. If this interrupt is enabled the TOUT bit in the MISO Status Nibble is also used to indicate the end of a cycle.

The channels will wait for start of transmission until a configured cycle time has passed, the output buffer is filled, and the SYNC pin is toggled or a synchronization request is triggered over the SYNC register. These requests can be broadcasted to different chips, specifically triggering different channels on each chip by using the SMSK register. This gives a fine granularity for synchronizing channels, even over multiple chips.

For the best possible accuracy, it is highly recommended to control the synchronization via the dedicated pins.

Chip	MODE1/2	FHC1/2	CYCT1/2	SMSK
IC1	0h0A / 0h0A	0h0E / 0h0E	0h14 / 0h00	0h09
IC2	0h0A / 0h0A	0h0E / 0h0E	0h14 / 0h00	0h09
IC3	0h0A / 0h0A	0h0E / 0h06	0h00 / 0h00	0h04

As an example, we have three CCE4510 chips with the configurations from seen as in the table above. If we broadcast a synchronization request via SPI by writing a one to the ST1 bit in the SYNC register, channel 1 from IC1 and IC2 will start their transaction as soon as the configured cycle time has passed. If we write a one to the ST2 bit of the sync register, channel 2 of IC1 and IC2 and channel 1 of IC3 will start their transaction immediately.

References: SMSK (0x61), SYNC (0x62), Pin Descriptions

5.6.4. LED Drivers

The chip integrates a LED driver for each of the two channels. The LEDs are controlled by the LSEQ and LHLD registers. There are various ways of influencing the timing of a blinking sequence. It is also possible to synchronize the LED blinking sequences over each channel or various chips. This is done by writing one to the SYNC registers PRE and LED bits. The user can choose between two driver strengths of 5 mA or 10 mA using the ILED bit in the CFG register.

As an example, writing LSEQ 0hCC and LHLD 0h80 will resemble the specified blinking sequence for channels that operate in IO-Link mode, starting with the “LED off” state (IO-Link Spec v1.1, 10.9.3).

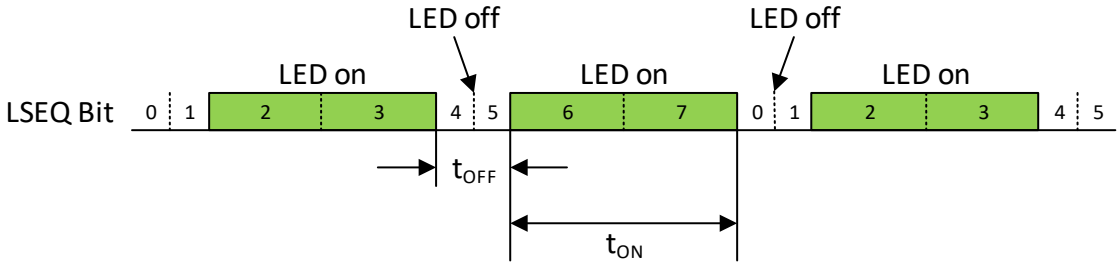


Figure 9: IO-Link LED Timing

$$t_{HLDL} = 50\ ms + 50\ ms * HLDL = 50\ ms$$

$$t_{OFF} = 2 * t_{HLDL} = 100\ ms$$

$$t_{HLDH} = 50\ ms + 50\ ms * HLDH = 450\ ms$$

$$t_{ON} = 2 * t_{HLDH} = 900\ ms$$

References: FHC1/2 (0x25/0x45), LSEQ1/2 (0x2D/0x4D), LHLD1/2 (0x2E/0x4E), SYNC (0x62)

5.7 Serial Peripheral Interface

5.7.1. Transaction Format

The CCE4510 is configured as SPI slave and uses the CPOL=0, CPHA=0 configuration. During each transaction, a minimum number of two bytes must be transferred. For bulk access to the frame handler buffers via the FHD1/2 registers, n bytes can be transferred. The first byte after a falling SSX edge always reflects the current state of the two channels. The format depends on the configured modes.

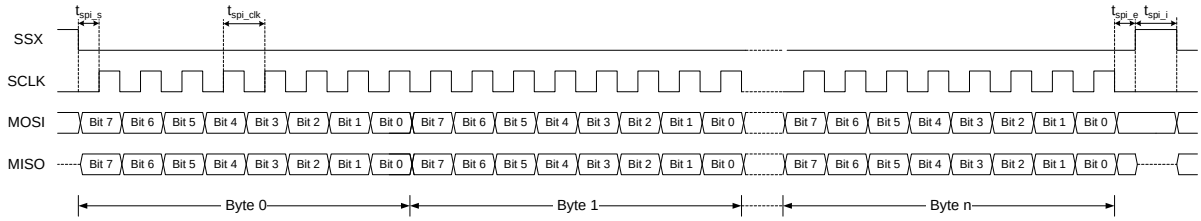


Figure 10: SPI Timing Diagram

5.7.2. MOSI Format

Bit	7	6	5	4	3	2	1	0
1st Byte	ADR							R/W
2nd Byte	DATA							
	…							
nth Byte	DATA							

ADR **Address for register access**

0x20-0x3F	Channel 1 registers
0x40-0x5F	Channel 2 registers
0x60-0x7F	Control registers

RW **Register access type**

0b0	write to address
0b1	read from address

DATA **Value for write access**

0x00-0xFF	3rd -nth byte is optional; ignored on read access

5.7.3. MISO Format

Table 1: MISO Format

Bit	7	6	5	4	3	2	1	0
1st Byte	STAT2				STAT1			
2nd Byte	DATA							
	…							
nth Byte	DATA							

STAT1/2 **Status code for channel 1/2**

0x0-0xF	Format is dependent on configured mode

DATA **Current value on read access to register**

0x00-0xFF	3rd -nth byte is optional; not valid on write access

5.7.4. MISO Status Nibble

Table 2: MISO Status Nibble

Name	STAT Bit 3	STAT Bit 2	STAT Bit 1	STAT Bit 0
Standard I/O	WURQ	RXD	TXEN	TXD
UART	OFLW	RXERR	RXRDY	TXRDY
Frame Handler	TOUT/EOC	STATE		

TXD **Current channel output value**

0b0	Channel is driven high
0b1	Channel is driven low

TXEN **Current output enable state**

0b0	Channel driver is disable
0b1	Channel driver is enabled

RXD **Current channel input value**

0b0	Channel input is driven high
0b1	Channel input is driven low

WURQ **Wake-up pulse indicator**

0b0	No wake-up pulse is detected
0b1	Wake-up pulse is detected

TXRDY **UART transmit state indicator**

0b0	TX is busy
0b1	TX us ready for transmission

RXRDY **UART receive state indicator**

0b0	RX is busy
0b1	RX is ready for receiving

RXERR **UART RX parity error**

0b0	no parity error detected
0b1	parity error detected

OFLW **UART RX overflow indicator**

0b0	no data overflow detected
0b1	data overflow is detected, byte is lost

STATE **Reflects the current frame handler state**

0b000	Idle
0b001	transmission output required
0b010	transmission active; no further output required
0b011	transmission active; further output required
0b100	receiving active
0b101	receiving active; new input available
0b110	receiving active; message erroneous
0b111	receiving active; message erroneous; new input available

TOUT/EOC **Frame timeout / End of cycle time**

0b0	no timeout detected / cycle time not passed
0b1	timeout detected / cycle time passed

5.8 Register Description

5.8.1. Register Overview

Address	Name	Description	Access
0x00-0x1F	-	reserved	-
0x20	MODE1	Channel 1 – Mode	R/W
0x21	OVLD1	Channel 1 – Overload Protection	R/W
0x22	SHRT1	Channel 1 – Short Protection	R/W
0x23	SIO1	Channel 1 – SIO Control	R/W
0x24	UART1	Channel 1 – UART Data	R/W
0x25	FHC1	Channel 1 – FH Control	R/W
0x26	OD1	Channel 1 – On-Request Length	R/W
0x27	MPD1	Channel 1 – Master PD Length	R/W
0x28	DPD1	Channel 1 – Device PD Length	R/W
0x29	CYCT1	Channel 1 – Cycle Time	R/W
0x2A	FHD1	Channel 1 – FH Data	R/W
0x2B	BLVL1	Channel 1 – FH Buffer Level	R
0x2C	IMSK1	Channel 1 – Interrupt Masking	R/W
0x2D	LSEQ1	Channel 1 – LED Sequence	R/W
0x2E	LHLD1	Channel 1 – LED Hold Times	R/W
0x2F	CFG1	Channel 1 – Configuration	R/W
0x30	TRSH1	Channel 1 – Threshold Level	R/W
0x31-0x3F	-	reserved	-
0x40	MODE2	Channel 2 – Mode	R/W
0x41	OVLD2	Channel 2 – Overload Protection	R/W
0x42	SHRT2	Channel 2 – Short Protection	R/W
0x43	SIO2	Channel 2 – SIO Control	R/W
0x44	UART2	Channel 2 – UART Data	R/W
0x45	FHC2	Channel 2 – FH Control	R/W

Address	Name	Description	Access
0x46	OD2	Channel 2 – On-Request Length	R/W
0x47	MPDL2	Channel 2 – Master PD Length	R/W
0x48	DPDL2	Channel 2 – Device PD Length	R/W
0x49	CYCT2	Channel 2 – Cycle Time	R/W
0x4A	FHD2	Channel 2 – FH Data	R/W
0x4B	BLVL2	Channel 2 – FH Buffer Level	R
0x4C	IMSK2	Channel 2 – Interrupt Masking	R/W
0x4D	LSEQ2	Channel 2 – LED Sequence	R/W
0x4E	LHLD2	Channel 2 – LED Hold Times	R/W
0x4F	CFG2	Channel 2 – Configuration	R/W
0x50	TRSH2	Channel 2 – Threshold Level	R/W
0x51-0x5F	-	reserved	-
0x60	STAT	IC Status	R
0x61	SMSK	Channel Synchronization Masks	R/W
0x62	SYNC	Synchronization Triggers	W
0x63	PROT	Channel Protection	R/W
0x64	INT	Interrupt Register	R/W
0x65-0x6F	-	reserved	-
0x70	REV	Revision Code	R
0x71-0x7F	-	reserved	-

5.8.2. MODE1/2 (0x20/0x40)

Bit	7	6	5	4	3	2	1	0
Name	Reserved				COM		MODE	
Access	-				R/W		R/W	

Default: 0b00000000

MODE **Selects the channel operation mode**

0b00 Standard I/O
0b01 UART
0b10 Frame Handler
0b11 reserved

COM **Selects the UART communication speed**

0b00 Disabled
0b01 COM1 – 4.8 kBd
0b10 COM2 – 38.4 kBd
0b11 COM3 – 230.4 kBd

5.8.3. OVLD1/2 (0x21/0x41)

Bit	7	6	5	4	3	2	1	0
Name	ADIS		MULT					
Access	R/W		R/W					

Default: 0b10000000

ADIS **Channel overload protection mode**

0b00 Disabled
0b01 Enabled; FACTOR = 10
0b10 Enabled; FACTOR = 100
0b11 Enabled; FACTOR = 1000

MULT **Multiplier for overload detection/disable time**

0-63 Multiplier value

NOTE disabling this feature may cause damage to master and/or device

$t_{OVLDDET}$ = 100 µs + 100 µs * MULT

$t_{OVLDDIS}$ = $t_{OVLDDET}$ * FACTOR

5.8.4. SHRT1/2 (0x22/0x42)

Bit	7	6	5	4	3	2	1	0
Name	BASE		MULT					
Access	R/W		R/W					

Default: 0b00000101

BASE **Base/offset for channel short detection time**

0b00	BASE is 100 µs; OFFSET is 100 µs; disabled if MULT is 0
0b01	BASE is 400 µs; OFFSET is 6.8 ms
0b10	BASE is 1.6 ms; OFFSET is 33.6 ms
0b11	BASE is 3.2 ms; OFFSET is 134.4 ms

MULT **Multiplier for short detection time**

0-63	Multiplier value

NOTE disabling this feature may cause damage to master and/or device

$t_{SHRTDET}$ = OFFSET + BASE * MULT

5.8.5. SIO1/2 (0x23/0x43)

Bit	7	6	5	4	3	2	1	0
Name	WURQ	Reserved			DRV		TXEN	TXD
Access	R/W	-			R/W		R/W	R/W

Default: 0b00001100

TXD **Driver output value**

0b0	Drive CQ high
0b1	Drive CQ low

TXEN **Driver output state**

0b0	Disable output driver
0b1	Enable output driver

DRV **Driver output mode**

0b00	Multiplier value
0b01	N-Mode
0b10	P-Mode
0b11	Push-Pull

WURQ **Start/abort automated wake-up procedure**

0b0	Automated wake-up is not running; writing 0b1 starts procedure
0b1	Automated wake-up is running; writing 0b1 aborts procedure

5.8.6. UART1/2 (0x24/0x44)

Bit	7	6	5	4	3	2	1	0
Name	DATA							
Access	R/W							

Default: 0b00000000

DATA **Received/transmitted value over UART**

0-255 read returns received value, write transmits value

5.8.7. FHC1/2 (0x25/0x45)

Bit	7	6	5	4	3	2	1	0
Name	RST	SKIP	Reserved		SYNC	MAS	CRC	TOUT
Access	W	W	-		R/W	R/W	R/W	R/W

Default: 0b00000110

TOUT **Timeout behavior**

0b0 strict timeout detection
0b1 relaxed timeout detection (+ 3 tBIT)

CRC **Automatic checksum calculation**

0b0 disabled, sending a master message will start immediately
0b1 enabled

MAS **Frame handler mode**

0b0 slave mode
0b1 master mode

SYNC **Channel synchronization**

0b0 disabled
0b1 enabled; master mode only

SKIP **Skip a frame**

0b1 resets frame handler without resetting cycle time counter

RST **Reset frame handler**

0b1 resets frame handler and cycle time counter

NOTE when writing a "1" to the RST or SKIP bit, all other bits of the SPI frame will be ignored.

5.8.8. OD1/2 (0x26/0x46)

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							

Default: 0b00000001

LEN **On-Request Data length**

1-32 data length in bytes; valid values according to IO-Link spec: 1, 2, 8, 32

5.8.9. MPD1/2 (0x27/0x47)

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							

Default: 0b00000000

LEN **Master Process Data length**

0-32 data length in bytes

5.8.10. DPD1/2 (0x28/0x48)

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							

Default: 0b00000000

LEN **Device Process Data length**

0-32 data length in bytes

5.8.11. CYCT1/2 (0x29/0x49)

Bit	7	6	5	4	3	2	1	0
Name	BASE		MULT					
Access	R/W		R/W					

Default: 0b00000000

BASE **Base/offset for cycle time**

0b00 BASE is 100 µs; no OFFSET; disabled if MULT is 0
0b01 BASE is 400 µs; OFFSET is 6.4 ms
0b10 BASE is 1.6 ms; OFFSET is 32 ms
0b11 reserved

MULT **Multiplier for cycle time**

0-63 Multiplier value

t_{CYC} = OFFSET + BASE * MULT

5.8.12. FHD1/2 (0x2A/0x4A)

Bit	7	6	5	4	3	2	1	0
Name	DATA							
Access	R/W							

Default: 0b00000000

DATA **Received/transmitted value over frame handler**

0-255 read returns buffed input data, write buffers output data

5.8.13. BLVL1/2 (0x2B/0x4B)

Bit	7	6	5	4	3	2	1	0
Name	FCNT							
Access	R/W							

Default: 0b00000000

FCNT **Fill count of frame handler input buffer**

0-66 current input buffer fill count

5.8.14. IMSK1/2 (0x2C/0x4C)

Bit	7	6	5	4	3	2	1	0
Name	Reserved			SD	SOR	SOT	CYCT	LVL
Access	-			R/W	R/W	R/W	R/W	R/W

Default: 0b00011111

LVL **Level interrupt**

0b0 enabled; interrupt trigger level is defined in corresponding TRSH registers
0b1 disabled; no interrupt is triggered

CYCT **Cycle time interrupt**

0b0 enabled; interrupt is triggered after end of cycle, only in master mode
0b1 disabled; no interrupt is triggered

SOT **Start of transmission interrupt**

0b0 enabled; interrupt is triggered on start of transmission
0b1 disabled; no interrupt is triggered

SOR **Start of reception interrupt**

0b0 enabled; interrupt is triggered on start of reception
0b1 disabled; no interrupt is triggered

SD **Short detection interrupt**

0b0 enabled; interrupt is directly triggered when a short gets detected
0b1 disabled; no interrupt is triggered

5.8.15. LSEQ1/2 (0x2D/0x4D)

Bit	7	6	5	4	3	2	1	0
Name	SEQ							
Access	R/W							

Default: 0b00000000

SEQ **LED blinking sequence**

0x00	always off
0x01-0xFE	blinking; 0b0 represents off-state; 0b1 represents on-state; LSB processed first
0xFF	always on

5.8.16. LHLD1/2 (0x2E/0x4E)

Bit	7	6	5	4	3	2	1	0
Name	HLDH				HLDL			
Access	R/W				R/W			

Default: 0b00000000

HLDL **LED hold time configuration for off-state**

0-15 Base time multiplier

HLDH **LED hold time configuration for on-state**

0-15 Base time multiplier

t_{HLDL} = 50 ms + 50 ms * HLDL
t_{HLDH} = 50 ms + 50 ms * HLDH

5.8.17. CFG1/2 (0x2F/0x4F)

Bit	7	6	5	4	3	2	1	0
Name	GEN	Reserved			ILED	SDINT	RAT	ICQ
Access	R/W	-			R/W	R/W	R/W	R/W

Default: 0b00000000

ICQ **Current sink configuration for C/Q**

0b0	current sink disabled
0b1	10 mA current sink enabled

RAT **Input threshold configuration for C/Q**

0b0	static input threshold according to IO-Link specification
0b1	ratiometric input threshold for lower LP voltages

SDINT **Short detection mode**

0b0	external short detection; shunt required
0b1	internal short detection; no shunt required

ILED **LED driving current**

0b0	5 mA driving current
0b1	10 mA driving current

GEN **Gate driver enable**

0b0	disabled
0b1	enabled

5.8.18. TRSH1/2 (0x30/0x50)

Bit	7	6	5	4	3	2	1	0
Name	TLVL							
Access	R/W							

Default: 0b00000000

TLVL **Input buffer threshold level**

0-63 trigger interrupt after TLVL received characters; activate in IMSK register

5.8.19. STAT (0x60)

Bit	7	6	5	4	3	2	1	0
Name	TEMP	VCCOK	GDIS2	CDIS2	SD2	GDIS1	CDIS1	SD1
Access	R	R	R	R	R	R	R	R

Default: 0b01100100

SD1/2 **Short detected indicator**

0b0 no short detected
0b1 short detected

CDIS1/2 **Channel disabled indicator**

0b0 channel driver enabled
0b1 channel driver disabled

GDIS1/2 **Gate disabled indicator**

0b0 gate driver enabled
0b1 gate driver disabled

VCCOK **VCC Voltage monitor**

0b0 voltage too high/low
0b1 voltage inside valid range; (VCC_{OK_MIN} < VCC) or (VCC > VCC_{OK_MAX})

TEMP **Temperature monitor**

0b0 temperature okay; $\vartheta_{JUNC} \leq \vartheta_{INT}$
0b1 high temperature detected; $\vartheta_{JUNC} > \vartheta_{INT}$

5.8.20. SMSK (0x61)

Bit	7	6	5	4	3	2	1	0
Name	SC4		SC3		SC2		SC1	
Access	R/W		R/W		R/W		R/W	

Default: 0b00000000

SC1-4 **Synchronization masks 1-4**

0b00 disable synchronization signals
0b01 enable synchronization signal for channel 1
0b10 enable synchronization signal for channel 2
0b11 enable synchronization signals for channels 1 and 2

5.8.21. SYNC (0x62)

Bit	7	6	5	4	3	2	1	0
Name	Reserved		PRE	LED	ST4	ST3	ST2	ST1
Access	-		W	W	W	W	W	W

Default: 0b00000000

ST1-4 **Synchronous start of transmission trigger**

0b1 write 0b1 to trigger start of transmission; depends on corresponding SC1-4 mask

LED **LED output synchronization**

0b1 write 0b1 to trigger synchronization

PRE **LED prescaler synchronization**

0b1 write 0b1 to trigger synchronization

5.8.22. PROT (0x63)

Bit	7	6	5	4	3	2	1	0
Name	Reserved	TEMP	VCCH	VCCL	Reserved	PTEMP	PVCCH	PVCCL
Access	-	R	R	R	-	R/W	R/W	R/W

Default: 0b00000111

PVCCL **VCC low voltage protection**

0b0 protection disabled
0b1 protection enabled; disable outputs driver if VCC < VCC_{OK_MIN}

PVCCH **VCC high voltage protection**

0b0 protection disabled
0b1 protection enabled; disable outputs driver if VCC > VCC_{OK_MAX}

PTEMP **High temperature protection**

0b0 protection disabled
0b1 protection enabled; disable output driver if $\vartheta_{JUNC} > \vartheta_{INT}$

VCCL **VCC low voltage monitor**

0b0 voltage not too low
0b1 voltage too low; VCC < VCC_{OK_MIN}

VCCH **VCC high voltage monitor**

0b0 voltage not too high
0b1 voltage too high; VCC > VCC_{OK_MAX}

TEMP **Temperature monitor**

0b0 temperature okay; $\vartheta_{JUNC} \leq \vartheta_{INT}$
0b1 high temperature detected; $\vartheta_{JUNC} > \vartheta_{INT}$

5.8.23. INT (0x64)

Bit	7	6	5	4	3	2	1	0
Name	IMODE	Reserved				ISTAT	ICH2	ICH1
Access	R/W	-				R/W	R/W	R/W

Default: 0b00000000

ICH1/2 **Channel 1/2 interrupt**

0b0 no channel 1/2 interrupt
0b1 channel 1/2 interrupt occurred; write 0b1 to clear

ISTAT **Status interrupt**

0b0 no status interrupt
0b1 status interrupt occurred; write 0b1 to clear

IMODE **Interrupt mode**

0b0 interrupt mode 1
0b1 alternative interrupt mode 2

5.8.24. REV (0x70)

Bit	7	6	5	4	3	2	1	0
Name	MAJ				MIN			
Access	R				R			

Default: 0b00010011

MAJ **Major revision code**

1 latest major revision code

MIN **Minor revision code**

3 latest minor revision code

6. Application Notes

6.1 Gate Drivers / External Sense

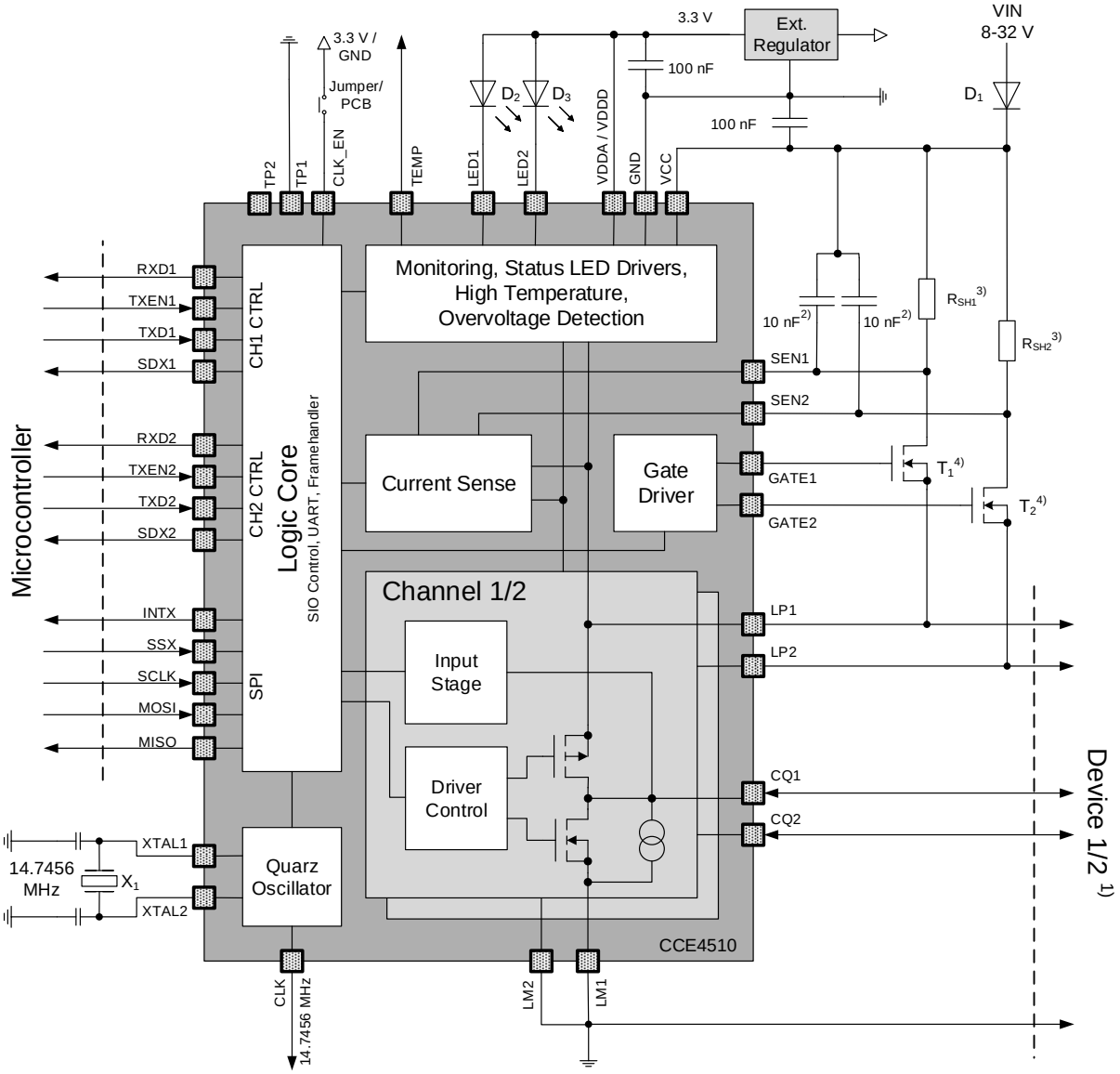


Figure 11: Gate Drivers / External Sense

1) Surge protection circuitry for channels needs to be applied externally

2) Optional

3) Typically 0.5 Ω

4) e.g. PMGD780SN, PHT6N06T

6.2 No Gate Drivers / Internal Sense

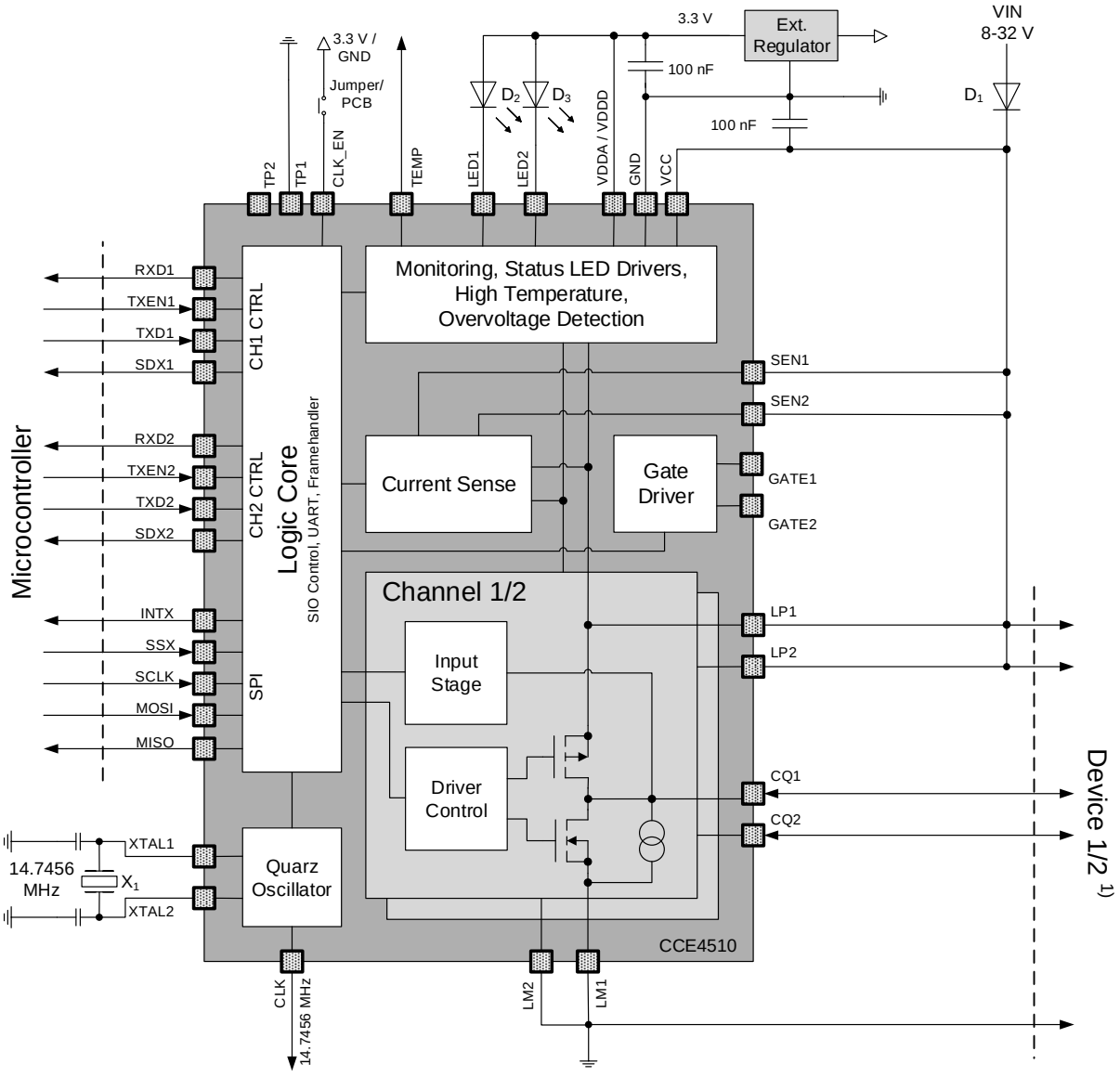


Figure 12: No Gate Drivers / Internal Sense

1) Surge protection circuitry for channels needs to be applied externally

7. Package Outline Drawings

7.1 QFN48 Package

Quad Flat No Lead Package; 48 Terminals; 7x7x0.85mm

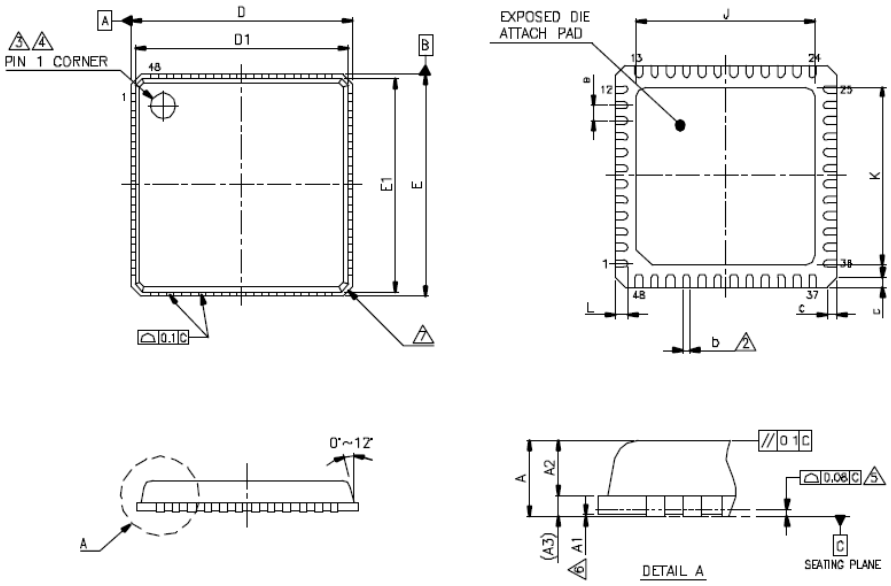


Figure 13: QFN48 Package

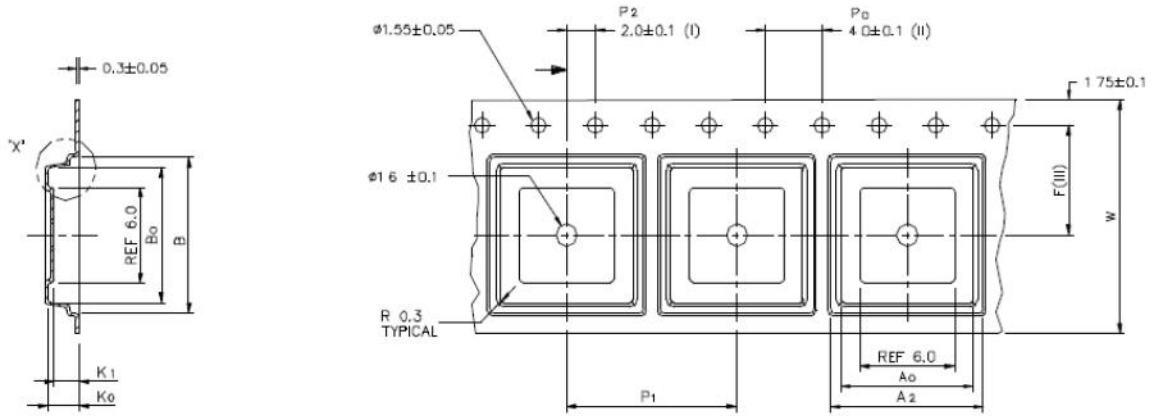
Symbol	A	A1	A2	A3	b	C	D	D1	E	E1	e	J	K	L
Min	0.80	0.00	0.65	0.203 REF.	0.18	0.24	7.00 BSC.	6.75 BSC.	7.00 BSC.	6.75 BSC.	0.50 BSC.	3.50	3.50	0.30
Typ	0.90	0.02	-		0.25	0.42						3.70	3.70	0.40
Max	1.00	0.05	1.00		0.30	0.60						3.90	3.90	0.50

UNIT : mm

NOTES ;
1. JEDEC : MO-220-J.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (0.012 INCHES MAXIMUM).
3. DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.2 AND 0.25mm FROM TERMINAL TIP.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
7. APPLIED ONLY TO TERMINALS.
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. Tape and Reel Information

8.1 Tape QFN48 Package

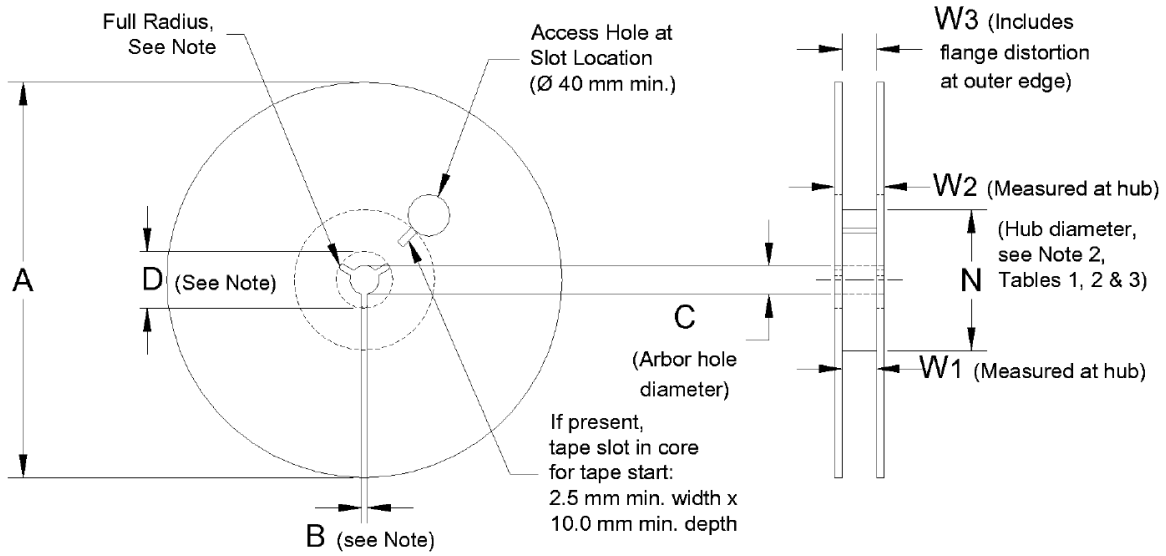


Ao	9.50 +/− 0.1
A2	10.80 +/− 0.1
Bo	9.50 +/− 0.1
B2	10.80 +/− 0.1
Ko	2.20 +/− 0.1
K1	1.70 +/− 0.1
F	7.50 +/− 0.1
P1	12.00 +/− 0.1
W	16.00 +/− 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

8.2 Reel Information



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Symbol	A	B	C	D	W_1 QFN48
Min	-	1.5	12.8	20.2	17.25
Typ	-	-	13.0	-	-
Max	330	-	13.5	-	17.75

UNIT: mm

9. Ordering Information

Please take the corresponding order number and consult your Renesas Electronics local sales representative.

Part	Order No.	Package	Delivery	Quantity
CCE4510	CCE4510 48QFN	QFN48 7 x 7 mm	Tape & Reel	3.000 parts per reel

Other packaging options are possible upon request.

10. Revision History

Revision	Date	Description
1.11	08-Apr-2024	Changed Features text on front page from “Two IO-Link compliant channels with 1 A peak driving current” to “Two IO-Link compliant channels with 1 A peak CQ driving current” Changed Features text on front page from “Includes NMOS gate drivers to switch power supply of devices” to “Includes NMOS gate drivers for ext. FETs controlling the power supply of devices with load currents of e.g. 2A (or higher)” Changed parameter name of I_{CQH}, I_{CQL}, I_{PEAKH} and I_{PEAKL} in IO-Link Channels Corrected typing error in Description of Pin 17 in 2.2 Pin Description
1.10	09-Aug-2023	Corrected BLVL1/2 (0x2B/0x4B) register description Corrected REV (0x70) binary default value
1.9	05-Dec-2022	Added Ψ_{JC_QFN48} and Ψ_{JC_QFN48} to General Parameters
1.8	09-Jun-2022	Added Power-up Sequence Added condition to VCC in General Parameters
1.7	24-Aug-2021	Removed all sections and information regarding QFN24 Fixed Skip and Reset Function description Fixed FHC1/2 register description (5.8.7) Fixed Automated Wake-up description Fixed Channel Synchronization description
1.6	22-Jul-2020	Updated Ordering Information
1.5	02-Jun-2020	Updated Template Added "(SIO)" to 1.1 Features Updated Pin Description Fixed and added information to FIT rate Fixed REV default value Fixed Overload/Short Protection description Fixed IO-Link Channels
1.4	31-Oct-2019	Updated Template
1.3	09-May-2016	Added/Updated Short Detection
1.2	28-July- 2014	Updated NMOS Gate Driver Parameters
1.1	22-July-2014	Updated General Description Updated Absolute Maximum Ratings Corrected PROT Register Description Changed Application Notes
1.0	17-Jun-2014	Initial version.

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Contact Information

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https://www.renesas.com/contact/