DA14592MOD

SmartBond Bluetooth® LE 5.2 Module

General Description

Based on DA14592 Bluetooth® low energy 5.2 system on chip (SoC), the DA14592 Module brings out all the DA14592 hardware features and capabilities. The module integrates all passives, antenna, and is supported by software that is easy to work with. The DA14592 Module targets broad market use and is certified across regions providing significant reductions in development cost and risks, and time-to-market.

The DA14592 is a multi-core wireless microcontroller, combining the latest Arm® Cortex® M33™ application processor with floating-point unit, advanced power management functionality, a cryptographic security engine, analog and digital peripherals, a software configurable protocol engine with a radio that is compliant to the Bluetooth® 5.2 Low Energy standard and 256 kB of embedded Flash accompanied by 96 kB of RAM.

The DA14592 is based on an Arm® Cortex®-M33 CPU with an 8-region MPU and a single-precision FPU offering up to 96 dMIPS at 64 MHz. The dedicated application processor executes code from RAM, embedded Flash or QSPI XiP Flash via an 8 kB 4-way associative cache controller. Bluetooth® 5.2 or other protocol connectivity is guaranteed by a software-configurable Bluetooth® Low Energy protocol engine (MAC) based on an Arm® Cortex®-M0+™ with an ultra-low-power radio transceiver, capable of +5.5 dBm output power and -97 dBm sensitivity offering a total link budget of 102.5 dB.

A variety of standard and advanced peripherals enable interaction with other system components.
and the development of advanced user interfaces and feature-rich applications.

Key Features

- Compatible with Bluetooth® 5.2, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)
- Flexible processing power
  - 32 kHz up to 64 MHz 32-bit Arm Cortex-M33™ with 8 kB, four-way associative cache and FPU
  - A flexible and configurable Bluetooth® LE MAC engine based on Arm Cortex-M0+™ with an 8 kB, four-way associative cache
- Memory
  - 256 kB embedded Flash
  - 96 kB Data SRAM with retention
  - 8 kB Caches with retention for Cortex M33 and M0+ respectively
  - 288 kB ROM (including boot ROM, PKI routines, and Bluetooth® LE stack)
- Power/Clock management
  - Buck DCDC converter
  - Operating range: from 1.7 V to 3.6 V
  - 32 MHz or 64 MHz system clock using a doubler
  - Fast wake-up from sleep in <15 µs
- Current Consumption
  - Hibernation <100 nA
  - 1.2 mA RX at V_{BAT} = 3 V
  - 2.3 mA TX at V_{BAT} = 3 V and 0 dBm
  - 3.5 µA at sleep with all RAM retained
- Peripherals and interfaces
  - Up to 32 General Purpose I/Os
  - Eight-channel 10-bit SAR ADC, 2 Msamples/s
  - ΣΔ ADC, 15 bits at 1 ksps, 13 bits at 16 ksps
  - QSPI PSRAM/Flash interface
  - 2 x UARTs up to 3 Mbps, one UART extended to support ISO7816
  - One SPI+™ and one I2C controller at 100 kHz, 400 kHz, or 3.4 MHz
  - PDM, PCM/I2S and dual SRC
  - 3-axis capable Quadrature Decoder
  - RTC with 10 ms resolution
  - Four General purpose, 24-bit up/down timers with PWM capabilities
  - Application cryptographic engine with AES-256 and SHA-256
- Radio transceiver
  - High Performance mode: TX output power -22 to +5.5 dBm, RX sensitivity -97 dBm
  - Low Power mode: TX output power -23 to 4.5 dBm, RX sensitivity -96 dBm
- Packaging
  - 18 mm x 14.5 mm x 2.5 mm package
- Module software Development Kit
  - SDK10 support

- Module software tools
  - Flash/OTP programmer
  - SUOTA support
  - Battery Life Estimation
  - Data Rate Monitoring
  - Real-Time Power Profiling
  - Production Line Testing
- Standards conformance
  - BT SIG QDID
  - Europe (CE/RED)
  - UK (UKCA)
  - US (FCC)
  - Canada (IC)
  - Japan (MIC)
  - South Korea (MSIP)
  - Taiwan (NCC)
  - South Africa (ICASA)
  - Brazil (ANATEL)
  - China (SRRC)
  - Thailand (NBTC)
  - India (WPC)

Applications

- Fitness trackers
- Sport watches
- Smartwatches
- Voice-controlled remote controls
- Toys
- Consumer appliances
- Home automation
- Industrial automation

Contents

Figures

Tables

1. Terms and Definitions

ADC	Analog-to-digital converter
DIO	Digital input-output
GND	Ground
I-PD	Input pulled down
I-PU	Input pulled up
MSL	Moisture sensitivity level
NTC	Negative temperature coefficient
PCB	Printed circuit board
PWR	Power
RDS	Reduced driving strength
VSWR	Voltage standing wave ratio

2. References

[1] DA14592, Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Module Variants

Table 1 presents the differentiation between the DA14592 Module variants.

Table 1: DA14592 module variants

Features	DA14592MOD-0100000	DA14592MOD-01F3200	DA14592MOD-01S1600
GPIOs	20	20	20
QSPI I/F	✓	✓	✓
On-board QSPI XiP Flash	×	✓	×
On-board QSPI PSRAM	×	×	✓
Package (mm)	18 x 14.5 x 2.5	18 x 14.5 x 2.5	18 x 14.5 x 2.5

4. Block Diagram

The DA14592 Module is based on the Renesas Electronics DA14592 SoC. With an on-board 32 MHz XTAL and a printed antenna, the module enables a faster time to market at reduced development costs.

4.1 DA14592MOD

The DA14592MOD-0100000 Module, as seen in Figure 1, consists of:

- 32 MHz XTAL
- Decoupling capacitors
- A power inductor
- A CLC filter and matching components for the printed antenna.

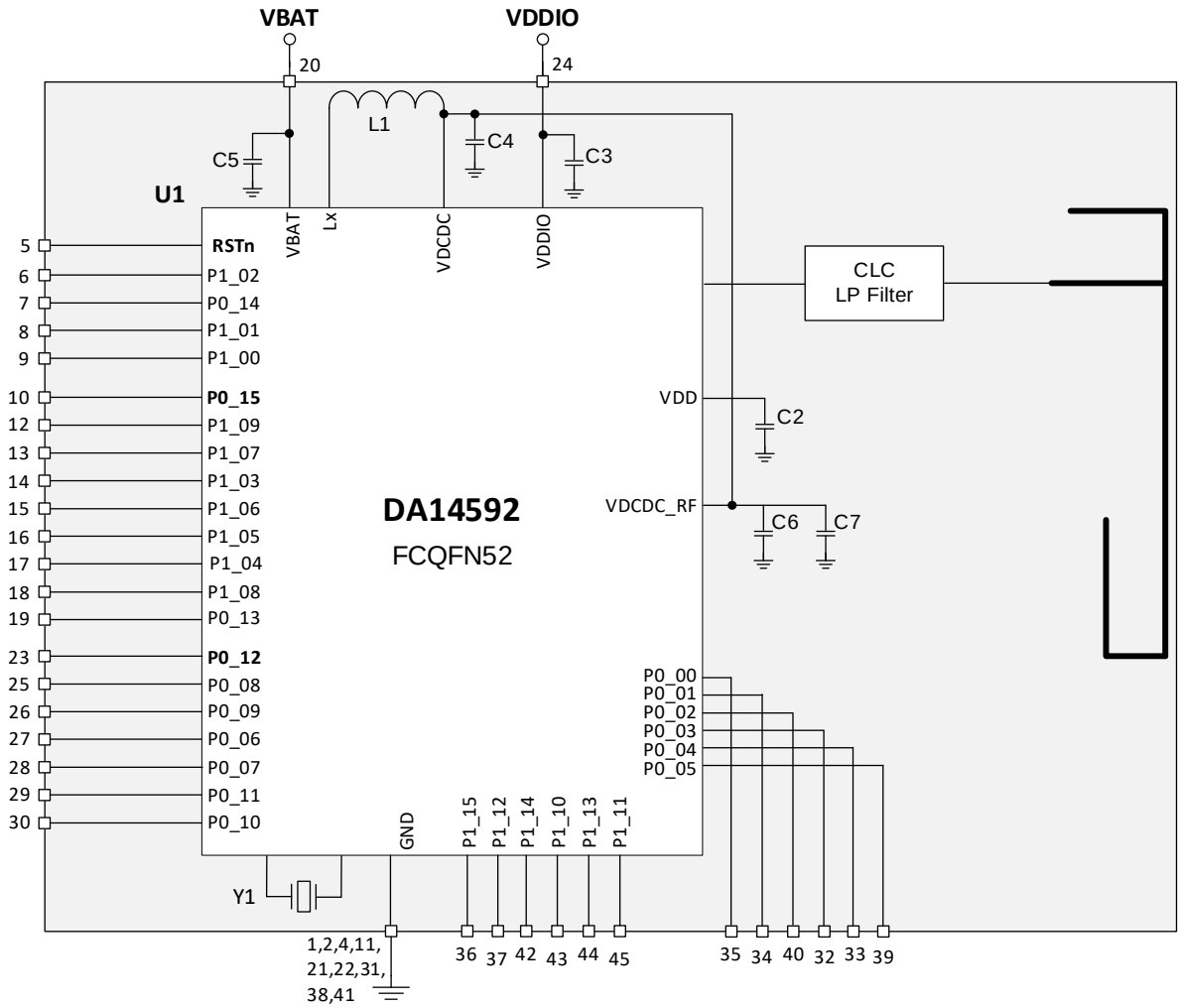


Figure 1. DA14592MOD-0100000 block diagram

4.2 DA14592MOD with On-board XiP Flash

The DA14592MOD-01F3200 Module, additionally to 0100000 variant, features also:

- An on-board 32Mbit QSPI XiP Flash.

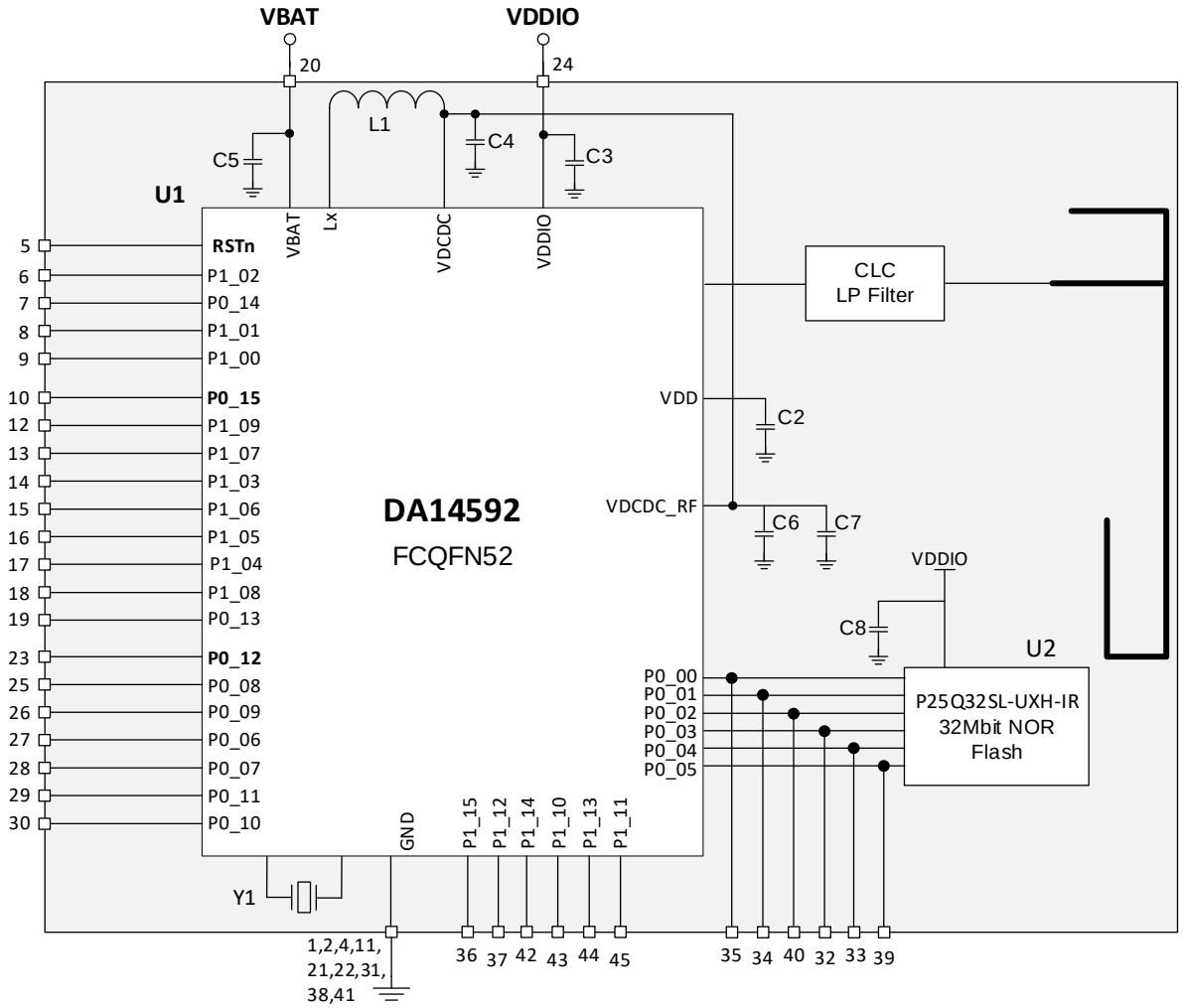


Figure 2. DA14592MOD-01F3200 block diagram

4.3 DA14592MOD with On-board PSRAM

The DA14592MOD-01S1600 Module, additionally to 0100000 variant, features also:

- An on-board 16Mbit PSRAM.

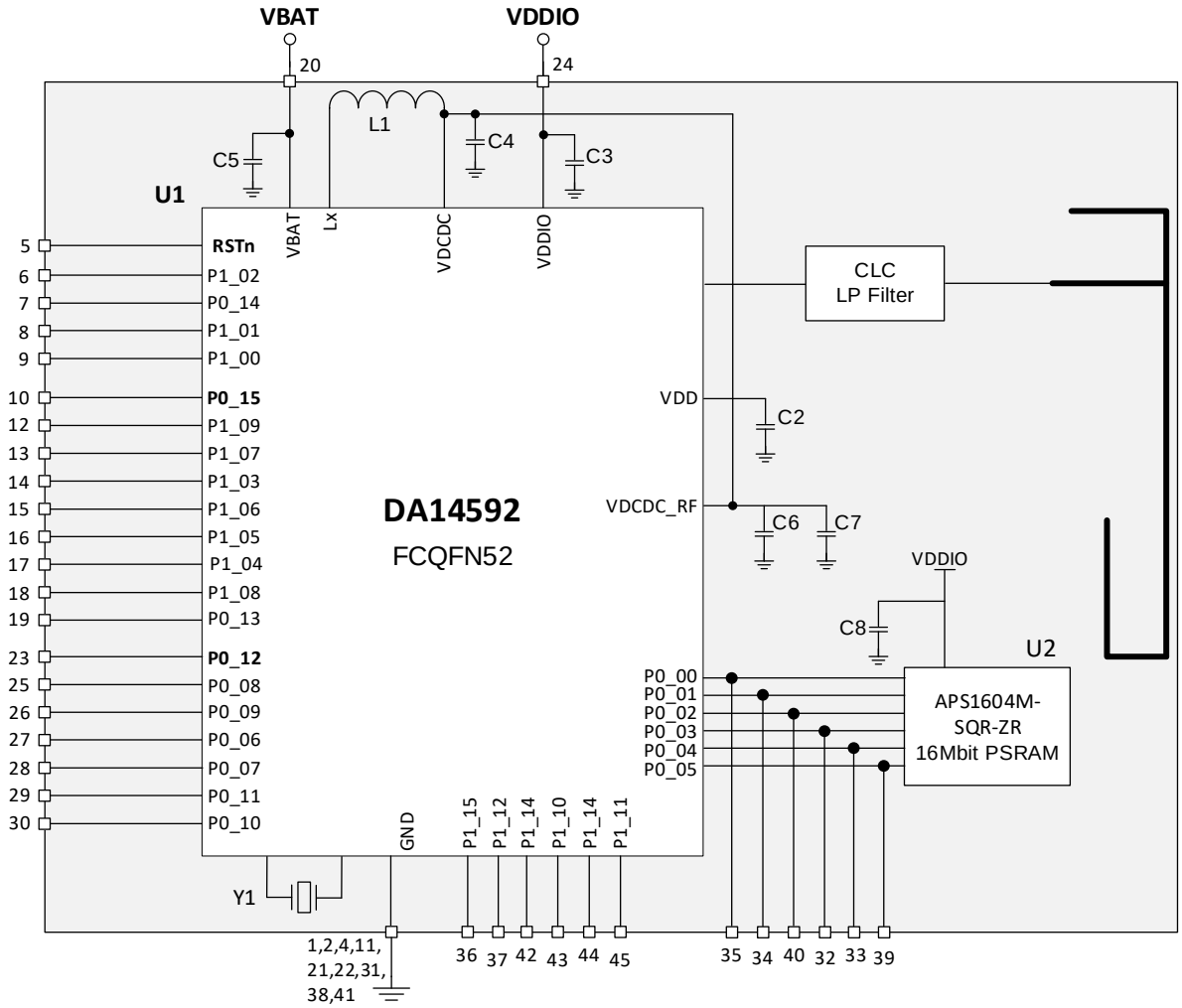


Figure 3. DA14592MOD-01S1600 block diagram

5. Pinout

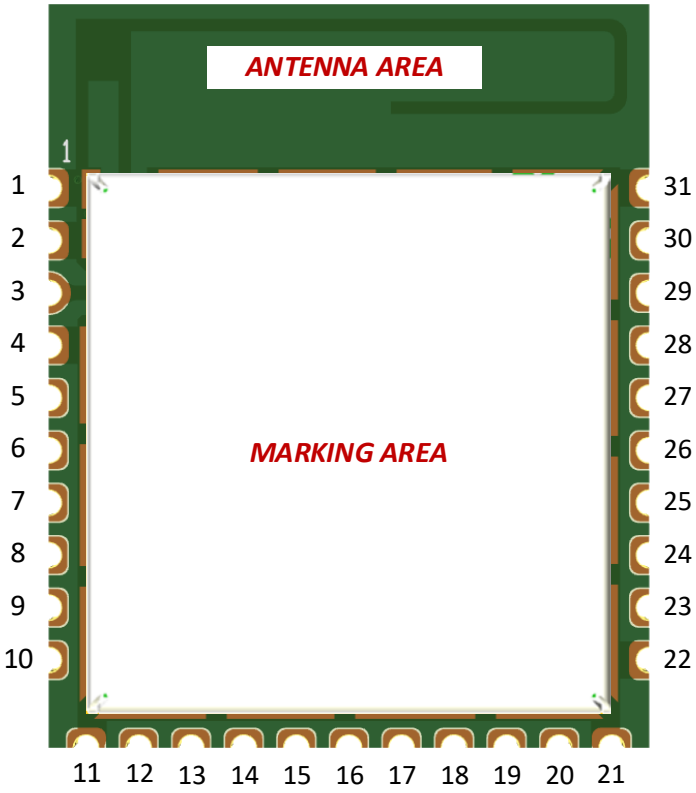


Figure 4. Pinout diagram – top view

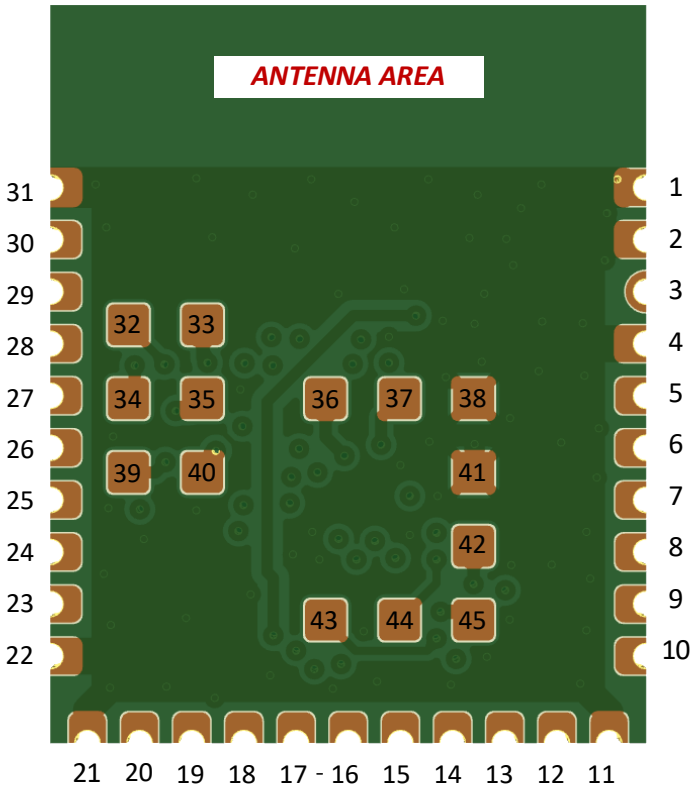


Figure 5. Pinout diagram – bottom view

Table 2: Edge pins description

Pin #	Pin Name	Type	Reset State	Description
1	GND	-		Ground.
2	GND	-		Ground.
3	Not Connected			Keep Floating.
4	GND	-		Ground.
5	RSTn	AI		INPUT. Reset signal (active LOW).
6	P1_02	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC_2	AI		INPUT. Analog input of the general-purpose ADC, channel 2.
	SDADC_2	AI		INPUT. Analog input of the SDADC, channel 2.
	RC32M	DO		OUTPUT. RC32M clock signal output (square wave).
7	P0_14	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	Hibernation Wake up 1	DI		INPUT. Wake up from hibernation mode source 1.
8	P1_01	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	PGA_INm	AI		INPUT. Programmable gain amplifier negative input.
	GPADC_1	AI		INPUT. Analog input of the general-purpose ADC, channel 1.
	SDADC_1	AI		INPUT. Analog input of the SDADC, channel 1.
9	P1_00	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	PGA_INp	AI		INPUT. Programmable gain amplifier positive input.
	GPADC_0	AI		INPUT. Analog input of the general-purpose ADC, channel 0.
	SDADC_0	AI		INPUT. Analog input of the SDADC, channel 0.
10	P0_15	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	UART Boot RX	DI		INPUT. UART Receive data input during boot.
11	GND	-		Ground.
12	P1_09	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC_6	AI		INPUT. Analog input of the general-purpose ADC, channel 6.
	SDADC_6	AI		INPUT. Analog input of the SDADC, channel 6.
13	P1_07	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
14	P1_03	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.

Pin #	Pin Name	Type	Reset State	Description
15	P1_06	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC_5	AI		INPUT. Analog input of the general-purpose ADC, channel 5.
	SDADC_5	AI		INPUT. Analog input of the SDADC, channel 5.
	SDADC_REFn	AI		INPUT. Analog input of the external SDADC negative.
16	P1_05	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC_4	AI		INPUT. Analog input of the general-purpose ADC, channel 4.
	SDADC_4	AI		INPUT. Analog input of the SDADC, channel 4.
	SDADC_REFp	AI		INPUT. Analog input of the external SDADC positive
	SDADC_INT_REF	AO		OUTPUT. Analog output of the internal SDADC voltage reference.
17	P1_04	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	Hibernation Wake Up 2	DI		INPUT. Wake up from hibernation mode source 2.
18	P1_08	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
19	P0_13	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	UART Boot TX	DO		OUTPUT. UART Transmit data output during boot.
20	VBAT	AI		INPUT. Battery connection.
21	GND	-		Ground.
22	GND	-		Ground.
23	P0_12	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Does not contain state retention mechanism during power down.
	LP_CLK	DO		OUTPUT. LP clock signal output (square wave), active during sleep.
	Timer.PWM	DO		OUTPUT. Timer/PWM output (PWM) in Sleep mode.
24	VDDIO	AIO		OUTPUT. 1.8 V power rail.
25	P0_08	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	CMAC_SWDIO	DIO		INPUT/OUTPUT. Arm Cortex-M0+ Serial Wire Debug data I/O signal.
	DIVN	DO		OUTPUT. DIVN clock signal output (square wave).
26	P0_09	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	CMAC_SWCLK	DI		INPUT. Arm Cortex-M0+ Serial Wire Debug clock signal.

Pin #	Pin Name	Type	Reset State	Description
27	P0_06	DIO	I-PU	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	M33_SWDIO	DIO		INPUT/OUTPUT. Arm Cortex-M33 Serial Wire Debug data I/O signal.
28	P0_07	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	M33_SWCLK	DI		INPUT. Arm Cortex-M33 Serial Wire Debug clock signal.
29	P0_11	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	XTAL32M	DO		OUTPUT. XTAL32M clock signal output (square wave).
30	P0_10	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	Timer2.PWM	DO		OUTPUT. Timer2/PWM output (PWM) in Sleep mode.
	GPADC_3	AI		INPUT. Analog input of the general-purpose ADC, channel 3.
	SDADC_3	AI		INPUT. Analog input of the SDADC, channel 3.
31	GND	-		Ground.
32	P0_03	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPI _D1	DIO		INPUT/OUTPUT. QSPI RAM/Flash Data line 1.
33	P0_04	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPI _D2	DIO		INPUT/OUTPUT. QSPI RAM/Flash Data line 2.
34	P0_01	DIO	I-PU	NPUT/OUTPUT with selectable pull-up/down resistor and open drain functionality. Pull-up enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPI_CS	DO		OUTPUT. QSPI RAM/Flash chip select.
35	P0_00	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPI_CLK	DO		OUTPUT. QSPI RAM/Flash clock.
36	P1_15	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
37	P1_12	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
38	GND	-		Ground.
39	P0_05	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after

Pin #	Pin Name	Type	Reset State	Description
				reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPI _D3	DIO		INPUT/OUTPUT. QSPI RAM/Flash Data line 3.
40	P0_02	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	QSPI _D0	DIO		INPUT/OUTPUT. QSPI RAM/Flash Data line 0.
41	GND	-		Ground.
42	P1_14	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	XTAL32kp	AI		INPUT. Analog input of the XTAL32k crystal oscillator.
		DI		INPUT. Digital input for an external clock (square wave).
43	P1_10	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
44	P1_13	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	XTAL32km	AO		OUTPUT. Analog output of the XTAL32k crystal oscillator.
45	P1_11	DIO	I-PD	INPUT/OUTPUT with selectable pull-up/down resistor and open-drain functionality. Pull-down enabled during and after reset. General-purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	GPADC_7	AI		INPUT. Analog input of the general-purpose ADC, channel 7.
	SDADC_7	AI		INPUT. Analog input of the SDADC, channel 7.

6. Characteristics

All MIN/MAX specification limits are guaranteed by design, production testing and/or statistical characterization. Typical values are based on characterization results at default measurement conditions and are informative only.

Default measurement conditions (unless otherwise specified): V_{BAT}= 3.0 V, T_A = 25°C. All radio measurements are done with standard RF measurement equipment.

6.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so the functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute maximum ratings

Parameter	Description	Conditions	Min	Max	Unit
$V_{PIN\_LIM\_DEF}$	Limiting voltage on any pin unless otherwise specified	Default, unless otherwise specified	-0.1	3.6	V
V_{BAT_LIM}	Limiting battery supply voltage	Pin V_{BAT}	0	3.6	V
$V_{PIN\_LIM\_3V0}$	Limiting voltage on a pin	3.0 V I/O pins	0	3.45	V
$V_{PIN\_LIM\_1V8}$	Limiting voltage on a pin	1.8 V I/O pins	0	1.98	V
T_{STG}	Storage temperature		-50	150	°C

6.2 Recommended Operating Conditions

Table 4: Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BAT}	Battery supply voltage	Pin V_{BAT}	1.7		3.6	V
V_{DDIO}	Pad supply voltage	Pin V_{DDIO}	1.65		3.6	V
V_{PIN_1V8}	Voltage on a pin	1.8 V I/O pins	0		1.8	V
V_{PIN_3V0}	Voltage on a pin	3.0 V I/O pins	0		3	V
$V_{PIN\_(1V2)}$	Voltage on a pin	XTAL32Kp, XTAL32Km, XTAL32Mp, XTAL32Mm	0		1.2	V
T_A	Ambient temperature		-40		85	°C

6.3 Electrical Characteristics

Table 5: DC characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{BAT_IDLE}	Battery supply current	CPU is idle (Wait for Interrupt - WFI); sys_clk = 32 MHz; pclk = 4 MHz; DCDC on; FLASH off; peripherals off; V_{BAT} = 3 V.		481		µA
$I_{BAT\_RUN\_32MHz\_RAM}$	Average active battery supply current	CPU is executing code from RAM; Cache bypassed; RC32M on; pclk = 4 MHz; DCDC on; Peripherals off; V_{BAT} = 3 V.		1.52		mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{BAT\_RUN\_64MHz\_RAM}$	Average active battery supply current	CPU is executing code from RAM; Cache bypassed; XTAL32M on; Doubler on; pclk = 8 MHz; DCDC on; Peripherals off; VBAT = 3 V.		4.78		mA
$I_{BAT\_RUN\_32MHz\_FLASH}$	Average active battery supply current	CPU is executing code from embedded FLASH; cache bypassed; RC32M on; pclk = 4 MHz; DCDC on; Peripherals off; V_{BAT} = 3 V.		1.16		mA
$I_{BAT\_RUN\_64MHz\_FLASH}$	Average active battery supply current	CPU is executing code from embedded FLASH; cache bypassed; XTAL32M on; Doubler on; pclk = 8 MHz; DCDC on; Peripherals off; VBAT = 3 V.		4.52		mA
I_{BAT_HIBERN}	Battery supply current	Hibernation mode; no RAM retained; all clocks off; DCDC off; V_{BAT} = 3 V.		100		nA
$I_{BAT\_DP\_SLP}$	Battery supply current	Deep Sleep mode; No RAM retained; RCX on; RTC on DCDC on; V_{BAT} = 3 V. Reset on wake-up		2		µA
$I_{BAT\_EX\_SLP\_32KB\_RET}$	Battery supply current	Extended Sleep mode; Both instruction caches retained. 32 kB (data) RAM retained; RCX on; DCDC on; RTC on; V_{DD} = 0.75 V; V_{BAT} = 3 V.		2.6		µA
$I_{BAT\_EX\_SLP\_64KB\_RET}$	Battery supply current	Extended Sleep mode; Both instruction caches retained. 64 kB (data) RAM retained; RCX on; DCDC on; RTC on; V_{DD} = 0.75 V; V_{BAT} = 3 V.		3		µA
$I_{BAT\_EX\_SLP\_96KB\_RET}$	Battery supply current	Extended Sleep mode; Both instruction caches retained. 96 kB (data) RAM retained; RCX on; DCDC on; RTC on; V_{DD} = 0.75 V; V_{BAT} = 3 V.		3.5		µA
$I_{BAT\_BLE\_RX\_32M}$	Battery supply current	Bluetooth LE receive in LP mode; f_{CLK} = 32 MHz; CPU idle; DCDC on; eFLASH on; V_{BAT} = 3 V.		2.67		mA
$I_{BAT\_BLE\_TX\_32M\_0dbm}$	Battery supply current	Bluetooth LE transmit mode in LP mode; TX output power 0dBm; f_{CLK} = 32 MHz; CPU idle; DCDC on; eFLASH on; V_{BAT} = 3 V.		4.33		mA
$I_{BAT\_BLE\_RX\_64M}$	Battery supply current	Bluetooth LE receive in HP mode; f_{CLK} = 64 MHz; CPU idle; DCDC on; eFLASH on; V_{BAT} = 3 V.		4.99		mA
$I_{BAT\_BLE\_TX\_64M\_0dbm}$	Battery supply current	Bluetooth LE transmit in HP mode; Tx output power 0 dBm; f_{CLK} = 64 MHz; CPU idle;		5.88		mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
		DCDC on; eFLASH on; V_{BAT} = 3 V.				
$I_{BAT\_BLE\_TX\_64M\_6dbm}$	Battery supply current	Bluetooth LE transmit in HP mode; TX output power 6 dBm; f_{CLK} = 64 MHz; CPU idle; DCDC on; eFLASH on; V_{BAT} = 3 V.		9.56		mA

Table 6: GPIO - Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage	V_{DD} = 0.9 V, V_{DDIO} = 1.8 V	0.63			V
V_{IL}	LOW level input voltage	V_{DD} = 0.9 V, V_{DDIO} = 1.8 V			0.27	V

Table 7: GPIO - DC characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH level input current	V_I=VDDIO = 3.0 V, T = 25		0.5		nA
I_{IL}	LOW level input current	V_I=VSSIO = 0 V, VDDIO = 3.0 V, T = 25		0.5		nA
I_{IH_PD}	HIGH level input current	V_I=VDDIO = 1.8 V	35		110	µA
I_{IL_PU}	LOW level input current	V_I=V_{SS} = 0 V, VDDIO = 1.8 V	-110		-35	µA
V_{OH}	HIGH level output voltage	I_O = 3.5 mA, VDDDIO = 1.8 V	1.44			V
V_{OL}	LOW level output voltage	I_O = 3.5 mA, VDDIO = 1.8 V			0.36	V
V_{OH_LOWDRV}	HIGH level output voltage	I_O = 0.35 mA, VDDIO = 1.8 V	1.44			V
V_{OL_LOWDRV}	LOW level output voltage	I_O = 0.35 mA, VDDIO = 1.8 V			0.36	V

Table 8: RCX - Timing characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$\Delta f_{RC}/\Delta T_{\_1}$	Frequency accuracy per ºC	0<T<60			150	ppm/deg
$\Delta f_{RC}/\Delta T_{\_2}$	Frequency accuracy per ºC	-40<T<115		100	250	ppm/deg
$\Delta f_{RC}/\Delta V_{\_VBAT}$	Supply voltage dependency	For V_{BAT}		50		ppm/V
$\Delta f_{RC}/\Delta V_{\_VDD}$	Supply voltage dependency	For V_{DD}		50		ppm/V
f_{RC}	RC oscillator frequency	At default trim setting	12	15	19	kHz

Table 9: XTAL32K - Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
Δf_{XTAL_32K}	Crystal frequency tolerance (including aging)	Timing accuracy is dominated by crystal accuracy. A much smaller value is preferred.	-250		250	ppm

Table 10: XTAL32M - Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{XTAL_32M}	Crystal oscillator frequency			32		MHz
Δf_{XTAL_32M}	Crystal frequency tolerance	After optional trimming; including aging and temperature drift	-20		20	ppm

Table 11: RADIO 1M LP - AC characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_CLEAN}	Sensitivity level	Dirty Transmitter disabled; DCDC converter disabled; PER = 30.8%; V_{DCDC_RF} = 1.1 V Note 1		-96		dBm
P_{SENS_EPKT}	Sensitivity level	Extended packet size (255 octets)		-93.5		dBm
P_{SENS}	Sensitivity level	Normal Operating Conditions; DCDC converter disabled; PER = 30.8% Note 1		-95		dBm
P_O	Output power level	PA_POWER_SETTING = 15		4		dBm

Note 1 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS/4.0.1, section 6.4.1.

Table 12: RADIO 1M HP - AC characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_CLEAN}	Sensitivity level	Dirty Transmitter disabled; DCDC converter disabled; PER = 30.8%; V_{DCDC_RF} = 1.4 V Note 1		-97		dBm
P_{SENS_EPKT}	Sensitivity level	Extended packet size (255 octets)		-94.5		dBm
P_{SENS}	Sensitivity level	Normal Operating Conditions; DCDC converter disabled; PER = 30.8% Note 1		-96		dBm
P_O	Output power level	PA_POWER_SETTING = 15		5.5		dBm

Note 1 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS/4.0.1, section 6.4.1.

Table 13: RADIO 2M LP - AC characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_CLEAN}	Sensitivity level	Dirty Transmitter disabled; DCDC converter disabled; PER = 30.8%; V_{DCDC_RF} = 1.1 V Note 1		-93		dBm

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_EPKT}	Sensitivity level	Extended packet size (255 octets)		-91		dBm
P_{SENS}	Sensitivity level	Normal Operating Conditions; DCDC converter disabled; PER = 30.8% Note 1		-93		dBm
P_O	Output power level	PA_POWER_SETTING = 15		4		dBm

Note 1 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS/4.0.1, section 6.4.1.

Table 14: RADIO 2M HP - AC characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_CLEAN}	Sensitivity level	Dirty Transmitter disabled; DCDC converter disabled; PER = 30.8%; V_{DCDC_RF} = 1.4 V Note 1		-94		dBm
P_{SENS_EPKT}	Sensitivity level	Extended packet size (255 octets)		-91.5		dBm
P_{SENS}	Sensitivity level	Normal Operating Conditions; DCDC converter disabled; PER = 30.8% Note 1		-93.5		dBm
P_O	Output power level	PA_POWER_SETTING = 15		5.5		dBm

Note 1 Measured according to Bluetooth® Low Energy Test Specification RF-PHY.TS/4.0.1, section 6.4.1.

7. Mechanical Specifications

7.1 Mechanical Dimensions and Land Pattern

The module's dimensions are accessible from the Renesas website – 45-Module.

7.2 Marking

The module's shield marking is shown in Figure 6.

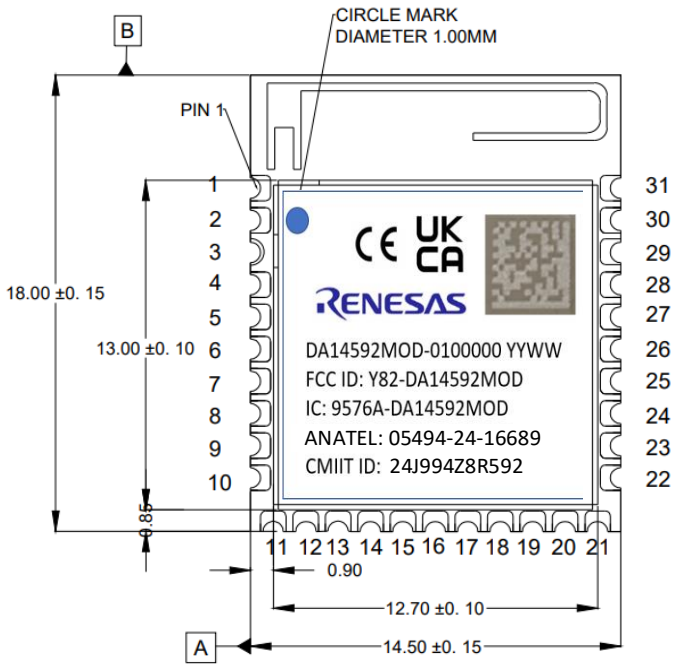


Figure 6. Module shield marking

Marking legend:

DA14592MOD-xxxxxxx yyww

xxxxxxx: module variant

yy: production year

ww: production week

All dimension in mm. Tolerance: 0.4 mm

8. BOM

Table 15: Bill of materials

#	Designator	Type	Value	Description	Manufacturer	MPN
1	U1	IC	DA14592-010006F2	Renesas DA14592 BLE 5.2 SoC with embedded Flash	Renesas Electronics	DA14592-010006F2
2	C2	Capacitor	4.7 µF	CAP CERAMIC 4.7 µF ±20% 6.3 V X5R 0402	Murata	GRM155R60J475ME47D
3	C3, C4, C6	Capacitor	10 µF	CAP CER. 10 µF ±20% 6.3 V X5R 0402	Murata	GRM155R60J106ME05D
4	C5	Capacitor	1.0 µF	CAP CER G.P. 1 µF 10V ±20% X6S 0201	Murata	GRM033C81A105ME05D
5	C7, C8	Capacitor	100 nF	CAP CERAMIC 0.1 µF ±10% 6.3 V X5R, 0201	Murata	GRM033R60J104KE19D
6	Z1, Z3	Capacitor	0.7 pF	CAP CERAMIC 0.7 pF ±0.05 pF 50 V C0G/NP0 0201	Murata	GJM0335C1HR70WB01D
7	Z2	Inductor	2.8 nH	INDUCTOR 2.8 nH Unshielded ±0.1 nH 450 mA 250 mΩ Max 0201	Murata Electronics	LQP03TG2N8B02D
8	R3, Z4	Capacitor	10 pF	CAP CER 10PF ±5% 50 V C0G/NP0 0201	Murata	GRM0335C1H100JA01D
9	L1	Inductor	2.2 µH	INDUCTOR POWER 2.2 µH ± 20% 1.7 A 140 mΩ 0806	Taiyo Yuden	LSANB2016KKT2R2M
10	Y1	Crystal	32.0000 MHz	CRYSTAL 32 MHz 2.0X1.6X0.65 MM XRCGB32M000F1S1AR0	Murata	XRCGB32M000F1SBAR0
11	U2	IC (Note 1)	P25Q32SL-UXH-IR	FLASH 32MBIT QSPI 104 MHz 8USON 3x2x0.55 mm	Puya Semiconductor	P25Q32SL-UXH-IR
12		IC (Note 2)	APS1604M-SQR-ZR	PSRAM 16MBIT QSPI 84 MHz 8USON 3x2x0.45 mm	AP Memory Technology	APS1604M-SQR-ZR

Note 1 Available only in DA14592MOD-01F3200.

Note 2 Available only in DA14592MOD-01S1600.

9. Design Guidelines

The DA14592MOD comes with an integrated PCB trace antenna. The antenna area is 14.5 x 3.95 mm. The antenna's Voltage Standing Wave Ratio (VSWR) and efficiency depend on the installation location.

The radiation performance of the PCB trace antenna depends on the host PCB layout. The maximum antenna gain is -0.4 dBi when installed on a 43x35 mm reference board, as shown in Figure 9. Antenna Radiation Efficiency is better than -3.7 dB for all mounting positions. The RF front end is optimized to achieve the maximum possible efficiency for various installation positions of the module on a host PCB. To obtain similar performance, follow the guidelines described in the following subsections.

9.1 Installation Location

For optimum performance, install the module at the edge of a host PCB with the antenna edge facing out. The module can be located on either of the outer corners or in the middle of the host PCB with equivalent performance.

The antenna should have 4.0 mm free space in all directions. Copper or laminate in the proximity of the PCB trace antenna will affect the efficiency of the antenna. Laminate or copper under the antenna should be avoided as it severely affects the performance of the antenna. The antenna keep-out area is shown in Figure 8.

Metals close to the antenna degrade the antenna's performance. The amount of degradation depends on the host system's characteristics. Table 16 summarizes the antenna efficiency at different installation locations on a host PCB as shown in Figure 7.

Table 16: Antenna efficiency vs DA14592MOD module positions

	Position # 1 (Left)	Position # 2 (Middle)	Position # 3 (Right)
Freq	**Antenna efficiency**	**Antenna efficiency**	**Antenna efficiency**
[MHz]	[dB]	[dB]	[dB]
2405	-2.2	-3.3	-3.7
2445	-2.8	-3.0	-3.1
2480	-3.3	-3.0	-3.2

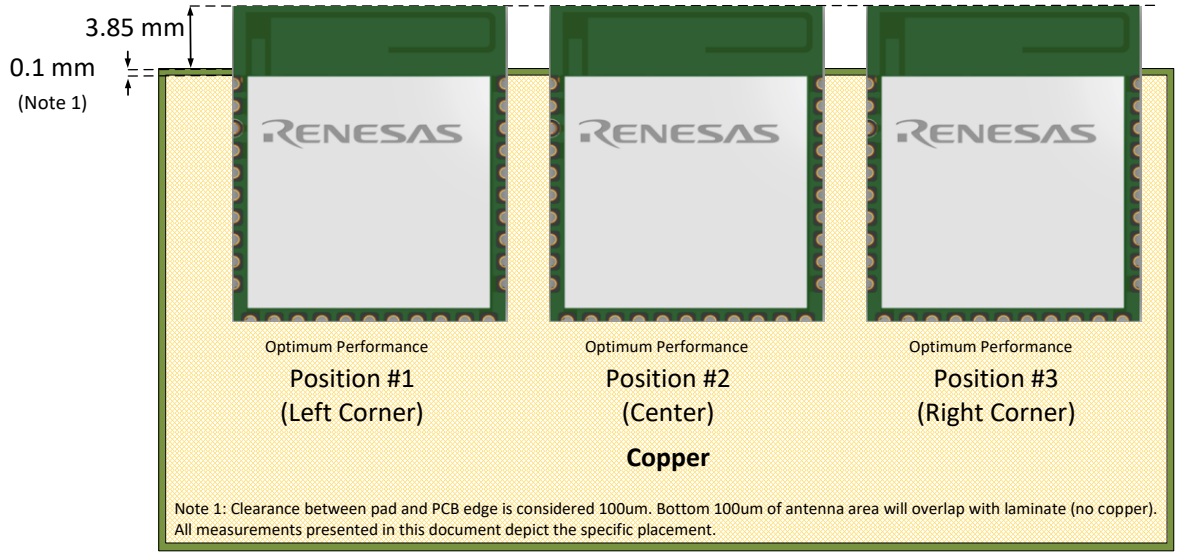


Figure 7. Installation locations for optimum antenna performance

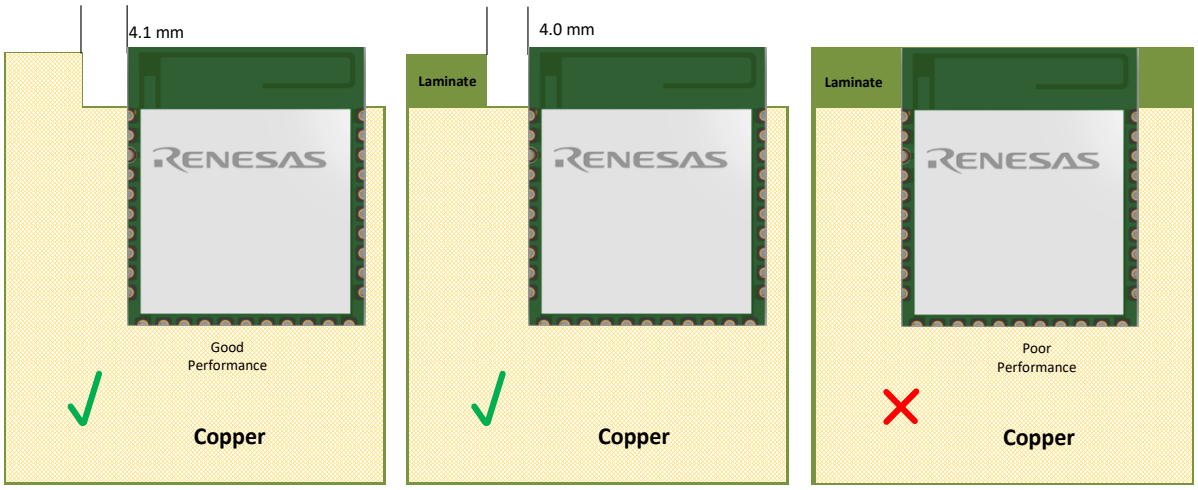


Figure 8. Antenna performance in proximity of copper (left), laminate (middle), and laminate under antenna (right)

The actual DA14592MOD module evaluation board layout that has been used to conduct measurements is shown in Figure 9.

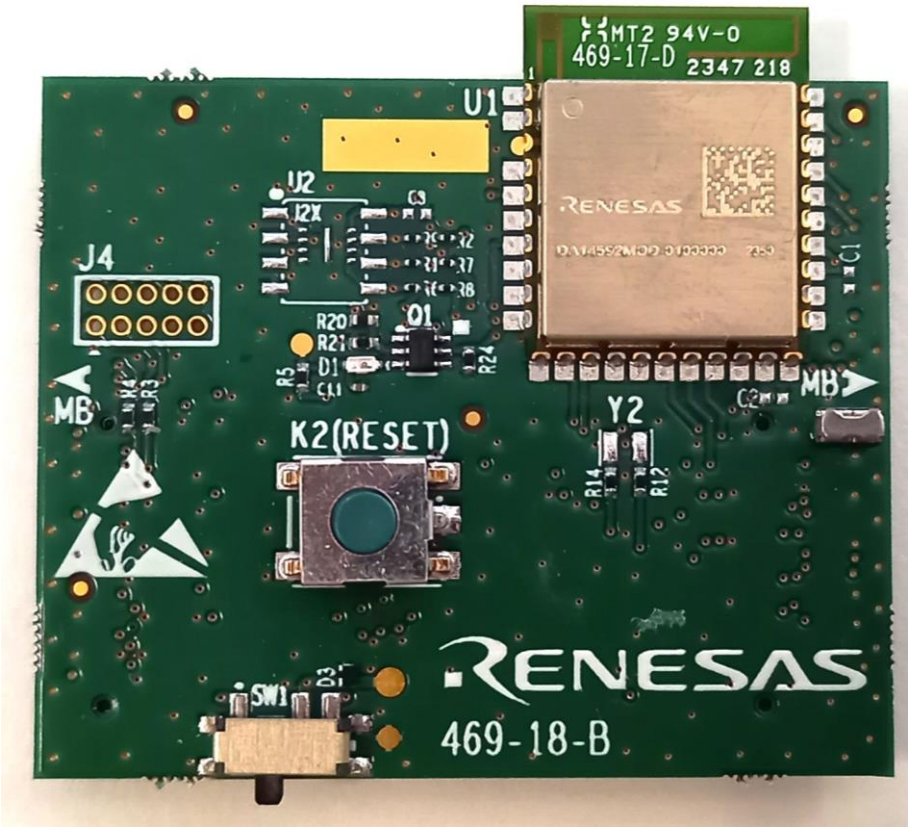


Figure 9. DA14592MOD module evaluation board

9.2 Antenna Graphs

The antenna Voltage Standing Wave Ratio measurements for the three installation positions are shown in Figure 10, Figure 11, and Figure 12.

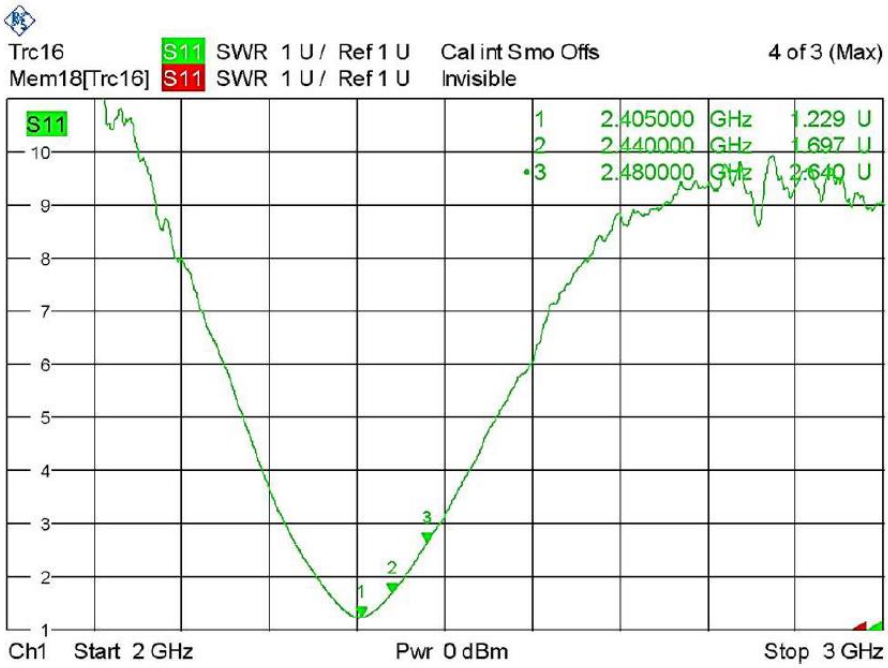


Figure 10. VSWR installed in the upper-left corner (position #1) of evaluation board

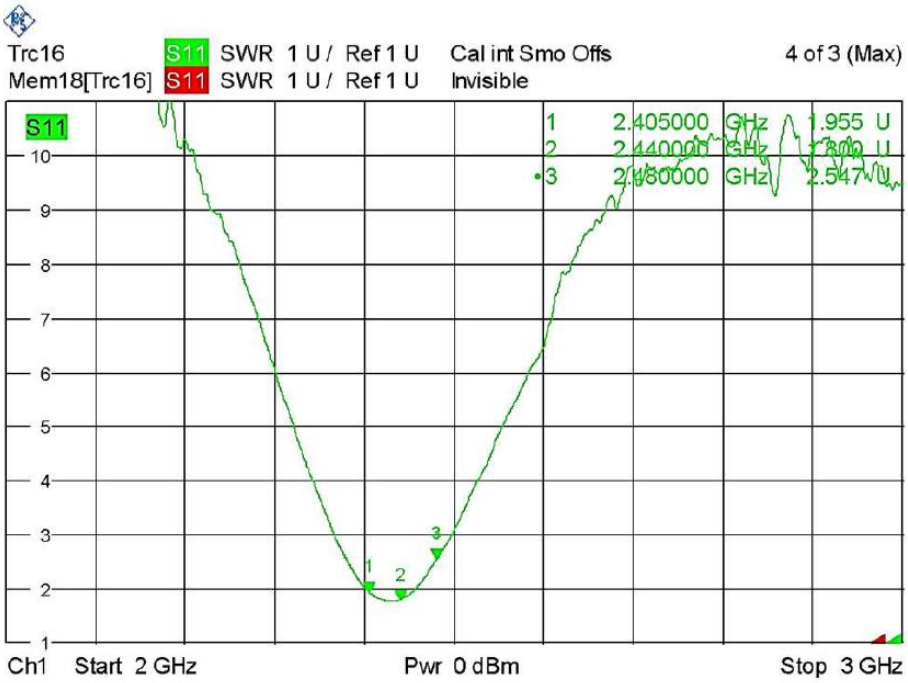


Figure 11. VSWR with module installed in center (position #2) of the evaluation board

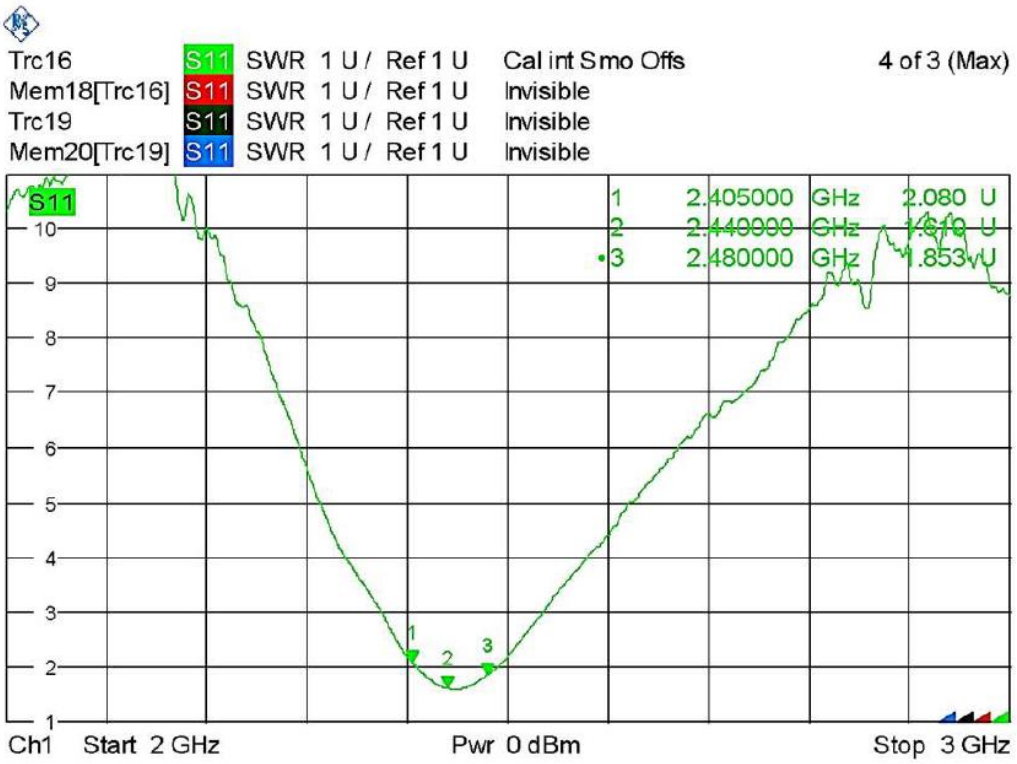


Figure 12. VSWR with module installed in the upper-right corner (position #3) of the evaluation board

9.3 Radiation Pattern

The antenna radiation pattern measurements are carried out in an anechoic chamber. Radiation patterns are presented for three measurement planes: XY, XZ, and YZ- planes with horizontal and vertical polarization of the receiving antenna.

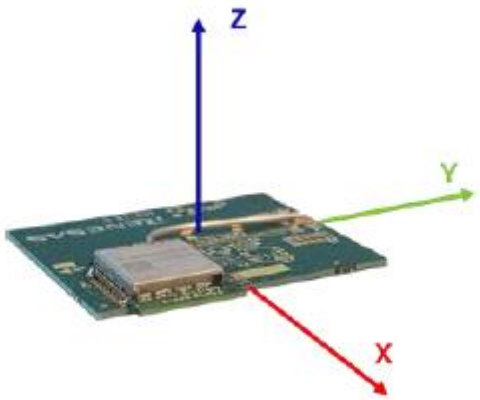


Figure 13. Measurement plane definition

Measurements are carried out for the module installed in the upper-right corner on the reference board with no laminate below the antenna trace.

XY plane XZ plane YZ plane

Figure 14. Board orientation at different planes

Horizontal polarization	Vertical polarization

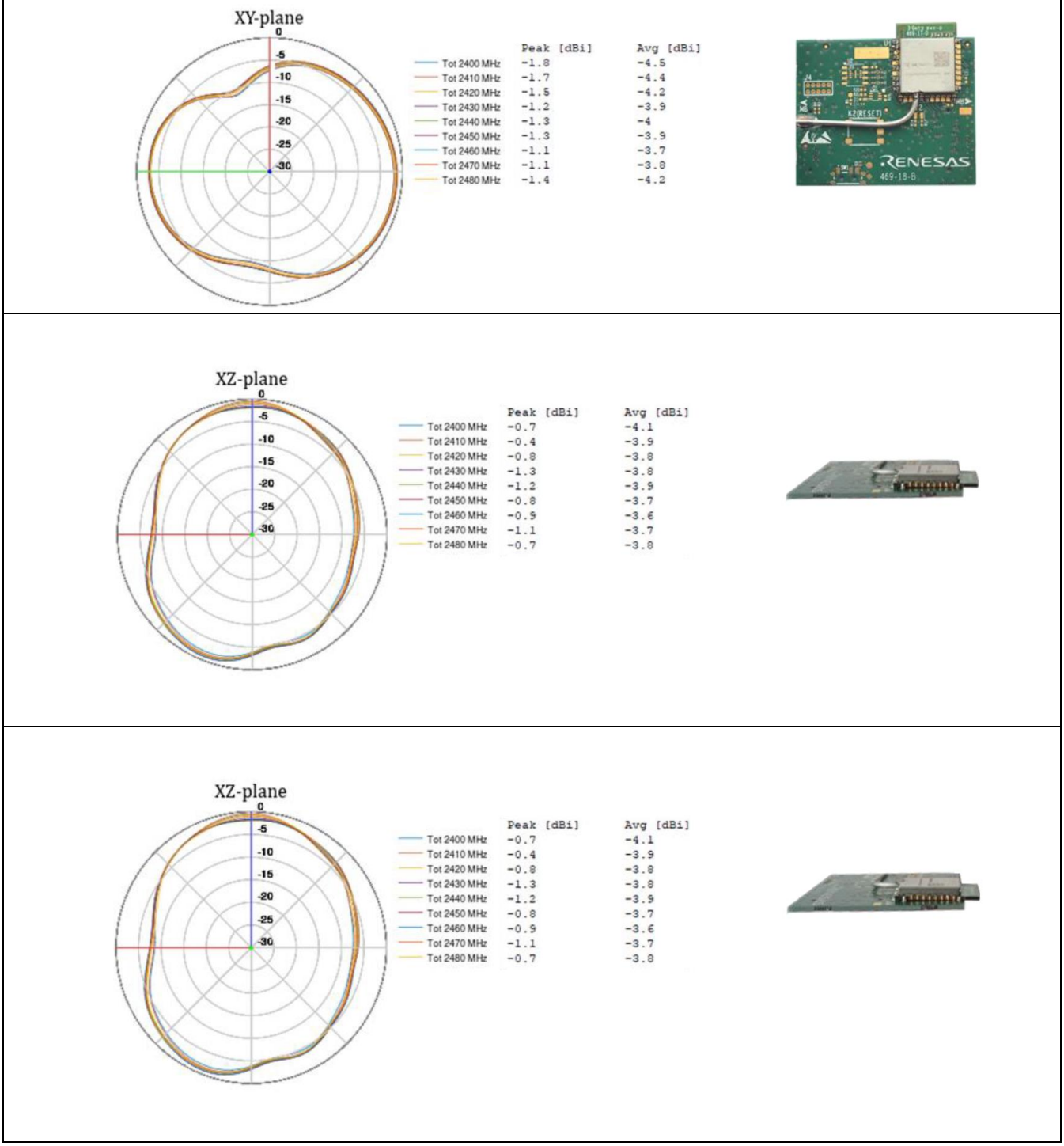


Figure 15. Radiation pattern for trace antenna

Table 17 summarizes the antenna peak gain for the module mounted on the right corner position of the evaluation board.

Table 17: Antenna peak gain for 2.4 GHz frequency band

Frequency band	XY-Plane	YZ-Plane	XZ-Plane
	Peak gain [dBi]	Peak gain [dBi]	Peak gain [dBi]
2.4 GHz	-1.1	-0.4	-0.4

10. Soldering

The successful reflow soldering of the DA14592 Module on a PCB depends on several parameters such as the thickness of the stencil, the pads solder paste aperture, the solder paste characteristics, the reflow soldering profile, the size of the PCB, and so on.

The volume of solder paste applied to the board is mainly determined by the aperture size and stencil thickness. An initial solder paste aperture for the pads is provided on the solder paste layer of the PCB footprint. This aperture is modified by the assembly process experts according to stencil thickness, solder paste, and available assembly equipment.

The solder profile depends on the solder paste type used. For example, the soldering profile of a lead-free solder paste, Sn3Ag0.5Cu with no clean Flux (ROL0) and Solder Powder Type 4, is shown in Figure 16.

No clean flux is recommended because washing must not be applied after assembly to avoid that moisture is trapped under the shield.

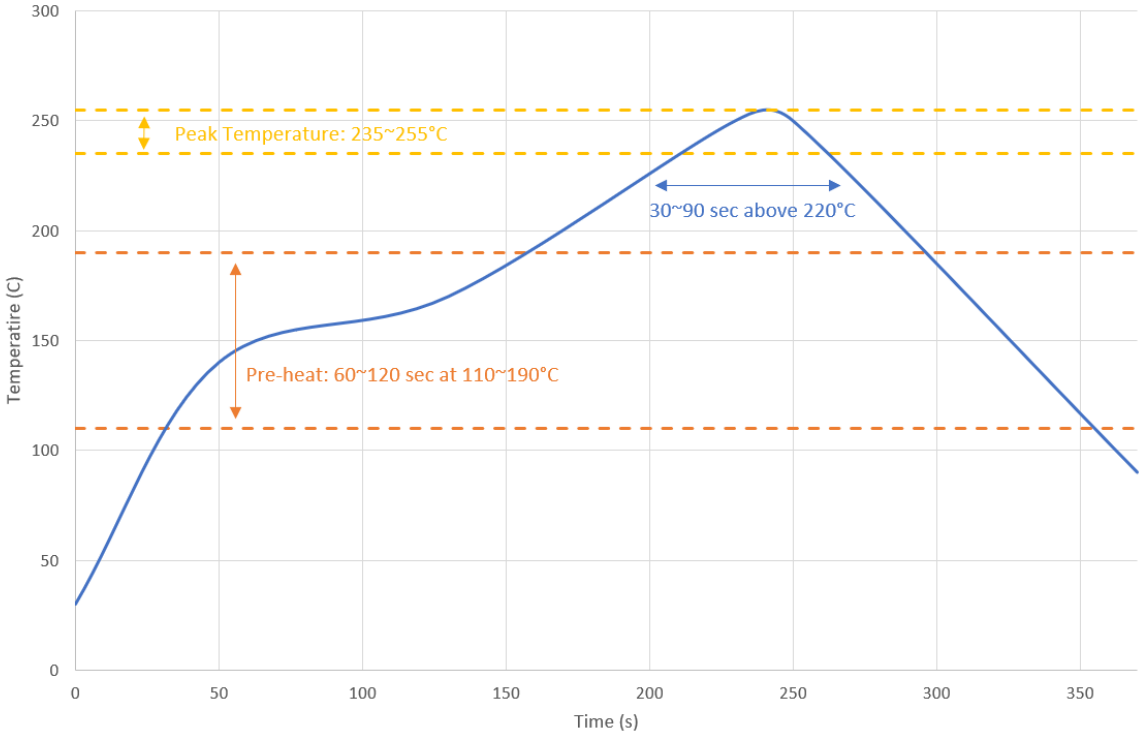


Figure 16. Recommended reflow profile for lead free solder

Table 18: Reflow profile specification

Statistic name	Low limit	High limit	Units
Slope1 (Target = 2.0) Between 30.0 and 70.0	1	3	Degrees/Second
Slope2 (Target = 2.0) Between 70.0 and 150.0	1	3	Degrees/Second
Slope3 (Target = -2.8) Between 220.0 and 150.0	-5	-0.5	Degrees/Second
Preheat time 110–190 °C	60	120	Seconds
Time above reflow at 220 °C	30	90	Seconds
Peak temperature	235	255	Degrees Celsius
Total time above at 235 °C	10	55	Second

Solderability reflow check of five cycles was performed, applying the procedures mentioned in JESD-A113E standard.

The MSL is an indicator for the maximum allowable time period (floor lifetime) in which a moisture-sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60% RH before the solder reflow process.

The DA14592 SmartBond™ Module is qualified for MSL 3.

Table 19: MSL level vs floor lifetime

MSL level	Floor lifetime
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30 °C/85% RH

11. Packaging Information

11.1 Tape and Reel

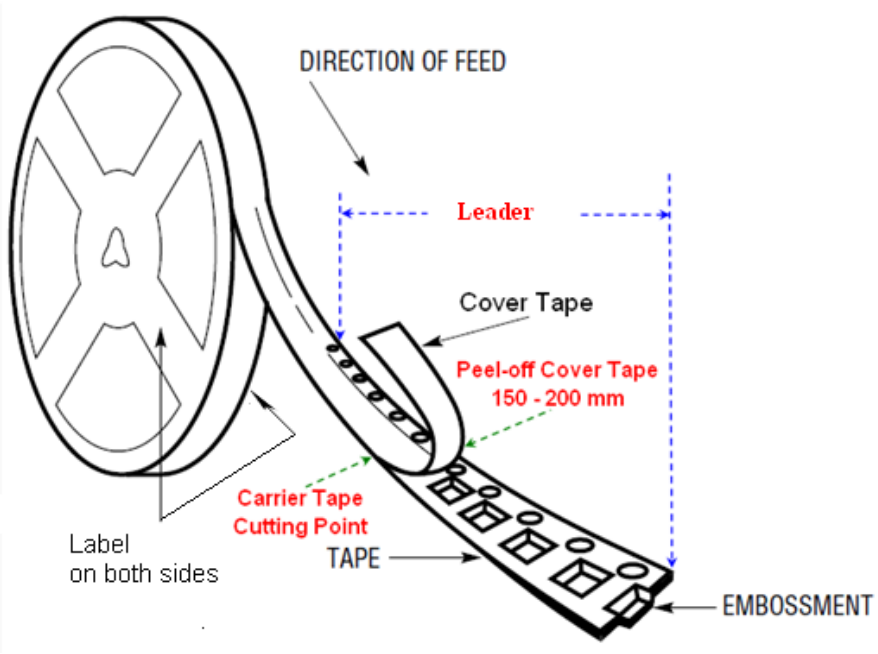


Figure 17. Tape and reel

The reel specifications are shown in Table 20.

Table 20: Reel specifications

Parameter	Value
Diameter	13 inches
Reel tape width	22 inches
Tape material	Static Dissipative Black Conductive Polystyrene Alloy
Qty/Reel	
Leader	400 mm + 10%
Trailer	160 mm + 10%
Round Sprocket Hole Diameter	1.50 ± 0.10 mm
Round Sprocket Hole Pitch	4.00 ± 0.10 mm

11.2 Labeling

On each reel, a set of labels are placed. The information label shows information regarding the batch number, date code, reel date and number, quantity, and part number as in Figure 18.

Figure 18. Reel part information label

The directives label shows information regarding directives conformity as in Figure 19, Figure 20, and Figure 21.

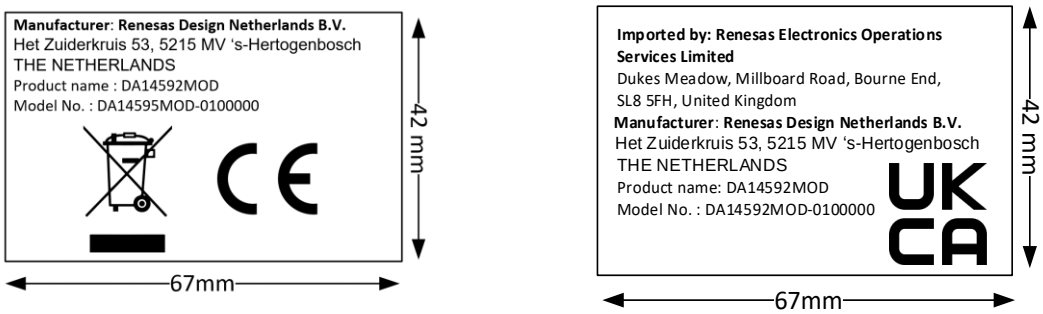


Figure 19. EU-UK directives conformity labels

Figure 20. ICASA conformity label

Figure 21. CMIIT ID label

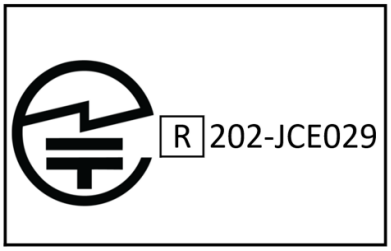


Figure 22. JAPAN GITEKI Mark Label

12. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, consult your Renesas Electronics Corporation local sales representative.

Table 21: Ordering information (samples)

Part number	Size (mm)	Shipment form	Pack quantity	MOQ
DA14592MOD-0100000C	18 x 14.5 x 2.5	Reel	100	1
DA14592MOD-01F3200C	18 x 14.5 x 2.5	Reel	Contact sales for availability	
DA14592MOD-01S1600C	18 x 14.5 x 2.5	Reel	Contact sales for availability	

Table 22: Ordering information (production)

Part number	Size (mm)	Shipment form	Pack quantity	MOQ
DA14592MOD-01000002	18 x 14.5 x 2.5	Reel	700	1
DA14592MOD-01F32002	18 x 14.5 x 2.5	Reel	Contact sales for availability	
DA14592MOD-01S16002	18 x 14.5 x 2.5	Reel	Contact sales for availability	

13. Regulatory Information

This section outlines the regulatory information for the DA14592 SmartBond™ Module. The module is certified for the global market. This facilitates the market entry of the end product. The end product would need to apply for the end product certification, however, the module certification listed below will facilitate that procedure.

When the user sends the end product to those markets, the end product may need to follow additional requirements according to the specific market regulation.

For example, some markets have additional testing and/or certification like Korea EMC, South Africa SABS EMC and some have the requirement to put on the end product label a modular approval ID or mark that consists of an approved Bluetooth® Low Energy modular ID on host label directly, like Japan, Taiwan, Brazil.

A list of the Conformance Standards that the DA14592 SmartBond™ Module meets is shown in Table 23.

Table 23: Standards conformance

Area	Item	Service	Standard	Certificate ID
Global	Safety for module	CB	IEC 62368-1	DE 2-042373 Note 1
Europe	Wireless	RED	EN 300 328 v2.2.2 EN 62479:2010	EU24-0098-01-TEC
	Safety for module	CE	IEC 62368-1	
	EMC	RED	EN 301 489-1 v2.2.3 Draft EN 301 489-17 v3.2.5	
UK	Wireless	UKCA-RED	EN 300 328 v2.2.2 EN 62479:2010	UK24-0018-01-TEC
	Safety for module	UKCA-LVD	IEC 62368-1	
	EMC	UKCA-RED	EN 301 489-1 V2.2.3 Draft EN 301 489-17 V3.2.5	
US/CA	Wireless	FCC ID	47 CFR PART 15 Subpart C: 2021 section 15.247	Y82-DA14592MOD
		IC ID	RSS-247 Issue 3: August 2023 RSS-Gen Issue 5: April 2018 +A1: March 2019+A2: February 2021	9576A-DA14592MOD
Japan	Wireless	MIC	JRL	R 202-JCE029
Taiwan	Wireless	NCC	LP0002	CCAH24Y10540T7
South Korea	Wireless	MSIP	방송통신표준 KS X 3123 "무선 설비 적합성 평가 시험 방법" KN 301 489	R-R-8DL- DA14592MOD100
South Africa	Wireless	ICASA	Based on RED	TA-2024/1068
Brazil	Wireless	Anatel	ATO No.14448/2017 Resolution No.680	05494-24-16689
China	Wireless	SRRC	信部无【2002】353	24J994Z8R592
Thailand	Wireless	NBTC	NBTC TS 1035-2562	SD01917-24
India	Wireless	WPC	Based on RED	ETA-SD-20240504443

Note 1 Include national differences of **EU Group Differences, IT, JP, US, CA, AU, NZ**

13.1 CE (Radio Equipment Directive 2014/53/EU (RED)) – (Europe)

Model no. DA14592MOD-0100000

Model no. DA14592MOD-01F3200

Model no. DA14592MOD-01S1600

The DA14592 SmartBond™ Module is a Radio Equipment Directive (RED) assessed radio that is CE marked. The module has been manufactured and tested with the intention of being a subassembly to a final product. The module has been tested to RED 2014/53/EU Essential Requirements for Health, Safety, and Radio.
The applicable standards are:

- **Radio: EN 300 328 V2.2.2 (2019-07)**
- **Health: (SAR) EN 62479:2010**
- **Safety: IEC 62368-1: 2014 (2.Ed)/Cor. 1: 2015, EN 62368-1: 2014/AC: 2015/A11: 2017/AC:2017**
- **EMC: EN 301 489-1 v2.2.3, Draft EN 301 489-17 v3.2.5**

End product will need to perform the radio EMC tests according to EN 301 489. The conducted tests can be inherited from the module test report. It is recommended to repeat the EN 300 328 radiated testing with the end product assembly.

Simplified Declaration of Conformity
Hereby, Renesas Design Netherlands B.V. declares that radio type equipment DA14592MOD-0100000 is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet address: www.renesas.com

13.2 FCC – (U.S.A.)

Model no. DA14592MOD-0100000

Model no. DA14592MOD-01F3200

Model no. DA14592MOD-01S1600

FCC ID: Y82-DA14592MOD

13.2.1 List of Applicable FCC Rules

The module complies with FCC Part 15.247.

13.2.2 Summarize the Specific Operational Use Conditions

The module has been certified for Portable applications. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

13.2.3 Limited Module Procedures

Not applicable.

13.2.4 Trace Antenna Designs

Not applicable.

13.2.5 RF Exposure Considerations

This equipment complies with FCC's RF radiation exposure limits set forth for an uncontrolled environment. The module integrator has to integrate the device within 10mm minimum distance to the human body, otherwise the module integrator has to do SAR testing and certification. The antenna(s) used for this transmitter must not be collocated or operating in conjunction with any other antenna or transmitter.

13.2.6 Antennas

Type	Gain	Impedance	Application
PCB Antenna	-0.4dBi	50Ω	Fixed

The antenna is permanently attached, cannot be replaced.

13.2.7 Label and Compliance Information

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Note
The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications or changes to this equipment. Such modifications or changes could void the user's authority to operate the equipment.

Warning
Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: ● Reorient or relocate the receiving antenna. ● Increase the separation between the equipment and receiver. ● Connect the equipment into an outlet on a circuit different from that to which the receiver is connected. ● Consult the dealer or an experienced radio/TV technician for help.

The system integrator must place an exterior label on the outside of the final product housing the DA14592MOD-0100000 Module. Below are the contents that must be included on this label.

OEM labeling requirements:

Notice
The OEM must make sure that FCC labeling requirements are met. This includes a clearly visible exterior label on the outside of the final product housing that displays the contents shown below.

Model: DA14592MOD-0100000
Contains FCC ID: Y82-DA14592MOD

13.2.8 Information on Test Modes and Additional Testing Requirements

When testing the host product, the host manufacture should follow FCC KDB Publication 996369 D04 Module Integration Guide for testing the host products. The host manufacturer may operate their product during the measurements. In setting up the configurations, if the pairing and call box options for testing do not work, then the host product manufacturer should coordinate with the module manufacturer for access to test mode software.

13.2.9 Additional Testing, Part 15 Subpart B Disclaimer

The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 15.247) list on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuity.

13.3 IC (Canada)

Model no. DA14592MOD-0100000

Model no. DA14592MOD-01F3200

Model no. DA14592MOD-01S1600

IC ID: 9576A-DA14592MOD

The DA14592 SmartBond™ Module is certified for the IC as a single-modular transmitter. The module meets IC modular approval and labeling requirements. The IC follows the same testing and rules as the FCC regarding certified modules in authorized equipment.

The module has been tested according to the following standards:

- Radio: RSS-247 Issue 3: August 2023, RSS-Gen Issue 5: April 2018 +A1: March 2019+A2: February 2021
- Health: RSS-102 Issue 6:2023

This device contains license exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's license-exempt RSS(s). Operation is subject to the following two conditions:

(1) this device may not cause interference

(2) this device must accept any interference, including interference that may cause undesired operation of the device.

L'emitteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Inovvation, Sciences et Développement economic Canada applicables aux appareils radio exempts de licence.
L'exploitation est autorisée aux deux conditions suivantes:
(1) L'appareil ne doit pas produire de brouillage

(2) L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

RF Exposure Statement

This device complies with IC radiation exposure limits set forth for an uncontrolled environment and meets RSS-102 of the IC radio frequency (RF) Exposure rules. The module integrator has to integrate the device within 10 mm minimum distance to the human body, otherwise the module integrator has to do SAR testing and certification. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Le présent appareil est conforme à l'exposition aux radiations IC définies pour un environnement non contrôlé et répond aux RSS-102 de la fréquence radio (RF) IC règles d'exposition. L'intégrateur de module doit intégrer l'appareil à une distance minimale de 10 mm du corps humain, sinon l'intégrateur de module doit effectuer des tests et une certification SAR. L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

OEM Responsibilities to comply with IC Regulations

OEM integrator is responsible for testing their end product for any additional compliance requirements needed for the module installation like IC ES003 (EMC). This can be combined with the FCC Part 15B test.

End product labeling

The DA14592 SMARTBOND™ Module is labeled with its own IC ID: 9576A-DA14592MOD. If the IC ID is not visible when the module is installed inside another device, the host product must be labelled to display the ISED certification number for the module, preceded by the word "contains" or similar wording expressing the same meaning, as follows: "Contains IC: 9576A-DA14592MOD".

13.4 UKCA (UK)

Model no. DA14592MOD-0100000

Model no. DA14592MOD-01F3200

Model no. DA14592MOD-01S1600

The module has been tested and found to comply with the standards harmonized with the regulations listed below according to UKCA-Radio Equipment Regulations 2017-CHAPTER 1 6(1)(a) Health, 6(1)(b) and 6(2).

The applicable standards are:

- **Radio: EN 300 328 V2.2.2 (2019-07)**
- **Health: (SAR) EN 62479:2010**
- **Safety: IEC 62368-1: 2014 (2.Ed)/Cor. 1: 2015, EN 62368-1: 2014/AC: 2015/A11: 2017/AC:2017**

- **EMC: EN 301 489-1 v2.2.3, Draft EN 301 489-17 v3.2.5**

End product will need to perform the radio EMC tests according to EN 301 489. The conducted tests can be inherited from the module test report. It is recommended to repeat the EN 300 328 radiated testing with the end-product assembly.

Simplified Declaration of Conformity
Hereby, Renesas Design Netherlands B.V. declares that radio type equipment DA14592MOD-0100000 is in compliance with Radio Equipment Regulations 2017. The full text of the UK declaration of conformity is available at the following internet address: www.renesas.com

13.5 NCC (Taiwan)

Model no. DA14592MOD-0100000

NCC ID:CCAH24Y10540T7

The DA14592 SmartBond™ Module has received compliance approval in accordance with the Telecommunications Act. The module has been tested according to the following standard:

- Radio: Low Power Radio Frequency Devices Technical Regulations (LP0002)

End product may need to follow additional requirements according to the regulation EMC.

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。低功率射頻器材之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。前述合法通信，指依電信管理法規定作業之無線電通信。低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

End product labeling

The NCC ID can be applied directly to the end product's label.

NCC Warning
本模組於取得認證後將依規定於模組本體標示審驗合格標籤，並要求最終產品平台廠商(OEM Integrator)於最終產品平台(End Product)上標示" 本產品內含射頻模組， 其NCC型式認證號碼為: CCAH24Y10540T7

13.6 MSIP (South Korea)

Model no. DA14592MOD-0100000

MSIP ID: R-R-8DL- DA14592MOD100

The DA14592 SmartBond™ Module has received certification of conformity in accordance with Radio Waves Act. The module has been tested according to the following standard:

- Radio: Ministry of Science and ICT Notice No. 2019-105

For the end product wireless test, you can refer to Renesas' own certification report so that the lab knows the module itself has passed although it still needs to be tested.

Additionally, EMC for wireless (KN301489).

End product labeling

The MSIP ID can be applied directly to the end product's label. The ID should be clearly visible on the final end product. The integrator of the module should refer to the labeling requirements for Korea available on the Korea Communications Commission (KCC) website.

13.7 ICASA (South Africa)

South Africa certification is based on RED(CE) approval.

Model no. DA14592MOD-0100000

Equipment Type Approval Number: TA-2024/1068

Approval is granted to print labels for the products as described below:

1. **For use as Label on the user manual: 40 mm (W) X 20 mm (H).**
2. **For use as Label on the package size: 80 mm (W) X 40 mm (H).**

End product may need to follow additional requirements according to the regulation EMC.

13.8 ANATEL (Brazil)

Model no. DA14592MOD-0100000

Model no. DA14592MOD-01F3200

Model no. DA14592MOD-01S1600

ANATEL ID: 05494-24-16689

ANATEL

05494-24-16689

The module has been tested and found to be compliant according to the following standards:

- ATO (Act) No 14448/2017

End product may need to follow additional requirements according to the regulation EMC.

"Este equipamento não tem direito à proteção contra interferência prejudicial e não pode causar interferência em sistemas devidamente autorizados. Para mais informações consulte o site da ANATEL www.anatel.gov.br"

Translation of the text:

"This equipment is not entitled to protection against harmful interference and must not cause interference in duly authorized systems. For more information, consult the ANATEL website www.anatel.gov.br"

13.9 SRRC (China)

Model no. DA14592MOD-0100000

CMIIT ID: 24J994Z8R592

The module has been tested and found to be compliant according to the following standards:

- 信部无【2002】353号

End product may need to follow additional requirements according to the regulation EMC.

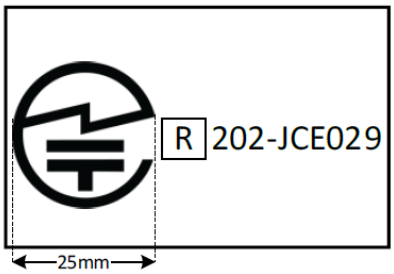
13.10 MIC (Japan)

Model no. DA14592MOD-0100000

Model no. DA14592MOD-01F3200

Model no. DA14592MOD-01S1600

MIC ID: R 202-JCE029



The DA14592 SmartBond™ Module has received type certification as required to conform to the technical standards regulated by the Ministry of Internal Affairs and Communications (MIC) of Japan pursuant to the Radio Act of Japan.

The module has been tested according to the following standard:

- Radio: JRL "Article 49-20 and the relevant articles of the Ordinance Regulating Radio" Equipment

End product may need to follow additional requirements according to the regulation EMC.

End product labeling

The MIC ID can be applied directly to the end product's label. **The end product may bear the GITEKI mark and certification number so that is clear that the end product contains a certified radio module. The following note may be shown next to, below, or above the GITEKI mark and certification number in order to indicate the presence of a certified radio module:**

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation of the text:

"This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law."

13.11 NBTC (Thailand)

Model no. DA14592MOD-0100000

Model no. DA14592MOD-01F3200

Model no. DA14592MOD-01S1600

DA14592MOD-0100000 SDoC ID: SD01917-24

DA14592MOD-01F3200 SDoC ID: SD01918-24

DA14592MOD-01S1600 SDoC ID: SD01919-24

"This telecommunication equipment conforms to the technical standards or requirements of NBTC."

End product may need to follow additional requirements according to the regulation EMC.

End product labeling

End products will have their own ID and labeling requirements.

(Translation of content: This radiocommunication equipment is exempted to possess license, user license, or radiocommunication station license as per NBTC notification regarding radiocommunication equipment and radiocommunication station has been exempted for license according to radio communication act B.E.2498)

13.12 WPC (India)

Model no. DA14592MOD-0100000

Model no. DA14592MOD-01F3200

Model no. DA14592MOD-01S1600

Registration No: ETA-SD-20240504443

Registration No: ETA-SD-20240504440

Registration No: ETA-SD-20240504442

India certification is based on RED(CE) approval/reports. There are no **marking/labeling requirements.**

End product may need to follow additional requirements according to the regulation EMC.

13.13 WEEE Directive (2012/19/EU)

The Waste Electrical and Electronic Equipment Regulations 2013

For Customers in the UK and European Union

The WEEE (Waste Electrical and Electronic Equipment)
regulations put responsibilities on producers for the collection and recycling or disposal of electrical and electronic waste. Return of WEEE under these regulations is applicable in the UK and European Union.

This equipment (including all accessories) is not intended for household use. After use, the equipment cannot be disposed of as household waste, and the WEEE must be treated, recycled, and disposed of in an environmentally sound manner.
Renesas Electronics Europe GmbH can take back the end of life equipment. Register for this service at:
https://www.renesas.com/eu/en/support/regional-customer-support/weee

14. Bluetooth SIG Qualification

The DA14592 SmartBondTM Module is listed on the Bluetooth® SIG Website as a qualified product. The customers can refer to the following QDIDs to qualify their product:

- QDID 221791 for Host Subsystem
- QDID 221790 for Controller Subsystem.

Revision History

Revision	Date	Description
3.0	Aug 07, 2024	Datasheet status: Final, Product Status: Production
2.0	May 30, 2024	Datasheet Status: Preliminary, Product Status: Qualification
1.1	Feb 08, 2024	Datasheet status: Target. Product status: Development

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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