8 W Mono Class-D Amplifier for 2S Battery Devices

General Description

The DA7202 is a powerful, high-efficiency, low-EMI Class-D speaker driver that can drive 8 W into 4 Ω loads directly from a 2S lithium-ion battery pack.

The DA7202 is a standalone high performance mono Class-D audio amplifier targeted at powering a variety of two cell portable applications such as Ultrabooks™ and tablets.

It uses a fully-differential switched-mode amplifier architecture with a fixed +18 dB gain, with differential analogue inputs. It also has a PWM modulator and an H-bridged switched power output stage that delivers 5 W (dynamic) into an 8 Ω load, making a speaker sound louder on portable devices.

The DA7202 can be directly connected between the two-cell battery and the speaker. Noise suppression circuitry to reduce audible pops and clicks at the speaker output is also included.

Available as a 9-bump WL-CSP package with 0.5 mm pitch that is suited to low-cost PCB technology, it is ideal for portable applications that require small footprints.

Key Features

- PRMS: 3.6 W into 8 Ω load at 8.2 V, 1% THD+N
- Efficiency:
  - 86% at P_{OUT} = 3.5 W at 8.2 V, 8 Ω
  - 75% at P_{OUT} = 5.7 W at 8.2 V, 4 Ω
- Supports 4 Ω and 8 Ω loads
- SNR (A-weighted) 104 dB
- THD+N: 94 dB at 3.0 W, 8.2 V, 8 Ω
- PSRR: 78 dB
- Auto-Shutdown/Start-up: <3.5 ms
- Ultra low standby current: 7 µA
- Short-circuit and thermal-overload Protection with auto-recovery
- Wide supply voltage range 4.5 to 9.0 V
- 9-bump 1.7 x 1.5 mm WL-CSP with 0.5 mm pitch
- 2S battery pack

Applications

- Tablets
- Personal navigation devices
- Ultrabooks™
- Speaker accessories
- Handheld gaming devices

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1 Terms and Definitions

CTA-2006	Consumer Technology Association - Testing and Measurement Methods for Mobile Audio Amplifiers
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FCC	Federal Communications Commission
LDO	Low Dropout regulator
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
PSRR	Power Supply Rejection Ratio
RF	Radio Frequency
RMS	Root Mean Square
SNR	Signal to Noise Ratio
THD	Total Harmonic Distortion
THD+N	Total Harmonic Distortion plus Noise
WL-CSP	Wafer Level-Chip Scale Packaging

2 Block Diagram

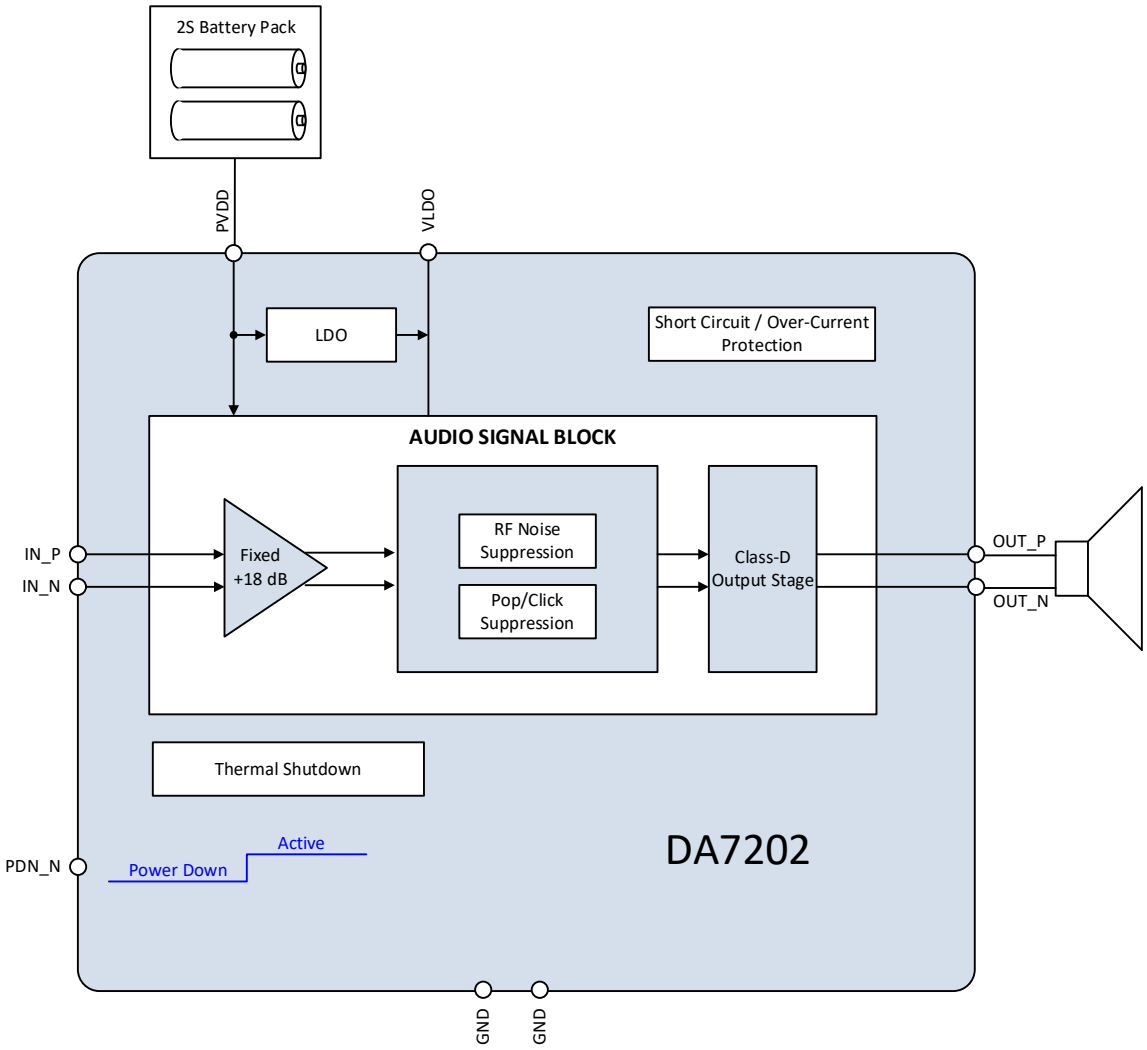


Figure 1. DA7202 block diagram

3 Pinout

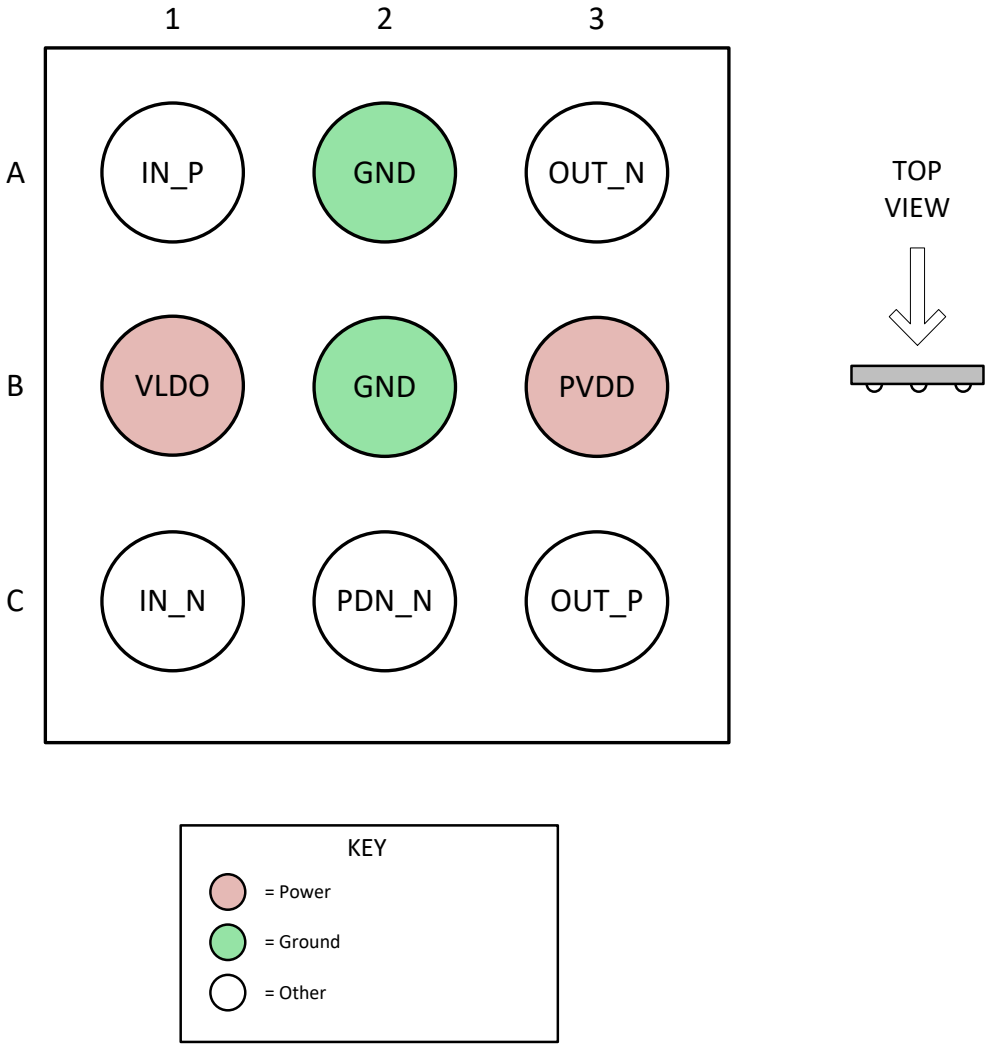


Figure 2. Connection diagram

Table 1: Pin description

Pin no.	Pin name	Description
A1	IN_P	Positive Analogue Input
A2	GND	Ground
A3	OUT_N	Negative Output
B1	VLDO	Output voltage from LDO
B2	GND	Ground
B3	PVDD	Power Supply
C1	IN_N	Negative Analogue Input
C2	PDN_N	Power Down Control (0 = Power Down/1 = Active)
C3	OUT_P	Positive Output

4 Characteristics

4.1 Absolute maximum ratings

Table 2: Absolute maximum ratings

Parameter	Description	Conditions (Note 1)	Min	Typ	Max	Unit
	Storage temperature		-65		+85	°C
	Operating temperature		-45		+85	°C
	Junction temperature (T_J)				+150	°C
PVDD	Supply voltage		+4.5	+8.2	+10.0	V
VLDO				+5.0		V
	Audio input signal	IN_P, IN_N			+5.0	V
PDN_N	Power down control		-0.3		+5.0 (VLDO)	V
	ESD susceptibility	Human body model			2	kV

Note 1 Stresses beyond those listed under "Absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Recommended operating conditions

Table 3: Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
PVDD	Supply voltage		4.5		9.0	V
T_A	Ambient operating temperature	In air	-40		+85	°C

4.3 Electrical characteristics

V_{DD} = 8.2 V, T_A = 25 °C, R_L = 8 Ω + 33 µH, unless otherwise noted.

Table 4: Performance

Parameter	Description	Conditions	Min	Typ	Max	Unit
VLDO		Output		5.0		V
	Input impedance			30		kΩ
	Load inductance		18			µH
P_{RMS}	Continuous output power	R_{LOAD} = 8 Ω V_{PWR} = 8.2 V THD+N = 1%		3.6		W
		R_{LOAD} = 4 Ω V_{PWR} = 8.2 V THD+N = 1%		5.7		W
$P_{MPO\ (RMS)}$	Dynamic output power	R_{LOAD} = 8 Ω			4.6	W

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Note 1	V_{PWR} = 8.2 V THD+N = 10%				
		R_{LOAD} = 4 Ω V_{PWR} = 8.2 V THD+N = 10%			8.3	W
	Efficiency	P_{OUT} = 3.5 W R_{LOAD} = 8 Ω + 18 µH audio = 1 kHz			86	%
	THD+N	P_{OUT} = 3.0 W, 8 Ω, 8.2 V		94		dB
	SNR			104		dB
	PSRR (AC grounded)	Frequency = 217 Hz		78		dB
	Gain	Fixed		18		dB
	Output switching frequency	Fixed		1		MHz
	Output Noise (RMS)	Integrated over bandwidth SNR = 99 dB, Gain = 18 dB			60	µV
	Standby current consumption at Shutdown			7		µA

Note 1 Dynamic power measured with a burst signal, according to CTA-2006, to simulate headroom for typical music programme and avoid significant self-heating.

Table 5: Digital inputs (PDN_N)

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input-Voltage High		1.3		+5 (VLDO)	V
V_{IL}	Input-Voltage Low		0		0.7	V
V_H	Input Hysteresis			0.4		V
I_{IH}	Input High Leakage current	V_{IN} = 5 V, T_A = 25 °C			25	µA
I_{IL}	Input Low Leakage current	V_{IN} = GND, T_A = 25 °C			0.1	µA

Note 1 V_{IH} and V_{IL} define logic levels to enable or disable the DA7202.

5 Functional Description

The DA7202 is a powerful, high efficiency, low EMI Class-D speaker driver that can drive a maximum of 8 W into 4 Ω loads directly from a 2S lithium-ion battery pack.

The device provides audio noise and RF noise suppression. It also has short circuit protection, as well as protection against over-heating.

The DA7202 is available in a 9-bump WL-CSP package with 0.5 mm pitch that enables low-cost PCB technology which is ideal for portable applications that require small footprints.

5.1 Pop and click suppression

DA7202 includes noise suppression circuitry that reduces audible pops and clicks at the speaker output when enabling or disabling the device.

5.2 Short circuit/over-current protection

The DA7202 is protected by a short circuit/over current detector. If a short circuit is detected, regardless of the frequency of the signal, the device is disabled immediately. After 8 ms, the short-circuit status is checked. If the short condition has been resolved, the chip will be re-enabled. If the short condition still persists, the DA7202 remains disabled. The short-circuit status is checked every 8 ms until the short condition has been resolved. The chip will then be re-enabled.

The disabling of the chip and its later re-enabling are both performed without using the noise suppression circuitry. Audible artefacts may be present in the output signal.

Whenever the DA7202 has been powered down, the power stage is placed in a high impedance (high-Z) state to minimise power consumption.

5.3 Thermal performance

5.3.1 Maximum power dissipation

Given the Junction-to-Ambient thermal impedance (72 °C/W), the Power Dissipation versus Output Power (from Figure 11 and Figure 12), and the maximum junction temperature ($T_{J(MAX)}$ specified in Table 6), it is possible to calculate the maximum ambient temperature ($T_{A(MAX)}$) using the following equation:

$$T_{A(MAX)} = T_{J(MAX)} - \theta_{JA} \times P_{D(MAX)}$$

Up to an ambient temperature of 85 °C, DA7202 can dissipate 0.56 W of heat before reaching 125 °C, when in a 1 ft^3 enclosure. Different PCB designs and enclosures will affect this dissipation.

If the DA7202 is operated continuously at, or close to, its maximum output power, there is a risk of overheating and thermal shutdown, unless steps are taken to dissipate this excess heat.

5.3.2 Thermal shutdown

The DA7202 is provided with a thermal protection feature that automatically disables the power stage and the LDO if the junction temperature reaches 150 °C.

When a thermal shutdown is performed, the chip is disabled, leaving only the temperature sensor block active. The process of disabling the chip is performed using the noise suppression circuitry, so no audible artefacts will be present on the output signal during the disabling process. The time taken for a noise free shutdown is shown in Figure 10.

If thermal shutdown is activated, the chip is not re-enabled until the temperature has dropped to 100 °C. When the temperature has reached 100 °C, the DA7202 restarts with an automatic soft start. The process of re-enabling the chip is performed using the noise suppression circuitry, so no audible artefacts will be present on the output signal during start-up process. The time taken for a noise free start-up is shown in Figure 9.

Whenever the DA7202 has been powered down, the power stage is placed in a high impedance (high-Z) state to minimise power consumption.

5.3.3 Thermal protection

Monitoring of the ambient temperature does not guarantee that the junction temperature (T_J) is within the specified temperature limits.

The junction temperature of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). An estimation of the junction temperature (T_J) can be calculated using the formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

- T_J = junction temperature
- T_A = ambient temperature of the package (°C)
- P_D = power dissipation of the package (W)
- θ_{JA} = junction to ambient thermal resistance (°C/W) = 72 °C/W

The value of θ_{JA} can vary, depending on PCB material, the layout, and the environmental conditions. The specified value of θ_{JA} (72°C/W) is based on a 4-layer, 101.5 mm x 114.5 mm circuit board in a 1 ft^3 enclosure, as specified in the JEDEC standard JESD51-9.

Table 6: Thermal protection

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Thermal Shutdown Threshold			150		°C
	Thermal Shutdown Restart Threshold			100		°C
	Thermal Shutdown Hysteresis			50		°C
θ_{JA}	Junction to ambient thermal resistance			72		°C/W

5.4 Gain

The DA7202 has a fixed gain of +18 dB.

Output volume is directly proportional to the input signal strength. It is assumed that any required variation in output volume will be controlled by varying the DA7202 input signal. The input signal amplitude can be reduced using resistor dividers in conjunction with the known input impedance.

5.5 Class D output stage

The class D output stage is connected directly to the PVDD (two cell battery pack) power supply. High-efficiency operation is achieved by operating the output transistors as switches. The output power transistors are either fully On or fully Off, providing a minimum resistance path for current from the power supply to the load. The block's outputs are connected directly to the speaker at OUT_P and OUT_N.

Filterless operation is achieved by connecting a load (a speaker) between the output terminals of the Class D output block. As a result, the voltage across the load represents a PWM (Pulse Width Modulated) audio signal, while the output current in the load is a filtered, demodulated representation of the input audio signal.

For filterless operation, the speaker load can be considered as a first order output filter with a cut-off frequency well below the PWM carrier signal (the current in the load is a filtered version of the output PWM voltage signal). See Section 7.2 for further details on speaker selection.

5.6 Power Down (PDN_N)

The DA7202 is powered down by pulling the PDN_N pin low. When the device is powered down, a controlled shutdown process is performed, thus ensuring that there are no audible artefacts (pops and clicks) on the output path.

Figure 10 shows the time to disable the device.

Table 7: Actions of the PDN_N pin

PDN_N value	Description
0	Power Down
1	Active

6 Typical Performance Plots

6.1 THD versus output power (8 Ω + 33 µH)

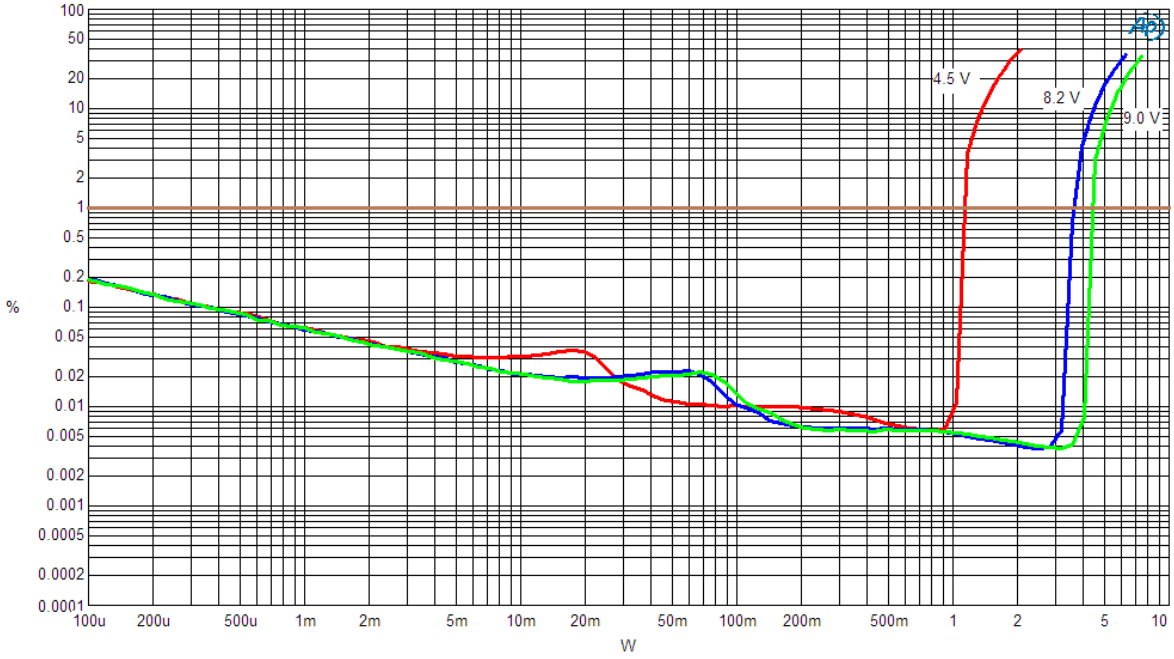


Figure 3. THD versus continuous output power (8 Ω + 33 µH)

6.2 THD versus output power (4 Ω + 33 µH)

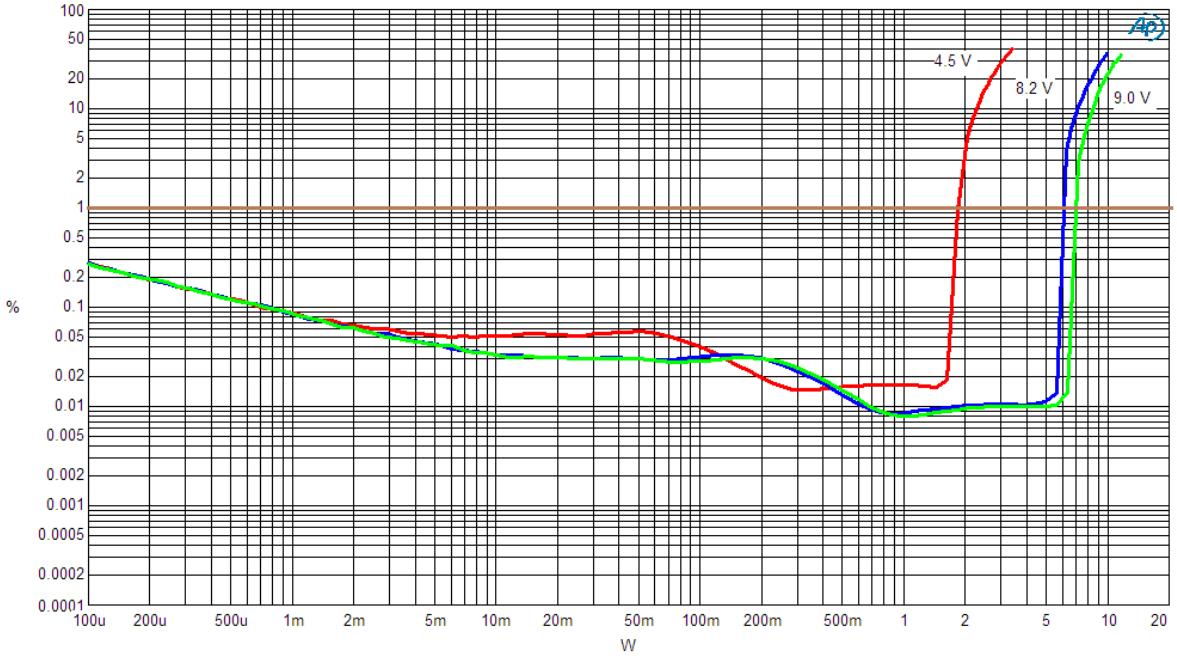
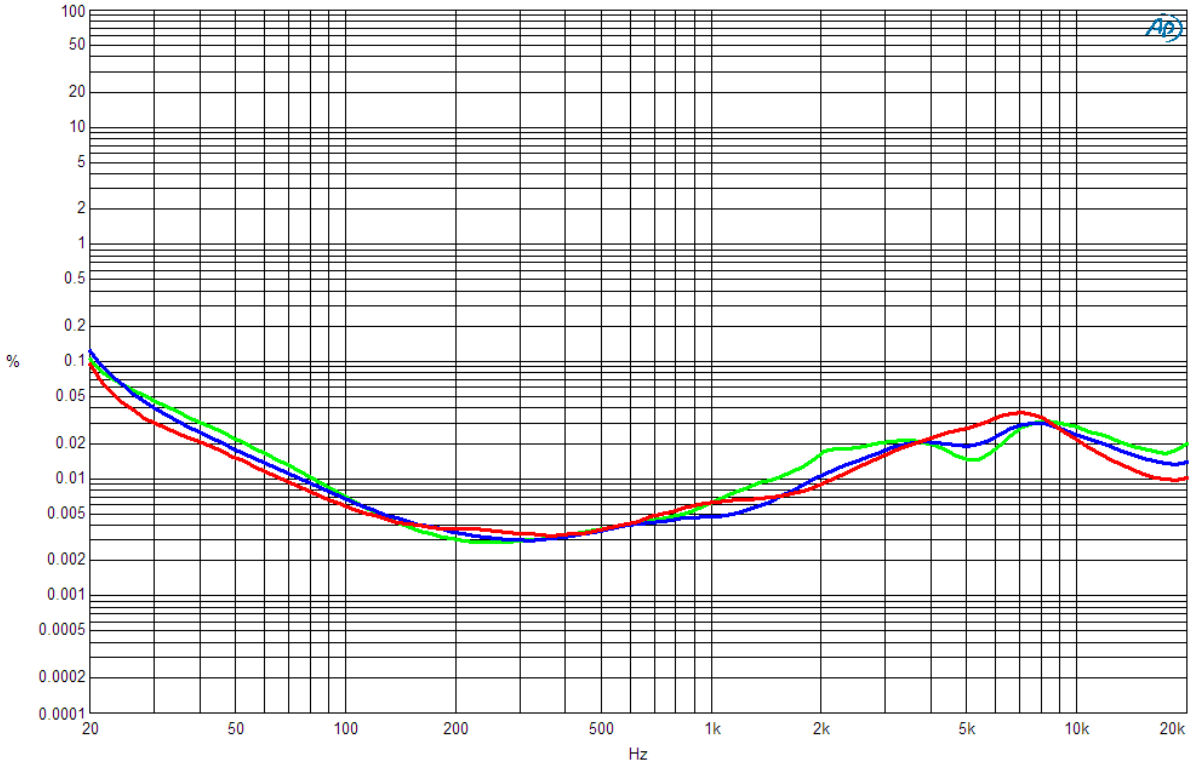


Figure 4. THD versus continuous output power (4 Ω + 33 µH)

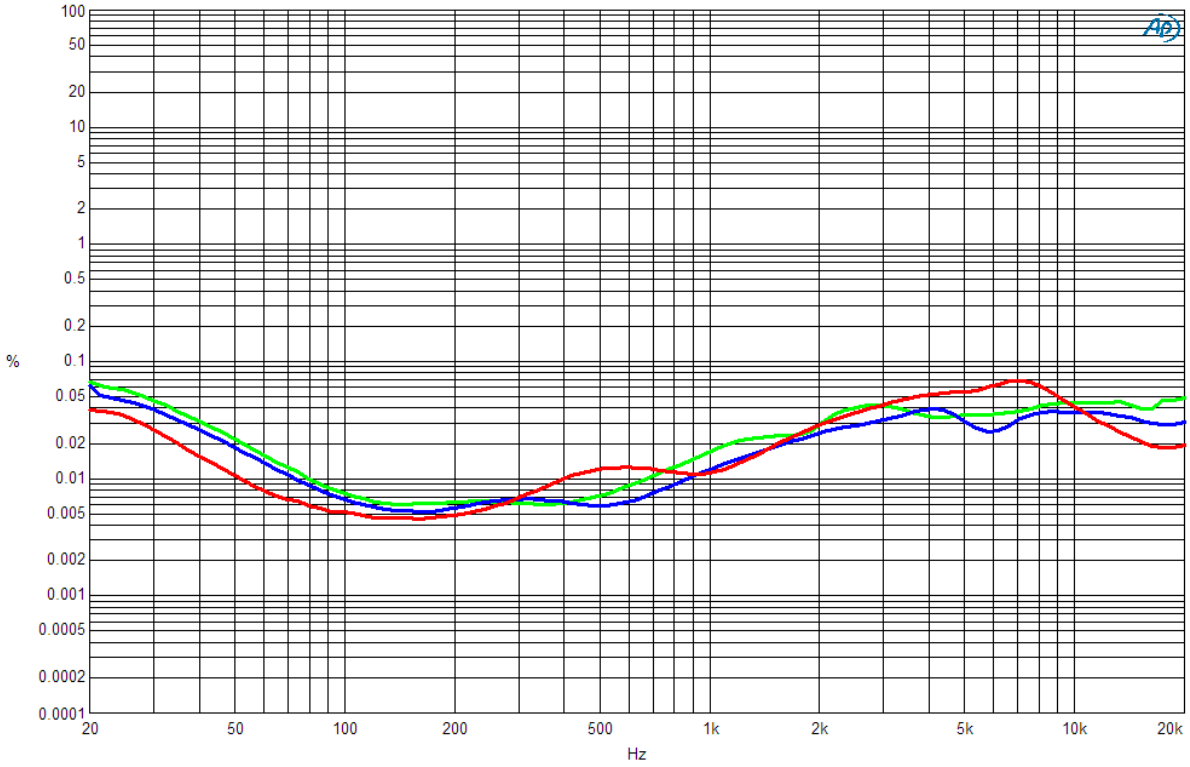
6.3 THD versus frequency (8 Ω + 33 µH) 8.2 V



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Green	Solid	3	Anlr.THD+N Ratio	Left	POUT = 3.0W
2	1	Blue	Solid	3	Anlr.THD+N Ratio	Left	POUT = 2.0W
3	1	Red	Solid	3	Anlr.THD+N Ratio	Left	POUT = 1.0W

Figure 5. THD versus frequency (8 Ω + 33 µH) 8.2 V

6.4 THD versus frequency (4 Ω + 33 µH) 8.2 V



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Green	Solid	3	Anlr.THD+N Ratio	Left	POUT = 5W
2	1	Blue	Solid	3	Anlr.THD+N Ratio	Left	POUT = 3W
3	1	Red	Solid	3	Anlr.THD+N Ratio	Left	POUT = 1W

Figure 6. THD versus frequency (4 Ω + 33 µH) 8.2 V

6.5 Efficiency versus output power (8 Ω + 33 µH)

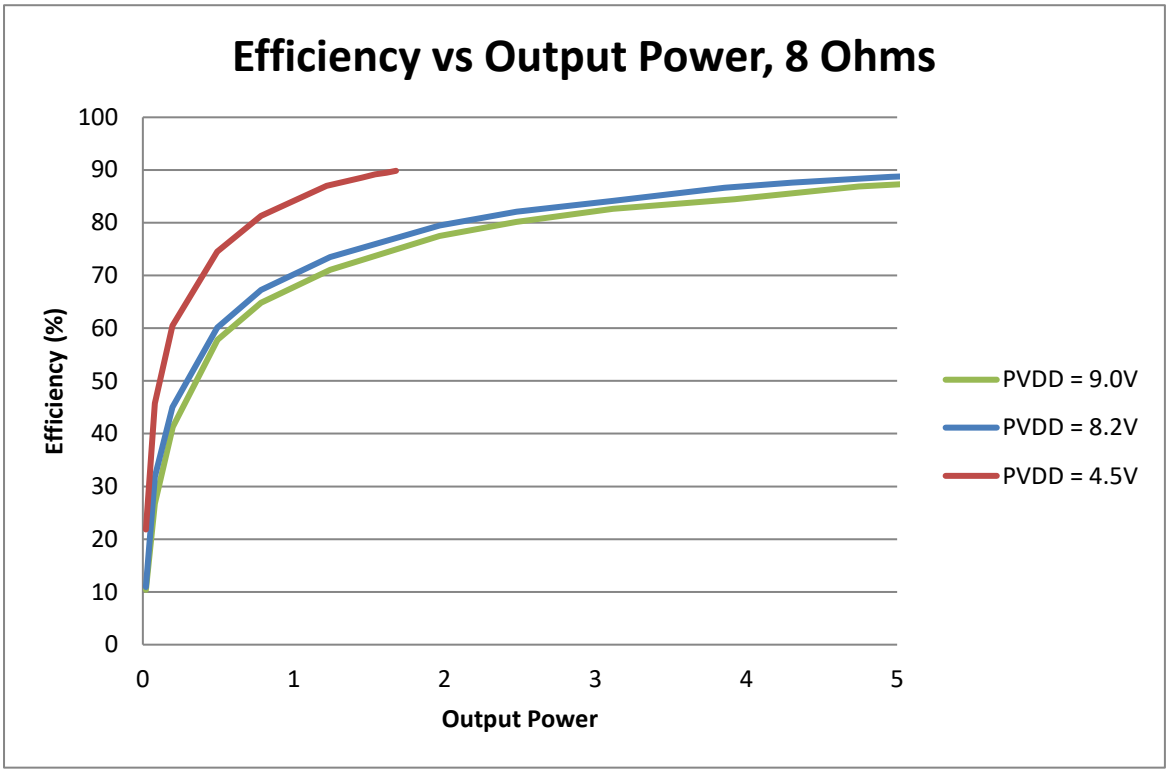


Figure 7. Efficiency versus output power (8 Ω + 33 µH)

6.6 Efficiency versus output power (4 Ω + 33 µH)

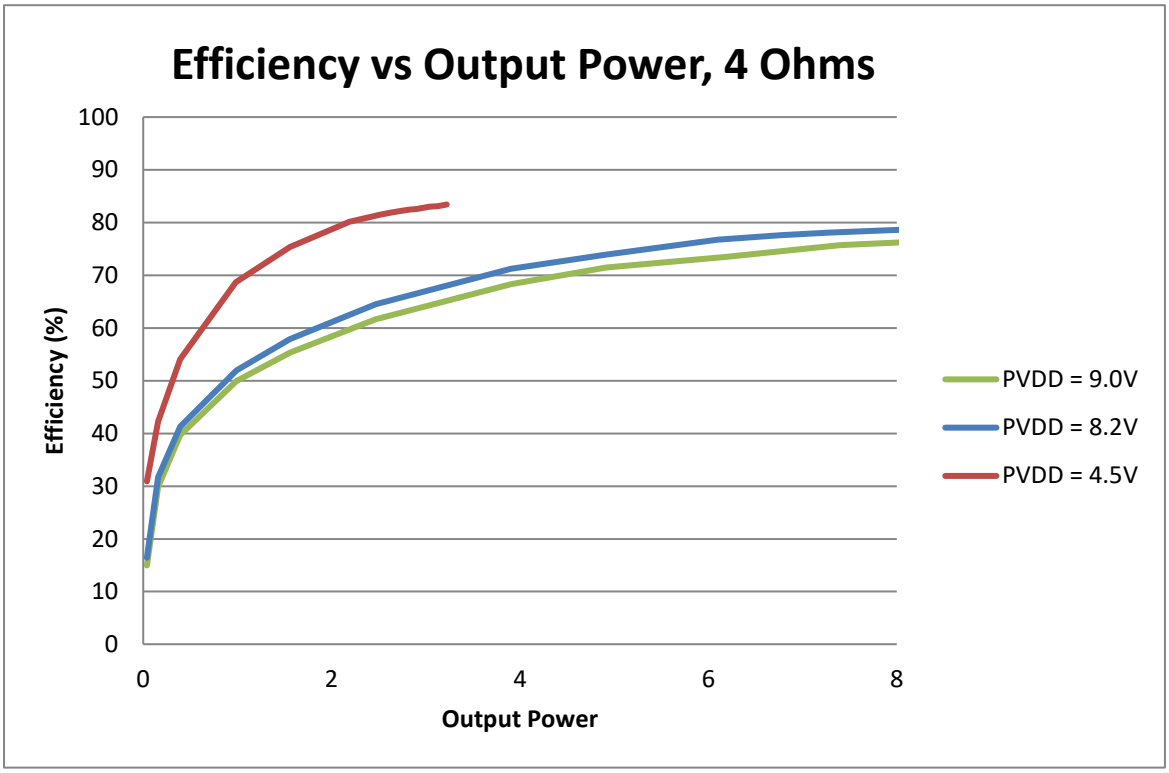


Figure 8. Efficiency versus output power (4 Ω + 33 µH)

6.7 Start-up timing

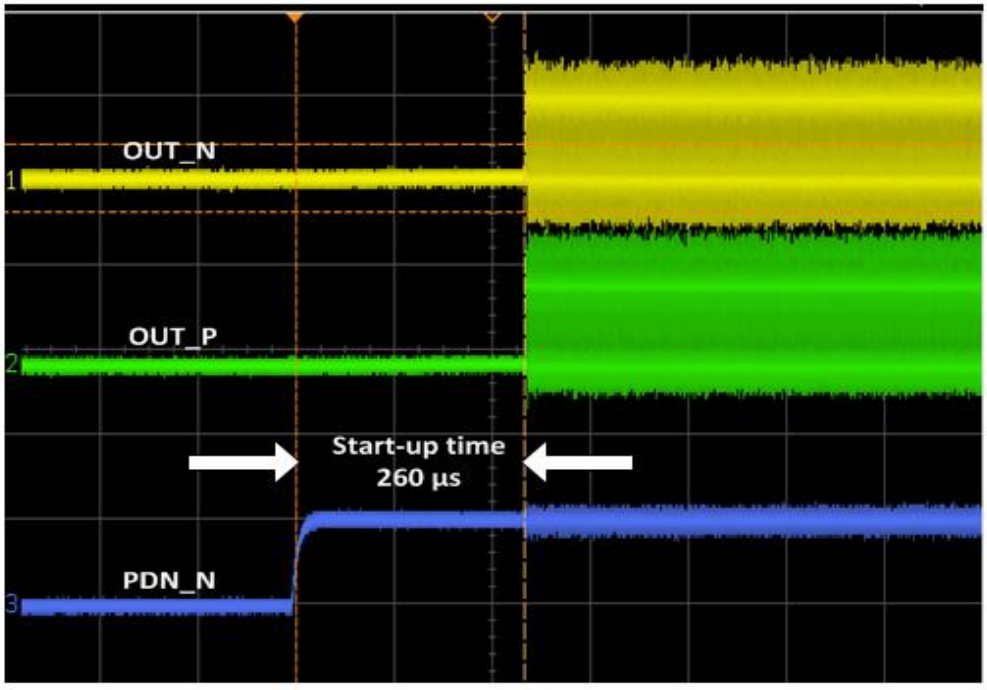


Figure 9. Start-up timing (260 µs from asserting PDN_N to valid output)

6.8 Shutdown timing

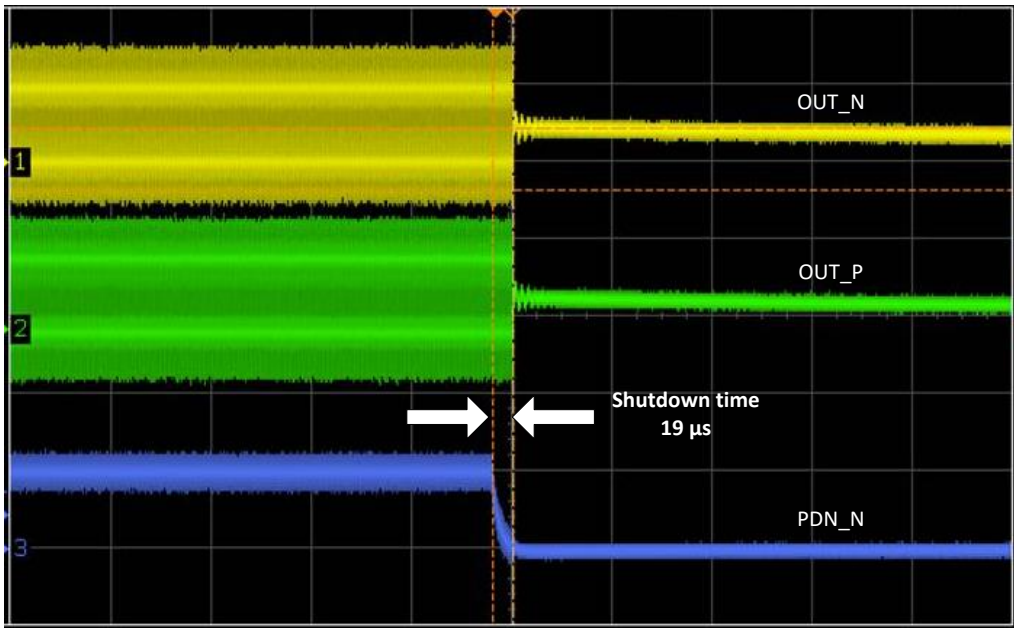


Figure 10. Shutdown timing (19 µs from de-asserting PDN_N to zero output)

6.9 Power dissipation versus output power (8 Ω + 33 µH)

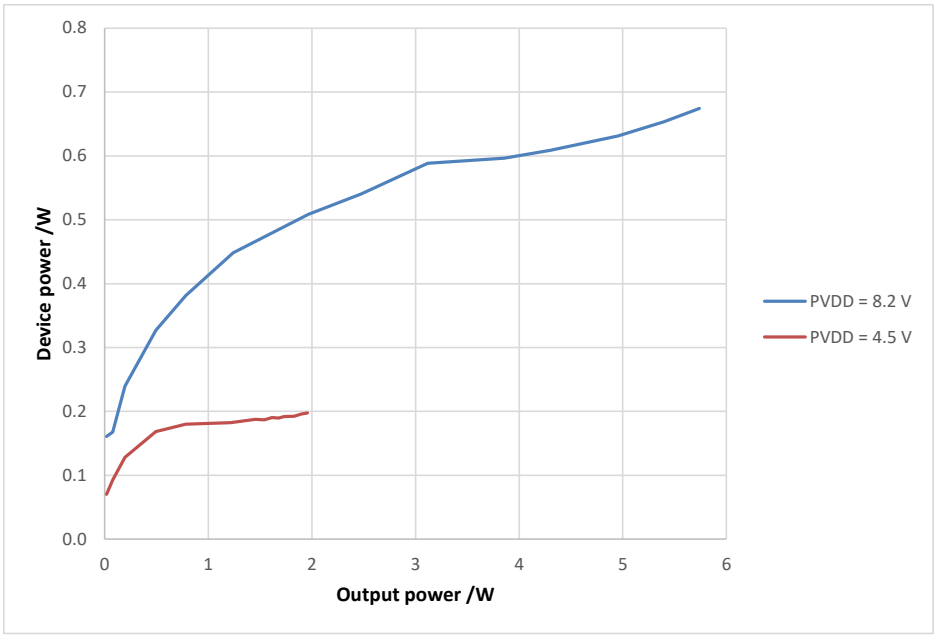


Figure 11. Power dissipation versus output power (8 Ω + 33 µH)

NOTE
The maximum continuous power dissipation will be limited by the IC package and its environment.

6.10 Power dissipation versus output power (4 Ω + 33 µH)

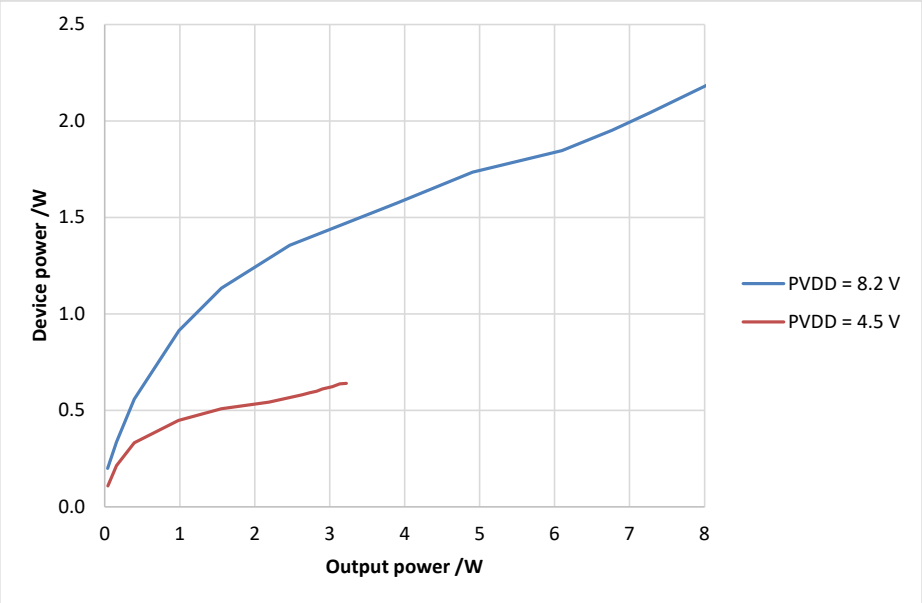


Figure 12. Power dissipation versus output power (4 Ω + 33 µH)

NOTE
The maximum continuous power dissipation will be limited by the IC package and its environment.

6.11 Electromagnetic interference (EMI) performance

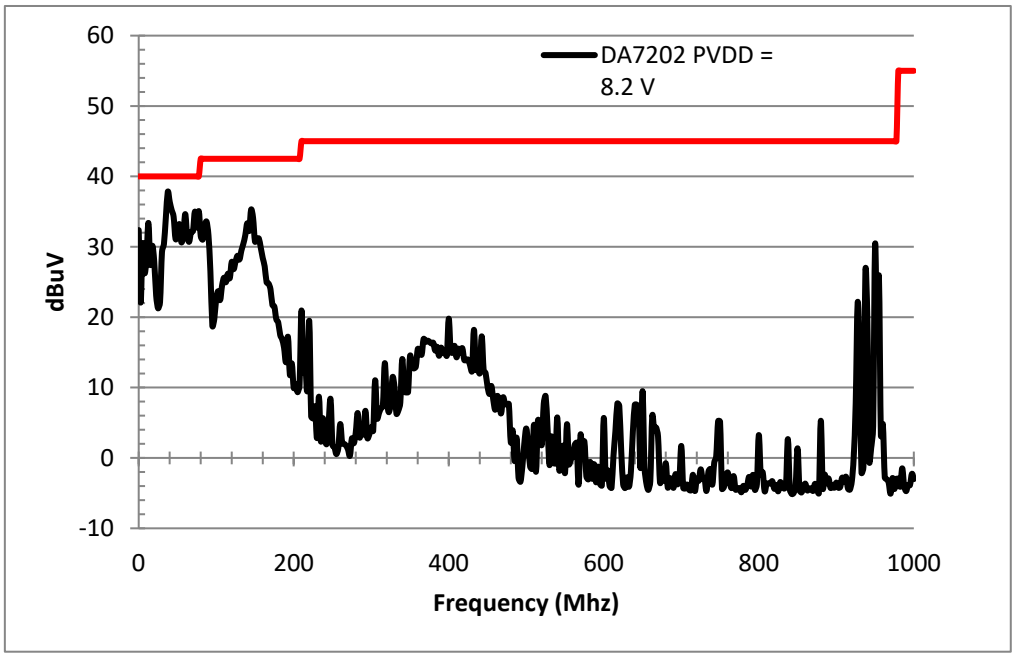


Figure 13. EMI performance with FCC Class-D limit also shown

NOTE
Measurements taken using a typical layout as shown in Figure 14 (speaker cable length = 12 cm).

7 Application Information

7.1 PCB layout

The performance of the DA7202 relies on a good PCB layout. Failure to follow best practice can have undesired side effects that include, but are not limited to, electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. Renesas recommends following the guidelines:

- Place any input capacitors and output capacitors close to the device using short tracks. These components carry high switching frequencies, and long tracks can act as an antenna.
- Maximise the size of ground metal on the component side to help with thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- If external resistors are to be used to change the gain, these should be placed close to the device.
- It is recommended that ferrite beads are included on the output paths to reduce EMI interference and noise.

7.2 Speaker selection

The output from the DA7202 Class-D amplifier contains high frequency signals that are a result of its switched PWM operation. These high frequency harmonics are at a much higher frequency than is recommended for most speakers, so they must be filtered out to protect the speaker.

The correct choice of speaker is therefore important since the speaker itself can act as a low-pass filter, attenuating the undesirable high frequency harmonics while still passing the desired audio frequencies.

The 3 dB cut-off frequency for speaker inductance and resistance can be calculated using the following formula:

$$f_c = R_{LOAD} / 2\pi L$$

Therefore, to achieve a 3 dB cut-off frequency of 20 kHz with an 8 Ω speaker, a speaker should be selected with an inductance of:

$$L = R_{LOAD} / 2\pi fc = 8\ \Omega / 2\pi * 20\ kHz = 64\ \mu H$$

8 Ω speakers for portable applications typically have an inductance in the range of 20 µH to 100 µH. Speakers with a higher inductance than the 64 µH calculated above have a 3 dB cut-off frequency below 20 kHz, resulting in a reduced audio bandwidth. Conversely, speakers with an inductance lower than 64 µH have a higher cut-off frequency.

7.3 Recommended external component layout

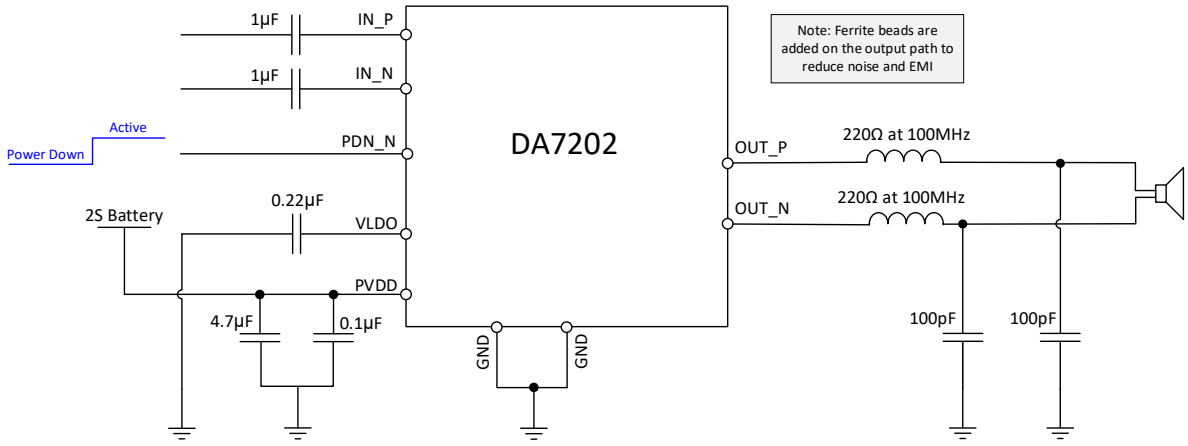


Figure 14. Layout of recommended external components and their values

7.4 Recommended external components

Table 8: Recommended external components

Pin name	Capacitance	Tolerance	Voltage	Dielectric	Manufacturer	Part number
PVDD	4.7 µF	±10%	35 V	X5R	muRata	GRM188R6YA475KE15
PVDD OUT_P OUT_N	100 pF	±5%	50 V	COG/NPO	muRata	GRM1555C1H101JD01D
VLDO	4.7 µF	±10%	16 V	X7R	muRata	GRM155R71C224KA12D
IN_P IN_N	1 µF	±10%	10 V	X5R	muRata	GRM155R61A105KE15D
Ferrite bead	220 Ω at 100 MHz	±25%	2 A		TDK	MPZ1608S221A

7.5 Capacitor selection

7.5.1 Input and output capacitors

The DA7202 is designed for operation with small, space-saving ceramic capacitors, but function with most commonly used capacitors as long as attention is paid to the ESR value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 3.0 µF capacitance with an ESR of 1 Ω or less is recommended for the input capacitor on PVDD to ensure the stability of the DA7202. Input capacitors IN_P, IN_N are required if the input signal is not biased, if high-pass filtering is needed, or if a single-ended source is used.

Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the DA7202's transient response to large changes in load current.

7.5.2 Input and output capacitor properties

Use any good quality ceramic capacitors with the DA7202 that meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behaviour over temperature and applied voltage. Capacitors must have a dielectric

sufficient to ensure that the minimum capacitance is over the required temperature range and the DC bias conditions. X5R or X7R dielectrics with a voltage rating of greater than 16 V are recommended for best performance. Y5V and Z5U dielectrics are not recommended.

The voltage stability of a capacitor is strongly influenced by the capacitor size and its voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about 15% over the −40 °C to +85 °C operating temperature range of the DA7202 and is not a function of package or voltage rating.

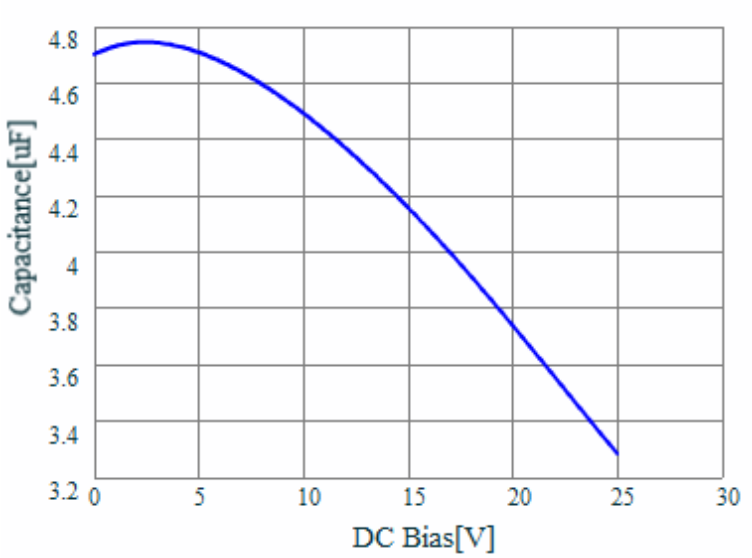


Figure 15. Performance plot of the sample capacitor used in the example (below)

Use the following equation to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{OUT} = C_{EFF} \times (1 - TEMPCO) \times (1 - TOL)$$

Where:

- **C_{EFF}** is the effective capacitance at the operating voltage
- **TEMPCO** is the worst-case capacitor temperature coefficient, specified as a value between 0 and 1.
- **TOL** is the worst-case component tolerance, specified as a value between 0 and 1.

In this example, the worst-case temperature coefficient (TEMPCO) over −40 °C to +85 °C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and CEFF is 4.6 µF at 7.2 V, as shown in Figure 15. Substituting these values into the equation yields

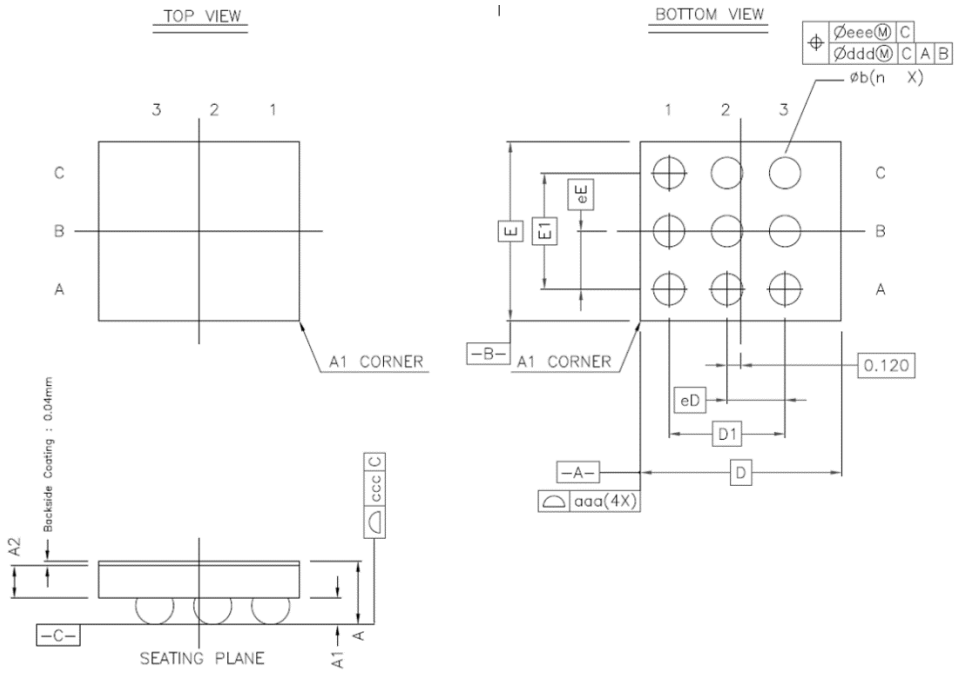
$$C_{OUT} = 4.6\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 3.5\ \mu F$$

The capacitor chosen in this example therefore meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the DA7202, it is imperative that the effects of DC bias and temperature on the behaviour of the capacitors are evaluated for each application.

8 Package Information

8.1 Package outlines



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	0.506	0.546	0.586
Stand Off	A1	0.212	–	0.242
Wafer Thickness	A2	0.279 ±0.025		
Body Size	D	1.730 BSC		
	E	1.540 BSC		
Ball Diameter (Size)		0.300		
Ball/Bump Width	b	0.312	0.327	0.342
Ball/Bump Pitch	eD	0.500		
	eE	0.500		
Ball/Bump Count	n	9		
Edge Ball Center to Center	D1	1.000 BSC		
	E1	1.000 BSC		
Package Edge Tolerance	aaa	0.03		
Coplanarity (whole wafer)	ccc	0.03		
Ball/Bump Offset (Package)	ddd	0.05		
Ball/Bump Offset (Ball)	eee	0.015		

Figure 16. DA7202 package outline drawing (9-bump WL-CSP 0.5 mm pitch)

8.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, when removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60% RH. before the solder reflow process.

WLCSP packages are qualified for MSL 1.

MSL level	Floor life time
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30 °C / 85% RH

8.3 WLCSP handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal will cause damage to the solder balls and therefore a removed sample cannot be reused.

WLCSP is sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

8.4 Soldering information

Refer to the JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

9 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, contact Renesas support or your local sales representative.

Table 9: Ordering information

Part number	Package	Shipment form	Pack quantity
DA7202-00UH2	9-bump CSP Pb free/green	T and R	4000

Revision History

Revision	Date	Description
DA7202-IDS1a-18042013	Apr 2013	Initial draft release
DA7202-IDS2a-18042013	Jun 2013	Updated headline power number, page 1 Updated parametric Added performance plots Updated ordering info
DA7202-IDS2b-110614	Jun 2014	Added typical performance plots (section 2.7) Updated section 2.3.2 (Power Dissipation) Added input impedance and standby current flow figures Modified External Layout diagram to include ferrite beads to reduce EMI Corrected/updated a few performance figures in light of the latest information External components modified
DA7202-IDS3a-20150820	Aug 2015	Converted to latest template Updated Absolute maximum ratings table with latest Junction temperature data Updated H-bridge to Class D output stage Corrected $R\theta_{JA}$ and θJA to θ_{JA} Production revision number now assigned
3.1	July 03, 2018	Removed Company Confidential status Updated back page
3.2	Feb 01, 2019	THD+N characteristics altered based on lab results from was 90 dB now 94 dB
3.3	Mar 09, 2021	Added MSL information
3.4	Dec 23, 2021	Rebranded document
3.5	June 21, 2022	Updated Section 7.5.1
3.6	Mar 03, 2024	Updated thermal and performance specifications

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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