Ultra-Low Quiescent Current PMIC

General Description

DA9070 is a highly integrated, configurable, low quiescent current PMIC that integrates the most common needs for wearables, home automation and low power battery applications.

The Power Management IC (PMIC) comprises a linear charger with Power Path management, ultra-low quiescent current (Iq) buck regulator and LDO/Load Switches, wide output voltage boost regulator, analog battery monitor, watchdog and protection features in an I^2C configurable compact WLCSP package.

DA9070 has several power saving modes to increase battery life whether the product sits on the shelf or is in operation. Further savings in power are achieved with the ultra-low Iq buck converter that is efficient down to 10 µA load currents and low Iq LDOs. The uncommitted inputs of LDOs can be connected to either the battery or buck output.

The integrated, high-efficiency boost regulator supports both sensors and display supply needs with a wide range configurable output voltage.

DA9070 provides charge current up to 500 mA to speed up the charge cycle. The charge profile is programmable by external resistors or in software, allowing either stand-alone operation or host control.

DA9070 includes dynamic power path management which automatically balancing current delivered to the system and battery charging.

Suitable for small battery applications, the battery monitor facilitates on-demand battery voltage and discharge current monitors to an external MCU's ADC for supporting software fuel gauging.

Key Features

- Increased battery life
  - 800 nA (no load, total battery current) buck converter, programmable down to 0.6 V, 300 mA-capable
  - Three configurable 800nA Quiescent Current LDOs/Load Switches, 150 mA-capable
- Power saving modes optimized for storage and operation
- Battery protection
  - Battery thermal- and over-discharge protection
  - 20 V tolerant input
  - Automatic battery temperature monitoring in all operation modes
- Configurable battery monitors
  - Battery current (IMON)
  - Battery voltage (VBAT_DIV)
  - Battery temperature (TEMP_SNS)
- High integration and configurability
  - Wide output voltage boost regulator (4.5V to 18 V)
  - I^2C enabled analog battery monitors for Software Fuel Gauging
  - Watchdog input and power-cycling to prevent system stall
  - Reset input and status outputs
  - Low external component count
  - Compact, 42 pin, 2.97 mm x 2.66 mm WLCSP package
- Fast charge
  - 500 mA (max) charge current; 2 mA (min)
  - Programmable pre-charge, fast charge, and termination voltage
  - Dynamic power path balances multiple power sources
  - Termination current programmable down to 500 µA
  - ±0.5 % accurate termination voltage

Applications

- Wearable devices - Fitness trackers, smart watches, wireless headphones
- Home automation devices - Smoke detectors, Smart thermostats, Smart door locks
- Health monitoring medical accessories
- Rechargeable toys
- High efficiency, ultra-low power applications

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1 System Diagram

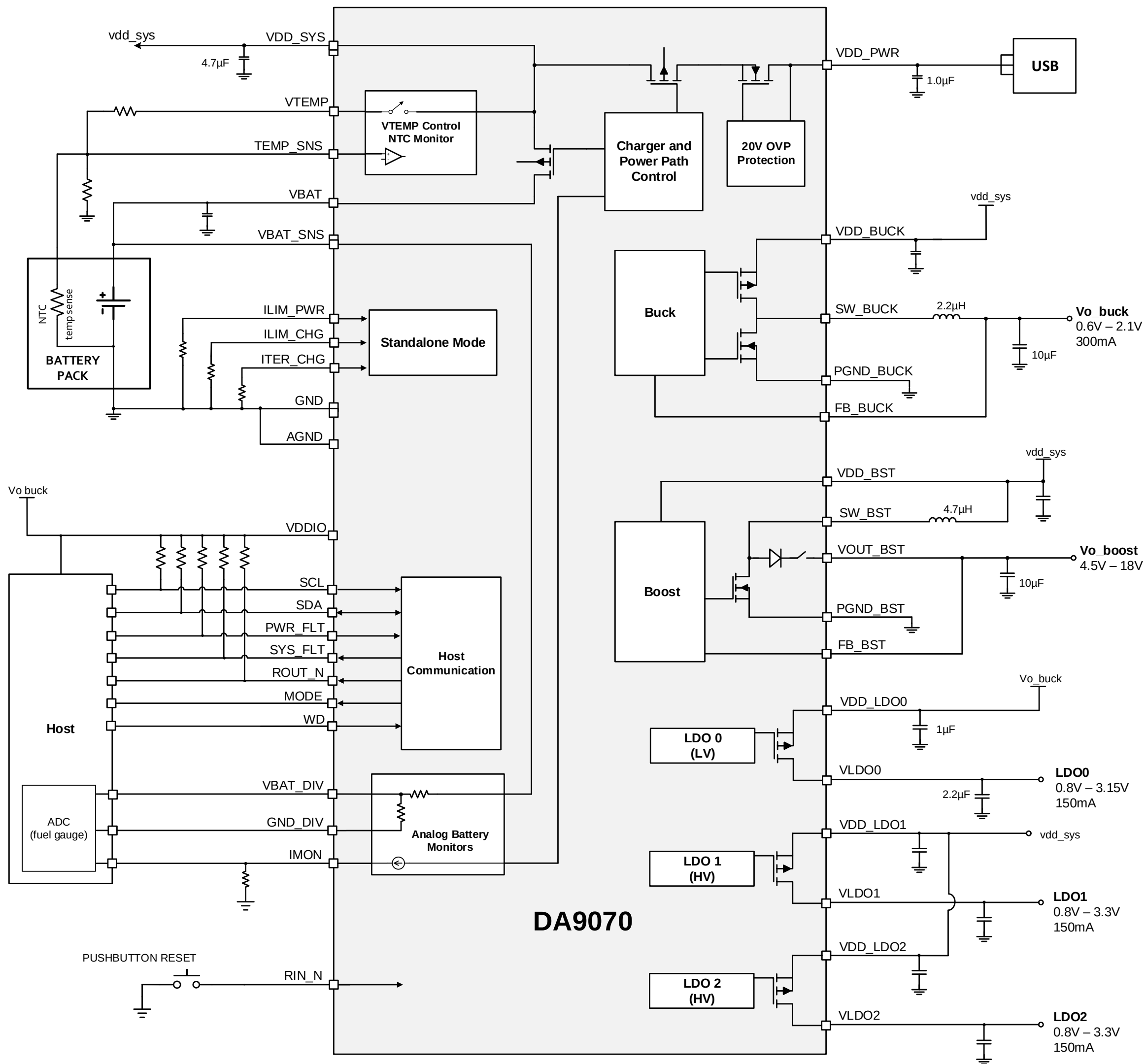


Figure 1: System Diagram

2 Pinout

	7	6	5	4	3	2	1
A	PGND_BUCK	SW_BUCK	VDD_BUCK	VDD_SYS	VDD_SYS	VDD_PWR	GND
B	FB_BUCK	SDA	SYS_FLT	TEMP_SNS	IMON	VBAT	VBAT
C	AGND	SCL	RIN_N	WD	ILIM_CHG	ITER_CHG	VBAT_SNS
D	PWR_FLT	ROUT_N	MODE	VBAT_DIV	GND	ILIM_PWR	VDD_BST
E	VDD_LDO0	VDD_LDO1	VDD_LDO2	GND_DIV	VDDIO	VTEMP	PGND_BST
F	VLDO0	VLDO1	VLDO2	GND	FB_BST	VOUT_BST	SW_BST

COLOR KEY:

Charger/Power Path | Buck | Boost | Reset/Timer

LDO0 | LDO1 | LDO2 | Control | Temp Sense | Common

Figure 2: Connection Diagram (Bottom View)

Table 1: Pin Description

Pin No.	Pin Name	Type (Table 2)	Description
A1, D3, F4	GND	GND	Ground connection. Connect to the ground plane
A2	VDD_PWR	POWER	Input power supply. VDD_PWR is a 20V-tolerant input. Bypass to GND with a minimum 1uF ceramic capacitor.
A3, A4	VDD_SYS	POWER	VDD_SYS is the intermediate rail which typically supplies VDD_BUCK and VDD_BST. Bypass to ground with a 4.7uF ceramic capacitor.
A5	VDD_BUCK	POWER	Input of the buck converter. Bypass to PGND_BUCK with a minimum 2.2uF ceramic capacitor.
A6	SW_BUCK	POWER	Buck switching node. Connect to the buck inductor.
A7	PGND_BUCK	POWER	Power ground for the buck. Connect to the buck input capacitor and ground plane.
B1,B2	VBAT	POWER	Battery connection. Connect to the positive terminal of the battery. Bypass to ground with a minimum 1uF ceramic capacitor.
B3	IMON	AO	Battery discharge current monitor output
B4	TEMP_SNS	AI	Battery Pack NTC monitor. Connect to a resistive network and thermistor.
B5	SYS_FLT	DOD	Open drain status output. Connect to VDDIO through a 1K to 100KOhm pull-up resistor.
B6	SDA	DIO	I^2C Interface Data. Connect SDA to VDDIO through a 2k to10k pull-up resistor.
B7	FB_BUCK	AI	Buck output voltage feedback connection.
C1	VBAT_SNS	AI	Battery voltage sense connection. Connect to the positive battery terminal.
C2	ITER_CHG	AI	Termination current setting pin. Connect a resistor between ITER_CHG and ground to set the pre-charge and termination currents (ITER). Alternatively, short this pin to ground to allow ITER to be programmed by register setting.
C3	ILIM_CHG	AI	Fast-Charge current setting pin. Connect a resistor between ILIM_CHG and ground to set the fast-charge current (ICHG). Alternatively, short this pin to ground to allow ICHG to be programmed by register setting
C4	WD	DI	Watchdog input. Toggle WD within the watchdog time-out period to avoid power reset.
C5	RIN_N	DI	Manual reset input pin. RIN_N is internally pulled high. Pulling this pin low wakes the device from Ship Mode or performs a reset.
C6	SCL	DI	I^2C interface clock. Connect SCL to VDDIO through a 2 k to10 k pull-up resistor.
C7	AGND	GND	Quiet ground connection. Connect to a quiet ground area.
D1	VDD_BST	POWER	Input for Boost FET driver. Bypass with a minimum 1 µF capacitance.

Pin No.	Pin Name	Type (Table 2)	Description
D2	ILIM_PWR	AI	Input current limit setting pin. Connect a resistor between ILIM_PWR and ground to set the VDD_PWR current limit (ILIM). Alternatively, short this pin to ground to allow ILIM to be programmed by register.
D4	VBAT_DIV	AO	Battery voltage divider, positive output
D5	MODE	DI	Mode control input pin. MODE is internally pulled low. If VDD_PWR is powered, driving MODE high disables charging. If VDD_PWR is unpowered, driving MODE low enables Hi-Z mode.
D6	ROUT_N	DOD	Reset output pin. Connect this open-drain output to VDDIO through a 1 k to 100 k ohm pull-up resistor.
D7	PWR_FLT	DOD	Power status indicator output. Connect this open-drain output to VDDIO through a 1 K to 100 KOhm pull-up resistor. PWR_FLT pulls low when VDD_PWR is plugged into a valid power source.
E1	PGND_BST	POWER	Power ground for the boost regulator. Connect to the boost output capacitors and ground plane.
E2	VTEMP	AO	Switched VDD_SYS supply for battery temp sense resistor divider
E3	VDDIO	POWER	IO voltage
E4	GND_DIV	AO	Battery voltage divider, ground reference.
E5	VDD_LDO2	POWER	Input to Load Switch / LDO 2. Bypass to ground with a minimum 1 µF ceramic capacitor.
E6	VDD_LDO1	POWER	Input to Load Switch / LDO 1. Bypass to ground with a minimum 1 µF ceramic capacitor.
E7	VDD_LDO0	POWER	Input to Load Switch / LDO 0. Bypass to ground with a minimum 1 µF ceramic capacitor.
F1	SW_BST	POWER	The boost switching node. Connect to the boost inductor.
F2	VOUT_BST	POWER	Output of the boost converter. Bypass with a minimum of 10 µF.
F3	FB_BST	AI	Boost output voltage feedback connection.
F5	VLDO2	POWER	Load Switch or LDO2 output. Bypass to ground with a minimum 1 µF ceramic capacitor.
F6	VLDO1	POWER	Load Switch or LDO1 output. Bypass to ground with a minimum 1 µF ceramic capacitor.
F7	VLDO0	POWER	Load Switch or LDO0 output. Bypass to ground with a minimum 1 µF ceramic capacitor.

Table 2: Pin Type Definition

Pin Type	Description
DI	Digital input
GND	Ground
DIO	Digital input/output
DOD	Digital output open drain
POWER	Power
AI	Analog input
AO	Analog output

3 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_S	Storage temperature		-65	150	°C
V_{PWR}	VDD_PWR	1 V / µsec max slew rate	-0.3	22	V
V_{BAT}	VBAT, VBAT_SNS		-0.3	6	V
V_{SYS}	VDD_SYS, VDD_BUCK, SW_BUCK, VDD_BST, VDD_LDOx, VTEMP		-0.3	6	V
V_{IO}	VDDIO and all IO pins (unless otherwise stated)	Note 1	-0.3	6	V
V_{BST}	SW_BST, VOUT_BST, FB_BST		-0.3	22	V

Note 1 VDDIO and IO voltages must be less than the higher of VBAT or VDD_PWR.

4 Recommended Operating Conditions

Recommended operating conditions are conditions for which the device is intended to be functional, but parameter specifications may not be guaranteed. For guaranteed specifications and associated test conditions, refer to the Electrical Characteristics tables.

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating Ambient Temperature		-40		85	C
V_{DD_PWR}	VDD_PWR voltage	Including OVP range	3.6	5	20	V
	VDD_PWR operating voltage		3.6	5	5.5	V
V_{BAT}	Battery voltage	VDD_PWR supplied	0	3.7	4.7	V
	Battery voltage (act.bat)	VDD_PWR not supplied	2.5	3.7	4.7	V
V_{DD_LDO}	VDD_LDO voltage	Load switch mode	0.8		5.5	V
		LDO mode	1.8		5.5	V
V_{DDIO}	IO voltage	VDDIO < VDD_PWR or VBAT, whichever is greater	1.4	1.8	3.3	V
V_{DD_BST}	Boost input voltage		2.5		5.5	V
V_{DD_BUCK}	Buck input voltage	Note 1	2.5		5.5	V

Note 1 V_{DD_BUCK} must be greater than Buck output voltage +600 mV.

Table 5: Recommended External Components

Component values shown are typical values (not de-rated). For capacitors assume X5R type or better with a DC voltage rating of 2x the maximum applied voltage. For inductors, the saturation current rating is equal or greater than the current limit value. The Electrical Specifications are based on the typical values where applicable.

Parameter	Description	Conditions	Min	Typ	Max	Unit
$C_{\_VDD\_SYS}$	VDD_SYS capacitance		3.3	4.7	100	µF
$C_{\_VDD\_PWR}$	VDD_PWR capacitance		1.0	4.7	10	µF
$C_{\_VBAT}$	VBAT capacitance		1.0	2.2	10	µF
$C_{\_VO\_BUCK}$	Buck output capacitance			10		µF
$C_{\_VDD\_BUCK}$	Buck input capacitance		1.0	2.2		µF
$L_{\_BUCK}$	Buck inductor			2.2		µH
$C_{\_VO\_BOOST}$	Boost output cap.	1 MHz	4.7	10		µF
$C_{\_VDD\_BOOST}$	Boost input capacitance	VDD_BST connected to VDD_SYS	1.0	1.0		µF
		VDD_BST powered by independent supply		10		µF
$L_{\_BOOST}$	Boost inductor			4.7		µH

Parameter	Description	Conditions	Min	Typ	Max	Unit
$C_{\_VO\_LDO}$	LDO output capacitance		1.0	2.2	2.2	µF
$C_{\_VDD\_LDO}$	LDO input capacitance			1.0		µF

5 ESD Ratings

Parameter	Description	Conditions	Value	Unit
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 Note 1	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 Note 2	±500	

Note 1 JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Note 2 JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6 Electrical Characteristics

Electrical characteristics table limits are guaranteed by production testing, design, or correlation using standard statistical quality control methods unless otherwise stated. Typical (Typ) specifications are mean or average values 25 °C and are not guaranteed.

Unless otherwise noted, V_{BAT} = 3.7 V, V_{DD_SYS} = 3.7 V, V_{DD_PWR} = 5.0 V, V_{DDIO} = 1.8 V, T_A = -40 C to 85 C.

6.1 Battery Charger

Table 6: Battery Charger

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{DD\_SYS\_THR\_DPPM}$	VDD_SYS DPPM voltage threshold	VDD_SYS falling, above V_{BAT_CHG}		0.2		V
$R_{ON\_CHG\_INT}$	battery charger MOSFET on-resistance	Measured from V_{BAT} to V_{VDD_SYS}		300	400	mΩ
$V_{DROP\_BAT\_TO\_VDD\_SYS}$	V_{VBAT} - V_{VDD_SYS}	$_{VBAT}$ > 3 V, IBAT discharge = 400 mA		120	160	mV
V_{BAT_SUP}	Threshold to enter the battery supplement mode	V_{VBAT} > V_{VBAT_UVLO}		VDD_ SYS < VBAT		V
$I_{BAT\_DCHG\_RNG}$	Discharge current limit setting range	Selectable 0.2A / step	0.55		1.75	A
V_{BAT_CHG}	Charge voltage range	Operating in voltage regulation, programmable range in 10mV steps	3.6		4.65	V
$V_{BAT\_CHG\_ACC}$	Charge voltage accuracy	0°C< T_J < 85°C	-0.5		0.5	%
I_{CHG}	Fast charge current range		2		500	mA
I_{CHG_ACC}	Fast charge current accuracy		-5		5	%
I_{TER_RNG}	Termination and pre-charge current setting range	Termination current programmable range maximum over I^2C.	0.5		50	mA
I_{TER_ACC}	Termination charge current accuracy	Peak current below termination threshold	-10		10	%
$t_{TER\_DEGLITCH}$	Termination deglitch time	Charge current falling		64		ms
$V_{THR\_PRE\_TO\_FASTCHG}$	Pre charge to fast charge threshold voltage range		2.7		3.2	V
$I_{CHG\_PRE\_ACC}$	Pre-charge current accuracy	VBAT > 2V	-10		10	%

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{RCHG}	Recharge threshold voltage	VBAT below V_{BAT_CHG}	100	120	140	mV
$t_{RCHG\_DEGLITCH}$	Recharge threshold deglitch time	t_{FALL} = 100 ns typ, V_{RCHG} falling		32		ms

6.2 Battery Temperature Monitor

Table 7: Battery Temperature Monitor

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{TEMP_HI}	High temperature threshold	% of VVDD_SYS, VTEMP_SNS falling	14.5	15	15.2	%
V_{TEMP_WARM}	Warm threshold	% of VVDD_SYS, VTEMP_SNS falling	20.1	20.5	20.8	%
V_{TEMP_COOL}	Cool threshold	% of VVDD_SYS, VTEMP_SNS rising	34.4	35	35.4	%
V_{TEMP_LO}	Low temperature threshold	% of VVDD_SYS, VTEMP_SNS rising	39.3	39.8	40.2	%
$V_{OFF\_TEMP\_SNS}$	TEMP_SNS disable threshold	% of $V_{VDD_SYS}$for rising V_{TEMP_SNS}	55		60	%
$t_{TEMP\_SNS\_DEGLITCH}$	TEMP_SNS deglitch time	TEMP_SNS at any threshold		10		ms

6.3 LDO / Load Switches

Table 8: LDO0/Loadswitch (LV)

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{IN\_LDSW\_0}$	Input voltage range for LDSW	Load Switch mode V_{VDD_LDO} > V_{VLDO}	0.8		5.5	V
$V_{IN\_LDO\_0}$	Input voltage range for LDO	LDO mode, V_{VDD_LDO} > V_{VLDO}	1.8		5.5	V
$V_{OUT\_ACC\_LO\_0}$	DC output accuracy	V_{VDD_LDO} > V_{VLDO} + 0.2V	-3		3	%
$V_{OUT\_LDO\_0}$	Output range	Programmable range, 50mV or 75mV steps	0.8		3.15	V
$V_{OUT\_LINE\_0}$	DC line regulation	1.8V < V_{VDD_LDO} < 5.5V I_{OUT}=500uA	-0.8		0.8	%
$V_{OUT\_LD\_0}$	DC load regulation	0< I_{OUT} < 50 mA, V_{VDD_LDO} =1.85V V_{VLDO} =1.8V	-3		0	%
$V_{OUT\_TR2\_LD\_0}$	Load transient	2u to 50 mA, 100mA/usec, VVDD_LDO >2.0V VVLDO=1.8V	-120		60	mV
$V_{OUT\_TR\_LD\_0}$	Load transient	2u to 50 mA, 100mA/usec, VVDD_LDO =1.85V VVLDO=1.8V	-140		60	mV
$R_{ON\_LDSW\_ILIM\_0}$	On resistance of LDSW mode with current limit	V_{VDD_LDO} = 3.7V		0.7		Ω
$R_{ON\_LDSW\_NO\_ILIM\_0}$	On resistance of LDSW mode without current limit	V_{VDD_LDO} = 3.7V		0.11		Ω
$R_{DCHG\_LDO\_ON\_0}$	MOSFET on-resistance for LDO discharge	I_{LOAD} = -10 mA		32		Ω
$I_{LIM\_OUT\_LDO\_0}$	Output current limit for LDO mode	V_{LDO} = 0.9 x $V_{LDO(nom)}$	155			mA
$I_{OUT\_LDO\_LO\_0}$	Output current	V_{VDD_LDO} =1.85V V_{LDO} = 1.8V			50	mA
$I_{OUT\_LDO\_HI\_0}$	Output current	V_{VDD_LDO} > V_{VLDO} + 0.2V V_{VLDO} = 1.8 V			150	mA
$I_{IN\_LDO\_ON\_0}$	Quiescent current	LDO mode		0.75		µA
$I_{IN\_LDO\_OFF\_0}$	OFF-state supply current			0.001		µA
$PSRR_{vddldo\_0}$	Power supply rejection ratio	@10KHz, IOUT=75mA		43		dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{START_LDO0}	LDO start-up delay time			20		ms

Table 9: LDO1/Loadswitch

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{IN\_LDSW\_1}$	Input voltage range for Load Switch	Load Switch mode V_{VDD_LDO} > V_{VLDO}	0.8		5.5	V
$V_{IN\_LDO\_1}$	Input voltage range for LDO	LDO mode, V_{VDD_LDO} > V_{VLDO}	1.8		5.5	V
$V_{OUT\_ACC\_LO\_1}$	DC output accuracy	V_{VDD_LDO} > V_{VLDO} + 0.2V	-3		3	%
$V_{OUT\_LDO\_1}$	Output range	Programmable range, 50mV or 75mV steps	0.8		3.3	V
$V_{OUT\_LINE\_1}$	DC line regulation	1.8V < V_{VDD_LDO} < 5.5V I_{OUT}=500uA	-0.8		0.8	%
$V_{OUT\_LD\_1}$	DC load regulation	2uA < I_{OUT} < 100 mA, V_{VDD_LDO} > V_{VOUT_LDO} + 0.2V, V_{VLDO}=3.0V	-3		0	%
$V_{OUT\_TR\_LD\_1}$	Load transient	2uA to 100 mA, 100mA/usec, VVDD_LDO > VVLDO + 0.2V, VVLDO=3.0V	-120		60	mV
$R_{ON\_LDSW\_ILIM\_1}$	On resistance of LDSW mode with current limit	V_{VDD_LDO} = 3.7V		1.5		Ω
$R_{ON\_LDSW\_NO\_ILIM\_1}$	On resistance of LDSW mode without current limit	V_{VDD_LDO} = 3.7V		0.27		Ω
$R_{DCHG\_LDO\_ON\_1}$	MOSFET on-resistance for LDO discharge	I_{LOAD} = -10 mA		32		Ω
$I_{LIM\_OUT\_LDO\_1}$	Output current limit (LDO MODE)	V_{LDO} = 0.9 x $V_{LDO(nom)}$	155			mA
$I_{OUT\_LDO\_HI1\_1}$	Output current	V_{VDD_LDO} > V_{VLDO} + 0.2V			150	mA
$I_{IN\_LDO\_ON\_1}$	Quiescent current	LDO mode		0.8		µA
$I_{IN\_LDO\_OFF\_1}$	OFF-state supply current			0.001		µA
$PSRR_{vddldo\_1}$	Power supply rejection ratio	@10KHz, IOUT=75mA		40		dB
t_{START_LDO1}	LDO start-up delay time			20		ms

Table 10: LDO2/Loadswitch

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{IN\_LDSW\_2}$	Input voltage range for Load Switch	Load Switch mode, V_{VDD_LDO} > V_{VLDO}	0.8		5.5	V
$V_{IN\_LDO\_2}$	Input voltage range for LDO	LDO mode, V_{VDD_LDO} > V_{VLDO}	1.8		5.5	V
$V_{OUT\_ACC\_LO\_2}$	DC output accuracy	V_{VDD_LDO} > V_{VLDO} + 0.2V	-3		3	%
$V_{OUT\_LDO\_2}$	Output range for LDO	Programmable range, 50mV or 75mV steps	0.8		3.3	V
$V_{OUT\_LINE\_2}$	DC line regulation	1.8V < V_{VDD_LDO} < 5.5V I_{OUT}=500uA	-0.8		0.8	%
$V_{OUT\_LD\_2}$	DC load regulation	2uA < I_{OUT} < 100 mA, V_{VDD_LDO} > V_{VOUT_LDO} + 0.2V, V_{VLDO}=3.0V	-3		0	%
$V_{OUT\_TR\_LD\_2}$	Load transient	2uA to 100 mA, 100mA/usec, VVDD_LDO > VVLDO + 0.2V, VVLDO=3.0V	-120		60	mV
$R_{ON\_LDSW\_ILIM\_2}$	On resistance of LDSW mode with current limit	V_{VDD_LDO} = 3.7V		1.5		Ω
$R_{ON\_LDSW\_NO\_ILIM\_2}$	On resistance of LDSW mode without current limit	V_{VDD_LDO} = 3.7V		0.27		Ω
$R_{DCHG\_LDO\_ON\_2}$	MOSFET on-resistance for LDO discharge	I_{LOAD} = -10 mA		32		Ω
$I_{LIM\_OUT\_LDO\_2}$	Output current limit (LDO MODE)	V_{LDO} = 0.9 x $V_{LDO(nom)}$	155			mA
$I_{OUT\_LDO\_HI1\_2}$	Output current	V_{VDD_LDO} > V_{VLDO} + 0.2V			150	mA
$I_{IN\_LDO\_ON\_2}$	Quiescent current	LDO mode		0.8		µA
$I_{IN\_LDO\_OFF\_2}$	OFF-state supply current			0.001		µA
$PSRR_{vddldo\_@}$	Power supply rejection ratio	@10KHz, IOUT=75mA		35		dB
t_{START_LDO2}	LDO start-up delay time			20		ms

6.4 Digital Inputs (MODE and WD)

Table 11: Digital Input Pins (MODE,WD)

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
t_{MIN_WD}	WD minimum input pulse width			25		µs
Electrical Performance						
V_{IN_LO}	Input low threshold				0.25*VDDIO	V
V_{IN_HI}	Input high threshold		0.75*VDDIO			V
R_{PD_MODE}	Internal pull-down resistance			900		kΩ
$t_{\_DEGLITCH\_MODE}$	MODE pin deglitch time	rising/falling		100		µs

6.5 I²C Interface

Table 12: I2C Interface

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
f_{I2C_CLK}	SCL frequency range		100		400	kHz
V_{OUT_LO}	Output low threshold level	SDA 5mA sink current			VDDIO*0.25	V
V_{IN_LO}	Input low threshold level	Input low threshold level for SDA and SCL			VDDIO*0.25	V
V_{IN_HI}	Input high threshold level	Input high threshold level for SDA and SCL	VDDIO*0.75			V
I_{LKG_HILVL}	leakage current	SDA and SCL, high level			1	µA

6.6 Input Currents

Table 13: Input Currents

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$I_{BAT\_HIZ\_BUCK\_ON\_LDO\_OFF}$	Battery discharge current in Hiz mode, no LDO enable	0 °C < T_J < 60 °C, V_{VDD_PWR} = 0V or floating, Hi-Z mode, Buck switching, no load		0.8	1.5	µA
$I_{BAT\_HIZ\_BUCK\_ON\_LDO0\_ON}$	Battery discharge current in Hiz mode, LDO_0 enable	0 °C < T_J < 60 °C, V_{VDD_PWR} = 0V, Hi-Z mode, Buck switching, LDO_0 enabled, No load		1.6		µA
$I_{BAT\_ACT\_LDO0\_LDO1\_ON}$	Battery discharge current in Active battery mode	0 °C < T_J < 85 °C, V_{VDD_PWR} = 0V, Active battery mode, Buck switching, LDO_0 + LDO_1 enabled, I²C enabled, V_{BAT_UVLO} < V_{BAT} < 4.65 V		2.5		µA
$I_{BAT\_ACT\_BUCK\_ON\_LDO\_OFF}$	Battery discharge current in Active battery mode	0 °C < T_J < 85 °C, V_{VDD_PWR} < $V_{VDD\_PWR\_UVLO}$, Active battery mode, Buck switching, LDO disabled, I²C enabled, MODE = low, V_{BAT_UVLO} < V_{BAT} < 4.65 V		1.1		µA
I_{BAT_SHIP}	Battery discharge current in ship mode	0 °C < T_J < 85 °C, V_{VDD_PWR} = 0V, Ship mode		2	200	nA
$I_{IN\_BUCK\_ON}$	Supply Current for control	V_{VDDPWR_UVLO} < V_{VDD_PWR} < V_{OVP} and V_{VDD_PWR} > V_{VBAT} + V_{SLP} Buck switching,		0.8	3	mA
$I_{IN\_CHG\_READY}$	Supply Current for control	0 °C < T_J < 85 °C, V_{VDD_PWR} = 5 V, Charge ready			1.5	mA

6.7 Power-Path Management and Current Limit

Table 14: Power-Path Management and ILIM

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$I_{USBSUSPEND}$	Input current in USB suspend mode				2.5	mA
$V_{DROP\_IN\_TO\_VDD\_SYS}$	V_{DD_PWR} - V_{VDD_SYS}	V_{VDD_PWR} = 5 V, I_{IN} = 300 mA, includes ball resistance		125	170	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{DDPWR\_LIM\_MAX}$	Input Current limit	Programmable Range MAX, 50-mA steps		600		mA
$I_{DDPWR\_LIM\_MIN}$	Input Current limit	Programmable Range MIN, 50-mA steps		50		mA
$I_{DDPWR\_LIM\_ACC\_RNG\_LO}$	Current limit accuracy	50 mA to 100 mA	-12		12	%
$I_{DDPWR\_LIM\_ACC\_RNG\_HI}$	Current limit accuracy	100 mA to 600 mA	-5		5	%
$V_{DDPWR\_IIN\_DWN}$	DPM threshold	At VDD_PWR, programmable range, 100mV steps	4.2		4.9	V
$V_{DDPWR\_IIN\_DWN\_ACC}$	DPM threshold accuracy		-3		3	%

6.8 Protection

Table 15: Protection

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{BAT\_SHRT\_THR}$	Battery short circuit threshold	Battery voltage falling, VDD_PWR=5V		2		V
$V_{BAT\_SHRT\_HYS}$	Hysteresis for V_{BAT_SHRT}			100		mV
I_{BAT_SHRT}	Battery short circuit charge current			ITER		mA
$V_{BAT\_UVLO\_THR}$	Battery under-voltage lockout threshold range	Programmable range, 100mV steps VBAT falling	2.5		3	V
$V_{BAT\_UVLO\_ACC}$	Default battery under-voltage lockout accuracy	VBAT_UVLO=2.5V	-3		3	%
$V_{BAT\_UVLO\_HYS}$	Battery under-voltage lockout threshold hysteresis			200		mV
V_{DDPWR_OVP}	VDD_PWR over voltage protection threshold voltage	V_{VDD_PWR} rising	5.35	5.55	5.75	V
$V_{DDPWR\_OVP\_HYS}$	Over voltage protection hysteresis			100		mV
$t_{DEGLITCH\_OVP}$	Over voltage protection recovery deglitch time	V_{VDD_PWR} falling		32		ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{SLP}	Sleep entry threshold	VVDD_PWR - VBAT , VDD_PWR falling		65	120	mV
V_{SLP_HYS}	Sleep-mode hysteresis	V_{VDD_PWR} rising	80	130	200	mV
T_{SHDN}	Thermal shutdown	TJ		118		°C
T_{HYS}	Thermal shutdown hysteresis	TJ		20		°C
$t_{DEGLITCH\_TH\_SHDN}$	Thermal shutdown deglitch time	T_J rising		1		ms
$V_{DDPWR\_UVLO\_HYS}$	VDD_PWR under-voltage lockout threshold hysteresis	V_{VDD_PWR} falling		150		mV
$V_{DDPWR\_UVLO\_THR}$	VDD_PWR under-voltage lockout threshold	V_{VDD_PWR} rising	3.4	3.6	3.8	V

6.9 Pushbutton Timer (RIN_N)

Table 16: Pushbutton Timer(RIN_N)

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{RIN\_N\_LOLVL}$	Low-level input voltage				0.3	V
$R_{PU\_RIN\_N}$	Internal pull-up resistance			120		kΩ

6.10 Digital Outputs (SYS_FLT, PWR_FLT, and ROUT_N)

Table 17: Digital Output Pins (SYS_FLT, PWR_FLT, and ROUT_N)

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{OUT_LO}	Low level output threshold	Sinking current = 5 mA			0.25*VDDIO	V
$I_{LKG\_TO\_IN}$	Leakage current into pin	High impedance state		0	12	nA
t_{INTR}	Interrupt pulse width	SYS_FLT		128		µs
t_{RST_D}	Reset pulse duration	ROUT_N		400		ms

6.11 Buck Regulator

Table 18: Buck

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
R_{ON_PMOS}	High-side on resistance			600	800	mΩ
R_{ON_NMOS}	Low-side on resistance			300	450	mΩ
t_{START}	Start-up delay time	From BUCK_EN =1 to switching		3		ms
$I_{LIM\_SW\_PMOS}$	SW current limit PMOS	$_{VFB\_BUCK}$=1.8V		600		mA
t_{OFF_BUCK}	Off time	VFB_BUCK=1.8V		270		ns
f_{SW_BUCK}	Switching frequency	Continuous conduction mode			3	MHz
$I_{LIM\_PMOS\_SOFTSTART}$	PMOS switch current limit during softstart			300		mA
$V_{OUT\_FB\_BUCK}$	Buck output voltage range	Programmable range, 50 mV steps ($V_{OUT\_FB\_BUCK\_HI}$ > 1.9V, V_{VDD_BUCK}>2.7V)	0.6		2.1	V
$V_{OUT\_FB\_BUCK\_HI}$	Buck output voltage range	HI programmable range, 50 mV steps, $V_{OUT\_RANGE\_HI}$ = 1	1.3		2.1	V
$V_{OUT\_FB\_BUCK\_LO}$	Buck output voltage range	LO programmable range, 50 mV steps, $V_{OUT\_RANGE\_HI}$ = 0	0.6		1.3	V
$V_{OUT\_VBUCK\_OUT\_ACC}$	Buck output voltage accuracy	V_{VDD_BUCK} = 5 V, PFM mode, I_{OUT} = 10 mA, $_{VFB\_BUCK}$ = 1.8 V	-2.5	0	2.5	%
$V_{OUT\_LD1\_BUCK}$	DC output voltage load regulation	V_{OUT} = 1.8 V 100 mA < I_{OUT} < 300 mA		0.01		%/mA
$V_{OUT\_LD2\_BUCK}$	DC output voltage load regulation	V_{OUT} = 0.9 V 100 mA < I_{OUT} < 300 mA		0.02		%/mA
$V_{OUT\_LINE\_BUCK}$	DC output voltage line regulation	V_{OUT} = 1.8 V I_{OUT} = 100 mA		0.1		%/V
$t_{STARTUP\_BUCK}$	Softstart time	Vout=1.8V, no load		50		µs
$t_{STARTUP\_L}$	Softstart time	VOUT = 0.9 V No load		25		µs

6.12 Boost Regulator

Table 19: Boost

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$t_{STARTUP}$	Startup time	V_{VBAT}=3.7 V, C_{OUT}=2.2 uF, V_{BST_OUT}=12 V	2	5		ms
I_{Q_SHDN}	Quiescent current	V_{VDD_BST}=4.65 V Boost disabled		1	100	nA
$V_{OUT\_BST\_HI}$	Output voltage range, 250 mV step size		9	12	18	V
$V_{OUT\_BST\_LO}$	Output voltage range, 125 mV step size		4.5		9	V
V_{SCP_HI}	SCP threthhold for higher Vout range	VOUT_BST=9V to 18V		4		V
V_{BST_UVLO}	Boost UVLO			2.38		V
V_{SCP_LO}	SCP threthhold for lower Vout range	VOUT_BST=4.5V to 9V		2		V
V_{OVP}	OVP threshhold	Referenced to nominal VOUT_BST setting		120		%
V_{OVP_RLS}	OVP threshhold	Referenced to nominal VOUT_BST setting		100		%
V_{OUT_ACC}	Boost output voltage accuracy	V_{VDD_BST} = 3.7 V, V_{BST_OUT} = 12 V ,I_{OUT}=10mA	-2.5		2.5	%
R_{ON_SHDN}	True shutdown, RDSon resistance			100	200	mΩ
R_{ON_LS}	Low side, RDSon resistance			300		mΩ
I_{LIM_POS}	Peak current limit	Programmable range	0.9		2.1	A
$I_{LIM\_POS\_ACC}$	Peak current limit accuracy		-30		30	%
$I_{LIM\_SOFTSTART}$	Softstart current limit	Programmable range	0.51		0.92	A
$f_{SW\_BST\_1M}$	Switching frequency	Typical value depends on OTP setting. 1MHz	0.95	1	1.05	MHz
$f_{SW\_BST\_2M}$	Switching frequency	Typical value depends on OTP setting. 2MHz	1.9	2	2.1	MHz
t_{ON_BST}	Minimum on time			105		ns
t_{OFF_BST}	Minimum off time			100		ns

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OUT_LD}	Boost load reg	VOUT = 12 V 1mA < Iload < 100mA		0.0015		%/mA
V_{OUT_LINE}	Boost line reg	VOUT = 12 V Iload=10mA		0.2		%/V

6.13 Battery Monitors (VBAT_DIV and IMON)

Table 20: Battery Monitors (VBAT_DIV and IMON)

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
A_{IMON_GAIN}	IMON current gain			1		mA/A
I_{IMON}	VBAT IQ current increase with IMON enabled	0 A discharge current			4	µA
$I_{MON\_ACC\_HI}$	IMON accuracy	Discharge current range 100 mA to 1 A	-20		20	%
$I_{MON\_ACC\_LO}$	IMON accuracy	Discharge current range 10 mA to 100 mA	-40		40	%
V_{IMON_MAX}	IMON maximum recommended voltage	2.5 V <V_{BAT}< 4.7 V I_{IMON} x R_{IMON}	1.4			V
R_{BAT_DIV}	Voltage divider resistance	From VBAT_SNS to GND_DIV		150		kΩ
V_{BAT_DIV1}	Voltage	2.5 V < V_{BAT} < 4.65 V 0 °C < T_J < 85 °C	VBAT* 0.585	VBAT* 0.6	VBAT* 0.615	V
V_{BAT_DIV2}	Voltage	2.5 V < V_{BAT} < 4.65 V 0 °C < T_J < 85 °C	VBAT* 0.285	VBAT* 0.3	VBAT* 0.315	V

7 Thermal Characteristics

Table 21: Thermal Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
$R_{TH\_JA\_A}$	Junction-to-ambient thermal resistance	JEDEC 8-layer pcb, no airflow		34		°C/W
R_{PSI_JC}	Junction-to-case (top) thermal resistance	Ψ_{JT}		0.5		°C/W
R_{TH_JB}	Junction-to-board thermal resistance	1 mm from IC edge		10		°C/W
$R_{TH\_JA\_B}$	Junction-to-ambient thermal resistance	25 mm x 25 mm pcb, 8-layer, no airflow		79		°C/W

8 Typical Performance

Unless otherwise noted, V_{BAT} = 3.6 V, T_A =25 °C

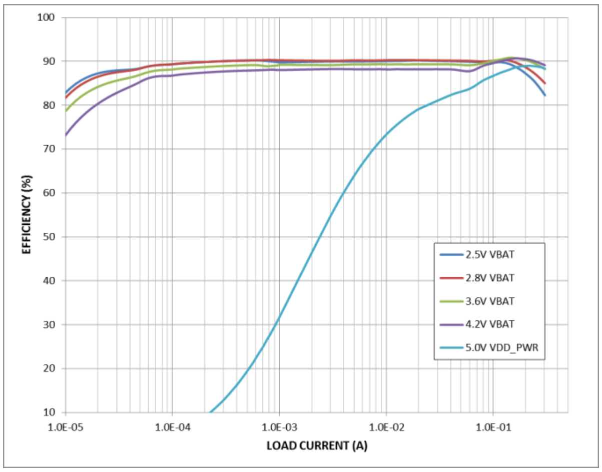


Figure 3: Buck Efficiency, V_{OUT} = 1.8 V

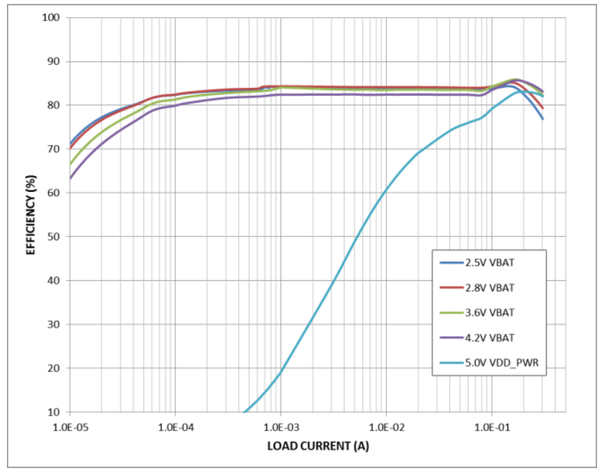


Figure 5: Buck Efficiency, V_{OUT} = 0.9 V

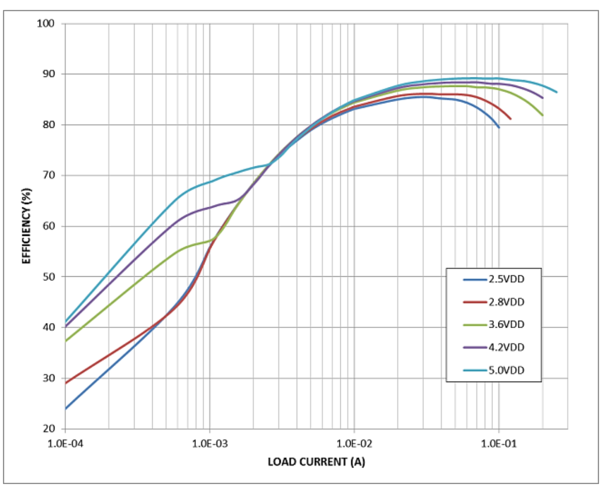


Figure 4: Boost Efficiency, V_{OUT} = 12 V, V_{IN} = V_{DD_BST}

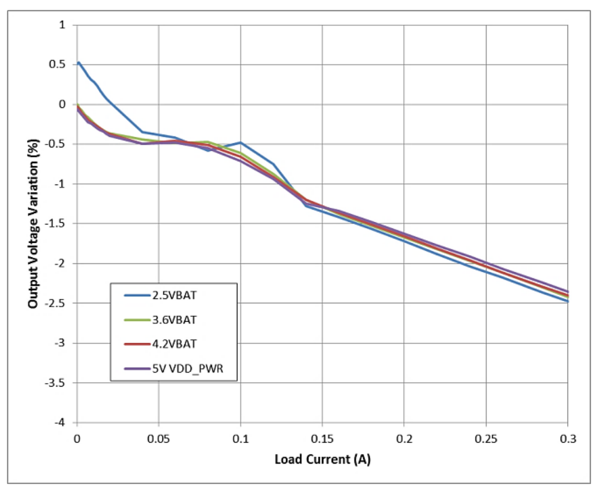


Figure 6: Buck Regulation, V_{OUT} = 1.8 V

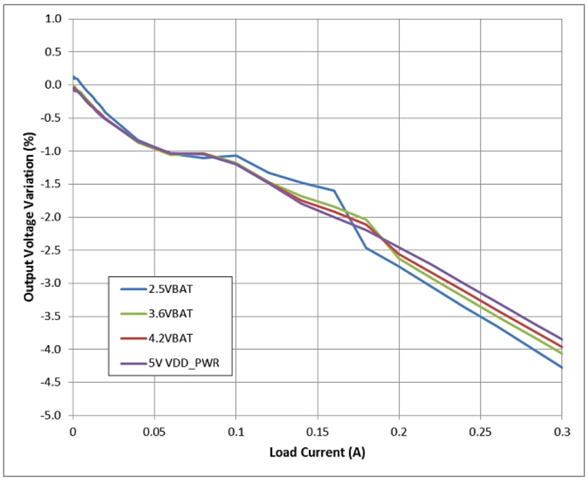


Figure 7: Buck Regulation, V_{OU} = 0.9 V

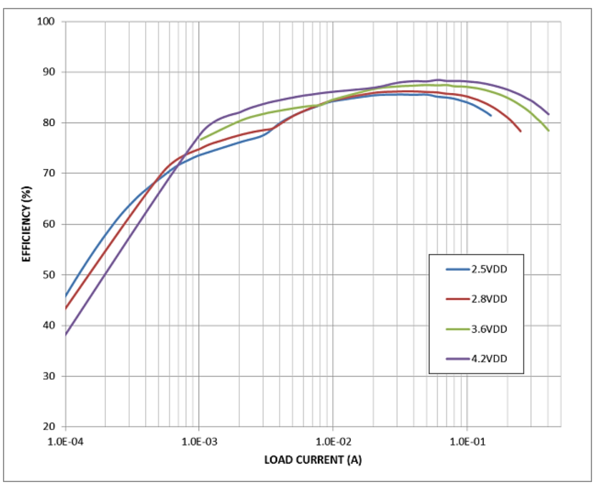


Figure 8: Boost Efficiency, V_{OUT} = 5 V, V_{IN} = V_{DD_BST}

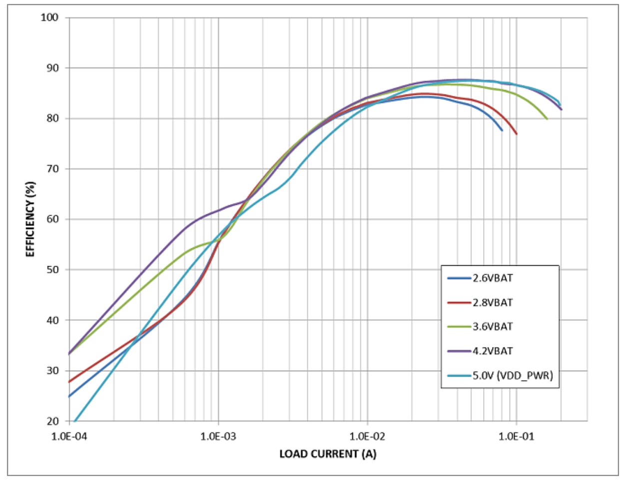


Figure 9: Boost Efficiency, V_{OUT} = 12 V, V_{IN} = V_{BAT}

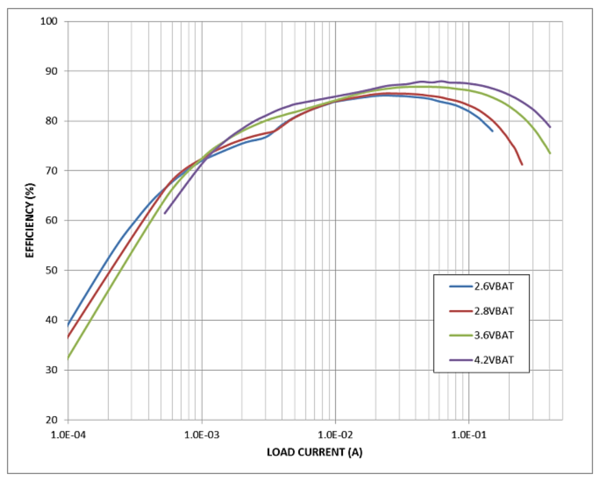


Figure 10: Boost Efficiency, V_{OUT} = 5 V, V_{IN} = V_{BAT}

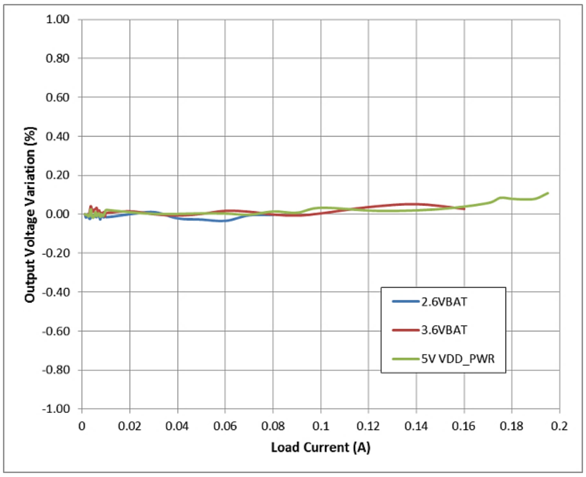


Figure 11: Boost Regulation, V_{OUT} = 12 V

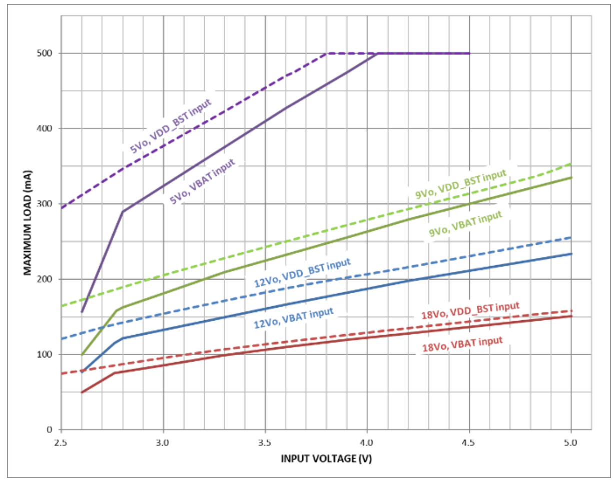


Figure 13: Boost Maximum Load Current Capability

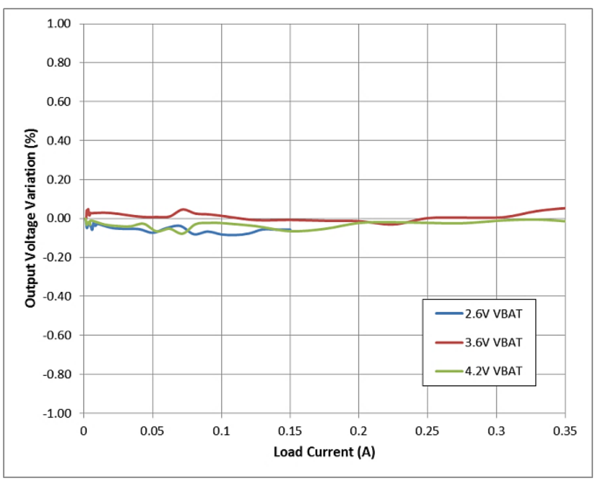


Figure 12: Boost Regulation, V_{OUT} = 5 V

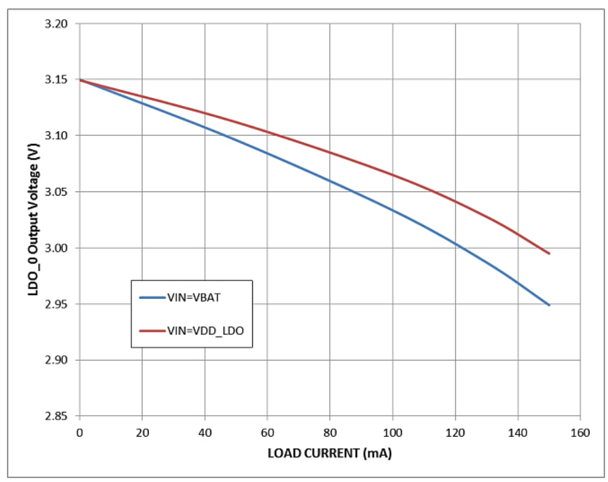


Figure 14: LDO_0 Dropout, V_{IN} = 3.15 V, V_{OUT} Setting = 3.15 V

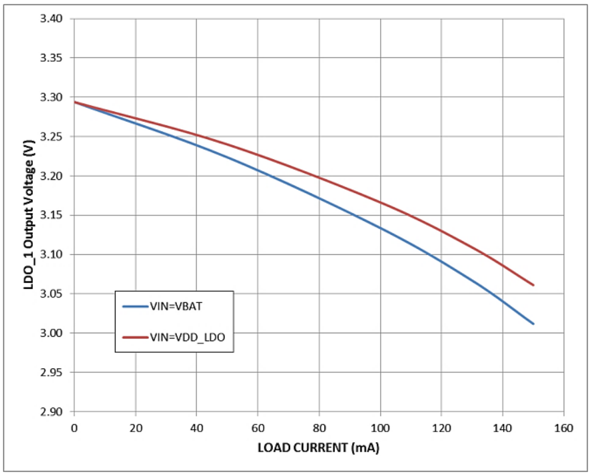


Figure 15: LDO_1 and LDO_2 Dropout, V_{IN} = 3.3 V, V_{OUT} Setting = 3.3 V

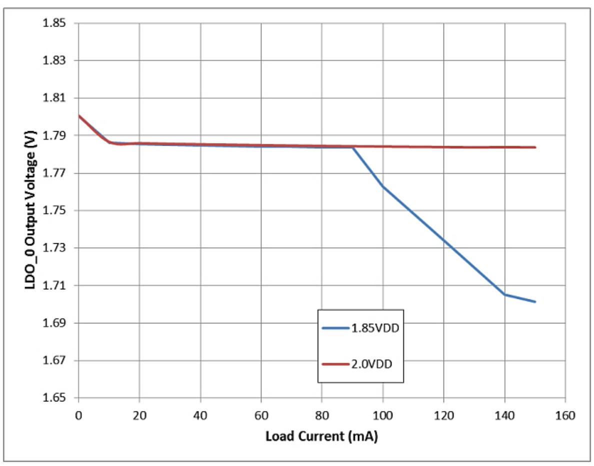


Figure 16: LDO_0 Regulation and Dropout, V_{OUT} = 1.80 V

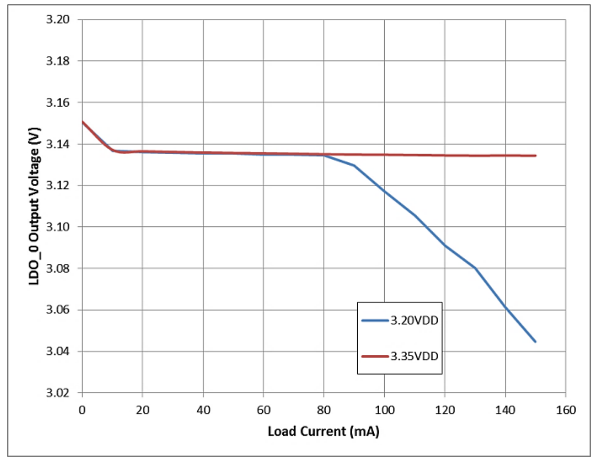


Figure 17: LDO_0 Regulation and Dropout, V_{OUT} = 3.15 V

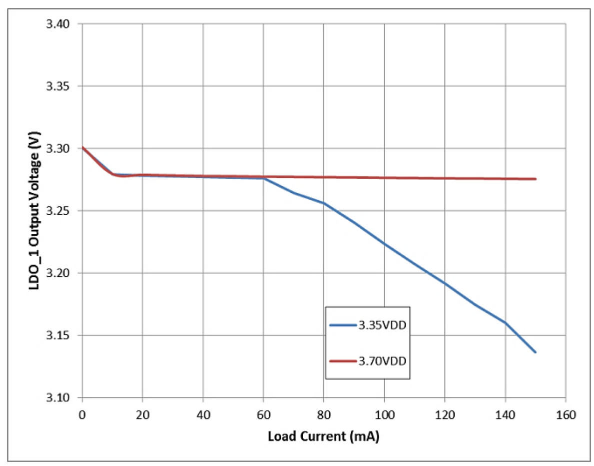


Figure 18: LDO_1 Regulation and Dropout, V_{OUT} = 3.30 V

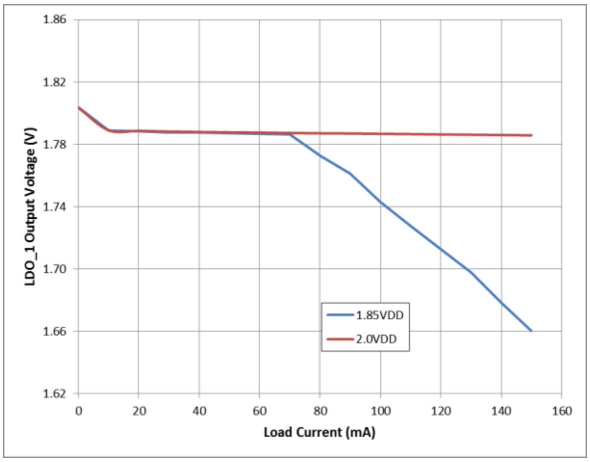


Figure 19: LDO_1 Regulation and Dropout, V_{OUT} = 1.80 V

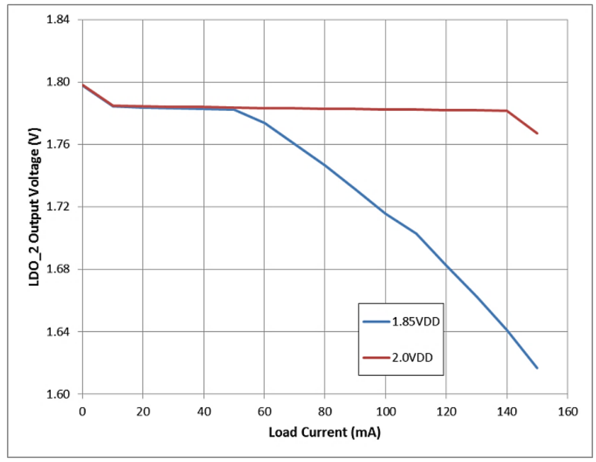


Figure 21: LDO_2 Regulation and Dropout, V_{OUT} = 1.80 V

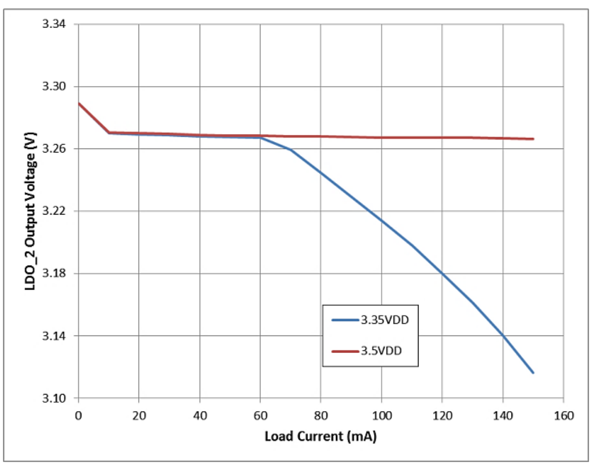


Figure 20: LDO2 Load Regulation, V_{OUT} = 3.30 V

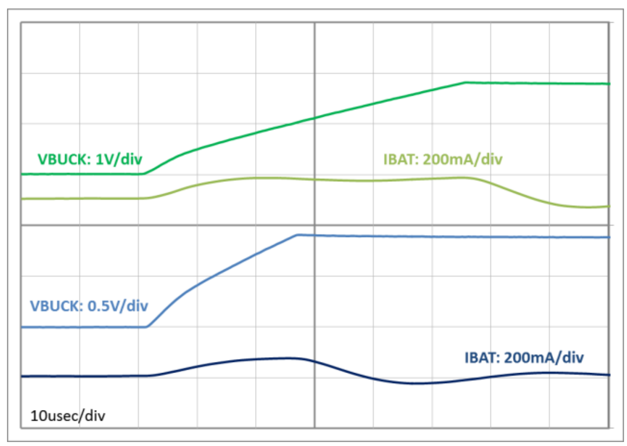


Figure 22: Typical Buck Startup, V_{BAT} = 3.6 V, V_{BUCK} = 1.8 V and 0.9 V, 0 A

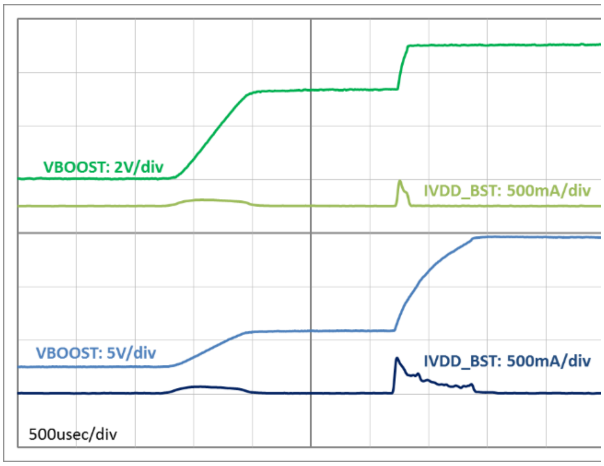


Figure 23: Typical Boost Startup, V_{DD_BST} = 3.6 V, V_{OUT} = 5 V and 12 V, 0 A

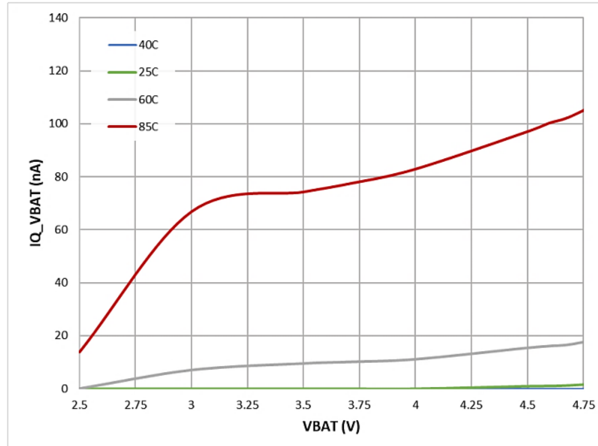


Figure 25: VBAT IQ, Ship Mode

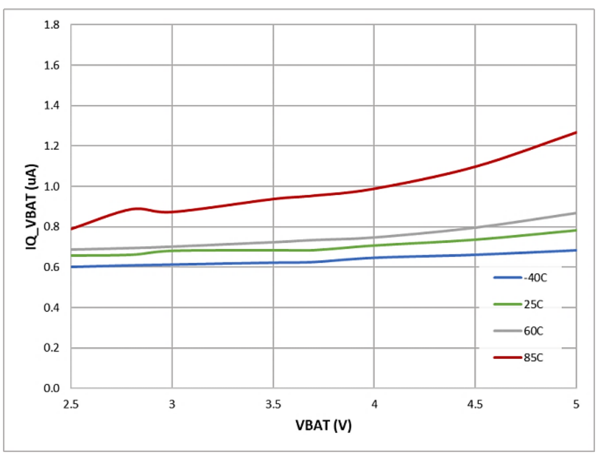


Figure 24: VBAT IQ, Buck Switching, no load, Hi-Z mode

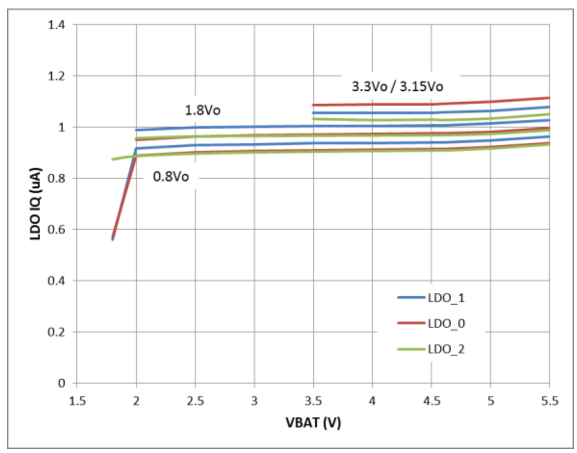


Figure 26: VDD_LDO IQ, no load

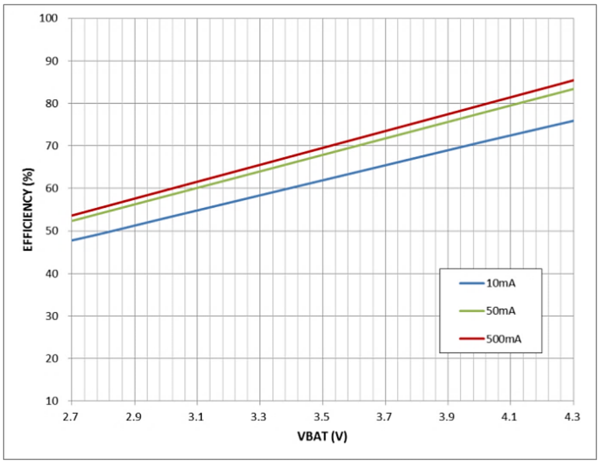


Figure 27: Charger Efficiency, V_{DD_PWR} = 5 V

9 Functional Description

9.1 Overview

In a typical application, the DA9070 manages to two power inputs: a battery at VBAT and a USB supply at VDD_PWR. The larger of these supplies feeds the unregulated system output voltage at VDD_SYS. VDD_SYS in turn is used as the input supply to the linear charger, buck, boost, and LDOs. Due to its extremely low IQ (< 1 µA), the buck can remain always on as the primary system power rail without draining the battery excessively.

When USB power is present, VDD_SYS will be near 5 V and the linear charger is active. When USB power in not connected, VDD_SYS will track the battery voltage. Battery discharge current can be monitored using the IMON pin. The DA9070 actively manages this power path, reducing charging current and input current as necessary, and allowing VDD_SYS to draw current from both supplies during peak loads.

The DA9070 includes multiple configurable protection features including battery and input over-current. All settings can be controlled by I2C, but stand-alone operation is also possible with features such as a pushbutton input timer, resistor programmable charge settings, and the MODE pin to enable and disable charging.

As there are two input sources, the DA9070 has multiple regions of operation, illustrated below in Figure 28.

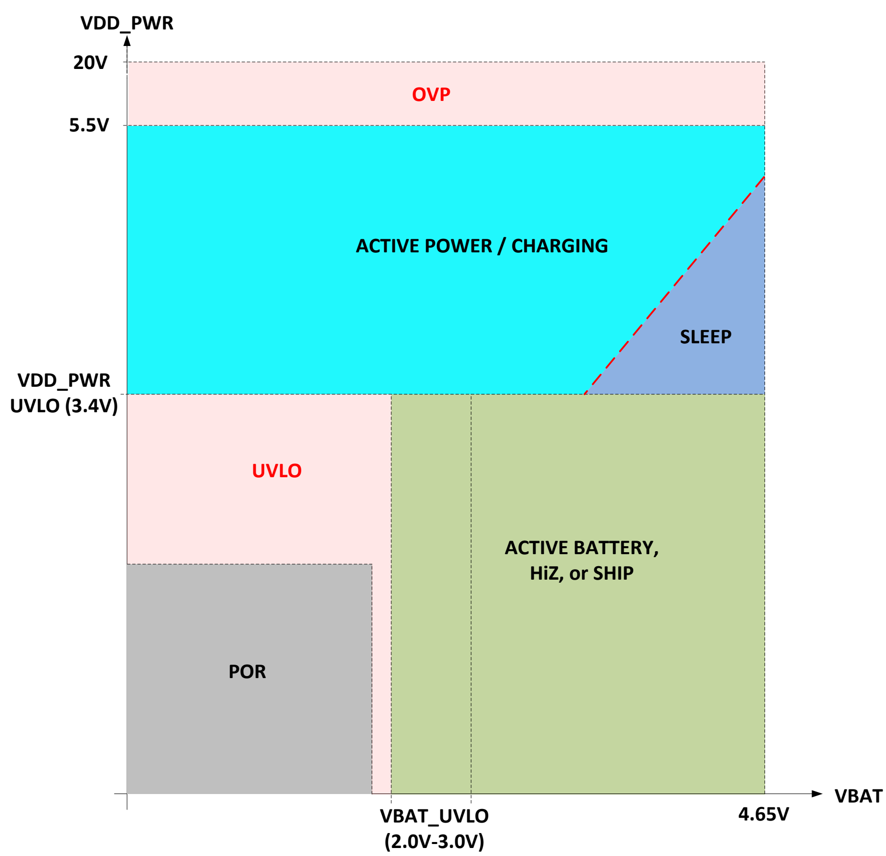


Figure 28: Regions of Operation

9.2 Battery-Powered Operation

When the power source is unplugged (VDD_PWR < UVLO), the DA9070 is battery-powered provided that VBAT exceeds VBAT_UVLO (register 0x0E). In this condition, the device will be in one of three modes: Ship mode, Active battery mode, or High Impedance mode (Hi-Z).

9.2.1 Ship Mode

Ship mode is an ultra low leakage standby state that minimizes battery depletion while the product sits on the shelf. Typical battery current in ship mode is 5 nA.

There are two methods to enter Ship mode:

1. By Register Write
    a. VDD_PWR disconnected
    b. MODE pin high
    c. Enter Ship mode by setting EN_SHIPMODE bit high: 0x0D [0] = 1
    d. The IC enters Ship mode immediately

(If VDD_PWR is plugged in, Ship mode entry is delayed until power is removed)

2. By Pushbutton Timer pin, RIN_N
    a. VDD_PWR disconnected
    b. MODE pin high
    c. Enable RIN_N control of ship mode: 0x10 [1:0] = 0x01
    d. Pull RIN_N low for longer than the reset period: RIN_N_PER_RST (0x10 [7:6])
    e. The IC enters Ship mode when RIN_N is released (internally pulled up)

To exit Ship mode, apply VDD_PWR or toggle RIN_N low for longer than 50 msec. Upon waking from Ship mode, all pre-programmed OTP values are loaded.

9.2.2 Active Battery and High Impedance Modes

Under battery power there are two modes of operation, controlled by the MODE pin. A rising edge on MODE puts the DA9070 in Active Battery mode. In this mode, all functions are active.

Conversely, a falling edge on MODE puts the DA9070 into Hi-Z mode, intended to be used during system standby states with low power consumption. In this mode, the following communication functions are placed in a high impedance mode to reduce leakage from the battery: I^2C interface, the SYS_FLT and PWR_FLT status outputs, and watchdog timer (WD).

All other functions and outputs remain active, with the exception of TSD.

Caution: The Thermal Shutdown function is not active in Hi-Z mode. Hi-Z mode should not be used in high power dissipation or heavy load conditions.

Hi-Z mode can also be entered by setting the HZ_MODE bit to 1 (0x0D [1]); or by using RIN_N pushbutton by setting 0x10 [1:0] to 2 and pulling RIN_N low for more than the RIN_N reset time (0x10 [7:6]).

The DA9070 exits Hi-Z mode at a MODE pin rising edge or when VDD_PWR is applied. When VDD_PWR is removed, the part will enter Active Battery mode regardless of the MODE pin state.

The behaviour of the MODE pin depends on whether VDD_PWR is connected, shown in Table 22. The MODE pin is internally pulled low.

Table 22: MODE Functionality

VDD_PWR	MODE = 0	MODE = 1
Disconnected	Hi-Z mode (edge triggered)	Active Battery mode
Connected	Charge enabled if CE_N = 0 Charge disabled if CE_N = 1	Charge disabled

9.2.3 Battery Protection

The DA9070 includes several types of battery protection. The battery is protected during discharge by the IBAT_DCHG (over-current protection) and UVLO (over-discharge protection) functions. During charging, the TEMP_SNS function protects against over-temperature, and highly accurate voltage regulation and charging current prevent over-voltage and over-current conditions.

9.2.3.1 VBAT Over-Current Protection (OCP)

The battery discharge over-current protection threshold, IBAT_DCHG, is selectable from 0.55 A to 1.75 A at register 0x29 [4:2]. Over-current protection clamps the maximum battery current at the set threshold and is available in all modes of operation. Battery current will begin to be limited approximately 150 mA below the protection clamp. When an over-current condition occurs during charging, safety timers and charge termination are suspended.

In an over-current fault, a VBAT_OCP interrupt is generated at SYS_FLT and indicated by the event bit 0x04:[2].

All battery current flows from VBAT to VDD_SYS. Therefore, the IBAT_DCHG threshold should be set somewhat higher than the maximum expected system current from VDD_SYS. However, if the threshold is set higher than the battery can support, battery voltage may drop below VBAT_UVLO before the current is limited. When the IBAT_DCHG function clamps the battery current, VDD_SYS will droop. This may cause secondary fault conditions such as VDD_SYS UVLO.

9.2.3.2 VBAT_UVLO and SHORT

The battery under voltage protection threshold can be set from 2.5 V to 3.0 V at register 0x0E. This should be set at or above the battery's minimum discharge voltage specification. VBAT_UVLO protects the battery from over-discharge by disconnecting the discharge path when the battery voltage falls below the UVLO threshold.

When a VBAT_UVLO occurs in battery powered modes (VDD_PWR not connected), the DA9070 outputs, including VDD_SYS, will shut down and all registers will be reset to their default OTP values.

VBAT_UVLO will generate an interrupt at SYS_FLT and will be indicated by the event bit at 0x04[0].

With VDD_PWR connected, VBAT_UVLO is ignored, making pre-charge level charging available down to 0 V at VBAT. In this case, a separate fault condition applies: VBAT_SHORT. The VBAT_SHORT threshold is typically 2.0 V and is indicated by event bit 0x04[3].

9.2.3.3 Battery Temperature Sensing

The temperature sense function uses the battery's NTC thermistor to monitor battery temperature. If the battery is too cold or hot, the fast charge current or target voltage is reduced, or charging is terminated. Table 23 summarizes what protective measures are taken in each temperature range.

Table 23: Battery Thermal Protection Measures

Temperature Range	Voltage at TEMP_SNS	Charger Action	Interrupt name
$T_{BAT} < T_{LO}$	$V_{TEMP\_SNS} > V_{TEMP\_LO\_THR}$	Charging terminated	TS COLD
$T_{COLD} < T_{BAT} < T_{COOL}$	$V_{TEMP\_LO\_THR} > V_{TEMP\_SNS} > V_{TEMP\_COOL\_THR}$	Charge current = ½ x I_{CHG} setting	TS COOL
$T_{COOL} < T_{BAT} < T_{WARM}$	$V_{TEMP\_COOL\_THR} > V_{TEMP\_SNS} > V_{TEMP\_WARM\_THR}$	Normal charging	
$T_{WARM} < T_{BAT} < T_{HI}$	$V_{TEMP\_WARM\_THR} > V_{TEMP\_SNS} > V_{TEMP\_HI\_THR}$	Target voltage (V_{BAT_CHG}) reduced by 140mV	TS WARM
$T_{HI} < T_{BAT}$	$V_{TEMP\_SNS} < V_{TEMP\_HI\_THR}$	Charging terminated	TS HOT
	$V_{TEMP\_SNS} > V_{OFF\_TEMP\_SNS}$	Temp sense disabled, Optional Fault	TS OFF

Setting the Resistor Divider

The four temperature thresholds are fixed percentages of VTEMP as shown in the Electrical Characteristics table. VTEMP is enabled in short pulses to allow the battery temperature to be monitored without drawing unnecessary current through the resistor divider. VTEMP is derived from the VDD_SYS voltage. The TEMP_SNS voltage is measured after a deglitch time of 10 msec, which precludes any need for filtering at TEMP_SNS. To avoid measurement error, no filter capacitance larger than 10 nF should be added to TEMP_SNS pin.

Temperature monitoring can be disabled at the TS_EN register 0x26[1:0], or by pulling TEMP_SNS above the $V_{OFF\_TEMP\_SNS}$ threshold (TS_OFF). The TS_OFF state disables temperature sensing, and can optionally be flagged as a fault condition by setting register 0x26:[2] to 1. When TEMP_SNS is pulled high to enter TS_OFF, the off state is latched until TEMP_SNS is disabled.

Temp sense is disabled in Hi-Z mode.

Each temp sense threshold will generate an interrupt at SYS_FLT and has an event bit at register 0x04 or 0x05.

The battery NTC interfaces to the TEMP_SNS input through a resistive divider, see Figure 29.

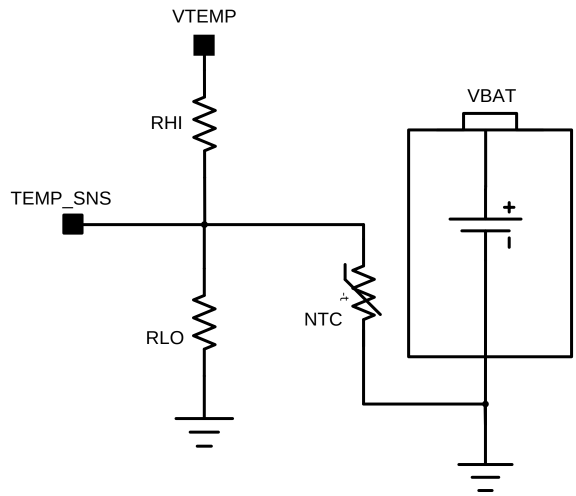


Figure 29: Battery Temperature Sensing with NTC

The resistor divider values (RHI and RLO) are selected as shown below so that the cold and hot TEMP_SNS thresholds are reached at the corresponding NTC values.

Equation 1:

$$R_{(LO)} = \frac{R_{(COLD)} \times R_{(HOT)} \times \left(\frac{1}{0.398} - \frac{1}{0.15}\right)}{R_{(HOT)} \times \left(\frac{1}{0.15} - 1\right) - R_{(COLD)} \times \left(\frac{1}{0.398} - 1\right)}$$

Equation 2:

$$R_{(HI)} = \frac{\left(\frac{1}{0.398} - 1\right)}{\left(\frac{1}{R_{(LO)}} + \frac{1}{R_{(COLD)}}\right)}$$

Where

- $R_{(HOT)}$ = the NTC resistance at the hot temperature
- $R_{(COLD)}$ = the NTC resistance at the cold temperature

The cool and warm thresholds are not independently programmable and are fixed once the cold and hot values are determined. The cool and warm thresholds can be determined by the NTC value at the threshold:

Equation 3:

$$R_{(COOL)} = \frac{R_{(LO)} \times R_{(HI)} \times 0.35}{R_{(LO)} - R_{(LO)} \times 0.35 - R_{(HI)} \times 0.35}$$

Equation 4:

$$R_{(WARM)} = \frac{R_{(LO)} \times R_{(HI)} \times 0.205}{R_{(LO)} - R_{(LO)} \times 0.205 - R_{(HI)} \times 0.205}$$

Where

- $R_{(COOL)}$ = the NTC resistance at the cool temperature
- $R_{(WARM)}$ = the NTC resistance at the warm temperature

Temp Sense Modes of Operation

The DA9070 provides two modes of battery temperature sense control: auto-mode and host control mode. In auto-mode, the DA9070 enables the VTEMP voltage every 2 second or every 50msec depending on the VDD_PWR state. At the start of each cycle, the VTEMP voltage is activated for 10ms after which the TEMP_SNS voltage is checked. This timing is shown in Figure 30.

Because auto-mode does not rely on the host to operate, it is ideally suited to provide continuous safety monitoring.

In battery powered operation, VTEMP is enabled for only 0.5 % of the time which reduces the typical current required for temperature sensing to less than 1µA.

While VDD_PWR is applied, the Temp Sense function is in auto-mode and host control of the VTEMP period is not available. This is illustrated in the Active Power section of Figure 30.

If lower current consumption is needed, temperature sensing can be controlled by the host. In host-controlled mode, an I2C command activates the same 10 msec VTEMP and TEMPS_SNS cycle.

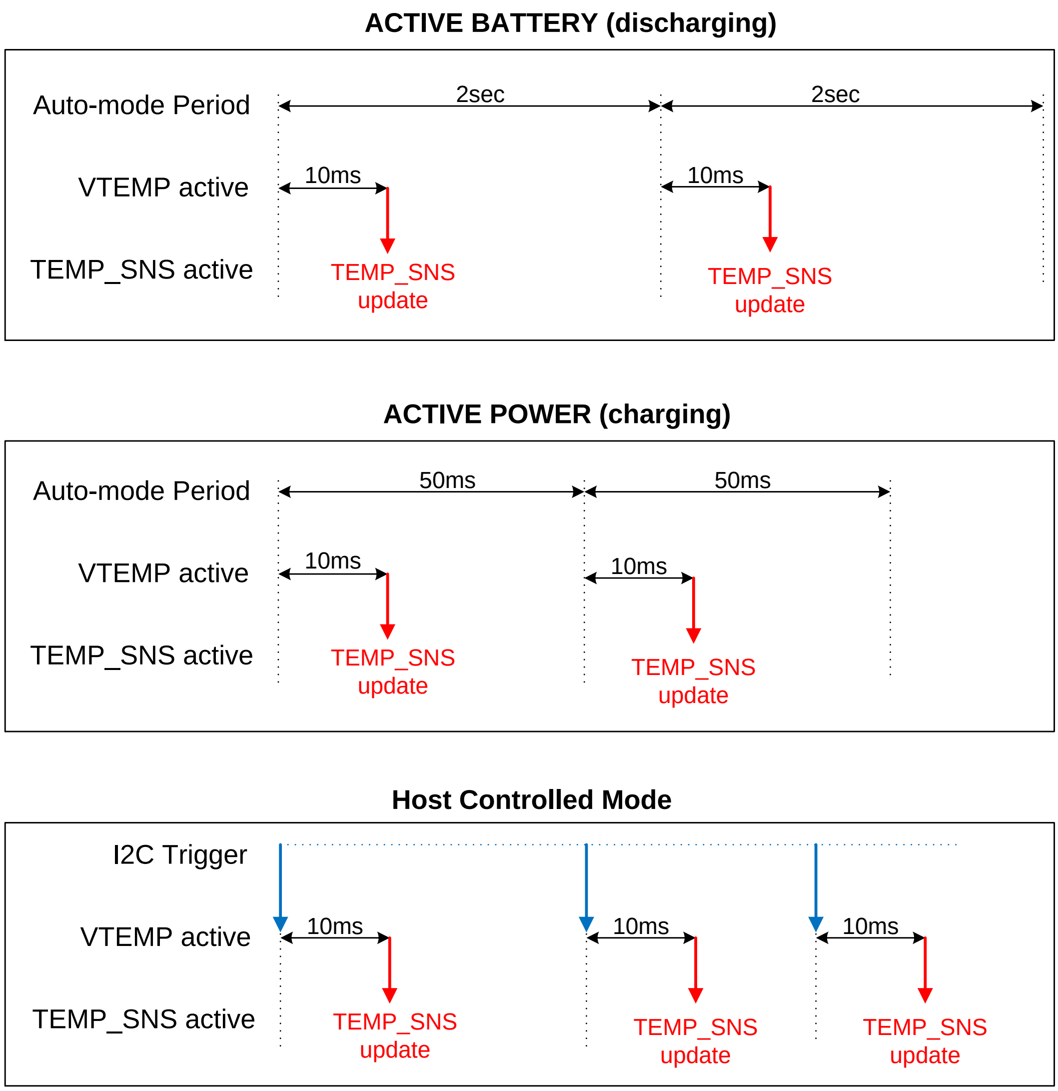


Figure 30: Battery Temperature Sense Timing

9.3 Analog Battery Monitor Functions

The DA9070 incorporates two features to support accurate fuel gauging: IMON and VBAT_DIV. These provide analog discharge current and battery voltage information scaled for compatibility with typical ADC inputs.

Filter capacitors on IMON and VBAT_DIV should not be used, or should be minimized, in order to minimize any time lag when using these outputs for fuel gauging.

IMON

The battery discharge current monitor (IMON) sources a current proportional to the battery discharge current at a 1mA/A scale. An external resistor from IMON to GND should be selected to optimize the dynamic range based on battery current range and maximum tolerance of both the DA9070 and ADC inputs. To maintain accuracy, a maximum voltage of 1.4 V is allowed at the IMON pin.

IMON can be enabled and disabled at register 0x2A. When enabled, the function draws an additional 4 µA of quiescent current from VBAT.

VBAT_DIV

The VBAT_DIV function divides down the kelvin sensed battery voltage (from VBAT_SNS) and provides a selectable output scaled at 60 % or 30 % of VBAT. The dedicated ground at GND_DIV should be used as the reference point for the VBAT_DIV output.

This is ideal for driving the differential input of an external ADC in battery monitoring functions.

VBAT_DIV can be enabled and disabled with the VBAT_DIV_EN register at 0x0F[0]. When enabled, the total resistance from VBAT_SNS to GND is 150 kΩ. To maintain accuracy, a high impedance connection is recommended at VBAT_DIV. When disabled the VBAT_DIV resistor divider is disconnected from VBAT to eliminate current drain.

Table 24: VBAT_DIV Ratios

VBAT_DIV_SEL, 0x0E:[4]	VBAT_DIV Ratio
0	0.6×VBAT
1	0.3×VBAT

9.4 Battery Charging

9.4.1 Battery Charging Process

When USB power is connected (VDD_PWR > V_{UVLO_THR}), the DA9070 is in one of four states as listed in Table 25. Charging is enabled and disabled with the MODE pin and CE_N register at 0x20:[0]. This status is indicated by the STS_CHG register 0x02:[5:4].

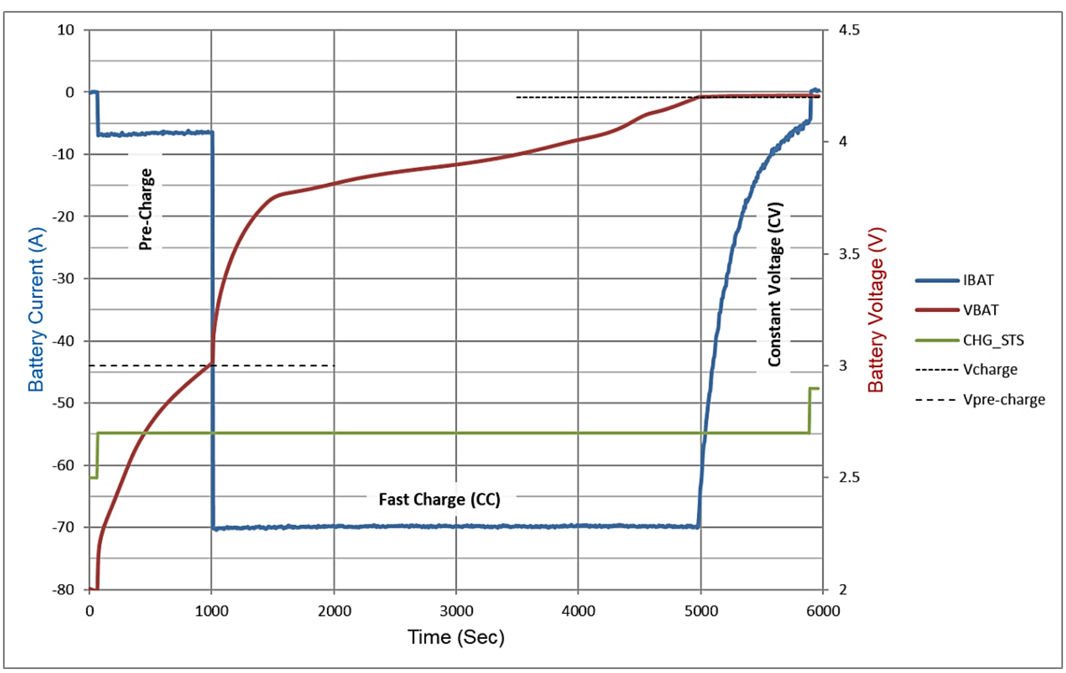
Table 25: Charge Status

MODE pin	CE_N Register 0x20 [0]	I_{CHG}	VBAT	Status	STS_CHG
Either High		N/A	N/A	Charge ready	0x0
L	L	> I_{TERM}	<= V_{BAT_CHG}	Charge in-progress	0x1
L	L	< I_{TERM}	>= V_{RCHG}	Charge done	0x2
L	L	N/A	N/A	Fault	0x3

STS_CHG is a read-only register which shows immediate charge status. The register does not hold status value and changes its value immediately when the charge status changes.

From the charge ready state, charging begins when the CE_N bit is low and the MODE input is pulled low. There is approximately 2.5 msec delay between enabling charging and charge starting.

Charging current operates in three regions based on battery voltage: pre-charge, fast charge (CC), and constant voltage (CV). These regions are shown in the typical charging example of Figu re 31. The charge status (CHG_STS) is also shown transitioning from the 'charge ready' to 'charge in-progress' to 'charge done' states.



Figu re 31: Example 70 mAh Charge Cycle

(V_Pre-charge = 3.0 V, I_Pre-charge = 7 mA, I_Charge = 70 mA, V_Term = 4.2 V)

9.4.2 Charge In-Progress

Assuming a depleted battery, the battery is initially charged at I_{CHG_PRE} until VBAT reaches the pre-charge threshold, at which point the charge current is increased to I_{CHG}. The charger continues to charge at constant current (CC) until VBAT approaches the target voltage programmed by VBREG, 0x24:[6:0]. The battery is then charged at near constant voltage (CV) and the charge current gradually falls. Charging ends when the charge current falls below I_{TER} (I_{TER} current is the same as I_{CHG_PRE}). If the VDD_PWR remains plugged in, recharging starts when VBAT falls below the recharge threshold, VBAT_CHG - 120 mV typically.

Charging modes are shown in Table 26.

Table 26: Charging Modes

VBAT Voltage	Charge Current	Charge mode	Pre-charge timer	Main timer
< $V_{PRECHARGE}$	I_{PRE_CHG}	Pre-charge	Running	Running
> $V_{PRECHARGE}$ < V_{BAT_CHG}	I_{CHG}	CC (fast charge)	Reset	Running
= V_{BAT_CHG}	< I_{CHG}	CV	Reset	Running
= V_{BAT_CHG}	=ITERM	Termination	Reset	Reset

From the charge ready state, the device enters charge in-progress state when all conditions below are met.

- $V_{VDD\_PWR} > V_{BAT} + V_{SLP}$ (not in sleep mode)
- VBAT< Recharge threshold
- RMEAS sequence completed, if enabled
- 50 ms TEMP_SNS delay, if enabled
- MODE input is pulled low and CE_N register is set to 0

If these conditions are met, charging starts automatically at the appropriate level when VDD_PWR is connected.

9.4.3 Pre-charge and Termination Current

In pre-charge mode, a constant low level charge current is supplied to the battery, up to 50 mA. Termination current is the charge current in CV mode at which charging is terminated. Both pre-charge current and termination current are identical and cannot be controlled independently. The current setting is selectable by the IPRETERM register at 0x23 within a range of 0.5 mA to 50 mA. Pre-charge and termination currents can also be set by an external resistor connected to the ITER_CHG pin.

Charge termination can be disabled by setting the termination enable bit at 0x21:[4] to 0. TS_WARM and TS_COOL conditions can also optionally disable termination at 0x21:[6:5]. This may be useful in conditions where the available charging current is reduced due to system load, or when charge current is reduced due to fault conditions.

The pre-charge to fast charge threshold voltage is programmable between 2.7 V and 3.2 V with the VBPRECHG register at 0x25: [2:0]. The threshold has 200 mV of hysteresis. When VBAT rises above the pre-charge threshold voltage, fast charging begins.

Pre-charging is indicated by an SYS_FLT interrupt and event bit at 0x05.

9.4.4 Fast Charge Current

In fast charge mode, a constant charging current is supplied to the battery at up to 500 mA. Fast charge current is selectable by the ICHG registers, 0x22. This can also be set by an external resistor connected to ILIM_CHG pin. Charge current is programmable from 5 mA to 500 mA with an accuracy of +/-5 % over the full range. Fast charge current settings down to 2 mA are available with some OTP variants.
When VBAT reaches V_{BAT_CHG} the device ends CC fast charge operation and starts CV operation.

9.4.5 CV Voltage Regulation and Termination

CV charging mode begins when the battery voltage rises into the regulation range. The regulated battery voltage, V_{BAT_CHG}, can be set between 3.6 V and 4.65 V by the VBCHG register at 0x24. Regulation accuracy is +/-0.5 % in CV mode.

When the DA9070 enters CV mode, charge current begins gradually decreasing, while battery voltage remains regulated at V_{BAT_CHG}. When charge current drops to the termination current level, charging is terminated and the charge status, STS_CHG, changes to charge done.

Charge done is indicated by an SYS_FLT interrupt and event bit at 0x05.

To ensure that the charging current is below the termination level, termination will not occur until the peak current is below the threshold. In noisy conditions or at very low termination currents, the average battery current at termination may be a few mA below the set threshold.

9.4.6 Charge Done and Recharge

To prevent rapid iterations of charging and discharging from the charge done state, there is 120 mV of hysteresis below the CV regulation level, V_{RCH}. Charging will not restart until VBAT falls below this threshold. In addition, there is a 32 msec deglitch time for noise immunity.

Recharging will start automatically, when VBAT falls below the V_{RCH} threshold.

Recharging is indicated by an SYS_FLT interrupt and event bit at 0x05.

9.4.7 Charge Faults

The DA9070 identifies multiple conditions as charge faults, indicated by the STS_CHG status bit. These conditions may reduce the charge current, reduce the target battery voltage, or take other actions. All are indicated by an interrupt and event bit. When the charger is unable to provide the programmed charge current to the battery, such as when VDD_PWR is in current limit, the termination current is ignored and charging is allowed to continue until the safety timer expires. All of the fault and event interrupts that affect charging are summarized in Table 27. VBAT_UVLO and VBAT_SHORT are included in the table although they are not indicated as faults when VDD_PWR is present. Normal pre-charging will continue in both cases.

Table 27: Charge Faults

Fault	Charging	Action	STS_CHG	Termination	Safety timer
VDD_PWR OVP	Suspend	VDD_PWR open	Fault	-	Reset
VDD_PWR UVLO	Suspend	VDD_PWR open	Fault	-	Reset
VDD_PWR DPM	Continue	VDD_PWR current limit decreased	Fault	Disable	x2

Fault	Charging	Action	STS_CHG	Termination	Safety timer
VDD_PWR ILIM	Continue	VDD_PWR current limited	Fault	Disable	x2
VBAT DPPM	Continue	Charge current reduced	Fault	Disable	x2
VBAT OCP	Suspend	VBAT current limited	Fault	-	Suspend
Sleep mode	Suspend		Fault	-	Suspend
Supplement mode	Suspend	Battery discharging	Fault	-	Suspend
TS COLD	Suspend		Fault	-	Suspend
TS HOT	Suspend		Fault	-	Suspend
TS COOL	Continue	Charge current reduced to ½	In-progress	Disable	x2
TS WARM	Continue	VBAT_CHG reduced by 140mV	In-progress	Disable	x1
TS OFF (fault option)	Suspend		Fault	-	Reset
Safety timer	Suspend		Fault	-	Reset
Over-temp.	Suspend		Fault	-	Reset
VDD_SYS UVLO	Suspend	Power-cycle	Fault		Reset
VBAT Short	Pre-charge		In-progress		x1

There are several option bits available to modify the fault behavior described above. Termination can be enabled during TS_WARM and TS_COOL, a TS_HOT fault can trigger a power-cycle, and a TS_OFF condition can trigger a fault or simply disable the battery Temp Sense feature.

9.4.8 Safety Timers

The safety timer starts counting as soon as a charge cycle begins, ensuring that the charge cycle is terminated even if the battery fails to reach the termination condition. The duration of the timer, t_{MAXCHG}, is set by register 0x21:[1:0] between 30 minutes and 9 hours. If the safety timer expires before charging is terminated, SYS_FLT toggles, and the CHG_TMR event bit is set to 1.

In pre-charge mode, the timer period is 10% of the safety timer setting. The pre-charge timer counts during pre-charging and is reset at the transition to fast-charge. If the charger is still in pre-charge at the end of the pre-charge timer period, the charge cycle is terminated. The main safety time is running during both fast charge and pre-charge modes.

To reset the safety timer and resume charging after the timer has expired, toggle the MODE pin or the CE_N bit, or remove and re-connect VDD_PWR.

Charge faults may cause the timer duration to be doubled, suspended, or reset as described in Table 27. The timer doubling function can be doubled using the TMR2x_EN bit at 0x21:[3].

Table 28. Safety Timer Register Settings (0x21)

TMR	Pre-charge timer	Main timer
0x0	3 min	30 min
0x1	18 min	3 h
0x2	54 min	9 h
0x3	(Disable)	(Disable)

9.5 USB Powered Operation and Power Path Management

The DA9070 monitors battery voltage and current as well as VDD_PWR input voltage and current during all modes of operation. At all levels of operation, the appropriate charge current is maintained while protecting the battery, system connections, and the input supply from over-voltage and over-current and other potential fault conditions.

The DA9070's power path management features ensure smooth transitions from charging to reduced charging to battery supplementing the load during load peaks.

9.5.1 Under-Voltage Lockout (VDD_PWR_UVLO)

The UVLO threshold for VDD_PWR is 3.6 V (typical). Below this voltage, VDD_PWR will be disconnected from the power path and the DA9070 will be in battery powered operation. VDD_PWR UVLO will cause SYS_FLT to toggle and will set the VDD_PWR_UVLO event bit to 1.

The UVLO threshold has typically 150 mV of hysteresis on the rising edge. When VDD_PWR rises above this threshold, charging is re-enabled. UVLO recovery will also toggle the SYS_FLT interrupt and will set the UVLO recovery event bit.

9.5.2 Sleep Mode

Sleep mode behavior is similar to VDD_PWR_UVLO, but the falling threshold is relative to VBAT. When VDD_PWR falls within 65 mV (typical) of VBAT, sleep mode is activated. In sleep mode, VDD_PWR is disconnected from the power path, SYS_FLT toggles, and the SLP event bit is set to 1. When VDD_PWR falls into the range of sleep mode, it will already be in DPPM mode (VDD_PWR<VBAT_CHG), therefore charge current will already be reduced to zero.

9.5.3 VDD_PWR Current Limit (IDD_PWR_LIM)

The VDD_PWR current limit feature protects both the DA9070 and the USB supply from excessive current. The current limit threshold is programmable from 50 mA to 600 mA in 50 mA steps at register 0x27. When the input current reaches the set threshold, VDD_PWR current is clamped and an event bit is set at register 0x03. If the load at VDD_SYS increases, the VDD_SYS voltage will drop eventually triggering a VDD_SYS UVLO.

The DPM function, when enabled, will reduce the current limit threshold as USB input voltage is reduced.

9.5.4 Input Voltage Dynamic Power Management (DPM)

If the charge current and system load exceed the current capability of the VDD_PWR input source, the input voltage will drop. Dynamic power management (DPM) prevents the input from dropping below the nominal USB range and into DPPM mode by scaling down the VDD_PWR current limit (I_{DDPWR_LIM}) until it matches current capability of the USB source.

This feature becomes active when VDD_PWR falls below $V_{DDPWR\_IIN\_DWN}$, which is programmable between 4.2 V and 4.9 Vat 0x28:[2:0]. The DPM feature can be disabled by setting the VDD_PWR_DPM_DIS bit to 1. However, when DPM is disabled, the USB power source may be pulled down, triggering sleep mode or input UVLO.

The VDD_PWR_DPM event bit is set to 1 and the SYS_FLT pin toggles whenever the DA9070 is in this current-limited mode. In charging mode, termination is ignored to allow the battery to be charged with whatever current is still available.

9.5.5 Dynamic Power Path Mode (DPPM)

Dynamic Power Path Mode (DPPM) manages the situation in which the total charging and system current exceeds the VDD_PWR current limit. When the input current is clamped, V_{VDD_SYS} drops until it reaches $V_{DD\_SYS\_THR\_DPPM}$ (DPPM threshold). In DPPM operation, charging current is reduced as needed to service the system current at VDD_SYS. DPPM is only active during charging, and will toggle SYS_FLT and set an interrupt bit at register 0x04.

If V_{VDD_SYS} drops further due to increasing load, the DA9070 eventually enters Battery supplement mode.

9.5.6 Battery Supplement Mode

The DA9070 enters Battery Supplement mode when VDD_SYS falls below VBAT. Supplement mode occurs in USB powered operation, regardless of whether the battery is charging or not. Similar to DPPM mode, the total current at VDD_SYS exceeds the VDD_PWR current limit, causing VDD_SYS to drop until it reaches the VBAT voltage. In this mode, the battery supplies current to VDD_SYS, thus supplementing the input current to supply the system demands. In battery supplement mode, the discharge current from the battery is limited by the over-discharge protection.

Supplement Mode toggles the SYS_FLT pin and sets an event bit at 0x05.

The device exits Supplement Mode when the system load is reduced and VDD_SYS rises above VBAT.

9.5.7 Input Over-Voltage Protection (VDD_PWR_OVP)

The DA9070 protects itself (and downstream connections to VDD_SYS) against input over-voltage conditions by disconnecting VDD_PWR from the power path. Over-voltage protection kicks in immediately when VDD_PWR exceeds the OVP threshold. Over-voltage events are common at USB plug-in due to the inductance of the long cable, where the transient overshoot may exceed 10 V depending on cable length, quality, and input capacitance. The VDD_PWR input is capable of withstanding up to 20 V and will remain in OVP until the voltage returns to nominal levels. During OVP, VDD_PWR is disconnected from the power path and the DA9070 will be in normal battery powered operation.

When an over-voltage occurs, the event bit is set to 1 and SYS-FLT toggles.

9.5.8 VDD_PWR Input Supply Impedance

The DA9070 charging path is typically supplied by a 5 V USB source. USB cable resistance can range from 100’s of milliohms to ohms. At higher charging currents, this parasitic input impedance may cause VDD_PWR to drop from 5V into the DPM range.

High USB cable resistance can lead to oscillations in DPM or Sleep mode. As VDD_PWR drops, the DA9070 attempts to reduce current demand, which in turn causes VDD_PWR and current draw to increase again. Follow the guidelines in Figure 32 to ensure that the DA9070’s internal hysteresis will be sufficient to overcome these effects. The worst case is at highest battery voltage, the VBAT_CHG regulation point.

It is recommended to always enable the DPM function, with the threshold set at least 0.4 V above the VBAT_CHG voltage. Referring to Figure 32, with a DPM setting of 4.5 V and VBAT = 4.2 V, the system has the potential to oscillate at any current greater than 75 mA. Note that this would only occur if VDD_PWR drops into the DPM or sleep region. For this example, a DPM setting of 4.6 V or 4.7 V is recommended for currents above 75 mA.

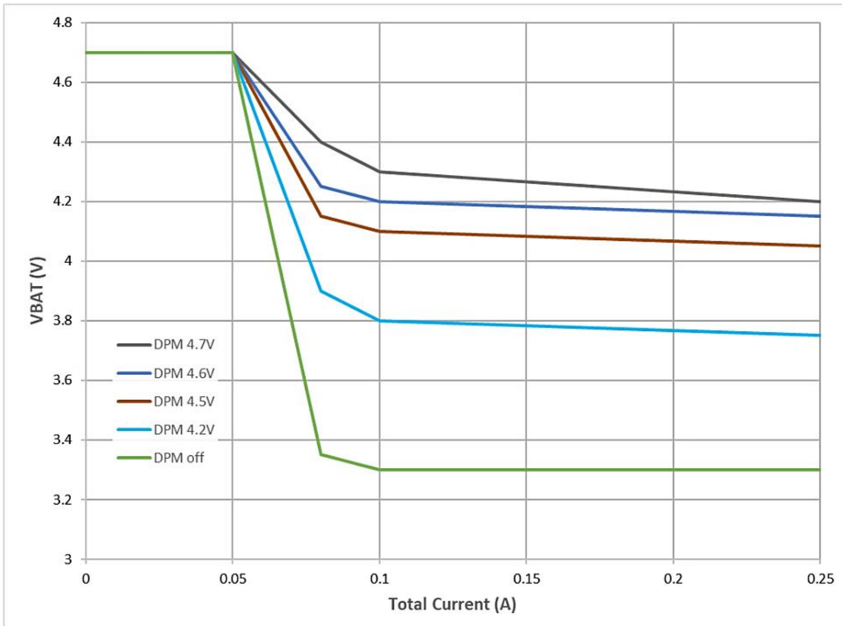


Figure 32: VDD_PWR DPM setting recommendations

(based on typical USB cable impedance)

9.6 Power-Cycling

The power-cycle function disables all outputs (buck, boost, and LDOs) for a programmable time period and then restarts. Power-cycle can be initiated by a fault condition, RIN_N pushbutton, VDD_PWR insertion, or I2C command. The primary purpose of power-cycling is to clear a serious fault condition such as IC over-temperature (OVT) or to reset the host.

9.6.1 Requested Power-Cycle

The power-cycle settings are configured at register 0x12. There are 3 methods to enter power-cycle: by register write to PWR_CYC_FRC, by holding the RIN_N pushbutton low for the reset period, or by inserting and removing VDD_PWR. The setting options are summarized in Table 29.

Table 29: Power Cycle Trigger Settings

PWR_CYC_EN 0x12 [0]	PWR_CYC_MODE 0x12 [1]	RIN_N RESET wake-up timer	VDD_PWR insertion / removal	PWR_CYC_FRC 0x12 [2]
0x0	(don't care)	Disable	Disable	Disable
0x1	0x0	Disable	Enable	Enable
0x1	0x1	Enable	Disable	Enable

After any of these three host or user-initiated power-cycles, the Buck, Boost, and LDO outputs will be disabled. When auto-restart occurs, only the Buck will restart. All register settings are preserved at restart with the exception of the output enable registers. There is also a READ clear event bit at 0x02:[1] to indicate that a power-cycle has occurred.

Two timers apply to power-cycling: the wait timer and the period timer. The wait time allows the host to take action before power is shut down and can be set between 0 seconds and 2 seconds. The period timer controls how long the outputs are powered down before restart and can be set between 5 and 20 seconds. Both timers are programmable at register 0x12.

Figure 33 below shows the power-cycle timing using the RIN_N pushbutton. The RESET time is set at register 0x10:[7:6]. The RIN_N pushbutton timer can be used for power-cycling only when VDD_PWR is present.

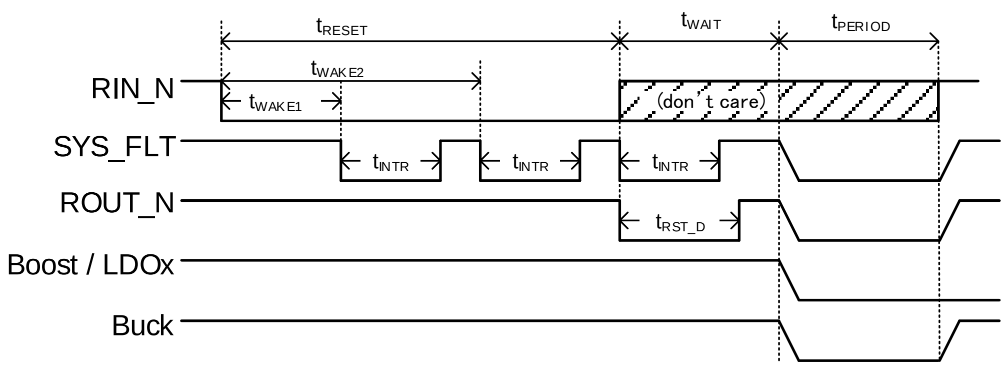


Figure 33: Power-Cycle by Pushbutton Timer

Alternately, the VDD_PWR plug can be used to initiate a power-cycle as shown in Figure 34. VDD_PWR must go low and high 3 times within 8 seconds. After the 8 second period, the power-cycle will begin.

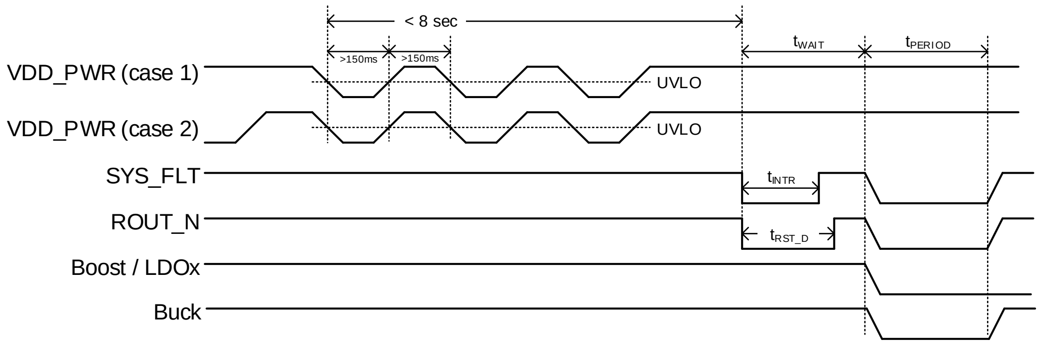


Figure 34: Power-Cycle by VDD_PWR Insertion

The force power-cycle bit (PWR_CYC_FRC) follows the same power-cycle period and behaviour, but does not impose any wait time; power-cycle shutdown occurs immediately.

9.6.2 Fault Triggered Power-Cycle

The DA9070 will also initiate a power-cycle in response to various fault conditions, listed in Table 30 and Table 31. Those not listed as “always on” will trigger a power-cycle only if that option is enabled. Fault triggered power-cycles are intended to protect the system from a potentially damaging condition. The behaviour is therefore somewhat different to a user-initiated power-cycle.

When a fault triggered power-cycle occurs, the wait time is skipped and all outputs will be shut-down immediately. When the power-cycle period ends, the initial OTP register values are re-loaded at restart, including any outputs that are enabled by default.

A fault triggered power-cycle will also disable VDD_SYS, thus creating a complete power system restart (a host or user-initiated power-cycle does not disable VDD_SYS).

Table 30: Power-Cycle Faults

Power-cycle Fault triggers	0x13 register bit	I2C Selectable	Register Reset
Battery Temp Sense HOT	0	YES	YES
Thermal Shutdown (OVT)	NA	Always On	YES
VBAT UVLO (in act bat mode)	NA	Always On	YES
VDD_SYS UVLO	NA	Always On	YES

There are also three power-cycle faults associated with the Buck, listed in Table 31. Any of these faults will cause an immediate power-cycle. Buck faults do not re-load the OTP register values, and only the buck will restart after a Buck fault power-cycle.

Table 31: BUCK Power Cycle Faults

Power-cycle Fault triggers	0x13 register bit	I2C Selectable	Register Reset
BUCK OCP	4	YES	NO
BUCK OVP	NA	Always On	NO
BUCK UVP	6	YES	NO

9.7 Standalone Mode

The DA9070 can operate without I^2C communication using external resistors to program three settings. Fast charge current, input current limit, and termination and pre-charge current can be set by external resistors at the ITER_CHG, ILIM_PWR and ILIM_CHG pins, respectively.

This feature is enabled by the RMEAS_EN register at 0x20 [1]. Whenever VDD_PWR is plugged-in, these three external resistors are evaluated and the control registers are set appropriately. If the pins are connected to ground, the internal register values will be used.

If used, all three resistors must be installed. If any of the three pins is grounded, all three currents will be determined by their respective register values.

The specification of RMEAS_EN register is described in Table 32.

Table 32: Enabling External Resistor Setting Mode

RMEAS_EN 0x20:[1]	External resistance [Ω]	Setting
0	(don't care)	Register settings used
1	0	Register settings used
1	> 0	Calculated from external resistance

9.7.1 Termination and Pre-Charge Current Programming (ITER_CHG)

The pre-charge and termination currents are the same value and set with the same resistor. When using the external resistor setting method, they can be set to 5 %, 10 %, 15 %, or 20 % of the fast charge current.

Connect a resistor from the ITER_CHG pin to ground. Table 33 shows the recommended resistor values to set the pre-charge and termination currents.

Table 33: ITER_CHG Recommended Resistor Values

% of ILIM_CHG (typ)	Resistance (kΩ)
5	68
10	22
15	8.2
20	2.2
Register Setting at 0x23 is used	0

Once VDD_PWR is connected, the set pre-charge and termination values can be read at register 0x20:[5:4].

The pre-charge current cannot be set higher than 50 mA, or lower than 0.5 mA. Settings which are out of range will result the minimum or maximum current setting. For example, with a 400 mA fast charge current, a 20 % setting would result in 80 mA, but the actual pre-charge current will be the maximum value of 50 mA.

9.7.2 Input Current Limit Programming (ILIM_PWR)

VDD_PWR input current limit is programmed by a resistor connected from the ILIM_PWR pin to ground. The resistor value can be calculated as: $R_{ILIM\_PWR}(\Omega) = \frac{1000}{ILIM(A)}$

Not all current limit register settings are available in resistor setting mode. The available current limit settings and corresponding resistor values are shown in Table 34.

Table 34: ILIM_PWR Recommended Resistor Values

VDD_PWR ILIM (typ)	Resistance (kΩ)
Register setting at 0x27 is used	0
600 mA	1.6
500 mA	2.0
400 mA	2.7
300 mA	3.6
200 mA	5.1
150 mA	6.8
100 mA	10.0
50 mA	20.0

9.7.3 Charge Current Programming (ILIM_CHG)

Fast charge current is programmed by a resistor connected from the ILIM_CHG pin to ground. The resistor value can be calculated as: $R_{ILIM\_CHG}(\Omega) = \frac{1000}{FastCharge(A)}$

Not all fast charge register settings are available. The available current limit settings and corresponding resistor values are shown in Table 35.

Table 35: ILIM_CHG Recommended Resistor Values

Fast Charge Current (typ)	Resistance (kΩ)
Register setting at 0x22 is used	0
500 mA	2.0
400 mA	2.7
300 mA	3.6
200 mA	5.1
150 mA	6.8
100 mA	10.0
70 mA	15.0
50 mA	20.0
40 mA	27.0
30 mA	36.0
20 mA	51.0

Fast Charge Current (typ)	Resistance (kΩ)
15 mA	68.0
10 mA	100.0
7 mA	150.0
5 mA	200.0

9.8 Host and Pushbutton Communication

The DA9070 features multiple digital pins for host and user communication, as listed in Table 36 with connections shown in Figure 35.

Table 36: Digital Pins for Host and Pushbutton Interface

Pin Name	Description
SCL / SDA	I^2C Interface
MODE	Mode control input Used to enter Hi-Z mode and control charging (Edge triggered for Hi-Z control; Level triggered for charge control)
RIN_N	Pushbutton Interface Used to wake up from ship mode and Hi-Z mode Also used to generate a low-active reset pulse on ROUT_N
SYS_FLT	IRQ Interrupt output flag Also functions as a charging status indicator
PWR_FLT	Power Input status flag Can also be configured as a voltage shifted RIN_N output
ROUT_N	Host Reset output which is controlled by RIN_N
WD	Watchdog input

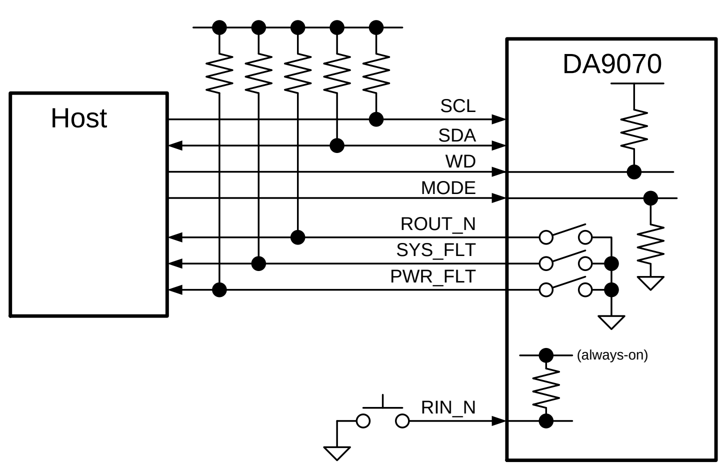


Figure 35: Digital Pin Connections

9.8.1 Watchdog Input and Timer

A programmable watchdog timer, WD, is available to detect a stall in the host. The WD function is enabled or disabled at register 0x14:[1:0]. Each time the host initiates I^2C or toggles the watchdog input, the timer resets. If no host activity is detected within the timeout period, the DA9070 toggles the SYS_FLT flag and sets the WD event bit at 0x07 to 1. If the register reset option is enabled, the outputs are disabled for a period of typically 20msec and then re-enabled to reset the host. The watchdog is automatically re-activated and the pre-programmed OTP values are loaded (except for RIN_N_RST_ROUT_EN and RIN_N_RST_REC at register 0x10:[3:0]).

The watchdog timeout period is programmable to 25 or 50 seconds via the 0x14 register.

Optionally, the WD function can also toggle the ROUT_N pin, also selectable at register 0x14.

The WD_EN register selects when the watchdog timer is available as described in Table 37.

Table 37: WD_EN Register 0x14 [1:0]

Register value	Charge mode	Active battery mode	Hi-Z mode
0x0	Disable	Disable	Disable
0x1	Enable	Disable	Disable
0x2	Enable	Enable	Disable
0x3	Enable	Enable	Enable

The WD_CLR_SEL register selects which activity the WD uses to clear the timer, described in Table 38.

Table 38: WD_CLR_SEL Register 0x14 [3:2]

Register value	Description
0x0	Only I^2C clears the timer
0x1	Only WD pin clears the timer
0x2	Both I^2C and WD pin clear the timer
0x3	Reserved

Figure 36 shows how to periodically feed the watchdog and what happens when the processor stalls.

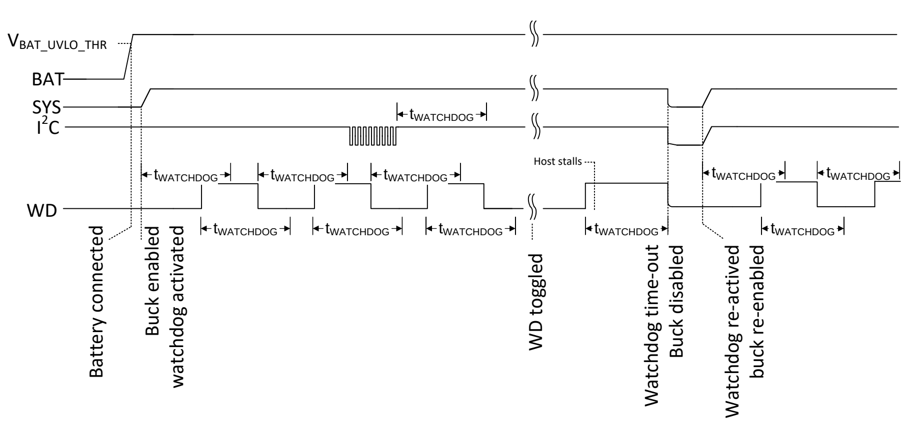


Figure 36: Watchdog Behaviour

9.8.2 VDDIO

VDDIO is the I/O supply rail for the DA9070. I^2C communication (SDA, SCL), MODE, WD, ROUT_N, SYS_FLT, and PWR_FLT are all referenced to the VDDIO level.

VDDIO is an input pin, which can be supplied with any voltage between 1.4 V and 3.3 V as required to interface with the host. However, the VDDIO voltage must not be higher than the VDD_PWR and VBAT voltages. Therefore, it is recommended to use the Buck or LDO output to supply VDDIO. The VDDIO pin should be bypassed with a 1 µF capacitor placed close to the pin, and grounded to AGND.

9.8.3 Interrupt Events and Status Control (SYS_FLT, PWR_FLT)

The DA9070 has an interrupt interface for 35 individual events. Some of these events are categorized as charge fault events. See 9.4.7 for more details about charge faults.

There is a READ-only event bit for each interrupt in the SYS_IMR registers 0x03 through 0x07. A high state indicates that an event has occurred. The bit will be kept in a high state, even if the fault condition is removed, until the bit is cleared. These are READ clear bits which can be READ once to identify the event and READ a second time to reset the bit to 0.

The DA9070 provides two open drain output flags to indicate system status and interrupts, SYS_FLT and PWR_FLT. These should be pulled up to VDDIO with a 1 kΩ to 100 kΩ resistor. Both pins have configuration options which can be selected at register 0x11.

The PWR_FLT output can be configured as an indicator of the VDD_PWR status, or as a level-shifted RIN_N monitor. Both options are shown below in Figure 37 and Figure 38.

When used as a level shifted RIN_N monitor, there is a typical delay of 1.5 msec between RIN_N and PWR_FLT signals.

In the case of VDD_PWR status indicator, PWR_FLT goes low only when VDD_PWR is within a valid range. In both cases a high state is high impedance.

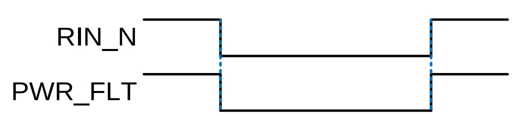


Figure 37: PWR_FLT Configured as RIN_N Monitor, 0x11:[4]=1

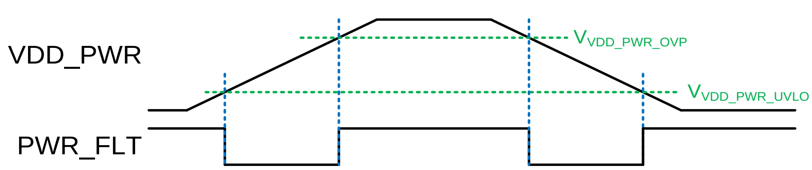


Figure 38: PWR_FLT Configured as VDD_PWR Status Indicator, 0x11:[4]=0

The SYS_FLT output indicates interrupt events with a 128 µs pulse and can be also be configured to indicate charging in progress. SYS_FLT is configured at 0x11:[0] as shown in Table 39.

Table 39: SYS_FLT Configuration, 0x11: [0]

Register Setting	Charge indicator	IRQ interrupt polarity
0	Disabled	Active-low
1	SYS_FLT low when charge in progress	Active-low when charge is not in-progress

		Active-high when charge is in-progress

The SYS_FLT interrupt flag can be masked for each individual interrupt by setting its mask bit to 1. Mask registers, SYS_IMR, are at registers 0x08 through 0x0C. Masking an interrupt will mask the SYS_FLT flag but does not mask the event bit.

Once an interrupt has occurred, the SYS_FLT flag will not toggle a second time for the same interrupt. The event bit must first be READ cleared before SYS_FLT will respond to that event again.

9.8.4 Pushbutton Reset Timer and Reset Output (RIN_N and ROUT_N)

The RIN_N input can be used to manually control the DA9070 even in ship mode, Hi-Z mode, or when the host has stalled. The pin has three functions: enter/exit ship mode, enter Hi-Z mode, and toggle the ROUT_N reset output. RIN_N is active in all modes of operation. The pin is internally pulled high and can be pulled directly to ground with an external pushbutton to activate the timer.

When RIN_N is pulled low, a reset timer begins counting. There are three programmable RIN_N timers; each associated with an event bit. Each time the RIN_N timer passes the programmable count the SYS_FLT flag toggles, and a WAKE event bit is set. In this way, requests to the host can be generated by pressing the button for different durations. The first two timers are WAKE1 and WAKE2; the third timer is the RESET timer. If RIN_N is held low for the set RESET time, the DA9070 can be set to enter ship mode, enter Hi-Z, or initiate a power-cycle. The WAKE and RESET periods are set as shown in Table 40.

Table 40: RIN_N Pushbutton wake-up timer control (0x10)

Timer Name	Timer control register	Programmable Period
WAKE1	RIN_N_PER_WAKE1 0x10 [4]	50 ms 500 ms
WAKE2	RIN_N_PER_WAKE2 0x10 [5]	1.0 s 1.5 s
RESET	RIN_N_PER_RST 0x10 [7:6]	4 s 8 s 10s 14s

The timer status registers, WAKE1, WAKE2, and RESET, are at 0x07. As with all other events, the SYS_FLT flag can be masked. The RIN_N timing is described in Figure 39.

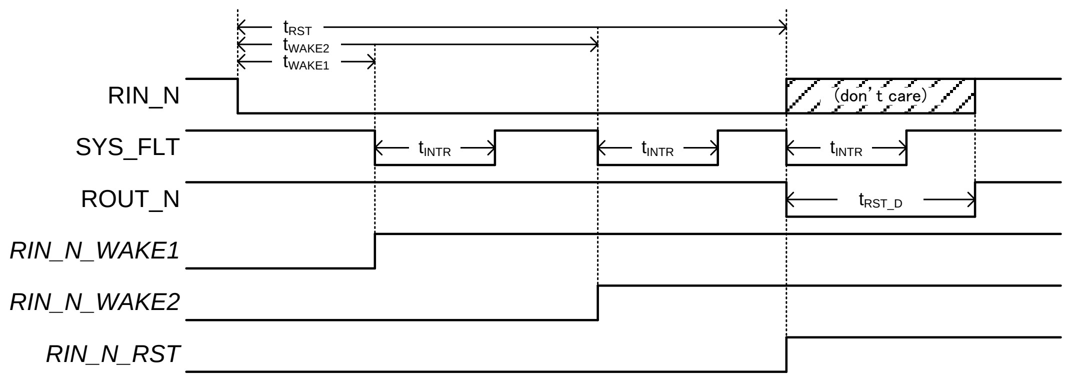


Figure 39: RIN_N Pushbutton Reset Timer Timing Diagram

The RESET behavior is configurable with the options shown in Table 41.

Table 41: RIN_N Reset Timer Configuration

Register	Configuration Description
RIN_N_RST_REC 0x10 [1:0]	0: RESET event has no effect 1: Enter ship mode at RESET 2: Enter Hi-Z mode at RESET
PWR_CYC_MODE 0x12 [1]	0: Power-cycle triggered by VDD_PWR insertion / removal 1: Power-cycle triggered by RESET timer when VDD_PWR present
RIN_N_RST_ROUT_EN 0x10 [3:2]	0: Disable ROUT_N toggle at RESET 1: Enable ROUT_N toggle at RESET 2: Enable ROUT_N toggle at RESET only when VDD_PWR is present

The RIN_N timer can also be used to exit Ship mode. A WAKE1 event will trigger Ship mode exit, with WAKE2 and RESET being ignored.

If ROUT_N is enabled, a RESET event will cause the ROUT_N output to toggle low for 400 msec (typ). ROUT_N is an open-drain output that should be pulled-up to the logic rail with a 1 kΩ to 100 kΩ resistor.

9.8.5 System Status Register

The System Status register (0x02) indicates the status of five system functions:

- BUCK: High = enabled with no faults
- BOOST: High = enabled with no faults
- Charge Status: Ready, Charge in Progress, Charge Done, or Fault
- MODE: Logic state of the MODE pin
- Power-Cycle: High indicates that a power-cycle has occurred

Only the power-cycle bit shows previous events and is read-clear. The others are READ only, reflecting the current status.

9.8.6 I²C Programming

The DA9070 includes an I²C compatible interface which allows READ/WRITE access to all registers. The interface is disabled in some modes and is configurable as described in Table 42.

Table 42: I²C Interface Configuration

I2C_HIZ_EN 0x15 [0]	Ship mode	Hi-Z mode	Active battery mode	Charge mode
0	disabled	disabled	active	active
1	disabled	active	active	active

I²C communication uses the SDA and SCL are open drain I/O pins. These should be pulled up to VDDIO with a 1 kΩ to 100 kΩ resistor. SCL is the serial clock generated by the host and SDA is the serial address and data input/output.

The DA9070 is compatible with the standard I²C protocol but only operates as a slave. The I²C bus supports a frequency range of 400 kHz (fast mode) to 100 kHz (slow mode). The transfer protocol is the same whether operating in fast or slow mode.

The device supports 8-bit addressing only. The I²C slave ID is 7-bit and can be set at register 0x40 [6:0], with a range of 00 to 7F.

When active, the I²C bus is monitored at all times for a valid SLAVE address, and an ACKNOWLEDGE (ACK) bit is generated if the SLAVE address is true.

This indicates to the master that the communication link has been established. The master then generates SCL clock cycles to transmit or receive data. After receiving data, an ACK is generated either by the DA9070 or the master. Basic communication is described below and in Figure 40.

- A START condition is initiated by a high to low transition on the SDA line while the SCL is in the high state
- A STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state
- An ACK is indicated by the receiver pulling the SDA line low during the following clock cycle

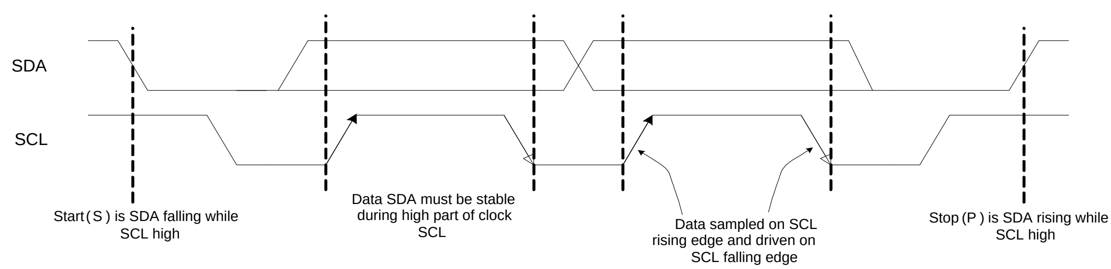


Figure 40: I²C Start and Stop Conditions

Each data sequence is 9-bit, consisting of 8-bit data and 1-bit ACK. Data sequences can be repeated indefinitely. At the end of the data transfer, the master generates a STOP condition.

The bus returns to IDLE mode if during a message a new START or STOP condition occurs. Data is transmitted as MSB first for both READ and WRITE operations.

9.9 Buck Regulator

The DA9070 includes a nano-ampere quiescent current buck regulator with adjustable output voltage, up to 300mA load capability, and power saving mode for excellent efficiency at light load. It also features Dynamic Voltage Scaling (DVS) capability and multiple protection features.

9.9.1 Buck Output Voltage Programmability

The DA9070 buck regulator output voltage is programmable in 50 mV steps between 0.6 V and 2.1 V. The output voltage is set by register BUCK_VOUT at 0x30 [4:0]. The voltage can be set within two ranges based on the value of the VOUT_RANGE_HI register, 0x30 [6]. The output voltage can be changed within one of the two range settings while the buck is enabled (0.6 V to 1.3 V or 1.3 V to 2.1 V). The range setting, however, can only be changed while the buck is disabled.

If a command is received outside of the allowable range (that is above 1.3 V for VOUT_RANGE_HI = 0 or below 1.3 V for VOUT_RANGE_HI = 1), digital will force the value of BUCK_VOUT<3:0> to 01110 (1.3 V).

Although the output voltage can be set up to 2.1 V, there is a headroom requirement of 600 mV for VDD_BUCK. Therefore, if the output voltage is set to 2.0 V or 2.1 V, the VBAT UVLO must be set to 2.6 V or 2.7 V respectively to ensure proper operation.

9.9.2 Buck Enable and Soft Start Operation

DA9070 buck integrates a soft start circuit to minimize output voltage over-shoot and input voltage droop during start-up. Writing 1 to BUCK_EN (0x30: [7]) enables the buck and switching starts after a typical delay of 3 ms. During soft-start, the cycle-by-cycle peak current limit is reduced to 300 mA (typ) to limit inrush current. Although the startup time is not controlled directly, a smooth startup can be expected with timing variations due to input and output voltage conditions.

Due to the reduced current limit in startup, starting the buck regulator into a heavy load is not recommended.

9.9.3 Power Saving Mode Operation

The DA9070 buck regulator features power saving mode that greatly reduces the quiescent current in light load conditions. When the load decreases to a certain level, the buck regulator enters discontinuous mode (DCM) and operates with Pulse Frequency Modulation (PFM). The low-side FET will be turned off based on a zero-crossing comparator to prevent negative inductor current, which can result in additional conduction loss. If both high and low-side FETs remain in the OFF state for a certain delay time after the inductor current crosses zero, the buck will enter power saving mode. In this mode, most of the internal circuitry is shut down to reduce quiescent current. The lighter the load, the longer the duration power saving mode will be, thus achieve the lowest quiescent current and improving light load efficiency. At no-load the buck regulator consumes only 900 nA of quiescent current typically.

At heavier loads, the buck operates in continuous conduction mode (CCM) with constant off-time. The off timer imposes a minimum off time on the switching cycle, thereby placing a ceiling on the switching frequency.

9.9.4 Dynamic Voltage Control

The DVC feature allows the buck output voltage to ramp up or down to a new target value in a controlled manner. When a new voltage setting is applied, the register setting value will be incremented or decremented by one bit every 4msec, which results in an output voltage slew rate of

50 mV / 4 ms. Since the buck output voltage can only be changed within the high or low range while enabled, DVC also has this restriction. DVC can be enabled and disabled at register 0x50 [1:0].

Because the buck works in DCM under light load, it cannot quickly discharge the output voltage during DCM. When a voltage ramp down is commanded in DCM, the slew rate will depend on the load. In CCM, the falling slew rate will be the same 50 mV / 4 msec as the rising slew rate.

Different DVC slew rates are available by OTP.

9.9.5 Over-Current Protection

The over-current Protection (OCP) monitors the peak current through high-side FET on a cycle-by-cycle basis. When the sensed current exceeds the current limit threshold, the high-side FET will be turned OFF immediately to limit the inductor current. The high-side FET will be turned on again after the constant-off time expires. Current limit will trigger a BUCK_OCP event bit at 0x06, and SYS_FLT will toggle.

In current limit conditions, the output voltage will drop, potentially causing an under-voltage fault. Both over-current and under-voltage can be set to initiate a power-cycle, restarting the buck after a programmable wait time. The power-cycle triggers can be configured at 0x13.

9.9.6 Output Under-Voltage Protection

When a buck output short or heavy loading occurs, inductor current will increase until the peak reaches the cycle-by-cycle current limit. Because the output is shorted, the inductor current down slope is very small during low-side FET on time. In this condition, the inductor current can potentially increase with each cycle. To prevent the inductor current from running away in a short-circuit condition, the buck output voltage is monitored. If an over-current condition happens and the buck output drops 400 mV below the reference voltage, the BUCK_UVP event bit will be set at 0x06. UVP can be set to trigger a power-cycle at register 0x13.

The under-voltage protection is not active during startup. Therefore, a short circuit during startup may not trigger a fault event or a power-cycle.

9.9.7 Output Over-Voltage Protection

Over-voltage protection (OVP) protects the load from unexpected output overshoots. When the buck output voltage is 200 mV greater than the target voltage, the high side FET is immediately turned off. Simultaneously, the output discharge FET will be turned on to discharge the output capacitor. A BUCK_OVP event bit will be set at 0x06:[1] and the SYS_FLT flag will toggle. The buck will remain off with the output pulled-down until the fault is cleared. BUCK_OVP can also be set to initiate a power-cycle.

9.9.8 Automatic Output voltage Discharge

To speed up the discharging of buck output capacitor and ensure a safe re-start, the buck regulator provides automatic output voltage discharge when the buck is disabled or shutdown due to a fault. Automatic output discharge when the buck is forced OFF by a fault is set at register 0x31:[4]. Automatic discharge when the buck is disabled is set at register 0x31:[5]. The output of the buck regulator is discharged through the FB_BUCK pin with resistance of 33 Ω (typical)..

9.9.9 External Component Selection

The choice of inductor and output capacitor is a trade-off between light load efficiency and load transient response. In general, the combination of a smaller L and larger COUT improves load transient performance and reduces the voltage ripple at light loads. A larger L improves light load efficiency by reducing the frequency of switching cycles and therefore switching losses.

The inductor must have a saturation rating which exceeds the maximum value of the current limit (ILIM_SW_PMOS). In order to optimize efficiency, decide the inductor value first and then select the inductor with the lowest DCR possible given the PCB constraints.

Recommended component values are shown in Table 43

Table 43: External Buck Components

Component	Value
L	2.2 µH
C_{OUT}	10uF

9.10 Boost Regulator

The DA9070's integrated boost is an asynchronous current mode control regulator. This architecture provides excellent stability over a wide range of output voltage and operates in DCM at light loads for excellent efficiency. The boost regulator also includes a true shutdown switch to disconnect the input from the output when disabled.

The boost input voltage (VDD_BST) is uncommitted and can be powered by VDD_SYS or any external supply between 2.5 V and 5.5 V. The output voltage can be set between 4.5 V and 18 V at register 0x36.

Load current capability is determined by the peak current limit, which depends primarily on input and output voltage conditions. With an output voltage of 12 V, the typical load capability is 100 mA. At 5 V output, the boost is capable of supporting 300 mA. And up to 80 mA at the maximum 18 V output. At light load, the boost enters DCM mode and will skip pulses as needed to maintain regulation. The peak current limit threshold can be selected between 0.5 A and 1.5 A at register 0x38:[5:4].

The boost regulator operates at either 1 MHz or 2 MHz, selectable at 0x37:[0]. A 1 MHz setting is recommended for higher efficiency and higher load capability. 2 MHz can be used to minimize the inductor and output capacitor sizes but will have a more limited operation range. Typical component values are shown Table 44. Always check capacitor voltage derating values. The values shown here assume no more than 50 % derating at the operating voltage.

Table 44: Recommended External Boost Components

Component	1 MHz Value	2 MHz Value
L	4.7 µH	2.2 µH
C_{OUT}, 5V	> 4.7 µF	> 3.3 µF
C_{OUT}, 12V	> 10 µF	> 6.8 µF
C_{IN} (VDD_SYS)	>3.3uF	>3.3uF
C_{IN} (VDD_BST)	>1uF	>1uF

9.10.1 Startup

When the boost is enabled at register 0x36, it begins the soft start cycle. To avoid inrush current and potential output overshoot, the true shutdown switch is enabled and a pre-charge current limit is imposed. This charges the output voltage to the same level as the input voltage in a controlled manner. After a selectable pre-charge time (0x37:[5:4]), the output will begin ramping up to the target voltage. During this second period of startup, the boost begins switching, but at a reduced peak current limit. The lower startup current limit is selectable at 0x38:[7:6] and will be active for a period programmable at 0x37:[7:6]. The default soft start configuration will result in a smooth output voltage ramp under almost any condition. When disabled, the true shutdown switch is open, allowing the output to slowly discharge to 0 V.

The boost should not be enabled before VDD_BST is applied, as this will result in improper startup.

If startup into a load is required, some derating is required below approximately 3.0 V input to avoid UVLO. Additional VDD_BST capacitance up to 47 µF is recommended when starting into a load. Figure 41 shows the typical maximum load capability at startup for battery voltage less than 3 V. Higher values can be achieved with larger input cap, or by supplying VDD_BST directly.

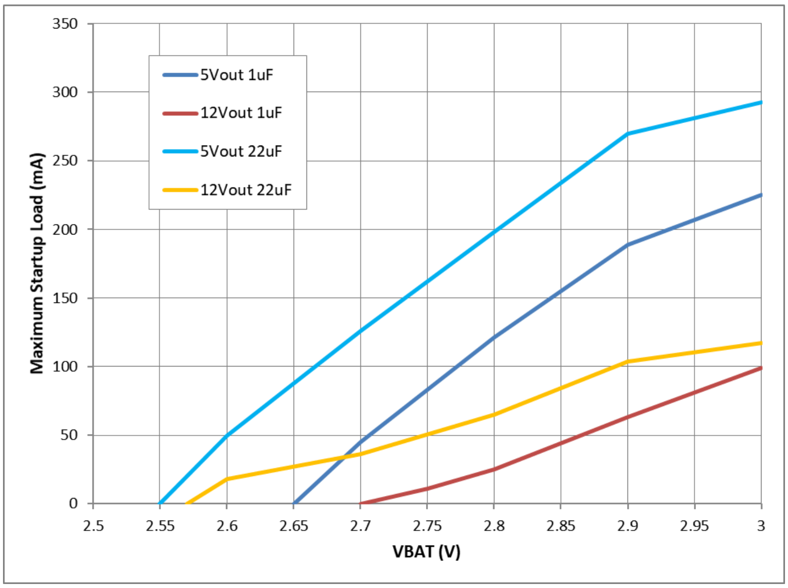


Figure 41: Maximum Boost Load at Startup vs VBAT

(VDD_BST cap = 1 µF and 22 µF)

9.10.2 Switch Node Anti-Ringing

An anti-ringing option is available and enabled by default at register 0x39:[4]. The anti-ringing function works during the high side OFF state to eliminate SW node ringing in DCM mode. The function creates a path across the inductor, between VDD_BST and SW_BST, to quickly bring SW_BST to the input voltage level. Anti-ringing eliminates DCM noise which may cause system interference while having a minimal impact on efficiency.

9.10.3 Protection

The boost regulator includes four types of protection, over-current, short-circuit, OVP, and UVLO. When the peak inductor current rises to the current limit threshold, the switching cycle is immediately terminated, reducing the duty cycle. If the load is maintained in current limit, the output voltage will drop. When the voltage drops to the short circuit threshold, SCP, the boost will stop switching, the true shutdown switch will be opened, and the boost will be disabled. The SCP threshold is 4 V for the output range of 9 V to 18 V, and 2 V for the output range of 4.5 V to 9 V. SCP will trigger an event flag and bit at 0x06.

If the output voltage rises 120% above the set value, and OVP fault will occur. This triggers an event flag and bit at 0x06. In OVP, the boost will stop switching but will not shutdown. Once the output voltage falls back to the target voltage, normal switching will resume.

The boost regulator has an independent UVLO threshold of 2.4 V typical. When the input voltage at VDD_BST drops to this threshold, the boost will be disabled. Boost UVLO also has an event flag and bit at 0x06. The boost will not automatically restart when VDD_BST rises above the UVLO threshold. Rather the Boost EN bit must be toggled.

9.10.4 Low Output Voltage Settings

The boost output voltage can be set as low as 4.5 V, which is below the maximum input voltage range of operation. Therefore, it is possible for the boost to be subjected to “buck” operating conditions. Because the boost is not designed for this range, the output will not be well regulated, but will drift upward towards Vin. The boost will continue to switch in pulse skipping mode which creates larger than normal output ripple. Additionally, in these “buck” conditions, the SCP may not function adequately as the output voltage is not controlled by switching.

9.11 LDO / Load Switches

Each of the three LDOs is configurable as either a load switch or an LDO and capable of delivering 150 mA to the load in either mode. All LDOs have uncommitted inputs which can be connected to VDD_SYS, the buck output, or another suitable source. If using the buck output, confirm that the buck provides sufficient headroom and current capability.

In LDO mode, LDO_0 can be programmed between 0.8 V and 3.15 V in 25 mV or 50 mV steps. LDO_1 and LDO_2 can be set between 0.8 V and 3.3 V in 50 mV or 75 mV steps. To ensure good regulation and full load capability, 200 mV of headroom is recommended at VDD_LDO, with load capability decreasing with lower headroom. With sufficient headroom the LDOs are current limited at a minimum of 215 mA. LDO_0 is designed to operate with lower headroom.

To achieve the best performance from the LDOs, it is recommended to place the input bypass cap as close as possible to the LDO input pins (VDD_LDO). A 1uF input capacitor is typically sufficient for each LDO, provided that there is at least that much capacitance at the VDD_SYS or BUCK output.

Each LDO is enabled and output voltage set at registers 0x32 through 0x34. The LDOs can be configured as load switches at register 0x36. There is an approximately 20 ms delay between the I2C enable command and LDO startup.

In load switch mode, there are two modes of operation: current limit enabled and full-on. Full-on mode disables the load switch current limit, while providing a much lower on-resistance. In current limit enabled operation, current limit is active with the same limit as the LDO mode limit.

Each load switch can operate over a wider range compared to LDO mode, with a minimum input voltage of 0.8 V. However, as with LDO mode, the load switch current capability is reduced at lower input voltages. At the minimum input voltage, expect a maximum load-switch capability of 1 mA.

9.12 Thermal Protection

The DA9070 is protected from internal overheating by the over-temperature shutdown function. When the junction temperature reaches T_{SHDN} , the device initiates power-cycle and the safety timer is reset.

When power-cycle ends, VDD_SYS will recover for several msec; if the junction temperature is still above T_{SHDN}, power-cycle will be initiated again. In this way, the DA9070 continually attempts to restart with an active duty cycle of less than 1%, sufficient to allow the IC to cool down. When the junction temperature has dropped below $T_{SHUTDOWN} – T_{HYS}$, power-cycling will stop. When an over-temperature fault occurs, SYS_FLT toggles and the OVT bit at 0x07 is set to 1.

To avoid tripping thermal shutdown, limit power dissipation to no more than:

$$P_{DISS} < \frac{118℃ - T_A}{R_{TH\_JA}}$$

Where T_A is the ambient temperature, R_{TH_JA} is the thermal resistance of the package and pcb. Typical values for R_{TH_JA} vary with pcb size, layer count, air-flow, and other factors. A typical value of 40 °C/W is a good starting point. P_{DISS} can be estimated as:

Equation 5:

$$P_{DISS} = P_{BUCK} + P_{LDO0} + P_{LDO1} + P_{LDO2} + P_{CHG} + P_{BST}$$

Where

- $P_{VLDO0} = (V_{VDD\_LDO0} – V_{VLDO0}) \times I_{LDO0}$
- $P_{VLDO1} = (V_{VDD\_LDO1} – V_{VLDO1}) \times I_{LDO1}$
- $P_{VLDO2} = (V_{VDD\_LDO2} – V_{VLDO2}) \times I_{LDO2}$
- $P_{CHG} = (V_{VDD\_PWR} – V_{BAT}) \times I_{CHG}$
- $P_{BUCK} = V_{O\_BUCK} \times I_{OUT\_BUCK} \times (1/\eta - 1) – DCR \times I_{OUT\_BUCK}$
- $P_{BST} = V_{O\_BST} \times I_{OUT\_BST} \times (1/\eta - 1) – DCR \times I_{OUT\_BST} \times V_{O\_BST}/V_{DD\_BST}$

  where η is the efficiency of the buck or boost converter and DCR is the inductor's DC resistance.

9.13 PCB Layout Guidelines

Following a few basic PCB design practices will ensure proper operation and optimal thermal performance from the DA9070.

The first priority is to reduce and isolate high frequency switching noise so that it does not disturb sensitive nodes. For the buck regulator, the primary sources of noise are at the input capacitor ground and VDD_BUCK nodes. The input capacitor should be connected as close as possible to the PGND_BUCK and VDD_BUCK pins. This reduces the parasitic inductance responsible for much of the voltage spikes during switching. The current carrying traces (VDD_BUCK, PGND, VOUT) should route directly to the pads of all capacitors, not through vias or separate traces. This applies to both input and output capacitors and is good practice in general. Where possible these current carrying traces should be wide or large copper areas to reduce impedance and improve thermal resistance. Route these traces on the top layer only. VDD_SYS and VDD_BUCK can be connected close to or at the pins to further reduce impedance.

These same guidelines apply somewhat differently to the boost, where VOUT_BST and PGND_BST are the primary sources of noise. Therefore, the output caps should be placed close to the pins and connected by thick traces on the top layer. On the boost input side, it is recommended to route the inductor current path and VDD_BST input path separately, with the input cap placed close to the VDD_BST pin. This provides some isolation from noise for VDD_BST.

The second largest noise sources are the SW nodes. Although the current here is not switching, the fast voltage swings can introduce noise through capacitive coupling. To reduce this, use the smallest area possible for the SW nodes, while keeping in mind the current handling requirements. Both SW_BST and SW_BUCK should be routed on the second layer with multiple vias, which allows the best routing for the buck input and boost output caps. As much as possible, surround the SW nodes with GND copper to help shield the nearby FB traces.

All signal traces such as FB, SDA, and SCL should be routed away from the SW nodes, buck input caps, boost output caps, and inductors. These sensitive traces can be shielded with GND copper or routed on a lower layer with a ground plane providing shielding.

To create a good shield, one inner layer should be flooded with copper and connected as a common ground to the GND pins of the IC (A1, D3, and F4) and external GND connections. Layer 2 is recommended. The PGND_BUCK pin should connect directly to the buck input cap before connecting to the ground plane. Similarly, the PGND_BST pin should connect directly to the boost output cap before connecting to the ground plane. Multiple ground planes, for example a mid-layer and bottom layer plane, are helpful to control high frequency noise and improve thermal performance.

It is very important that the AGND node should not be used as a ground plane. Instead, all AGND connections should connect to a small area or by star connection to the AGND pin. The AGND pin should connect to the larger ground plane in a quiet location.

A good example of top and second layer routing is shown in Figure 42 and Figure 43. The buck input cap is C21. C32 and C33 are the boost output caps. These three caps are placed close to the IC with no vias between the pin and the caps. C23 is the buck output cap, connected on the top layer. L20 and L30 are the buck and boost inductors; their SW nodes are routed on layer 2 and connected by multiple vias. C30 is the VDD_BST cap, placed close to the pin and connected by a different trace than L30.

Layer-2 is a mostly filled GND plane, which provides shielding around the SW nodes routed on this layer. The isolated AGND area is on the right side of Figure 43. AGND is connected to the GND area at a single point on another layer, not shown here.

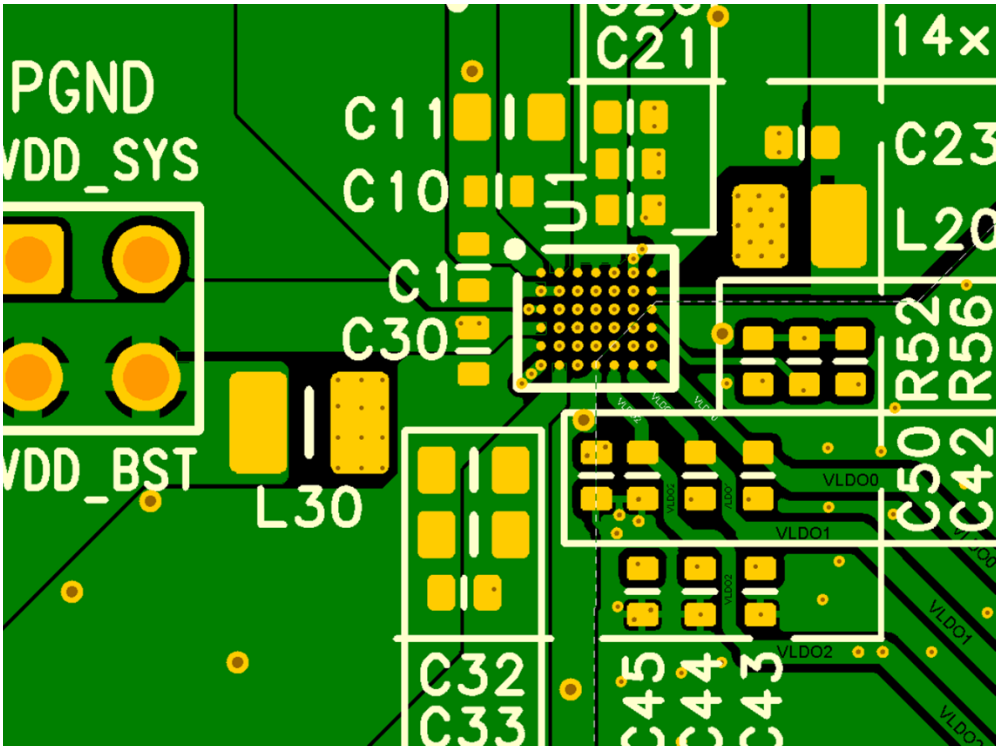


Figure 42: Example PCB Layout, Top Layer

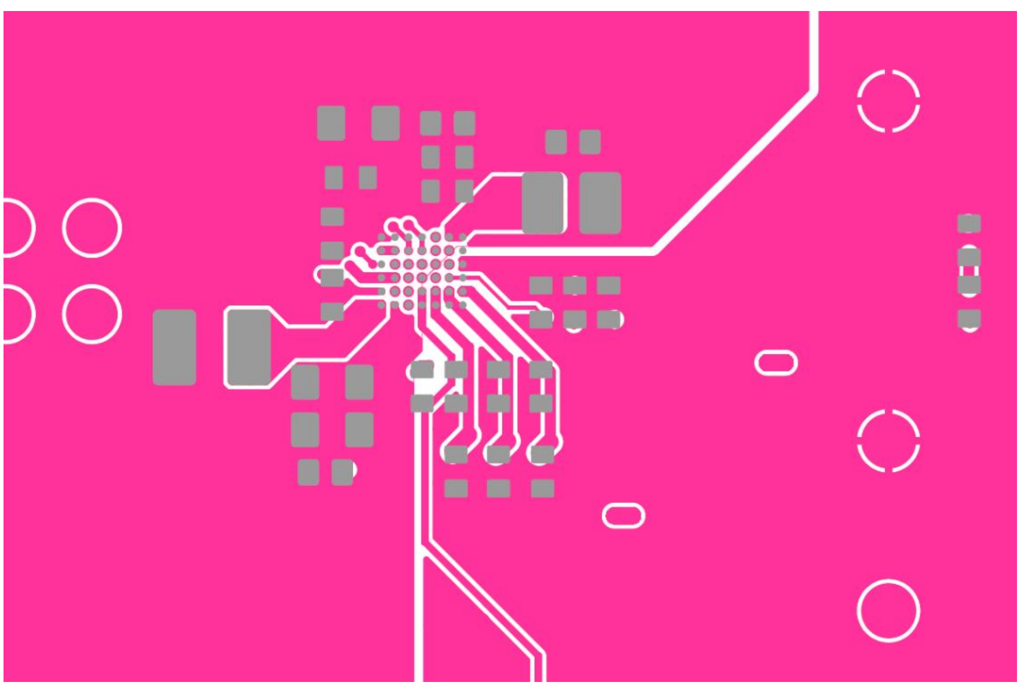


Figure 43: Example PCB Layout, Layer-2

10 Registers

10.1 Register Map

10.1.1 System

System									
Register	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYS_STS_0	0x0002	STS_BOOST	STS_BUCK	STS_CHG<1:0>		Reserved	Reserved	STS_PWR_CYC	STS_MODE
SYS_ISR_0	0x0003	Reserved	Reserved	ISR_VDD_SYS_UVLO	ISR_VDD_PWR_ILIM	ISR_VDD_PWR_DPM	ISR_VDD_PWR_UVLO_RCV	ISR_VDD_PWR_UVLO	ISR_VDD_PWR_OVP
SYS_ISR_1	0x0004	ISR_TS_HOT	ISR_TS_WARM	ISR_TS_COOL	ISR_TS_COLD	ISR_VBAT_SHORT	ISR_VBAT_OCP	ISR_VBAT_DPPM	ISR_VBAT_UVLO
SYS_ISR_2	0x0005	Reserved	ISR_TS_OFF	ISR_CHG_TMR	ISR_RECHG_START	ISR_CHG_DONE	ISR_PRECHG	ISR_BAT_SPPL	ISR_SLP
SYS_ISR_3	0x0006	Reserved	Reserved	ISR_BOOST_UVLO	ISR_BOOST_OVP	ISR_BOOST_SCP	ISR_BUCK_UVP	ISR_BUCK_OVP	ISR_BUCK_OCP
SYS_ISR_4	0x0007	ISR_PWR_PLGGD	ISR_MODE_FALL	ISR_MODE_RISE	ISR_WD	ISR_OVT	ISR_RIN_N_RST	ISR_RIN_N_WAKE2	ISR_RIN_N_WAKE1
SYS_IMR_0	0x0008	Reserved	Reserved	IMR_VDD_SYS_UVLO	IMR_VDD_PWR_ILIM	IMR_VDD_PWR_DPM	IMR_VDD_PWR_UVLO_RCV	IMR_VDD_PWR_UVLO	IMR_VDD_PWR_OVP
SYS_IMR_1	0x0009	IMR_TS_HOT	IMR_TS_WARM	IMR_TS_COOL	IMR_TS_COLD	IMR_VBAT_SHORT	IMR_VBAT_OCP	IMR_VBAT_DPPM	IMR_VBAT_UVLO
SYS_IMR_2	0x000A	Reserved	IMR_TS_OFF	IMR_CHG_TMR	IMR_RECHG_START	IMR_CHG_DONE	IMR_PRECHG	IMR_BAT_SPPL	IMR_SLP
SYS_IMR_3	0x000B	Reserved	Reserved	IMR_BOOST_UVLO	IMR_BOOST_OVP	IMR_BOOST_SCP	IMR_BUCK_UVP	IMR_BUCK_OVP	IMR_BUCK_OCP
SYS_IMR_4	0x000C	IMR_PWR_PLGGD	IMR_MODE_FALL	IMR_MODE_RISE	IMR_WD	IMR_OVT	IMR_RIN_N_RST	IMR_RIN_N_WAKE2	IMR_RIN_N_WAKE1

SYS_SYS_0	0x000D	INIT_REGS	Reserved	Reserved	Reserved	Reserved	Reserved 1	HZ_MODE	EN_SHIPMODE
SYS_BAT_0	0x000E	Reserved	Reserved	Reserved	VBAT_DIV_RATIO	Reserved	BUVLO<2:0>		
SYS_BAT_1	0x000F	Reserved	Reserved	Reserved	TS_TRIG	Reserved	Reserved	IDISCHG_MON_EN	VBATDIV_EN
SYS_RIN_N_0	0x0010	RIN_N_PER_RST<1:0>		RIN_N_PER_WAKE2	RIN_N_PER_WAKE1	RIN_N_RST_ROUT_EN<1:0>		RIN_N_RST_REC<1:0>	
SYS_STS_OUT_0	0x0011	Reserved	Reserved	Reserved	PWR_FLT_MODE	Reserved	Reserved	Reserved	SYS_FLT_MODE
SYS_PWR_CYC_0	0x0012	PWR_CYC_WAIT_PER<1:0>		PWR_CYC_PER<1:0>		Reserved	PWR_CYC_FRC	PWR_CYC_MODE	PWR_CYC_EN
SYS_PWR_CYC_1	0x0013	Reserved	BUCK_UVP_PWR_CYC_EN	Reserved 0	BUCK_OCP_PWR_CYC_EN	Reserved 0	Reserved	Reserved 0	BTS_PWR_CYC_EN
SYS_WD_0	0x0014	WD_RST_REGS_EN	WD_ROUT_EN	WD_TMR_PER<1:0>		WD_CLR_SEL<1:0>		WD_EN<1:0>	
SYS_I2C_0	0x0015	Reserved	Reserved	Reserved	Reserved	Reserved	I2C_RDCLR_DIS	I2C_RST_TMR_EN	I2C_HIZ_EN
Config									
Register	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SYS_CFG_I2C_0	0x0040	Reserved	I2C_SLAVE_ADDR<6:0>						

10.1.2 Charger

Charger and Power-path									
Register	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHG_CHG_0	0x0020	Reserved	Reserved	IPRETERM_REXT<1:0>		ICHG_MAX<1:0>		RMEAS_EN	CE_N
CHG_CHG_1	0x002	Reserve	TE_TS_COO	TE_TS_WARM	TE	TMRX2_EN	Reserved	TMR<1:0>	

	1	d	L						
CHG_ICHG_0	0x0022	Reserved	ICHG<6:0>						
CHG_IPRETERM_0	0x0023	Reserved	IPRETERM<6:0>						
CHG_VBREG_0	0x0024	Reserved	VBCHG<6:0>						
CHG_VBPRECHG_0	0x0025	Reserved	Reserved	Reserved	VBPRECHG_COMP_DIS	Reserved	VBPRECHG<2:0>		
CHG_BAT_TS_0	0x0026	Reserved	Reserved	TS_DISCHG_MODE_SEL	Reserved 0	TS_WARM_EN	TS_OFF_MODE	TS_EN_DISCHG	TS_EN_CHG
CHG_VDD_PWR_0	0x0027	Reserved	Reserved	Reserved	Reserved	ILIM<3:0>			
CHG_VDD_PWR_1	0x0028	Reserved	Reserved	VDD_PWR_OVP_DIS	VDD_PWR_DPM_DIS	ILIM_EN	VDD_PWR_DPM<2:0>		
CHG_IDISCHG_0	0x0029	Reserved	Reserved	Reserved	IDISCHG_OCP<2:0>			IDISCHG_OCP_HIZ_EN	IDISCHG_OCP_EN

10.1.3 Buck, Boost, and LDO Control

Vout User Registers									
Register	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VOUT_BUCK	0x0030	BUCK_EN	VOUT_RANGE_HI	Reserved	BUCK_VOUT<4:0>				
VOUT_BUCK_CFG	0x0031	Reserved	Reserved	BUCK_PD_CFG2	Reserved 0	Reserved	Reserved	SEL_ILIM_DLT<1:0>	
VOUT_LS_LDO0	0x0032	EN_LS_LDO_0	Reserved	LS_LDO_0<5:0>					
VOUT_LS_LDO1	0x0033	EN_LS_LDO_1	Reserved	LS_LDO_1<5:0>					
VOUT_LS_LDO2	0x0034	EN_LS_LDO_2	Reserved	LS_LDO_2<5:0>					
VOUT_LS_LDO_CFG	0x0035	Reserved	SEL_FULLON_2	SEL_FULLON_1	SEL_FULLON_0	Reserved	SEL_LDSW_2	SEL_LDSW_1	SEL_LDSW_0

VOUT_BOOST	0x0036	BOOST_EN	BOOST_VOUT<6:0>						
VOUT_BOOST_CFG0	0x0037	TSS_SEL<1:0>		TPCHG_SEL<1:0>		Reserved	Reserved	Reserved	BST_CFG_FREQ
VOUT_BOOST_CFG1	0x0038	BST_CFG_OCS<1:0>		BST_CFG_OC<1:0>		Reserved 0	Reserved 1	Reserved 1	Reserved 0
VOUT_BOOST_CFG2	0x0039	Reserved 0	Reserved 1	Reserved 1	BST_CFG_ANTI	BST_CFG_PCHGLMT<3:0>			
Vout Opt Registers									
Register	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VOUT_BUCK_OPT0	0x0050	Reserved 0	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 0	DVC_STEP<1:0>	
Vout Test Registers									
Register	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

10.2 Register Definitions

10.2.1 System

Table 45: Register SYS_STS_0

Address	Register Name	POR Value	Status
0x0002	SYS_STS_0	0x00	

7	6	5	4	3	2	1	0
STS_BOOST	STS_BUCK	STS_CHG<1:0>		Reserved	Reserved	STS_PWR_CYC	STS_MODE

Field Name	Bits	POR	Description
STS_BOOST	[7]	0x0	Boost no fault status
STS_BUCK	[6]	0x0	Buck power-good status
STS_CHG	[5:4]	0x0	Charge status Value: Description 0x0 (POR): Charge ready 0x1: Charge in progress 0x2: Charge done 0x3: Fault
STS_PWR_CYC	[1]	0x0	Power cycle status register. Cleared after being read
STS_MODE	[0]	0x0	MODE pin status

Table 46: Register SYS_ISR_0

Address	Register Name	POR Value	IRQ status
0x0003	SYS_ISR_0	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	ISR_VDD_SYS_UVLO	ISR_VDD_PWR_ILIM	ISR_VDD_PWR_DPM	ISR_VDD_PWR_UVLO_RCV	ISR_VDD_PWR_UVLO	ISR_VDD_PWR_OVP

Field Name	Bits	POR	Description
ISR_VDD_SYS_UVLO	[5]	0x0	VDD_SYS UVLO IRQ status
ISR_VDD_PWR_ILIM	[4]	0x0	VDD_PWR ILIM IRQ status
ISR_VDD_PWR_DPM	[3]	0x0	VDD_PWR DPM IRQ status
ISR_VDD_PWR_UVLO_RCV	[2]	0x0	VDD_PWR UVLO recovery IRQ status
ISR_VDD_PWR_UVLO	[1]	0x0	VDD_PWR UVLO IRQ status
ISR_VDD_PWR_OVP	[0]	0x0	VDD_PWR OVP IRQ status

Table 47: Register SYS_ISR_1

Address	Register Name	POR Value	IRQ status
0x0004	SYS_ISR_1	0x00	

7	6	5	4	3	2	1	0
ISR_TS_HOT	ISR_TS_WARM	ISR_TS_COOL	ISR_TS_COLD	ISR_VBAT_SHORT	ISR_VBAT_OCP	ISR_VBAT_DPPM	ISR_VBAT_UVLO

Field Name	Bits	POR	Description
ISR_TS_HOT	[7]	0x0	Battery temperature sensor IRQ status.TS_HOT
ISR_TS_WARM	[6]	0x0	Battery temperature sensor IRQ status.TS_WARM
ISR_TS_COOL	[5]	0x0	Battery temperature sensor IRQ status.TS_COOL
ISR_TS_COLD	[4]	0x0	Battery temperature sensor IRQ status.TS_COLD
ISR_VBAT_SHORT	[3]	0x0	VBAT short IRQ status
ISR_VBAT_OCP	[2]	0x0	VBAT OCP IRQ status
ISR_VBAT_DPPM	[1]	0x0	VBAT DPPM IRQ status
ISR_VBAT_UVLO	[0]	0x0	VBAT UVLO IRQ status

Table 48: Register SYS_ISR_2

Address	Register Name	POR Value	IRQ status
0x0005	SYS_ISR_2	0x00	

7	6	5	4	3	2	1	0
Reserved	ISR_TS_OFF	ISR_CHG_TMR	ISR_RECHG_START	ISR_CHG_DONE	ISR_PRECHG	ISR_BAT_SPPL	ISR_SLP

Field Name	Bits	POR	Description
ISR_TS_OFF	[6]	0x0	Battery temperature sensor IRQ status.TS_OFF
ISR_CHG_TMR	[5]	0x0	Charge safety timer IRQ status
ISR_RECHG_START	[4]	0x0	Recharge started IRQ status
ISR_CHG_DONE	[3]	0x0	Charge done IRQ status
ISR_PRECHG	[2]	0x0	Pre-charge IRQ status
ISR_BAT_SPPL	[1]	0x0	Battery supplement mode IRQ status
ISR_SLP	[0]	0x0	Sleep mode IRQ status

Table 49: Register SYS_ISR_3

Address	Register Name	POR Value	IRQ status
0x0006	SYS_ISR_3	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	ISR_BOOST_UVLO	ISR_BOOST_OVP	ISR_BOOST_SCP	ISR_BUCK_UVP	ISR_BUCK_OVP	ISR_BUCK_OCP

Field Name	Bits	POR	Description
ISR_BOOST_UVLO	[5]	0x0	Boost UVP IRQ status
ISR_BOOST_OVP	[4]	0x0	Boost OVP IRQ status
ISR_BOOST_SCP	[3]	0x0	Boost OCP IRQ status

ISR_BUCK_UVP	[2]	0x0	Buck UVP IRQ status
ISR_BUCK_OVP	[1]	0x0	Buck OVP IRQ status
ISR_BUCK_OCP	[0]	0x0	Buck OCP IRQ status

Table 50: Register SYS_ISR_4

Address	Register Name	POR Value	IRQ status
0x0007	SYS_ISR_4	0x00	

7	6	5	4	3	2	1	0
ISR_PWR_PLGGD	ISR_MODE_FALL	ISR_MODE_RISE	ISR_WD	ISR_OVT	ISR_RIN_N_RST	ISR_RIN_N_WAKE2	ISR_RIN_N_WAKE1

Field Name	Bits	POR	Description
ISR_PWR_PLGGD	[7]	0x0	VDD_PWR insertion/removal power cycle IRQ status
ISR_MODE_FALL	[6]	0x0	MODE pin falling edge IRQ status
ISR_MODE_RISE	[5]	0x0	MODE pin rising edge IRQ status
ISR_WD	[4]	0x0	Watchdog timer IRQ status
ISR_OVT	[3]	0x0	Overtemperature IRQ status
ISR_RIN_N_RST	[2]	0x0	RIN_N RESET timer IRQ status
ISR_RIN_N_WAKE2	[1]	0x0	RIN_N WAKE2 timer IRQ status
ISR_RIN_N_WAKE1	[0]	0x0	RIN_N WAKE1 timer IRQ status

Table 51: Register SYS_IMR_0

Address	Register Name	POR Value	IRQ mask
0x0008	SYS_IMR_0	0x3F	

7	6	5	4	3	2	1	0
Reserved	Reserved	IMR_VDD_SYS_UVLO	IMR_VDD_PWR_ILIM	IMR_VDD_PWR_DPM	IMR_VDD_PWR_UVLO_RCV	IMR_VDD_PWR_UVLO	IMR_VDD_PWR_OVP

Field Name	Bits	POR	Description
IMR_VDD_SYS_UVLO	[5]	0x1	VDD_SYS UVLO IRQ mask
IMR_VDD_PWR_ILIM	[4]	0x1	VDD_PWR ILIM IRQ mask
IMR_VDD_PWR_DPM	[3]	0x1	VDD_PWR DPM IRQ mask
IMR_VDD_PWR_UVLO_RCV	[2]	0x1	VDD_PWR UVLO recovery IRQ mask
IMR_VDD_PWR_UVLO	[1]	0x1	VDD_PWR UVLO IRQ mask
IMR_VDD_PWR_OVP	[0]	0x1	VDD_PWR OVP IRQ mask

Table 52: Register SYS_IMR_1

Address	Register Name	POR Value	IRQ mask
0x0009	SYS_IMR_1	0xFF	

7	6	5	4	3	2	1	0
IMR_TS_HOT	IMR_TS_WARM	IMR_TS_COOL	IMR_TS_COLD	IMR_VBAT_SHORT	IMR_VBAT_OCP	IMR_VBAT_DPPM	IMR_VBAT_UVLO

Field Name	Bits	POR	Description
IMR_TS_HOT	[7]	0x1	Battery temperature sensor IRQ mask.TS_HOT
IMR_TS_WARM	[6]	0x1	Battery temperature sensor IRQ mask.TS_WARM
IMR_TS_COOL	[5]	0x1	Battery temperature sensor IRQ mask.TS_COOL
IMR_TS_COLD	[4]	0x1	Battery temperature sensor IRQ mask.TS_COLD
IMR_VBAT_SHORT	[3]	0x1	VBAT short IRQ mask
IMR_VBAT_OCP	[2]	0x1	VBAT OCP IRQ mask
IMR_VBAT_DPPM	[1]	0x1	VBAT DPPM IRQ mask
IMR_VBAT_UVLO	[0]	0x1	VBAT UVLO IRQ mask

Table 53: Register SYS_IMR_2

Address	Register Name	POR Value	
0x000A	SYS_IMR_2	0x7F	IRQ mask

7	6	5	4	3	2	1	0
Reserved	IMR_TS_OFF	IMR_CHG_TMR	IMR_RECHG_START	IMR_CHG_DONE	IMR_PRECHG	IMR_BAT_SPPL	IMR_SLP

Field Name	Bits	POR	Description
IMR_TS_OFF	[6]	0x1	Battery temperature sensor IRQ mask.TS_OFF
IMR_CHG_TMR	[5]	0x1	Charge safety timer IRQ mask
IMR_RECHG_START	[4]	0x1	Recharge started IRQ mask
IMR_CHG_DONE	[3]	0x1	Charge done IRQ mask
IMR_PRECHG	[2]	0x1	Pre-charge started IRQ mask
IMR_BAT_SPPL	[1]	0x1	Battery supplement mode IRQ mask
IMR_SLP	[0]	0x1	Sleep mode IRQ mask

Table 54: Register SYS_IMR_3

Address	Register Name	POR Value	
0x000B	SYS_IMR_3	0x3F	IRQ mask

7	6	5	4	3	2	1	0
Reserved	Reserved	IMR_BOOST_UVLO	IMR_BOOST_OVP	IMR_BOOST_SCP	IMR_BUCK_UVP	IMR_BUCK_OVP	IMR_BUCK_OCP

Field Name	Bits	POR	Description
IMR_BOOST_UVLO	[5]	0x1	Boost UVP IRQ mask
IMR_BOOST_OVP	[4]	0x1	Boost OVP IRQ mask
IMR_BOOST_SCP	[3]	0x1	Boost OCP IRQ mask

IMR_BUCK_UVP	[2]	0x1	Buck UVP IRQ mask
IMR_BUCK_OVP	[1]	0x1	Buck OVP IRQ mask
IMR_BUCK_OCP	[0]	0x1	Buck OCP IRQ mask

Table 55: Register SYS_IMR_4

Address	Register Name	POR Value	IRQ mask
0x000C	SYS_IMR_4	0xFF	

7	6	5	4	3	2	1	0
IMR_PWR_PLGGD	IMR_MODE_FALL	IMR_MODE_RISE	IMR_WD	IMR_OVT	IMR_RIN_N_RST	IMR_RIN_N_WAKE2	IMR_RIN_N_WAKE1

Field Name	Bits	POR	Description
IMR_PWR_PLGGD	[7]	0x1	VDD_PWR insertion/removal power cycle IRQ mask
IMR_MODE_FALL	[6]	0x1	MODE pin falling edge IRQ mask
IMR_MODE_RISE	[5]	0x1	MODE pin rising edge IRQ mask
IMR_WD	[4]	0x1	Watchdog timer IRQ mask
IMR_OVT	[3]	0x1	Overtemperature IRQ mask
IMR_RIN_N_RST	[2]	0x1	RIN_N RESET timer IRQ mask
IMR_RIN_N_WAKE2	[1]	0x1	RIN_N WAKE2 timer IRQ mask
IMR_RIN_N_WAKE1	[0]	0x1	RIN_N WAKE1 timer IRQ mask

Table 56: Register SYS_SYS_0

Address	Register Name	POR Value	System configuration
0x000D	SYS_SYS_0	0x04	

7	6	5	4	3	2	1	0
INIT_REGS	Reserved	Reserved	Reserved	Reserved	Reserved 1	HZ_MODE	EN_SHIPMODE

Field Name	Bits	POR	Description
INIT_REGS	[7]	0x0	Initialize register trigger
HZ_MODE	[1]	0x0	Hi-Z mode entry control. Automatically cleared when HZ mode exit
EN_SHIPMODE	[0]	0x0	Shipmode entry control

Table 57: Register SYS_BAT_0

Address	Register Name	POR Value	System configuration
0x000E	SYS_BAT_0	0x06	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	VBAT_DIV_RATIO	Reserved	BUVLO<2:0>		

Field Name	Bits	POR	Description
VBAT_DIV_RATIO	[4]	0x0	VBATDIV divider ratio setting **Value** / **Description** 0x0 (POR): 60 % 0x1: 30 %
BUVLO	[2:0]	0x6	Battery UVLO threshold **Value** / **Description**

			0x0	Reserved
			0x1	2.5 V
			0x2	2.6 V
			0x3	2.7 V
			0x4	2.8 V
			0x5	2.9 V
			0x6 (POR)	3.0 V
			0x7	Reserved

Table 58: Register SYS_BAT_1

Address	Register Name	POR Value	System configuration
0x000F	SYS_BAT_1	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	TS_TRIG	Reserved	Reserved	IDISCHG_MON_EN	VBATDIV_EN

Field Name	Bits	POR	Description
TS_TRIG	[4]	0x0	Trigger register for one-shot battery temp sense enable
IDISCHG_MON_EN	[1]	0x0	Enable battery discharge current monitor
VBATDIV_EN	[0]	0x0	Battery voltage divider enable

Table 59: Register SYS_RIN_N_0

Address	Register Name	POR Value	RIN_N
0x0010	SYS_RIN_N_0	0x66	

7	6	5	4	3	2	1	0
RIN_N_PER_RST<1:0>		RIN_N_PER_WAKE2	RIN_N_PER_WAKE1	RIN_N_RST_ROUT_EN<1:0>		RIN_N_RST_REC<1:0>	

<table>
<tr><th>Field Name</th><th>Bits</th><th>POR</th><th>Description</th></tr>
<tr><td>RIN_N_PER_RST</td><td>[7:6]</td><td>0x1</td><td>RIN_N RESET timer period<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>4 s</td></tr><tr><td>0x1 (POR)</td><td>8 s</td></tr><tr><td>0x2</td><td>10 s</td></tr><tr><td>0x3</td><td>14 s</td></tr></table></td></tr>
<tr><td>RIN_N_PER_WAKE2</td><td>[5]</td><td>0x1</td><td>RIN_N WAKE2 timer period<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>1.0 s</td></tr><tr><td>0x1 (POR)</td><td>1.5 s</td></tr></table></td></tr>
<tr><td>RIN_N_PER_WAKE1</td><td>[4]</td><td>0x0</td><td>RIN_N WAKE1 timer period<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0 (POR)</td><td>50 ms</td></tr><tr><td>0x1</td><td>500 ms</td></tr></table></td></tr>
<tr><td>RIN_N_RST_ROUT_EN</td><td>[3:2]</td><td>0x1</td><td>ROUT_N pulse output enable for RESET wake-up<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>Disable</td></tr><tr><td>0x1 (POR)</td><td>Enable</td></tr><tr><td>0x2</td><td>Enable only when VDD_PWR is present</td></tr><tr><td>0x3</td><td>Reserved</td></tr></table></td></tr>
<tr><td>RIN_N_RST_REC</td><td>[1:0]</td><td>0x2</td><td>Reset timer Hi-Z / ship mode transition control<table><tr><th>Value</th><th>Description</th></tr></table></td></tr>
</table>

			0x0	Reset timer is not used for both
			0x1	Enter ship mode after RIN_N reset timer hit
			0x2 (POR)	Enter Hi-Z mode after RIN_N reset timer hit
			0x3	Reserved

Table 60: Register SYS_STS_OUT_0

Address	Register Name	POR Value	Status indicator
0x0011	SYS_STS_OUT_0	0x01	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	PWR_FLT_MODE	Reserved	Reserved	Reserved	SYS_FLT_MODE

Field Name	Bits	POR	Description	
PWR_FLT_MODE	[4]	0x0	PWR_FLT mode select	
			Value	**Description**
			0x0 (POR)	Power good indicator
			0x1	Voltage shifted RIN_N output
SYS_FLT_MODE	[0]	0x1	SYS_FLT mode select	
			Value	**Description**
			0x0	IRQ I/F enabled and charge status indicator disabled
			0x1 (POR)	IRQ I/F enabled and charge status indicator enabled

Table 61: Register SYS_PWR_CYC_0

Address	Register Name	POR Value	Power cycle
0x0012	SYS_PWR_CYC_0	0x91	

7	6	5	4	3	2	1	0
PWR_CYC_WAIT_PER<1:0>		PWR_CYC_PER<1:0>		Reserved	PWR_CYC_FRC	PWR_CYC_MODE	PWR_CYC_EN

<table>
<tr><th>Field Name</th><th>Bits</th><th>POR</th><th>Description</th></tr>
<tr><td>PWR_CYC_WAIT_PER</td><td>[7:6]</td><td>0x2</td><td>Power cycle wait period setting
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0x0</td><td>0 s</td></tr>
<tr><td>0x1</td><td>0.5 s</td></tr>
<tr><td>0x2 (POR)</td><td>1.0 s</td></tr>
<tr><td>0x3</td><td>2.0 s</td></tr>
</table></td></tr>
<tr><td>PWR_CYC_PER</td><td>[5:4]</td><td>0x1</td><td>Power cycle period setting
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0x0</td><td>5 s</td></tr>
<tr><td>0x1 (POR)</td><td>10 s</td></tr>
<tr><td>0x2</td><td>15 s</td></tr>
<tr><td>0x3</td><td>20 s</td></tr>
</table></td></tr>
<tr><td>PWR_CYC_FRC</td><td>[2]</td><td>0x0</td><td>Write 1 to force power-cycling</td></tr>
<tr><td>PWR_CYC_MODE</td><td>[1]</td><td>0x0</td><td>Power cycle trigger select
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0x0 (POR)</td><td>VDD_PWR insertion/removal</td></tr>
<tr><td>0x1</td><td>RESET wake-up timer when VDD_PWR present</td></tr>
</table></td></tr>
<tr><td>PWR_CYC_EN</td><td>[0]</td><td>0x1</td><td>Power cycle enable</td></tr>
</table>

Table 62: Register SYS_PWR_CYC_1

Address	Register Name	POR Value	Power cycle
0x0013	SYS_PWR_CYC_1	0x00	

7	6	5	4	3	2	1	0
Reserved	BUCK_UVP_PWR_CYC_EN	Reserved 0	BUCK_OCP_PWR_CYC_EN	Reserved 0	Reserved	Reserved 0	BTS_PWR_CYC_EN

Field Name	Bits	POR	Description
BUCK_UVP_PWR_CYC_EN	[6]	0x0	Power cycle enable triggered by Buck UVP
BUCK_OCP_PWR_CYC_EN	[4]	0x0	Power cycle enable triggered by Buck OCP
BTS_PWR_CYC_EN	[0]	0x0	Power cycle enable triggered by TS_HOT

Table 63: Register SYS_WD_0

Address	Register Name	POR Value	Watchdog timer
0x0014	SYS_WD_0	0x10	

7	6	5	4	3	2	1	0
WD_RST_REGS_EN	WD_ROUT_EN	WD_TMR_PER<1:0>		WD_CLR_SEL<1:0>		WD_EN<1:0>	

Field Name	Bits	POR	Description
WD_RST_REGS_EN	[7]	0x0	Register reset on watchdog timeout enable
WD_ROUT_EN	[6]	0x0	Reset output on watchdog timeout enable
WD_TMR_PER	[5:4]	0x1	Watchdog timer timeout period **Value** / **Description** 0x0: 25 s 0x1 (POR): 50 s

			<table><tr><td>0x2</td><td>Reserved</td></tr><tr><td>0x3</td><td>Reserved</td></tr></table>
WD_CLR_SEL	[3:2]	0x0	Watchdog timer clear condition<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0 (POR)</td><td>Only I2C clears the timer</td></tr><tr><td>0x1</td><td>Only WD pin clears the timer</td></tr><tr><td>0x2</td><td>Both I2C and WD pin clear the timer</td></tr><tr><td>0x3</td><td>Reserved</td></tr></table>
WD_EN	[1:0]	0x0	Watchdog timer enable<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0 (POR)</td><td>Disable</td></tr><tr><td>0x1</td><td>Enable only when VDD_PWR present</td></tr><tr><td>0x2</td><td>Disable in Hi-Z mode</td></tr><tr><td>0x3</td><td>Always enable</td></tr></table>

Table 64: Register SYS_I2C_0

Address	Register Name	POR Value	I2C
0x0015	SYS_I2C_0	0x00	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	Reserved	I2C_RDCLR_DIS	I2C_RST_TMR_EN	I2C_HIZ_EN

Field Name	Bits	POR	Description
I2C_RDCLR_DIS	[2]	0x0	I2C read clear disable for ISR registers and STS_PWR_CYC register
I2C_RST_TMR_EN	[1]	0x0	I2C reset timer enable

I2C_HIZ_EN	[0]	0x0	I2C enable in Hi-Z mode

10.2.2 Config

Table 65: Register SYS_CFG_I2C_0

Address	Register Name	POR Value	I2C
0x0040	SYS_CFG_I2C_0	0x68	

7	6	5	4	3	2	1	0
Reserved	I2C_SLAVE_ADDR<6:0>						

Field Name	Bits	POR	Description
I2C_SLAVE_ADDR	[6:0]	0x68	I2C slave addr

10.2.3 Charger

10.2.3.1 Charger and Power-Path

Table 66: Register CHG_CHG_0

Address	Register Name	POR Value	Charge
0x0020	CHG_CHG_0	0x01	

7	6	5	4	3	2	1	0
Reserved	Reserved	IPRETERM_REXT<1:0>		ICHG_MAX<1:0>		RMEAS_EN	CE_N

<table>
<tr><th>Field Name</th><th>Bits</th><th>POR</th><th>Description</th></tr>
<tr><td>IPRETERM_REXT</td><td>[5:4]</td><td>0x0</td><td>Charge termination/pre-charge current range by RITER_CHG. Read-only.
<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0 (POR)</td><td>5 % of ICHG</td></tr><tr><td>0x1</td><td>10 % of ICHG</td></tr></table></td></tr>
</table>

			0x2: 15 % of ICHG 0x3: 20 % of ICHG
ICHG_MAX	[3:2]	0x0	Maximum charge current limit. **Value** / **Description** 0x0 (POR): No limit 0x1: 20 mA 0x2: 70 mA 0x3: 200 mA
RMEAS_EN	[1]	0x0	External resistance programming enable. Write-locked when CE_N is 0.
CE_N	[0]	0x1	Charge enable **Value** / **Description** 0x0: Enable charging 0x1 (POR): Disable charging

Table 67: Register CHG_CHG_1

Address	Register Name	POR Value	
0x0021	CHG_CHG_1	0x19	Charge

7	6	5	4	3	2	1	0
Reserved	TE_TS_COOL	TE_TS_WARM	TE	TMRX2_EN	Reserved	TMR<1:0>	

Field Name	Bits	POR	Description
TE_TS_COOL	[6]	0x0	Termination enable during TS COOL. Write-locked when CE_N is 0.
TE_TS_WARM	[5]	0x0	Termination enable during TS WARM. Write-locked when CE_N is 0.
TE	[4]	0x1	Charge current termination enable. Write-locked when CE_N is 0.

TMRX2_EN	[3]	0x1	Safety timer half rate enable. Write-locked when CE_N is 0.
TMR	[1:0]	0x1	Safety timer period. Write-locked when CE_N is 0. **Value** / **Description** 0x0: 30 m 0x1 (POR): 3 h 0x2: 9 h 0x3: Timer disabled

Table 68: Register CHG_ICHG_0

Address	Register Name	POR Value	Charge current
0x0022	CHG_ICHG_0	0x41	

7	6	5	4	3	2	1	0
Reserved	ICHG<6:0>						

Field Name	Bits	POR	Description
ICHG	[6:0]	0x41	Charge current (mA) 2.0 to 4.8 mA settings are available when SEL_ICHG_LOW=1. **Value** / **Description** 0x0: 5 (2) 0x1: 6 (2.4) 0x2: 7 (2.8) 0x3: 8 (3.2) 0x4: 9 (3.6) 0x5: 10 (4) 0x6: 11 (4.4)

			0x7	12 (4.8)
			0x8	13
			0x9	14
			0x0A	15
			0x0B	16
			0x0C	17
			0x0D	18
			0x0E	19
			0x0F	20
			0x10	21
			0x11	22
			0x12	23
			0x13	24
			0x14	25
			0x15	26
			0x16	27
			0x17	28
			0x18	29
			0x19	30
			0x1A	31
			0x1B	32
			0x1C	33
			0x1D	34

			0x1E	35
			0x1F	Reserved
			0x3F	Reserved
			0x40	40
			0x41 (POR)	50
			0x42	60
			0x43	70
			0x44	80
			0x45	90
			0x46	100
			0x47	110
			0x48	120
			0x49	130
			0x4A	140
			0x4B	150
			0x4C	160
			0x4D	170
			0x4E	180
			0x4F	190
			0x50	200
			0x51	210
			0x52	220
			0x53	230

			0x54	240
			0x55	250
			0x56	260
			0x57	270
			0x58	280
			0x59	290
			0x5A	300
			0x5B	310
			0x5C	320
			0x5D	330
			0x5E	340
			0x5F	350
			0x60	360
			0x61	370
			0x62	380
			0x63	390
			0x64	400
			0x65	410
			0x66	420
			0x67	430
			0x68	440
			0x69	450
			0x6A	460

			0x6B | 470
			0x6C | 480
			0x6D | 490
			0x6E | 500
			0x6F | Reserved
			0x7F | Reserved

Table 69: Register CHG_IPRETERM_0

Address	Register Name	POR Value	Precharge / termination current
0x0023	CHG_IPRETERM_0	0x04	

7	6	5	4	3	2	1	0
Reserved	IPRETERM<6:0>						

Field Name	Bits	POR	Description
IPRETERM	[6:0]	0x4	Precharge / termination current
			Value | **Description**
			0x0 | 0.5
			0x1 | 1
			0x2 | 1.5
			0x3 | 2
			0x4 (POR) | 2.5
			0x5 | 3
			0x6 | 3.5

			0x7	4
			0x8	4.5
			0x9	5
			0x0A	Reserved
			0x3F	Reserved
			0x40	6
			0x41	7
			0x42	8
			0x43	9
			0x44	10
			0x45	11
			0x46	12
			0x47	13
			0x48	14
			0x49	15
			0x4A	16
			0x4B	17
			0x4C	18
			0x4D	19
			0x4E	20
			0x4F	21
			0x50	22
			0x51	23

			0x52	24
			0x53	25
			0x54	26
			0x55	27
			0x56	28
			0x57	29
			0x58	30
			0x59	31
			0x5A	32
			0x5B	33
			0x5C	34
			0x5D	35
			0x5E	36
			0x5F	37
			0x60	38
			0x61	39
			0x62	40
			0x63	41
			0x64	42
			0x65	43
			0x66	44
			0x67	45
			0x68	46

			0x69	47
			0x6A	48
			0x6B	49
			0x6C	50
			0x6D	Reserved
			0x7F	Reserved

Table 70: Register CHG_VBREG_0

Address	Register Name	POR Value	Battery regulation voltage
0x0024	CHG_VBREG_0	0x3C	

7	6	5	4	3	2	1	0
Reserved	VBCHG<6:0>						

Field Name	Bits	POR	Description	
VBCHG	[6:0]	0x3C	Battery regulation voltage	
			Value	**Description**
			0x0	3.6
			0x1	3.61
			0x2	3.62
			0x3	3.63
			0x4	3.64
			0x5	3.65
			0x6	3.66

			0x7	3.67
			0x8	3.68
			0x9	3.69
			0x0A	3.7
			0x0B	3.71
			0x0C	3.72
			0x0D	3.73
			0x0E	3.74
			0x0F	3.75
			0x10	3.76
			0x11	3.77
			0x12	3.78
			0x13	3.79
			0x14	3.8
			0x15	3.81
			0x16	3.82
			0x17	3.83
			0x18	3.84
			0x19	3.85
			0x1A	3.86
			0x1B	3.87
			0x1C	3.88
			0x1D	3.89

			0x1E	3.9
			0x1F	3.91
			0x20	3.92
			0x21	3.93
			0x22	3.94
			0x23	3.95
			0x24	3.96
			0x25	3.97
			0x26	3.98
			0x27	3.99
			0x28	4
			0x29	4.01
			0x2A	4.02
			0x2B	4.03
			0x2C	4.04
			0x2D	4.05
			0x2E	4.06
			0x2F	4.07
			0x30	4.08
			0x31	4.09
			0x32	4.1
			0x33	4.11
			0x34	4.12

			0x35	4.13
			0x36	4.14
			0x37	4.15
			0x38	4.16
			0x39	4.17
			0x3A	4.18
			0x3B	4.19
			0x3C (POR)	4.2
			0x3D	4.21
			0x3E	4.22
			0x3F	4.23
			0x40	4.24
			0x41	4.25
			0x42	4.26
			0x43	4.27
			0x44	4.28
			0x45	4.29
			0x46	4.3
			0x47	4.31
			0x48	4.32
			0x49	4.33
			0x4A	4.34
			0x4B	4.35

			0x4C	4.36
			0x4D	4.37
			0x4E	4.38
			0x4F	4.39
			0x50	4.4
			0x51	4.41
			0x52	4.42
			0x53	4.43
			0x54	4.44
			0x55	4.45
			0x56	4.46
			0x57	4.47
			0x58	4.48
			0x59	4.49
			0x5A	4.5
			0x5B	4.51
			0x5C	4.52
			0x5D	4.53
			0x5E	4.54
			0x5F	4.55
			0x60	4.56
			0x61	4.57
			0x62	4.58

			0x63 — 4.59 0x64 — 4.6 0x65 — 4.61 0x66 — 4.62 0x67 — 4.63 0x68 — 4.64 0x69 — 4.65 0x6A — Reserved 0x7F — Reserved

Table 71: Register CHG_VBPRECHG_0

Address	Register Name	POR Value	Battery precharge voltage
0x0025	CHG_VBPRECHG_0	0x06	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	VBPRECHG_COMP_DIS	Reserved	VBPRECHG<2:0>		

Field Name	Bits	POR	Description
VBPRECHG_COMP_DIS	[4]	0x0	Precharge comparator disable. Charger operates in pre-charge mode when VBAT short detected. Write-locked when CE_N is 0. **Value** — **Description** 0x0 (POR) — Precharge threshold is as specified by VBPRECHG 0x1 — Charger will ignore precharge threshold
VBPRECHG	[2:0]	0x6	Battery precharge voltage (V) **Value** — **Description**

			0x0	Reserved
			0x1	2.7
			0x2	2.8
			0x3	2.9
			0x4	3
			0x5	3.1
			0x6 (POR)	3.2
			0x7	Reserved

Table 72: Register CHG_BAT_TS_0

Address	Register Name	POR Value	Battery temperature sense
0x0026	CHG_BAT_TS_0	0x01	

7	6	5	4	3	2	1	0
Reserved	Reserved	TS_DISCHG_MODE_SEL	Reserved 0	TS_WARM_EN	TS_OFF_MODE	TS_EN_DISCHG	TS_EN_CHG

Field Name	Bits	POR	Description
TS_DISCHG_MODE_SEL	[5]	0x0	Temp sense mode selection during discharging **Value** / **Description** 0x0 (POR): Periodic sampling mode with 2s period 0x1: Host triggered sampling mode
TS_WARM_EN	[3]	0x0	TS WARM function enable. Write-locked when CE_N is 0, or when TS_EN is not 0.
TS_OFF_MODE	[2]	0x0	TS OFF mode control. Write-locked when CE_N is 0, or when TS_EN is not 0. **Value** / **Description**

			0x0 (POR): Battery TS feature is disabled when TS_OFF 0x1: Charger fault condition when TS_OFF
TS_EN_DISCHG	[1]	0x0	Battery temperature sense enable during discharging
TS_EN_CHG	[0]	0x1	Battery temperature sense enable during charging

Table 73: Register CHG_VDD_PWR_0

Address	Register Name	POR Value	VDD_PWR
0x0027	CHG_VDD_PWR_0	0x02	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	ILIM<3:0>			

Field Name	Bits	POR	Description
ILIM	[3:0]	0x2	Input current limit (mA) **Value** / **Description** 0x0: 2.5 0x1: 50 0x2 (POR): 100 0x3: 150 0x4: 200 0x5: 250 0x6: 300 0x7: 350 0x8: 400

			Value	Description
			0x9	450
			0xA	500
			0xB	550
			0xC	600
			0xD	Reserved
			0xE	Reserved
			0xF	Reserved

Table 74: Register CHG_VDD_PWR_1

Address	Register Name	POR Value	
0x0028	CHG_VDD_PWR_1	0x0C	VDD_PWR

7	6	5	4	3	2	1	0
Reserved	Reserved	VDD_PWR_OVP_DIS	VDD_PWR_DPM_DIS	ILIM_EN	VDD_PWR_DPM<2:0>		

Field Name	Bits	POR	Description	
VDD_PWR_OVP_DIS	[5]	0x0	VDD_PWR OVP disable	
VDD_PWR_DPM_DIS	[4]	0x0	VDD_PWR DPM disable	
ILIM_EN	[3]	0x1	Input current limit enable	
VDD_PWR_DPM	[2:0]	0x4	VDD_PWR DPM threshold voltage (V)	
			Value	**Description**
			0x0	4.2
			0x1	4.3
			0x2	4.4

			0x3	4.5
			0x4 (POR)	4.6
			0x5	4.7
			0x6	4.8
			0x7	4.9

Table 75: Register CHG_IDISCHG_0

Address	Register Name	POR Value	Battery discharge current limit
0x0029	CHG_IDISCHG_0	0x0D	

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	IDISCHG_OCP<2:0>			IDISCHG_OCP_HIZ_EN	IDISCHG_OCP_EN

Field Name	Bits	POR	Description	
IDISCHG_OCP	[4:2]	0x3	Battery discharge over-current protection setting (A)	
			Value	**Description**
			0x0	0.55
			0x1	0.75
			0x2	0.95
			0x3 (POR)	1.15
			0x4	1.35
			0x5	1.55
			0x6	1.75
			0x7	Reserved

IDISCHG_OCP_HIZ_EN	[1]	0x0	Battery discharge over-current protection enable, even during HiZ
IDISCHG_OCP_EN	[0]	0x1	Battery discharge over-current protection enable

10.2.4 Buck, Boost, and LDO Control

10.2.4.1 V_{OUT} User Registers

Table 76: Register VOUT_BUCK

Address	Register Name	POR Value	Buck enable & V_{out} control
0x0030	VOUT_BUCK	0x5C	

7	6	5	4	3	2	1	0
BUCK_EN	VOUT_RANGE_HI	Reserved	BUCK_VOUT<4:0>				

<table>
<tr><th>Field Name</th><th>Bits</th><th>POR</th><th>Description</th></tr>
<tr><td>BUCK_EN</td><td>[7]</td><td>0x0</td><td>BUCK enable</td></tr>
<tr><td>VOUT_RANGE_HI</td><td>[6]</td><td>0x1</td><td>Buck output range control.
This register can be written when buck is disabled or when BUCK_EN is being written to 0.<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0</td><td>0.60 V <= VBUCK <= 1.30 V</td></tr><tr><td>0x1 (POR)</td><td>1.30 V <= VBUCK <= 2.10 V</td></tr></table></td></tr>
<tr><td>BUCK_VOUT</td><td>[4:0]</td><td>0x1C</td><td>Buck output voltage setting (0.6 V to 2.1 V in 50 mV steps).
0.60 V to 1.30 V can be set when VOUT_RANGE_HI=0 and 1.3 V to 2.1 V can be set when VOUT_RANGE_HI=1.<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x00</td><td>0.60 V</td></tr><tr><td>0x01</td><td>0.65 V</td></tr></table></td></tr>
</table>

			0x02	0.70 V
			0x03	0.75 V
			0x04	0.80 V
			0x05	0.85 V
			0x06	0.90 V
			0x07	0.95 V
			0x08	1.00 V
			0x09	1.05 V
			0x0A	1.10 V
			0x0B	1.15 V
			0x0C	1.20 V
			0x0D	1.25 V
			0x0E	1.30 V
			0x0F	1.35 V
			0x10	1.40 V
			0x11	1.45 V
			0x12	1.50 V
			0x13	1.55 V
			0x14	1.60 V
			0x15	1.65 V
			0x16	1.70 V
			0x17	1.75 V
			0x18	1.80 V

			0x19	1.85 V
			0x1A	1.90 V
			0x1B	1.95 V
			0x1C (POR)	2.00 V
			0x1D	2.05 V
			0x1E	2.10 V
			0x1F	Reserved

Table 77: Register VOUT_BUCK_CFG

Address	Register Name	POR Value	
0x0031	VOUT_BUCK_CFG	0x00	Buck config

7	6	5	4	3	2	1	0
Reserved	Reserved	BUCK_PD_CFG2	Reserved 0	Reserved	Reserved	SEL_ILIM_DLT<1:0>	

Field Name	Bits	POR	Description	
BUCK_PD_CFG2	[5]	0x0	Output discharge enable at buck disable	
			Value	**Description**
			0x0 (POR)	Enable
			0x1	Disable
SEL_ILIM_DLT	[1:0]	0x0	Buck peak current limit setting	
			Value	**Description**
			0x0 (POR)	Default -50 mA
			0x1	Default current limit

			0x2 Default +50 mA 0x3 Default +100 mA

Table 78: Register VOUT_LS_LDO0

Address	Register Name	POR Value	LS_LDO_0 control
0x0032	VOUT_LS_LDO0	0x24	

7	6	5	4	3	2	1	0
EN_LS_LDO_0	Reserved	LS_LDO_0<5:0>					

Field Name	Bits	POR	Description
EN_LS_LDO_0	[7]	0x0	LS_LDO_0 enable. LDO becomes active 20ms after LDO0 gets enabled.
LS_LDO_0	[5:0]	0x24	LDO0 voltage setting, can't be written when LS_LDO0 is enabled. 0.8 V to 1.6 V in 25 mV steps and 1.6 V to 3.15 V in 50 mV steps. **Value** / **Description** 0x0 0.8 0x1 0.825 0x2 0.85 0x3 0.875 0x4 0.9 0x5 0.925 0x6 0.95 0x7 0.975 0x8 1

			0x9	1.025
			0x0A	1.05
			0x0B	1.075
			0x0C	1.1
			0x0D	1.125
			0x0E	1.15
			0x0F	1.175
			0x10	1.2
			0x11	1.225
			0x12	1.25
			0x13	1.275
			0x14	1.3
			0x15	1.325
			0x16	1.35
			0x17	1.375
			0x18	1.4
			0x19	1.425
			0x1A	1.45
			0x1B	1.475
			0x1C	1.5
			0x1D	1.525
			0x1E	1.55
			0x1F	1.575

			0x20	1.6
			0x21	1.65
			0x22	1.7
			0x23	1.75
			0x24 (POR)	1.8
			0x25	1.85
			0x26	1.9
			0x27	1.95
			0x28	2
			0x29	2.05
			0x2A	2.1
			0x2B	2.15
			0x2C	2.2
			0x2D	2.25
			0x2E	2.3
			0x2F	2.35
			0x30	2.4
			0x31	2.45
			0x32	2.5
			0x33	2.55
			0x34	2.6
			0x35	2.65
			0x36	2.7

			0x37	2.75
			0x38	2.8
			0x39	2.85
			0x3A	2.9
			0x3B	2.95
			0x3C	3
			0x3D	3.05
			0x3E	3.1
			0x3F	3.15

Table 79: Register VOUT_LS_LDO1

Address	Register Name	POR Value	LS_LDO_1 control
0x0033	VOUT_LS_LDO1	0x28	

7	6	5	4	3	2	1	0
EN_LS_LDO_1	Reserved	LS_LDO_1<5:0>					

Field Name	Bits	POR	Description	
EN_LS_LDO_1	[7]	0x0	LS_LDO_1 enable. LDO becomes active 20 ms after LS_LDO_1 gets enabled.	
LS_LDO_1	[5:0]	0x28	LDO1 voltage setting, can't be written when LS_LDO1 is enabled. 0.8 V to 2.4 V in 50 mV steps and 2.4 V to 3.3 V in 75 mV steps.	
			Value	**Description**
			0x0	0.8
			0x1	0.85

			0x2	0.9
			0x3	0.95
			0x4	1
			0x5	1.05
			0x6	1.1
			0x7	1.15
			0x8	1.2
			0x9	1.25
			0x0A	1.3
			0x0B	1.35
			0x0C	1.4
			0x0D	1.45
			0x0E	1.5
			0x0F	1.55
			0x10	1.6
			0x11	1.65
			0x12	1.7
			0x13	1.75
			0x14	1.8
			0x15	1.85
			0x16	1.9
			0x17	1.95
			0x18	2

			0x19	2.05
			0x1A	2.1
			0x1B	2.15
			0x1C	2.2
			0x1D	2.25
			0x1E	2.3
			0x1F	2.35
			0x20	2.4
			0x21	2.475
			0x22	2.55
			0x23	2.625
			0x24	2.7
			0x25	2.775
			0x26	2.85
			0x27	2.925
			0x28 (POR)	3
			0x29	3.075
			0x2A	3.15
			0x2B	3.225
			0x2C	3.3
			0x2D	Reserved
			0x3F	Reserved

Table 80: Register VOUT_LS_LDO2

Address	Register Name	POR Value	LS_LDO_2 control
0x0034	VOUT_LS_LDO2	0x14	

7	6	5	4	3	2	1	0
EN_LS_LDO_2	Reserved	LS_LDO_2<5:0>					

Field Name	Bits	POR	Description
EN_LS_LDO_2	[7]	0x0	LS_LDO_2 enable. LDO becomes active 20ms after LS_LDO_2 gets enabled.
LS_LDO_2	[5:0]	0x14	LDO2 voltage setting, can't be written when LS_LDO2 is enabled. 0.8 V to 2.4 V in 50 mV steps and 2.4 V to 3.3 V in 75 mV steps.

Value	Description
0x0	0.8
0x1	0.85
0x2	0.9
0x3	0.95
0x4	1
0x5	1.05
0x6	1.1
0x7	1.15
0x8	1.2
0x9	1.25
0x0A	1.3

			0x0B	1.35
			0x0C	1.4
			0x0D	1.45
			0x0E	1.5
			0x0F	1.55
			0x10	1.6
			0x11	1.65
			0x12	1.7
			0x13	1.75
			0x14 (POR)	1.8
			0x15	1.85
			0x16	1.9
			0x17	1.95
			0x18	2
			0x19	2.05
			0x1A	2.1
			0x1B	2.15
			0x1C	2.2
			0x1D	2.25
			0x1E	2.3
			0x1F	2.35
			0x20	2.4
			0x21	2.475

			0x22	2.55
			0x23	2.625
			0x24	2.7
			0x25	2.775
			0x26	2.85
			0x27	2.925
			0x28	3
			0x29	3.075
			0x2A	3.15
			0x2B	3.225
			0x2C	3.3
			0x2D	Reserved
			0x3F	Reserved

Table 81: Register VOUT_LS_LDO_CFG

Address	Register Name	POR Value	LS_LDO_CFG
0x0035	VOUT_LS_LDO_CFG	0x00	

7	6	5	4	3	2	1	0
Reserved	SEL_FULLON_2	SEL_FULLON_1	SEL_FULLON_0	Reserved	SEL_LDSW_2	SEL_LDSW_1	SEL_LDSW_0

Field Name	Bits	POR	Description	
SEL_FULLON_2	[6]	0x0	LS_LDO2 current limit enable, can't be written when LS_LDO2 is enabled.	
			Value	**Description**

<table>
<tr><td></td><td></td><td></td><td><table><tr><td>0x0 (POR)</td><td>Enable</td></tr><tr><td>0x1</td><td>Disable</td></tr></table></td></tr>
<tr><td>SEL_FULLON_1</td><td>[5]</td><td>0x0</td><td>LS_LDO1 current limit enable, can't be written when LS_LDO1 is enabled.<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0 (POR)</td><td>Enable</td></tr><tr><td>0x1</td><td>Disable</td></tr></table></td></tr>
<tr><td>SEL_FULLON_0</td><td>[4]</td><td>0x0</td><td>LS_LDO0 current limit enable, can't be written when LS_LDO0 is enabled.<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0 (POR)</td><td>Enable</td></tr><tr><td>0x1</td><td>Disable</td></tr></table></td></tr>
<tr><td>SEL_LDSW_2</td><td>[2]</td><td>0x0</td><td>LS_LDO2 function select, can't be written when LS_LDO2 is enabled.<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0 (POR)</td><td>LDO</td></tr><tr><td>0x1</td><td>LDSW</td></tr></table></td></tr>
<tr><td>SEL_LDSW_1</td><td>[1]</td><td>0x0</td><td>LS_LDO1 function select, can't be written when LS_LDO1 is enabled.<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0 (POR)</td><td>LDO</td></tr><tr><td>0x1</td><td>LDSW</td></tr></table></td></tr>
<tr><td>SEL_LDSW_0</td><td>[0]</td><td>0x0</td><td>LS_LDO0 function select, can't be written when LS_LDO0 is enabled.<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0 (POR)</td><td>LDO</td></tr><tr><td>0x1</td><td>LDSW</td></tr></table></td></tr>
</table>

Table 82: Register VOUT_BOOST

Address	Register Name	POR Value	BOOST control
0x0036	VOUT_BOOST	0x27	

7	6	5	4	3	2	1	0
BOOST_EN	BOOST_VOUT<6:0>						

<table>
<tr><th>Field Name</th><th>Bits</th><th>POR</th><th>Description</th></tr>
<tr><td>BOOST_EN</td><td>[7]</td><td>0x0</td><td>Boost enable</td></tr>
<tr><td>BOOST_VOUT</td><td>[6:0]</td><td>0x27</td><td>Boost voltage setting, can be written when boost is disabled or being disabled by the same write access.
4.5 V to 9 V in 125 mV steps and 9 V to 18 V in 250 mV steps.
Writing 0x1A or lower becomes writing 0x1B.
<table>
<tr><th>Value</th><th>Description</th></tr>
<tr><td>0x0</td><td>Reserved</td></tr>
<tr><td>0x1A</td><td>Reserved</td></tr>
<tr><td>0x1B</td><td>9</td></tr>
<tr><td>0x1C</td><td>9.25</td></tr>
<tr><td>0x1D</td><td>9.5</td></tr>
<tr><td>0x1E</td><td>9.75</td></tr>
<tr><td>0x1F</td><td>10</td></tr>
<tr><td>0x20</td><td>10.25</td></tr>
<tr><td>0x21</td><td>10.5</td></tr>
<tr><td>0x22</td><td>10.75</td></tr>
</table></td></tr>
</table>

			0x23	11
			0x24	11.25
			0x25	11.5
			0x26	11.75
			0x27 (POR)	12
			0x28	12.25
			0x29	12.5
			0x2A	12.75
			0x2B	13
			0x2C	13.25
			0x2D	13.5
			0x2E	13.75
			0x2F	14
			0x30	14.25
			0x31	14.5
			0x32	14.75
			0x33	15
			0x34	15.25
			0x35	15.5
			0x36	15.75
			0x37	16
			0x38	16.25
			0x39	16.5

			0x3A	16.75
			0x3B	17
			0x3C	17.25
			0x3D	17.5
			0x3E	17.75
			0x3F	18
			0x40	Reserved
			0x5A	Reserved
			0x5B	4.5
			0x5C	4.625
			0x5D	4.75
			0x5E	4.875
			0x5F	5
			0x60	5.125
			0x61	5.25
			0x62	5.375
			0x63	5.5
			0x64	5.625
			0x65	5.75
			0x66	5.875
			0x67	6
			0x68	6.125
			0x69	6.25

			0x6A	6.375
			0x6B	6.5
			0x6C	6.625
			0x6D	6.75
			0x6E	6.875
			0x6F	7
			0x70	7.125
			0x71	7.25
			0x72	7.375
			0x73	7.5
			0x74	7.625
			0x75	7.75
			0x76	7.875
			0x77	8
			0x78	8.125
			0x79	8.25
			0x7A	8.375
			0x7B	8.5
			0x7C	8.625
			0x7D	8.75
			0x7E	8.875
			0x7F	9

Table 83: Register VOUT_BOOST_CFG0

Address	Register Name	POR Value	BOOST config0
0x0037	VOUT_BOOST_CFG0	0x00	

7	6	5	4	3	2	1	0
TSS_SEL<1:0>		TPCHG_SEL<1:0>		Reserved	Reserved	Reserved	BST_CFG_FREQ

<table>
<tr><th>Field Name</th><th>Bits</th><th>POR</th><th colspan="2">Description</th></tr>
<tr><td rowspan="6">TSS_SEL</td><td rowspan="6">[7:6]</td><td rowspan="6">0x0</td><td colspan="2">BOOST Tss select, can't be written when boost is enabled.</td></tr>
<tr><td>Value</td><td>Description</td></tr>
<tr><td>0x0 (POR)</td><td>3 ms</td></tr>
<tr><td>0x1</td><td>6 ms</td></tr>
<tr><td>0x2</td><td>9 ms</td></tr>
<tr><td>0x3</td><td>12 ms</td></tr>
<tr><td rowspan="6">TPCHG_SEL</td><td rowspan="6">[5:4]</td><td rowspan="6">0x0</td><td colspan="2">BOOST Tpchg select, can't be written when boost is enabled.</td></tr>
<tr><td>Value</td><td>Description</td></tr>
<tr><td>0x0 (POR)</td><td>2 ms</td></tr>
<tr><td>0x1</td><td>4 ms</td></tr>
<tr><td>0x2</td><td>8 ms</td></tr>
<tr><td>0x3</td><td>16 ms</td></tr>
<tr><td rowspan="3">BST_CFG_FREQ</td><td rowspan="3">[0]</td><td rowspan="3">0x0</td><td colspan="2">Switching frequency select, can't be written when boost is enabled.</td></tr>
<tr><td>Value</td><td>Description</td></tr>
<tr><td>0x0 (POR)</td><td>1 MHz</td></tr>
</table>

			0x1	2 MHz

Table 84: Register VOUT_BOOST_CFG1

Address	Register Name	POR Value	BOOST config1
0x0038	VOUT_BOOST_CFG1	0xA6	

7	6	5	4	3	2	1	0
BST_CFG_OCS<1:0>		BST_CFG_OC<1:0>		Reserved 0	Reserved 1	Reserved 1	Reserved 0

Field Name	Bits	POR	Description	
BST_CFG_OCS	[7:6]	0x2	Over current protection during soft start, can't be written when boost is enabled.	
			Value	**Description**
			0x0	510 mA
			0x1	650 mA
			0x2 (POR)	780 mA
			0x3	920 mA
BST_CFG_OC	[5:4]	0x2	Over current protection at normal operation, can't be written when boost is enabled.	
			Value	**Description**
			0x0	0.9 A
			0x1	1.3 A
			0x2 (POR)	1.7 A
			0x3	2.1 A

Table 85: Register VOUT_BOOST_CFG2

Address	Register Name	POR Value	BOOST config2
0x0039	VOUT_BOOST_CFG2	0x70	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 1	Reserved 1	BST_CFG_ANTI	BST_CFG_PCHGLMT<3:0>			

Field Name	Bits	POR	Description
BST_CFG_ANTI	[4]	0x1	Anti ringing enable, can't be written when boost is enabled.
BST_CFG_PCHGLMT	[3:0]	0x0	Pre-charge current limit, can't be written when boost is enabled.

Value	Description
0x0 (POR)	x1
0x1	x2
0x2	x3
0x3	x4
0x4	x5
0x5	x6
0x6	x7
0x7	x8
0x8	x9
0x9	x10
0xA	x11
0xB	x12

			0xC	x13
			0xD	x14
			0xE	x15
			0xF	x16

10.2.4.2 V_{OUT} Opt Registers

Table 86: Register VOUT_BUCK_OPT0

Address	Register Name	POR Value	BUCK_OPT0
0x0050	VOUT_BUCK_OPT0	0x1B	

7	6	5	4	3	2	1	0
Reserved 0	Reserved 0	Reserved 0	Reserved 1	Reserved 1	Reserved 0	DVC_STEP<1:0>	

Field Name	Bits	POR	Description	
DVC_STEP	[1:0]	0x3	DVC step control; 00: No DVC, 01: 50 mV / 0.5 ms, 10: 50 mV / 1 ms, 11: 50 mV / 2 ms	
			Value	**Description**
			0x0	No DVC
			0x1	50 mV / 1 ms
			0x2	50 mV / 2 ms
			0x3 (POR)	50 mV / 4 ms

11 Package Information

11.1 Package Outlines

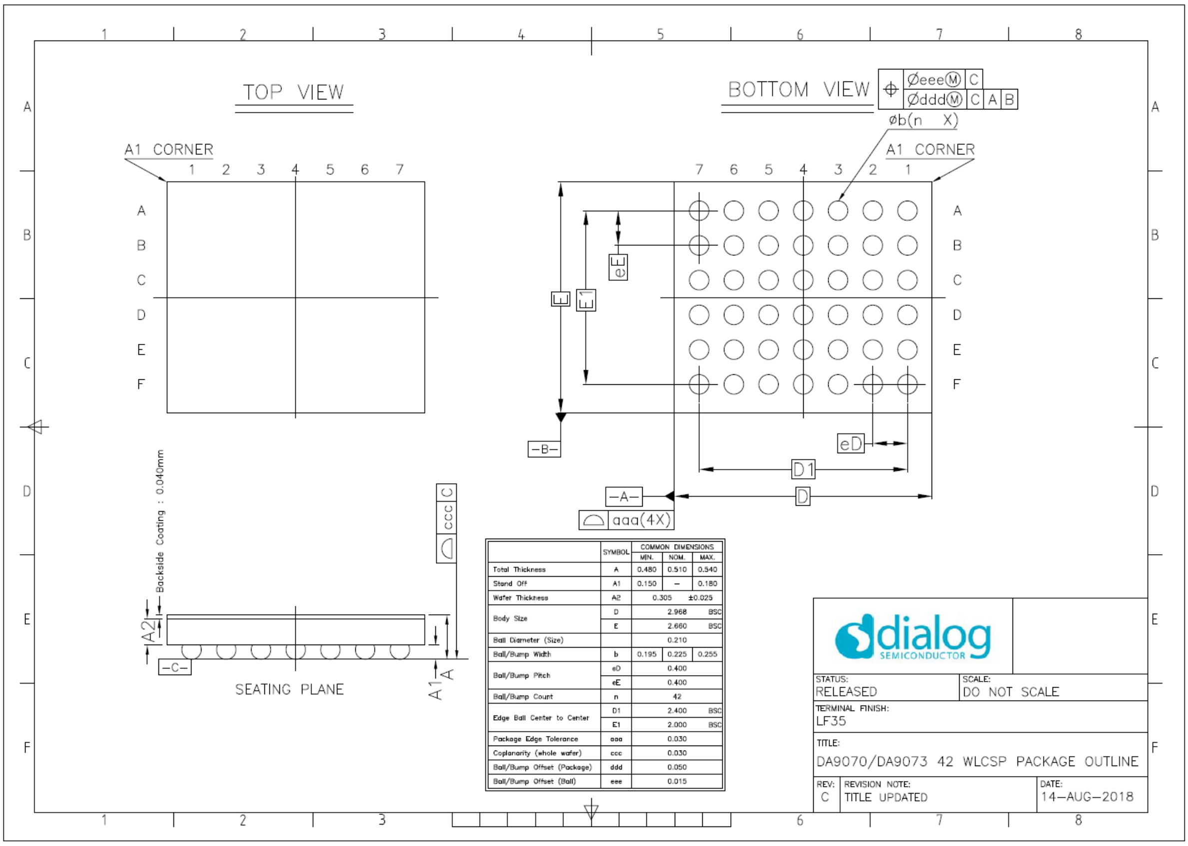


Figure 44: WLCSP-42 Package Outline Drawing

11.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30 °C and a maximum relative humidity of 60 % RH before the solder reflow process. The MSL classification is defined in Table 87.

The device package is qualified for MSL 1.

Table 87: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 1	Unlimited	30 °C / 85 % RH

11.3 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

12 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the OTP variant (xx), package type, and packing method. For details and availability, please consult Renesas Electronics' customer support portal or your local sales representative.

Table 88: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9070-xxV32	WLCSP	2.97 x 2.66	T&R	2000
DA9070-xxV36	WLCSP	2.97 x 2.66	Waffle	90

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterisation data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notifications.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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