High Current, Highly Configurable System PMIC with Four Bucks and One LDO

General Description

DA9080 is a five-channel advanced, configurable, system power management IC (PMIC) with four buck regulators and one LDO. This highly integrated, flexible PMIC is capable of up to 10 A of output current. The output voltage of the regulators can be programmed and sequenced based on the application needs. The DA9080 also integrates an 8-bit ADC, along with several other features, that simplifies overall system design. Dynamic voltage control (DVC), robust protection features, and a dedicated I²C interface that supports multiple modes extend the applicability of this device to a wide range of end applications.

The high-efficiency, fast transient response, and small footprint of the DA9080 lends itself to become the preferred power solution for a host of complex, high-performance applications. The DA9080 is offered in a QFN package.

Key Features

- Power supply voltage (V_{IN}) 4.0 V to 5.5 V
- Four buck converters
- Selectable output voltage range for bucks:
  - CH1 Buck: 2.1 V to 3.3 V, 20 mV step
  - CH2 Buck: 1.5 V to 2.6 V, 20 mV step
  - CH3 Buck: 0.9 V to 1.3 V, 5 mV step (supports 1.35 V and 1.8 V)
  - CH4 Buck: 0.8 V to 1.4 V, 5 mV step
- Maximum output current:
  - CH1, CH2, and CH3 Buck: 1.5 A
  - CH4 Buck: 5.0 A
- Interleaving of switching phases of bucks
- LDO:
  - V_{OUT}: 3.3 V, I_{OUT}: 0.2 A (max)
- General purpose ADC:
  - 8-bit SAR ADC
  - Two external inputs
  - Die temperature sense
- Protection functions:
  - Over-current protection
  - Over/under-voltage protection
  - Thermal shutdown protection
- I²C control interface:
  - Standard mode (100 kbit/s)
  - Fast mode (400 kbit/s)
  - Fast mode+ (1 Mbit/s)
- Package: 32 lead QFN, 5.0 mm x 5.0 mm

Applications

- Client and Enterprise SSD modules
- Embedded Computing
- Integrated Microcontroller Internet of Things
- DSPs or FPGAs with Peripherals

System Diagram

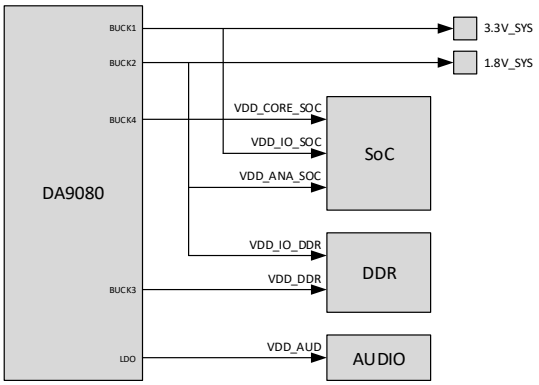

Figure 1: System Diagram

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1 Terms and Definitions

ADC	Analog to digital converter
CH<x>	Channel <x>, where x = 1 to 4
DVC	Dynamic voltage control
ESD	Electrostatic discharge
GPADC	General purpose ADC
LDO	Low dropout regulator
MSB	Most significant bit
OCP	Over-current protection
OTP	One-time programmable
OVP	Over-voltage protection
OVLO	Over-voltage lockout
PFM	Pulse frequency modulation
PMIC	Power management integrated circuit
POR	Power-on reset
PWM	Pulse width modulation
SAR	Successive approximation register
TSD	Thermal shutdown
UQFN	Ultra-thin quad flat-pack no-lead (package)
UVP	Under-voltage protection
UVLO	Under-voltage lockout

2 References

[1] NXP Semiconductors N.V., UM10204 I^2C-Bus Specification and User Manual, Revision 6

3 Block Diagram

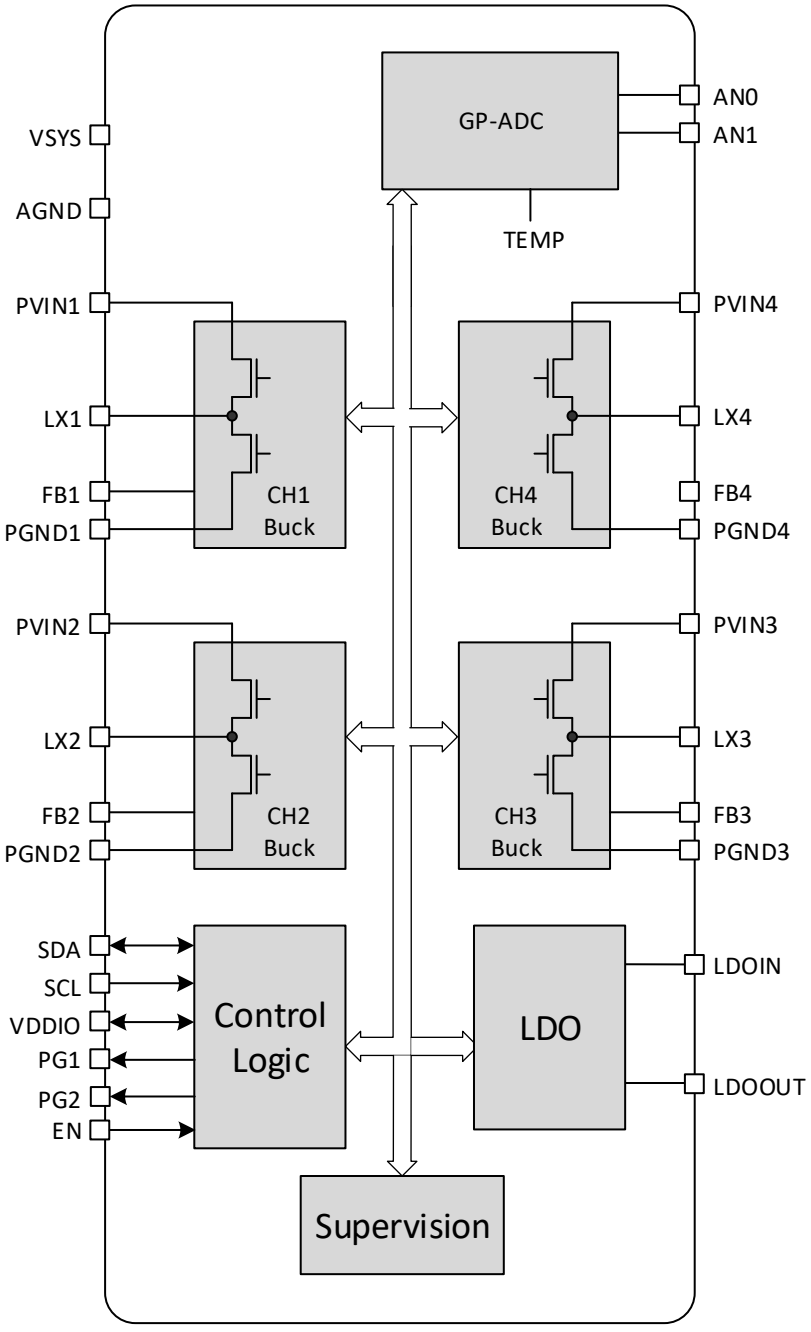


Figure 2: Block Diagram

4 Pinout

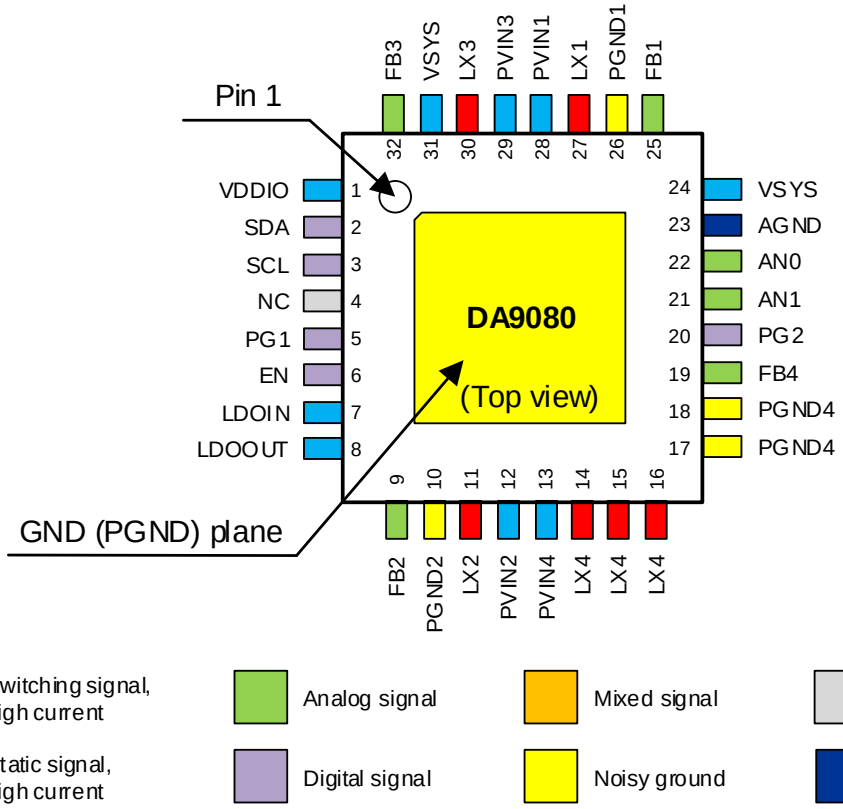


Figure 3: UQFN Pinout Diagram (Top View)

Table 1: Pin Description

Pin #	Pin Name	Type (Table 2)	Description
1	VDDIO	PWR	Supply for I²C interface
2	SDA	DIOD	I²C interface data, connect SDA to the logic rail via a pull-up resistor
3	SCL	DI	I²C interface data, connect SCL to the logic rail via a pull-up resistor
4	NC	DI	Not used, connect to GND
5	PG1	DO	Power good output 1, open drain
6	EN	DI	Chip enable (when pulled low, shuts down entire chip after power down sequencing complete)
7	LDOIN	PWR	LDO input, bypass to ground with a ceramic capacitor
8	LDOOUT	PWR	Output of LDO
9	FB2	AI	CH2 Buck output voltage feedback connection
10	PGND2	GND	CH2 Buck converter power ground
11	LX2	PWR	CH2 Buck converter switching node
12	PVIN2	PWR	CH2 Buck converter input
13	PVIN4	PWR	CH4 Buck converter input
14, 15, 16	LX4	PWR	CH4 Buck converter switching node
17, 18	PGND4	GND	CH4 Buck converter power ground

Pin #	Pin Name	Type (Table 2)	Description
19	FB4	AI	CH4 Buck output voltage feedback connection
20	PG2	DO	Power good output 1, open drain
21	AN1	AI	Input to ADC
22	AN0	AI	Input to ADC
23	AGND	GND	Quiet ground connection, connect to a quiet ground area
24, 31	VSYS	PWR	Filtered from VIN through an RC to provide a clean 5 V supply
25	FB1	AI	CH1 Buck output voltage feedback connection
26	PGND1	GND	CH1 Buck converter power ground
27	LX1	PWR	CH1 Buck converter switching node
28	PVIN1	PWR	CH1 Buck converter input – internally connected to PVIN3
29	PVIN3	PWR	CH3 Buck converter input – internally connected to PVIN1
30	LX3	PWR	CH3 Buck converter switching node
32	FB3	AI	CH3 Buck output voltage feedback connection
PAD	GND	GND	Package central pad, connect to PGND

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AIO	Analog input/output
DIO	Digital input/output	PWR	Power
DIOD	Digital input/output open drain	GND	Ground

5 Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature		-60	150	°C
V_{SYS}	System supply voltage	Referenced to AGND	-0.3	6	V
V_{PIN}	All other pins	Referenced to AGND	-0.3	6	V

5.2 Electrostatic Discharge Ratings

Table 4: Electrostatic Discharge Ratings

Parameter	Description	Conditions	Value	Unit
V_{ESD_HBM}	Maximum ESD protection	Human body model (HBM) All exposed pins	2	kV
V_{ESD_CDM}	Maximum ESD protection	Charged device model (CDM)	0.5	kV

5.3 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature		-40		85	°C
T_J	Operating junction temperature		-40		125	°C
V_{SYS}	Input supply voltage		4		5.5	V
V_{PIN}	Voltage on all other pins		-0.3		VIN+0.3	V

5.4 Thermal Characteristics

Table 6: UQFN Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{Θ_JA}	Package thermal resistance (Note 1)				24.3	°C/W
P_D	Power dissipation	Derating factor above T_A = 65 °C, 41.1 mW/°C ($1/R_{\Theta\_JA}$)			2.47	W

Note 1 Obtained from package thermal simulation, JEDEC JESD51-2 still air test environment using 4-layer board at T_A = 65 °C with 36 vias. Influenced by PCB technology and layout.

5.5 Electrical Characteristics

All Min/Max specification limits are guaranteed by design, production testing, and/or statistical characterization and are valid over the full operating temperature range and power supply range unless otherwise noted.

Typical values are based on characterization results at default measurement conditions and are informative only. Default measurement conditions (unless otherwise specified): V_{IN} = 5.0 V, T_A = 25 °C.

5.5.1 CH1 Buck Converter Characteristics

Table 7: CH1 Buck Converter Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage of power stage		4	5	5.5	V
C_{OUT}	Output capacitance, including voltage and temperature coefficient	2 x 47 µF	21		68	µF
ESR_{COUT}	Output capacitor series resistance	f > 100 kHz		3		mΩ
L	Inductor value, including current and temperature dependence		0.23	0.47	0.61	µH
DCR_L	Inductor DC resistance			20	50	mΩ
Electrical Performance						
I_{OUT}	Maximum output current		1500			mA
I_{Q_AUTO}	Quiescent current in Auto mode (no switching)			51		µA
f_{SW}	Switching frequency		1.9	2	2.1	MHz
V_{OUT}	Range of output voltage, programmable in 20 mV steps	V_{IN} = 4.0 V to 5.5 V	2.1	3.3	3.3	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OUT_STP}	Output voltage programable step			20		mV
$V_{OUT\_ACC\_DFLT}$	Accuracy of default output voltage	In PWM mode V_{OUT} = 3.3 V I_{OUT} = 1 A	3.267	3.3	3.33	V
$V_{OUT\_ACC\_LINE}$	Static line regulation			0.5		%/V
$V_{OUT\_ACC\_LD}$	Static load regulation	In PWM mode I_{OUT} = 1.5 A		0.1		%/A
$V_{OUT\_ACC\_ACDC}$	Output voltage accuracy, including PWM/PFM ripple and load transient	V_{OUT} = 3.3 V C_{OUT} = 2 x 47 µF Load transient 1: from 0.5*I_{MAX} to I_{MAX} in 0.2 A/µs Load transient 2: from 50 mA to 0.5*I_{MAX} in 0.2 A/µs I_{MAX} = 1.5 A V_{IN} = 5.0 V T_A = 25 °C	-2		3	%
I_{POSLIM}	Positive over-current limit threshold		3	4		A
$V_{THR\_OVP\_RISE}$	Over-voltage protection threshold		200	300	400	mV
$V_{THR\_UVP\_FALL}$	Under-voltage protection threshold		-400	-300	-200	mV
R_{DCHG}	Discharge resistance for LX node			67		Ω
t_{ON_MIN}	Buck LX minimum on time			20		ns
SR_{SS}	Soft start slew rate			2.5		mV/µs
SR_{SDCHG}	Soft discharge slew rate			2.5		mV/µs

5.5.2 CH2 Buck Converter Characteristics

Table 8: CH2 Buck Converter Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage of power stage		4	5	5.5	V
C_{OUT}	Output capacitance, including voltage and temperature coefficient	2 x 47 µF	30		85	µF
ESR_{COUT}	Output capacitor series resistance	f > 100 kHz		3		mΩ
L	Inductor value, including current and temperature dependence		0.23	0.47	0.61	µH
DCR_L	Inductor DC resistance			20	50	mΩ
Electrical Performance						
I_{OUT}	Maximum output current		1500			mA
I_{Q_AUTO}	Quiescent current in Auto mode (no switching)			51		µA
f_{SW}	Switching frequency		1.9	2	2.1	MHz
V_{OUT}	Output voltage range, programmable in 20 mV steps	V_{IN} = 4.0 V to 5.5 V	1.5	1.8	2.6	V
V_{OUT_STP}	Output voltage programable step			20		mV
$V_{OUT\_ACC\_DFLT}$	Accuracy of default output voltage	In PWM mode V_{OUT} = 1.8 V I_{OUT} = 1 A	1.782	1.8	1.818	V
$V_{OUT\_ACC\_DC}$	Output voltage accuracy in PWM mode, including static line and load regulation		-1		1	%
$V_{OUT\_ACC\_LINE}$	Static line regulation			0.5		%/V
$V_{OUT\_ACC\_LD}$	Static load regulation	In PWM mode I_{OUT} = 1.5 A		0.1		%/A

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OUT\_ACC\_ACDC}$	Output voltage accuracy, including PWM/PFM ripple and load transient	V_{OUT} = 1.8 V C_{OUT} = 2 x 47 µF Load transient 1: from 0.5*I_{MAX} to I_{MAX} in 0.2 A/µs Load transient 2: from 50 mA to 0.5*I_{MAX} in 0.2 A/µs I_{MAX} = 1.5 A V_{IN} = 5.0 V T_A = 25 °C	-2		3	%
I_{POSLIM}	Positive over-current limit threshold		3	4		A
$V_{THR\_OVP\_RISE}$	Over-voltage protection threshold		200	300	400	mV
$V_{THR\_UVP\_FALL}$	Under-voltage protection threshold		-400	-300	-200	mV
R_{DCHG}	Discharge resistance for LX node			67		Ω
t_{ON_MIN}	Buck LX minimum on time			20		ns
SR_{SS}	Soft start slew rate			2.5		mV/µs
SR_{SDCHG}	Soft discharge slew rate			2.5		mV/µs

5.5.3 CH3 Buck Converter Characteristics

Table 9: CH3 Buck Converter Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage of power stage		4	5	5.5	V
C_{OUT}	Output capacitance, including voltage and temperature coefficient	3 x 47 µF	70		153	µF
ESR_{COUT}	Output capacitor series resistance	f > 100 kHz		3		mΩ
L	Inductor value, including current and temperature dependence		0.23	0.47	0.61	µH
DCR_L	Inductor DC resistance			20	50	mΩ
Electrical Performance						
I_{OUT}	Maximum output current		1500			mA
I_{Q_AUTO}	Quiescent current in Auto mode (no switching)			56		µA
f_{SW}	Switching frequency		1.9	2	2.1	MHz
V_{OUT}	Output voltage range	V_{IN} = 4.0 V to 5.5 V	0.9	1.2	1.3	V
V_{OUT_STP}	Output voltage programable step			5		mV
$V_{OUT\_ACC\_DFLT}$	Accuracy of default output voltage	In PWM mode V_{OUT} = 1.2 V I_{OUT} = 1 A	1.188	1.2	1.1212	V
$V_{OUT\_ACC\_LINE}$	Static line regulation			0.5		%/V
$V_{OUT\_ACC\_LD}$	Static load regulation	In PWM mode I_{OUT} = 1.5 A		0.1		%/A
$V_{OUT\_ACC\_ACDC}$	Output voltage accuracy, including PWM/PFM ripple and load transient	V_{OUT} = 1.2 V C_{OUT} = 3 x 47 µF Load transient 1: from 0.5*I_{MAX} to I_{MAX} in 0.2 A/µs Load transient 2: from 50 mA to 0.5*I_{MAX} in 0.2 A/µs I_{MAX} = 1.5 A V_{IN} = 5.0 V T_A = 25 °C	-2		4	%
I_{POSLIM}	Positive over-current limit threshold		3	4		A

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{THR\_OVP\_RISE}$	Over-voltage protection threshold		200	300	400	mV
$V_{THR\_UVP\_FALL}$	Under-voltage protection threshold		-400	-300	-200	mV
SR_{DVC}	Output voltage slew rate			10		mV/µs
R_{DCHG}	Discharge resistance for LX node			67		Ω
t_{ON_MIN}	Buck LX minimum on time			20		ns
SR_{SS}	Soft start slew rate			1.25		mV/µs
SR_{SDCHG}	Soft discharge slew rate			1.25		mV/µs

NOTE

V_{OUT} can be extended to 1.35 V and 1.8 V.

To set V_{OUT} = 1.35 V, write the following sequence:

WRITE DA9080_I2C 0x0009 0x50 //V_{OUT} = 1.3 V

WRITE DA9080_I2C 0x005D 0x00 //Enable write access to Register 0x0017

WRITE DA9080_I2C 0x005E 0xB0

WRITE DA9080_I2C 0x005E 0xA9

WRITE DA9080_I2C 0x005E 0x8A

WRITE DA9080_I2C 0x005E 0xA7

WRITE DA9080_I2C 0x005E 0xA8

WRITE DA9080_I2C 0x005E 0xB1

WRITE DA9080_I2C 0x0017 0x5F //V_{OUT} = 1.35 V

WRITE DA9080_I2C 0x005D 0x00 //Disable write access to Register 0x0017

WRITE DA9080_I2C 0x005E 0x00

To set V_{OUT} = 1.8 V, write the following sequence:

WRITE DA9080_I2C 0x0009 0x50 //V_{OUT} = 1.3 V

WRITE DA9080_I2C 0x005D 0x00 //Enable write access to Register 0x0017

WRITE DA9080_I2C 0x005E 0xB0

WRITE DA9080_I2C 0x005E 0xA9

WRITE DA9080_I2C 0x005E 0x8A

WRITE DA9080_I2C 0x005E 0xA7

WRITE DA9080_I2C 0x005E 0xA8

WRITE DA9080_I2C 0x005E 0xB1

WRITE DA9080_I2C 0x0017 0x8C //V_{OUT} = 1.8 V

WRITE DA9080_I2C 0x005D 0x00 //Disable write access to Register 0x0017

WRITE DA9080_I2C 0x005E 0x00

5.5.4 CH4 Buck Converter Characteristics

Table 10: CH4 Buck Converter Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage of power stage		4	5	5.5	V
C_{OUT}	Output capacitance, including voltage and temperature coefficient	4 x 47 µF	94		203	µF
ESR_{COUT}	Output capacitor series resistance	f > 100 kHz		3		mΩ
L	Inductor value, including current and temperature dependence		0.23	0.47	0.61	µH
DCR_L	Inductor DC resistance			20	50	mΩ
Electrical Performance						
I_{OUT}	Maximum output current		5000			mA
I_{Q_AUTO}	Quiescent current in Auto mode (no switching)			56		µA
f_{SW}	Switching frequency		1.9	2	2.1	MHz
V_{OUT}	Output voltage range	V_{IN} = 4.0 V to 5.5 V	0.8	1	1.4	V
V_{OUT_STP}	Output voltage programable step			5		mV
$V_{OUT\_ACC\_DFLT}$	Accuracy of default output voltage	In PWM mode V_{OUT} = 1.0 V I_{OUT} = 1 A	0.99	1	1.01	V
$V_{OUT\_ACC\_LINE}$	Static line regulation			0.5		%/V
$V_{OUT\_ACC\_LD}$	Static load regulation	In PWM mode I_{OUT} = 5 A		0.1		%/A
$V_{OUT\_ACC\_ACDC}$	Output voltage accuracy, including PWM/PFM ripple and load transient	V_{OUT} = 1.0 V C_{OUT} = 4 x 47 µF Load transient 1: from 0.5*I_{MAX} to I_{MAX} in 0.2 A/µs Load transient 2: from 50 mA to 0.5*I_{MAX} in 0.2 A/µs I_{MAX} = 5 A V_{IN} = 5.0 V T_A = 25 °C	-4		4	%

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OUT\_ACC\_ACDC\_FULL}$	Output voltage accuracy, including PWM/PFM ripple and load transient in full load	V_{OUT} = 1.0 V C_{OUT} = 4 x 47 µF Load transient: from 50 mA to I_{MAX} in 0.2 A/µs I_{MAX} = 5 A V_{IN} = 5.0 V T_A = 25 °C	-5		5	%
I_{POSLIM}	Positive over-current limit threshold		7	8.5		A
$V_{THR\_OVP\_RISE}$	Over-voltage protection threshold		200	300	400	mV
$V_{THR\_UVP\_FALL}$	Under-voltage protection threshold		-400	-300	-200	mV
SR_{DVC}	Output voltage slew rate			10		mV/µs
R_{DCHG}	Discharge resistance for LX node			67		Ω
t_{ON_MIN}	Buck LX minimum on time			20		ns
SR_{SS}	Soft start slew rate			1.25		mV/µs
SR_{SDCHG}	Soft discharge slew rate			1.25		mV/µs

5.5.4.1 CH4 Buck Converter Efficiency Characteristics

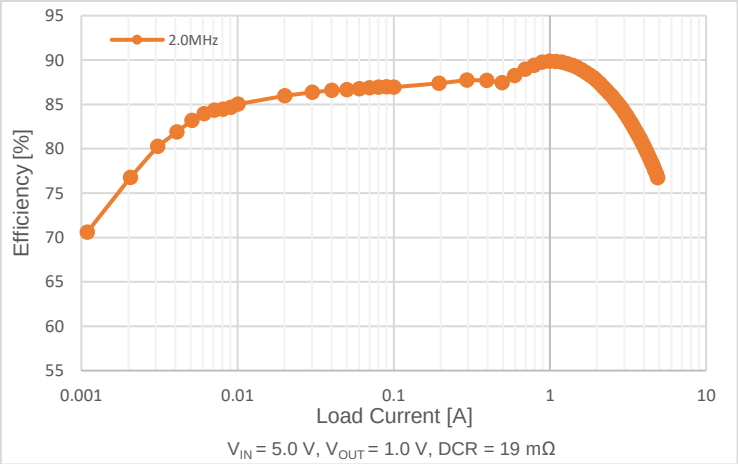


Figure 4: Measured Efficiency with Inductor 2520

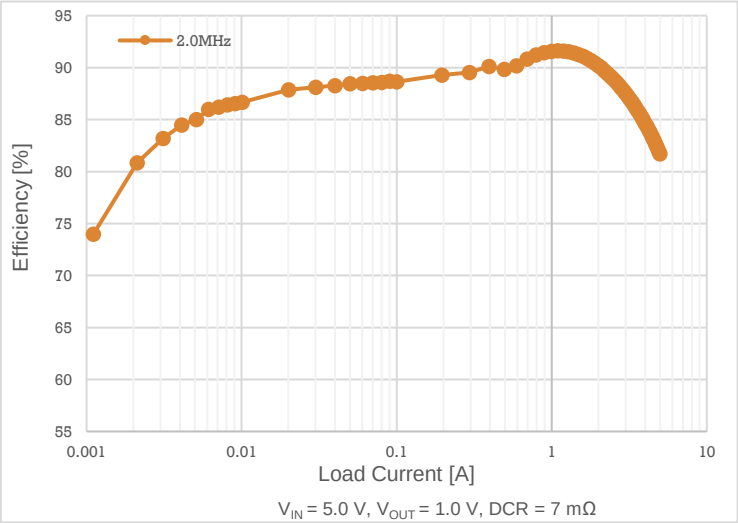


Figure 5: Measured Efficiency with Low DCR Inductor 4141

5.5.5 LDO Characteristics

Table 11: LDO Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage of power stage		4	5	5.5	V
C_{OUT}	Output capacitance, including voltage and temperature coefficient		2.3	4.7	6.1	µF
Electrical Performance						
I_{OUT}	Maximum output current		200			mA
I_Q	Quiescent current			3.7		µA
V_{OUT}	Output voltage			3.3		V
$V_{OUT\_ACC\_DFLT}$	Accuracy of default output voltage	V_{IN} = 5 V I_{OUT} = 10 mA T_A = 25 °C	3.267	3.3	3.33	V
$V_{OUT\_ACC\_LINE}$	Static line regulation	I_{OUT} = 10 mA		0.1		%/V
$V_{OUT\_ACC\_LD}$	Static load regulation	I_{OUT} = 0 mA to 0.2 A		0.83		%/A
$V_{OUT\_ACC\_ACDC}$	Output voltage accuracy including load transient	C_{OUT} = 4.7 µF Transient1: Load = 5 mA to 50 mA @ 0.2 A/µs Transient2: Load = 50 mA to 0.1 A @ 0.2 A/µs	-30		30	mV
t_{SS}	Soft start time (not DVC controlled)	No load condition C_{OUT} = 4.7 µF		0.56	0.8	ms
t_{SS_TOUT}	Soft start timeout time			1.3		ms
t_{LDO_OFF}	Time slot allocated for LDO off sequence			1.3		ms
I_{INRUSH}	Inrush current	V_{IN} = 5 V T_A = 25 °C C_{OUT} = 4.7 µF			300	mA
I_{LIM}	Current limit threshold	C_{OUT} = 4.7 µF	200			mA
$V_{THR\_UVP\_FALL}$	Under-voltage protection threshold			2.92		V
$V_{THR\_PG\_RISE}$	Power-good threshold			3		V
V_{HYS_PG}	Power-good hysteresis			80		mV
$V_{DROPOUT}$	Voltage drop from LDOIN to LDOOUT	I_{OUT} = 200 mA T_A = 25 °C C_{OUT} = 4.7 µF		200	400	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{DCHG}	Discharge resistance			47		Ω

5.5.6 ADC Characteristics

Table 12: ADC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{IN}	AN0/1 Input voltage range		0		5.1	V
R_{IN}	AN0/1 Input Resistance			1.235		MΩ
M	ADC resolution			8		bit
V_{ERR_RT}	Total conversion error	AN0/1 = 0.05 V to 5.1 V T_A = 25 °C	-20		20	mV
V_{ERR}	Total conversion error	AN0/1 = 0.05 V to 5.1 V	-40		40	mV
V_{OFS}	0 V input offset error	AN0/1 = 0 V	-40		50	mV
DNL	Differential non-linearity	AN0/1 = 0.05 V to 5.1 V	-1		1	LSB
INL	Integral non-linearity	AN0/1 = 0.05 V to 5.1 V	-2		2	LSB
V_{RES}	Voltage resolution	With respect to AN0/1		20		mV/LSB
T_{RES_SENSE}	Temperature sensor resolution	Per step		-1.97		°C/step
t_{ACQ_TOT}	Total acquisition Time			100		µs
I_Q	Quiescent current	ADC enabled		160		µA

5.5.7 Supervision Characteristics

Table 13: Supervision Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t_{FALL_DEB}	VSYS UVLO/VINGOOD Falling Debounce time			10		µs
t_{RISE_DEB}	VSYS UVLO/VINGOOD Rising Debounce time			1		ms
$V_{THR\_UVLO\_FALL}$	V_{IN} UVLO threshold for V_{IN} falling			3.6		V
$V_{THR\_UVLO\_HYS}$	V_{IN} UVLO hysteresis			0.2		V
V_{THR_RISE}	Input voltage good threshold	Voltage rising		4.6		V

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{THR\_RISE\_ACC}$	Input voltage good threshold accuracy		-2		2	%
V_{THR_HYS}	Input voltage good hysteresis			0.2		V
T_{THR_SHDN}	Thermal shutdown threshold		130	140	150	°C
$T_{THR\_SHDN\_HYS}$	Thermal shutdown hysteresis			15		°C
t_{FLT_DEB}	Fault detect debounce time	OVP and UVP		10		µs
t_{HICCUP}	Hiccup restart delay			64		ms
t_{PG}	Individual supply PG delay			2		ms
t_{PG1_2}	PG1 and PG2 pins PG delay			10		ms

5.5.8 Quiescent Current Characteristics

Table 14: Quiescent Current Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
I_{VSYS_SHDN}	Total current of VSYS pin	SHUTDOWN mode V_{SYS} = 5 V V_{DDIO} = 0 V T_A = -40 °C to 85 °C EN = L or FORCE_DISABLE = H CH<x> = All OFF		10	30	µA
I_{PVINx_SHDN}	Total current from PVIN1, PVIN2, PVIN3, and PVIN4 pins	SHUTDOWN mode V_{SYS} = 5 V V_{DDIO} = 0 V T_A = -40 °C to 85 °C EN = L or FORCE_DISABLE = H CH<x> = All OFF		0	10	µA
I_{LDOIN_SHDN}	Total current of LDOIN pin	SHUTDOWN mode V_{SYS} = 5 V V_{DDIO} = 0 V T_A = -40 °C to 85 °C EN = L or FORCE_DISABLE = H CH<x> = All OFF		0	1	µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{VSYS_OP}	Total current of VSYS pin	OPERATING mode EN = H and FORCE_DISABLE = L CH<x> = All ON Buck: ON with no switching and no load LDO: ON with no load ADC: ON IO: Non I^2C communication		500	600	µA
I_{PVINx_OP}	Total current from PVIN1, PVIN2, PVIN3, and PVIN4 pins	OPERATING mode EN = H and FORCE_DISABLE = L CH<x> = All ON Buck: ON with no switching and no load		0	10	µA
I_{VDDIO}	Total current from VDDIO pin	No I^2C communication V_{SYS} = 5 V V_{DDIO} = 3.3 V SCL = SDA = H		0.16	1	µA
I_{LDOIN_OP}	Total current of LDOIN pin	OPERATING mode EN = H and FORCE_DISABLE = L CH<x> = All ON LDO: ON with no load		2.7	10	µA

5.5.9 I^2C Characteristics

Table 15: I2C Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
Standard/Fast/Fast+ Mode						
t_{BUS}	Bus free time between a STOP and START condition		0.5			µs
C_{BUS}	Bus line capacitive load				150	pF
f_{SCL}	SCL clock frequency				1000	kHz
t_{LO_SCL}	SCL low time		0.5			µs
t_{HI_SCL}	SCL high time		0.26			µs
t_{RISE}	SCL and SDA rise time. Requirement for input.				1000	ns
t_{FALL}	SCL and SDA fall time. Requirement for input.				300	ns

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{SETUP_START}	Start condition setup time		0.26			µs
t_{HOLD_START}	Start condition hold time		0.26			µs
t_{SETUP_STOP}	Stop condition setup time		0.26			µs
t_{DATA}	Data valid time				0.45	µs
t_{DATA_ACK}	Data valid acknowledge time				0.45	µs
t_{SETUP_DATA}	Data setup time		50			ns
t_{HOLD_DATA}	Data hold time		0			ns
t_{SPIKE}	Spike suppression pulse width		0		50	ns

5.5.10 Digital I/O Characteristics

Table 16: Digital I/O Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{IH\_SCL\_SDA}$	Input high voltage, SCL, SDA		1.2			V
$V_{IL\_SCL\_SDA}$	Input low voltage, SCL, SDA				0.4	V
V_{OL_PG1}	PG1 output low voltage, POR	I_{OUT} = 3 mA			0.4	V
V_{OL_PG2}	PG2 output low voltage, POR	I_{OUT} = 3 mA			0.4	V
V_{OL_SDA}	Output low voltage, SDA	I_{OUT} = 3 mA			0.4	V
V_{IH_EN}	Input high voltage, CH1SEL		1.2			V
V_{IL_EN}	Input low voltage, CH1SEL				0.4	V
t_{ENH_DEB}	EN Pin rising debounce time			100		ms
t_{ENL_DEB}	EN Pin falling debounce time			10		µs

6 Functional States

DA9080 functional states are shown in Figure 6.

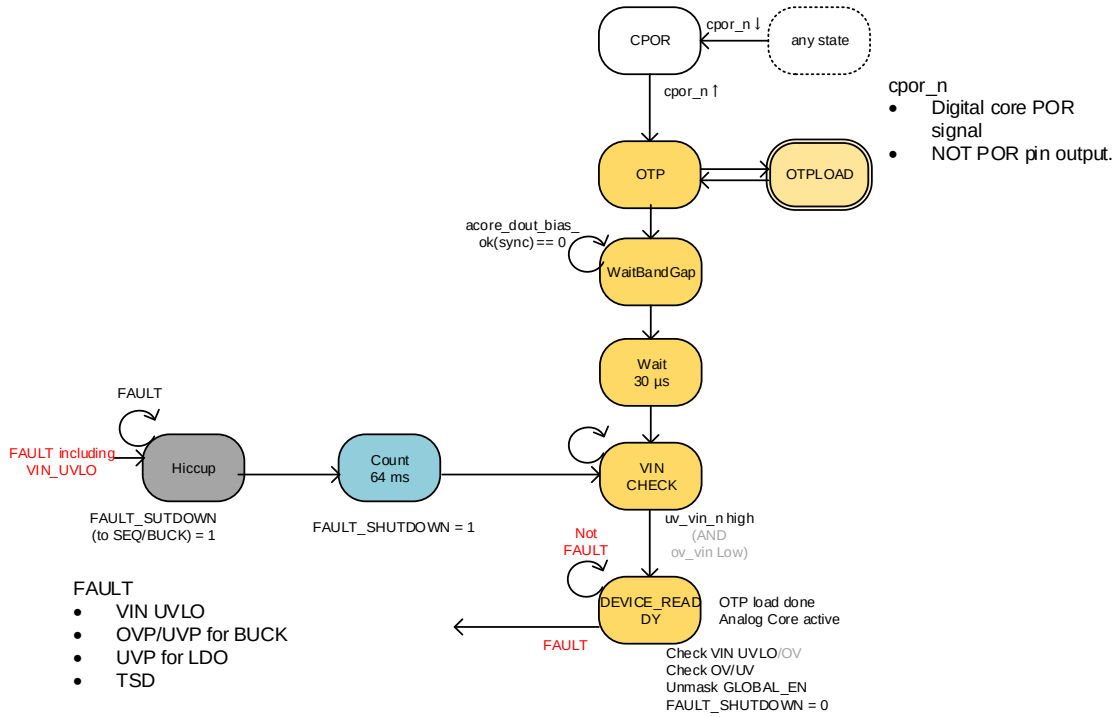


Figure 6: FSM States

7 Sequencer

7.1 Functional Description

DA9080 includes a sequencer to control the power-up and power-down behavior. Any number of voltage supplies (bucks and LDO) can be grouped and assigned to a sequencer slot; for example, PVIN1 and PVIN2 may both be assigned to slot one. Four sequencer slots are provided.

When the sequencer starts all supplies in slot one are enabled. The sequencer then waits until all the enabled supplies have started correctly as confirmed by the corresponding power-good indicator (see Section 8.3). A blanking time is applied during supply startup to prevent fault conditions being registered. A delay, t_{PG}, is applied between a supply starting correctly and that supply's power-good (PG) indicator being set.

Once all the power-good indicators have been set in slot one, the sequencer moves to slot two and repeat the process. When all slots are completed, the power-up sequence is finished.

If no supplies have been assigned to a slot then the slot completes immediately and the sequencer moves on to the next slot.

For power-down the sequencer is run with reverse slot order. Supplies assigned to slot four are disabled first. When disabled, each buck ramps down the output voltage to the minimum code and then discharges using the internal pull-down resistor. As the LDO is unable to actively discharge its output voltage, when disabled, the LDO uses an internal pull-down resistor to discharge the output voltage.

Once the output voltage discharge ramp is finished, and after a suitable delay, the slot is completed and the sequencer moves to slot three and repeats the process. When all slots are complete, the power-down sequence is finished.

The startup and shutdown sequencers may be triggered by register write. The FORCE_DISABLE register bit will shut down the regulators if written high whilst the chip is enabled. When using this register care should be taken that the regulators are not also disabled by writing their individual enable registers: The FORCE DISABLE register is located in the same register bank as the individual regulator enable bits (EN1/2/3/4/L) If the regulator enables are set low when FORCE_DISABLE is used then the regulators will not restart when FORCE_DISABLE is cleared.

7.2 Timing Diagrams

The following diagrams show examples of chip power-up and power-down.

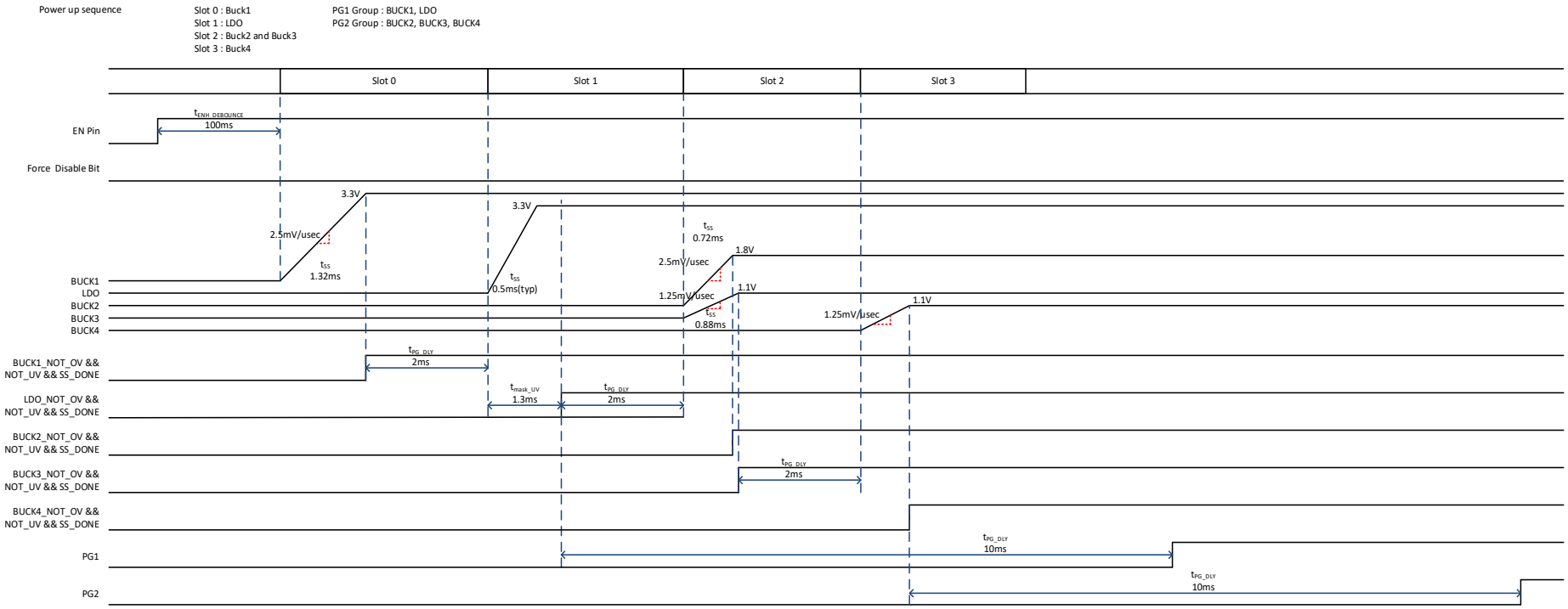


Figure 7: Timing Diagram Example for Power-Up

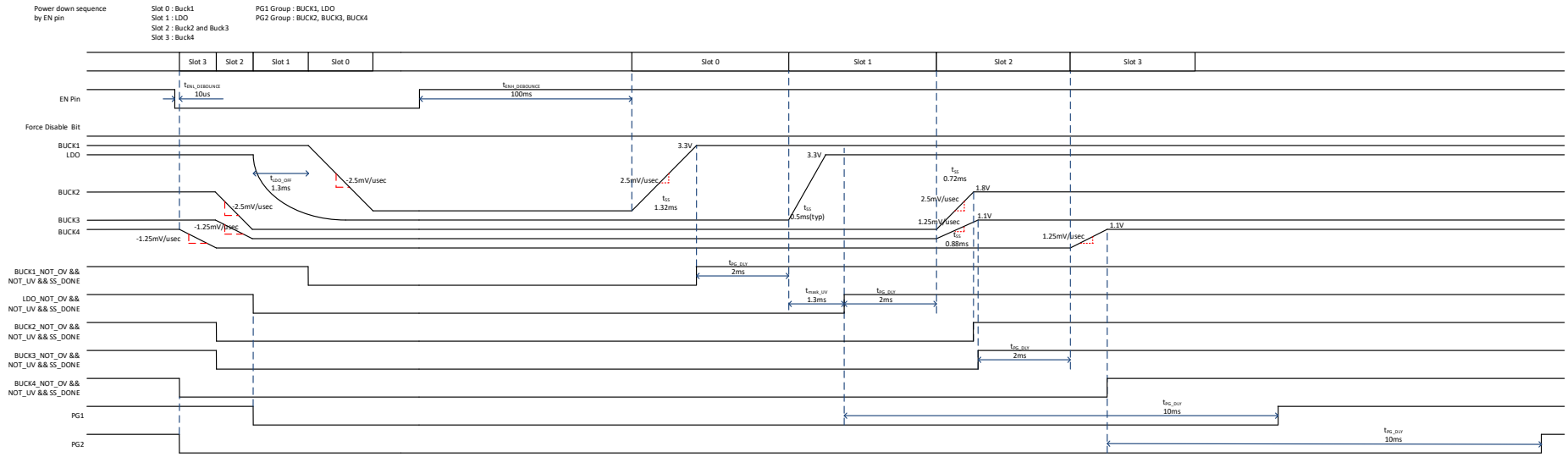


Figure 8: Timing Diagram Example for Power-Down by EN Pin

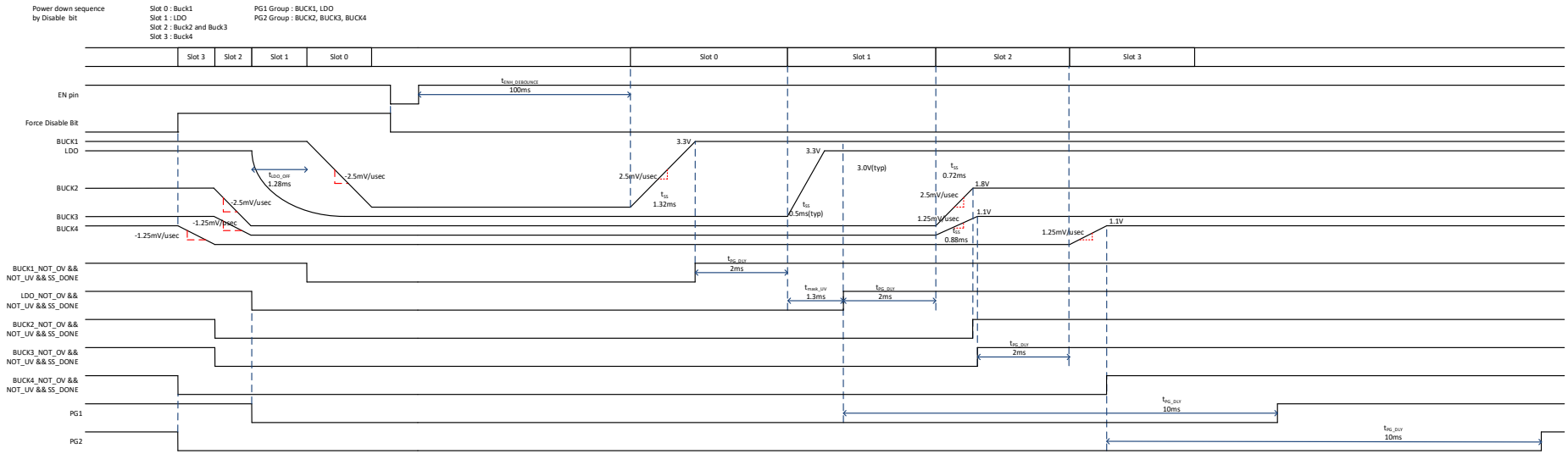


Figure 9: Timing Diagram Example for Power-Down by DISABLE Bit

8 Supervision

8.1 Input Voltage Monitor Flag

The voltage at the VSYS pin is continually monitored. The status of this pin is reported in a 2-bit register field. One bit provides the current status of this pin while the other bit is sticky, being set when the voltage on the VSYS pin transitions below 4.4 V. The input voltage monitor comparator has a 4.6 V rise, 4.4 V fall, and 0.2 V hysteresis. The host can poll these two bits to check the status of this pin. The sticky bit is cleared by writing 1 to it.

8.2 Fault Protection

8.2.1 Over-Voltage, Under-Voltage, and Over-Current Protection

Each buck has over-voltage (OV), under-voltage (UV), and over-current (OC) fault protection.

When the buck output drops below $V_{THR\_UVP\_FALL}$, the BUCK<x>_UV_STAT bit in the PMC_CH_UV register is set to 0x1. When the buck output increases above $V_{THR\_OVP\_RISE}$ the BUCK<x>_OV_STAT bit in the PMC_CH_OV register is set to 0x1.

Each of the bucks has current limit, I_{POSLIM}, with programmable thresholds. When the current limit is met, the BUCK<x>_OC_STAT bit in the PMC_CH_OC register is set to 0x1.

The LDO has under-voltage (UV) and over-current (OC) fault protection. When either of these conditions is met, status bits are set to 0x1 in dedicated registers, in a similar way to the bucks. A supply voltage fault condition (UV or OV), on any supply, causes a power down and all supplies are disabled. The sequencer is run with reverse slot order. Supplies assigned to slot four are disabled first.

A re-start is initiated, after a blanking time, with a hiccup behavior. The outputs are discharged by the internal pull-down resistors prior to being enabled again.

The UV, OV and OC register bits are sticky and remain set through a hiccup cycle, see Figure 10. The register bits are only cleared on a register write of 1.

8.2.2 Thermal Shutdown

DA9080 also has a thermal shutdown (TSD) function. When the die temperature goes above 140 °C (typ) (T_{THR_SHDN}), all the regulator outputs and the GPADC are shutdown. The sequencer is run with reverse slot order. Supplies assigned to slot four are disabled first.

The TSD event is recorded in a register OVERTEMP_EVENT bit<7> in PMC_CH_OC (0x01).

When the die temperature goes below 125 °C(typ), the start-up sequence is restarted.

Note that the I^2C communication is halted during TSD, the OVERTEMP_EVENT bit cannot be read back at this time. The host should check the OVERTEMP_EVENT bit after the device has recovered from TSD. The OVERTEMP_EVENT bit is sticky and is cleared by over-writing the bit with 1.

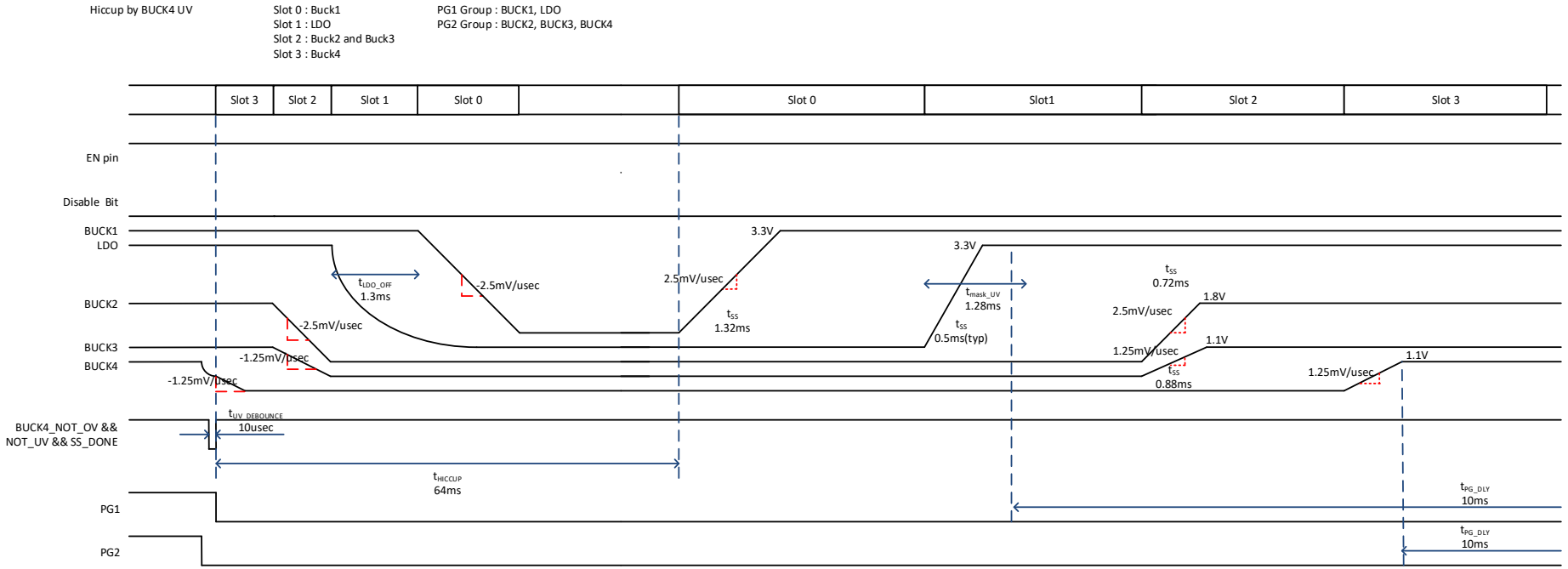


Figure 10: Timing Diagram Example for a Hiccup Cycle

8.3 Power Good Indicator

Each supply has a power-good (PG) indicator that is set once the supply has been enabled and has started correctly. After the supply becomes valid there is a delay, t_{PG}, before the PG indicator is set. For the bucks the PG indicator is the logical NOR of the UV and OV fault indicators.

During soft start the PG indicator is held low while the supply output is being ramped. When this ramp is completed, and assuming no fault conditions exist, the PG indicator is set (after t_{PG}). If a fault exists once the soft-start voltage ramp is completed a fault will be registered and all supplies are immediately disabled.

For the LDO there is a soft-start timeout period, $t_{SS\_TIMEOUT}$, during which UV fault detection is blanked. After this period the LDO output is monitored for fault conditions.

During a dynamic voltage ramp the PG detection is blanked and held high. After the ramp has completed the blanking is removed and the PG status is re-evaluated.

The PG indicators are cleared immediately in the event of a fault.

8.3.1 Monitoring Groups of Power Good Indicators via PG Pins

The output pins PG1 and PG2 are used to monitor the status of groups of PG indicators. Each pin's group is determined by setting a register bit associated with an individual supply's PG indicator. A PG pin is only set when all the PG indicators assigned to its group are set.

If no supplies are assigned to a PG pin then the pin is high impedance.

A delay is applied between the condition for the PG pin to be set and the PG1 or PG2 pin going high. This delay is in addition to the delay added to the individual supply PG indicators.

The status of any PG indicator can be read back via I^2C.

9 Buck Converters

DA9080 has four channels of switching buck converters, CH1 Buck to CH4 Buck. Each of the bucks has an I^2C programable voltage register, which defines the output voltage. The channels are phase shifted by 0°, 90°, 180°, or 270°.

When a buck is enabled, its output voltage is controlled by a soft-start, output voltage ramp. When the buck output reaches the target voltage, the power-good indicator status bit is set.

If a buck is enabled while the output capacitor is already charged (at a non-zero voltage) the buck will not discharge the output during startup. The buck will not draw negative current while the soft-start target voltage is lower than the actual output voltage and the voltage will then rise smoothly once the soft-start voltage ramp exceeds the actual output voltage.

After a buck is disabled, the output voltage is completely discharged by the integrated pull-down resistor before a new start-up is executed.

A pull-down resistor for each channel is enabled when the channel is disabled. This feature can be disabled by setting dedicated register bits, each pull-down can be disabled individually per-buck.

9.1 Dynamic Voltage Control

CH1 and CH2 Buck converters do not support dynamic voltage control (DVC), their output voltage is set by OTP register setting.

CH3 and CH4 Buck converters support DVC, with the following features:

- When the value of the target voltage changes, the output voltage updates to the new target value.
- The DVC controller operates in pulse width modulation (PWM) mode (Note 1) with synchronous rectification. During DVC operation the power-good indicator is available.

Note 1 At higher loads the bucks will operate in PWM at a fixed frequency. To support light loads the bucks will operate in pulse frequency modulation (PFM) mode. The bucks move between PFM and PWM automatically depending on the load requirements.

10 LDO

DA9080 has one LDO which provides a fixed, regulated 3.3 V output voltage.

The LDO has soft-start function and its output voltage gradually increases when the LDO is enabled.

A pull-down resistor for the LDO output is enabled when the LDO is disabled. This feature can be disabled by setting dedicated register bits.

11 General Purpose Analog-to-Digital Converter

DA9080 features an 8-bit successive approximation register (SAR) analog-to-digital converter (ADC).

The GPADC allows measurement of:

- die temperature
- external voltages (AN0 and AN1)

The GPADC consists of an analog-to-digital converter (ADC) with 8-bit resolution, combined with an analog input multiplexer to select a variety of channels. The input MUX selects from the inputs and presents the channel to be measured to the ADC input.

11.1 Measurements on Internal Die Temperature Sensors

A die temperature sensor is placed near known heat sources on the die for managing power. The sensor consists of a bipolar junction diode which is fed by a current source. A measurement on this channel produces a reading of the voltage across the diode.

When using the ADC to measure the die temperature sensor, the output ADC code can be converted into ºC using the formula: T(ºC) = -1.97 * CODE + 349.

11.2 Measurements of External Analog Signals

External analog signals can be measured using the GPADC. The pins AN0 and AN1 are provided as inputs for signals to be measured. Signals to be measured should be in the range 0 V to 5.1 V. In the case where the supply voltage, V_{SYS}, is lower than 5.1 V this does not limit the range of the GPADC and signals up to 5.1 V can still be measured.

Signals from AN0 and AN1 are directly input to the GPADC during conversion and so should not vary during conversion period. The GPADC assumes signals are DC for the duration of the conversion.

When using the ADC to measure the external signals, the output ADC code can be converted into a voltage by using the formula: AN0/1 = CODE * 20 mV + 10 mV.

11.3 Triggering GPADC Conversions

GPADC operations are enabled by setting ADC_EN = 0x1. The ADC automatically converts all inputs sequentially, an ADC read command automatically updates all ADC input values. The 8-bit result is stored in the PMC_TEMP, PMC_ADC0, and PMC_ADC1 registers.

12 I²C Communication

DA9080 includes an I²C-compatible 2-wire serial interface to access the internal registers. Through the I²C interface, the host processor controls each channel and reads back system status. The DA9080 only operates as a slave device.

The host processor provides the serial clock at the SCL pin. DA9080 supports I²C Standard-mode at 100 kHz, Fast-mode at 400 kHz, and Fast-mode Plus at 1000 kHz.

DA9080 SLAVE address is 0x1B.

The I²C data pin, SDA, is open drain which allows multiple devices to share a communication line.

All transmissions begin with a START condition issued from the Master while the bus is in an IDLE state (the bus is free). The START condition is initiated by a high to low transition on SDA while SCL is high. Alternately, a STOP condition is indicated by a low to high transition on SDA while SCL is high, see Figure 11.

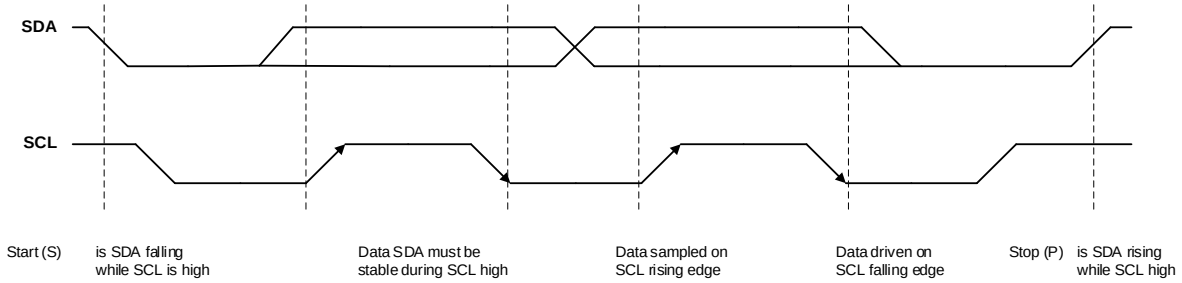


Figure 11: I²C Start (S) and Stop (P)

The I²C interface uses a two-byte serial protocol containing one byte for address and one byte for data. The data and address are transferred with MSB transmitted first for both read and write operations.

DA9080 monitors the serial bus for a valid SLAVE address when the interface is enabled. When it receives its own slave address, DA9080 immediately gives an Acknowledge signal to the host by pulling SDA low during the following clock cycle. A Not Acknowledge signal is given by a logic 1, not pulling down the SDA line.

A single-byte write is shown in Figure 12. Here the slave address is followed by a write bit (low), the register address, and the write data. Finally, the transaction is terminated with a STOP.

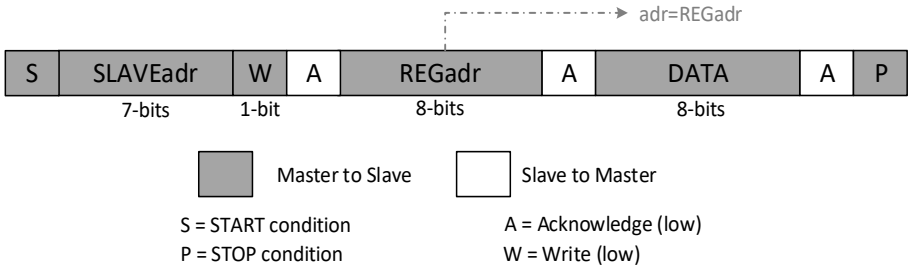


Figure 12: Single Write Command

DA9080 also supports multiple byte writes, shown in Figure 13. By not sending the STOP command, data is written to consecutive addresses.

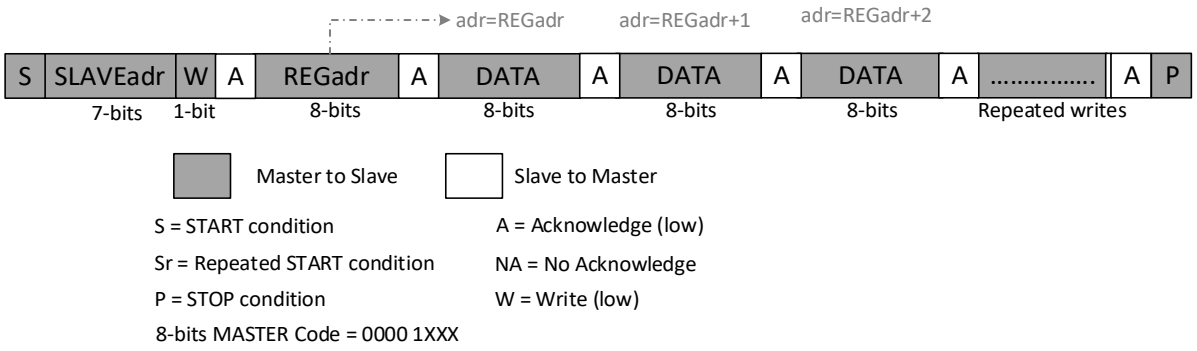


Figure 13: Consecutive Write Command

The data read protocol differs from the write protocol. A read does not have a register address immediately preceding it. To read from a specific address, the register address is given by using a write command followed by a Repeated START. A single-byte read is shown in Figure 14. A Repeated START is followed by the slave address and a read bit. After the read data is returned to the host, the host then responds with a Not Acknowledge and a STOP.

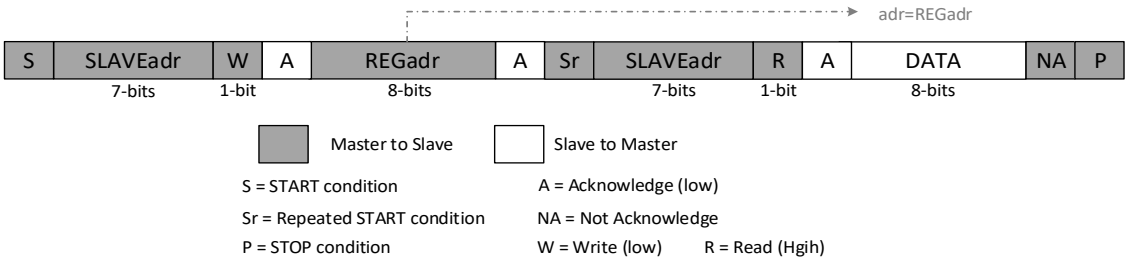


Figure 14: Single Read Command

The DA9080 also supports a multiple byte read protocol. If the host responds to the returned data with an Acknowledge rather than Not Acknowledge and STOP, data will be read from sequential addresses until a Not Acknowledge and STOP command is given, as shown in Figure 15. If a read address is given with a write and Repeated START, consecutive addresses are read from the write address.

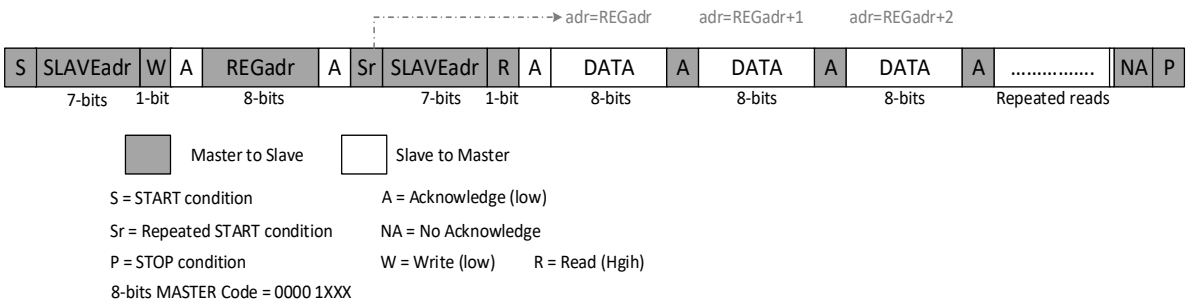


Figure 15: Consecutive Read Command

13 Register Definitions

13.1 Register Map

Table 17: Register Map

Addr	Register	7	6	5	4	3	2	1	0	Reset
Functional Registers										
PMIC Function Registers										
0x0000	PMC_PGOOD_UV	Reserved 0	UV_FLAG	UV_CURRENT	BUCK4_PG_STAT	BUCK3_PG_STAT	BUCK2_PG_STAT	BUCK1_PG_STAT	LDO_PG_STAT	0x00
0x0001	PMC_CH_OC	OVERTEMP_EVENT	Reserved	Reserved	BUCK4_OC_EVENT	BUCK3_OC_EVENT	BUCK2_OC_EVENT	BUCK1_OC_EVENT	LDO_OC_EVENT	0x00
0x0002	PMC_CH_OV	Reserved	Reserved	Reserved	BUCK4_OV_EVENT	BUCK3_OV_EVENT	BUCK2_OV_EVENT	BUCK1_OV_EVENT	Reserved	0x00
0x0003	PMC_CH_UV	Reserved	Reserved	Reserved	BUCK4_UV_EVENT	BUCK3_UV_EVENT	BUCK2_UV_EVENT	BUCK1_UV_EVENT	LDO_UV_EVENT	0x00
0x0004	PMC_ADC_ENABLE	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	ADC_EN	0x01
0x0005	PMC_CH_EN	Reserved	Reserved	FORCE_DISABLE	EN4	EN3	EN2	EN1	ENL	0x1F
0x0007	PMC_VOUT_BUCK1	VBUCK1<7:0>								0x3C
0x0008	PMC_VOUT_BUCK2	VBUCK2<7:0>								0x0F
0x0009	PMC_VOUT_BUCK3	VBUCK3<7:0>								0x3C
0x000A	PMC_VOUT_BUCK4	VBUCK4<7:0>								0x28
0x000B	PMC_PHASE_INTERLEAVING	BUCK4_PHASE<1:0>		BUCK3_PHASE<1:0>		BUCK2_PHASE<1:0>		BUCK1_PHASE<1:0>		0xE4
0x000C	PMC_BUCK_SEQ_GRP	BUCK4_GRP<1:0>		BUCK3_GRP<1:0>		BUCK2_GRP<1:0>		BUCK1_GRP<1:0>		0xF9
0x000D	PMC_LDO_SEQ_GRP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	LDO_GRP<1:0>		0x00

Addr	Register	7	6	5	4	3	2	1	0	Reset
0x000E	PMC_PG1	Reserved	Reserved	Reserved	BUCK4_PG1	BUCK3_PG1	BUCK2_PG1	BUCK1_PG1	LDO_PG1	0x04
0x000F	PMC_PG2	Reserved	Reserved	Reserved	BUCK4_PG2	BUCK3_PG2	BUCK2_PG2	BUCK1_PG2	LDO_PG2	0x1A
0x0010	PMC_DISCHARGE	Reserved	Reserved	Reserved	BUCK4_DISCHARGE	BUCK3_DISCHARGE	BUCK2_DISCHARGE	BUCK1_DISCHARGE	LDO_DISCHARGE	0x1F
0x0011	PMC_TEMP	TEMP<7:0>								0x00
0x0012	PMC_ADC0	ADC0<7:0>								0x00
0x0013	PMC_ADC1	ADC1<7:0>								0x00
0x0014	PMC_REVISION_ID	REVISION_ID<7:0>								0xE9
OTP Control										
Chip ID										
0x0062	OTP_CONFIG_ID	CONFIG_REV<7:0>								0x00

13.2 Register Descriptions

13.2.1 PMIC Function Registers

Table 18: PMC_PGOOD_UV (0x0000)

Bit	Type	Field Name	Description	Reset
[6]	RW1C	UV_FLAG	Indicates the VSYS voltage once fell below 4.4 V after having once risen above 4.6 V. This is a sticky flag. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 No UV_EVENT has happened 0x1 UV_EVENT has happened	0x0
[5]	R	UV_CURRENT	Indicates current VSYS under-voltage (UV) status. **Value** **Description** 0x0 Not in UV state. Current VSYS > 4.6 V 0x1 In UV state. Current VSYS < 4.4 V	0x0
[4]	R	BUCK4_PG_STAT	CH4 Buck power good (PG) status. **Value** **Description** 0x0 CH4 Buck output voltage is more than +/- 300 mV of target voltage 0x1 CH4 Buck output voltage is within +/- 300 mV of target voltage	0x0
[3]	R	BUCK3_PG_STAT	CH3 Buck PG status. **Value** **Description** 0x0 CH3 Buck output voltage is more than +/- 300 mV of target voltage 0x1 CH3 Buck output voltage is within +/- 300 mV of target voltage	0x0
[2]	R	BUCK2_PG_STAT	CH2 Buck PG status. **Value** **Description** 0x0 CH2 Buck output voltage is more than +/- 300 mV of target voltage 0x1 CH2 Buck output voltage is within +/- 300 mV of target voltage	0x0
[1]	R	BUCK1_PG_STAT	CH1 Buck PG status. **Value** **Description** 0x0 CH1 Buck output voltage is more than +/- 300 mV of target voltage 0x1 CH1 Buck output voltage is within +/- 300 mV of target voltage	0x0
[0]	R	LDO_PG_STAT	LDO PG status. **Value** **Description**	0x0

Bit	Type	Field Name	Description	Reset
			0x0 LDO output voltage is not higher than 3.0 V 0x1 LDO output voltage is higher than 3.0 V	

Table 19: PMC_CH_OC (0x0001)

Bit	Type	Field Name	Description	Reset
[7]	RW1C	OVERTEMP_EVENT	Indicates an over-temperature event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 No over-temperature event. 0x1 Over-temperature event.	0x0
[4]	RW1C	BUCK4_OC_EVENT	Indicates a CH4 Buck over-current (OC) event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH4 Buck no OC event 0x1 CH Buck OC event	0x0
[3]	RW1C	BUCK3_OC_EVENT	Indicates a CH3 Buck over-current event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH3 Buck no OC event 0x1 CH3 Buck OC event	0x0
[2]	RW1C	BUCK2_OC_EVENT	Indicates a CH2 Buck over-current event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH2 Buck no OC event 0x1 CH2 Buck OC event	0x0
[1]	RW1C	BUCK1_OC_EVENT	Indicates a CH1 Buck over-current event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH1 Buck no OC event 0x1 CH1 Buck OC event	0x0
[0]	RW1C	LDO_OC_EVENT	Indicates an LDO over-current event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 LDO no OC event 0x1 LDO OC event	0x0

Table 20: PMC_CH_OV (0x0002)

Bit	Type	Field Name	Description	Reset
[4]	RW1C	BUCK4_OV_EVENT	Indicates a CH4 Buck over-voltage (OV) event. Clear by a POR or writing 1 via I2C.	0x0

Bit	Type	Field Name	Description	Reset
			Value **Description** 0x0 CH4 Buck no OV event 0x1 CH4 Buck OV event	
[3]	RW1C	BUCK3_OV_EVENT	Indicates a CH3 Buck over-voltage event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH3 Buck no OV event 0x1 CH3 Buck OV event	0x0
[2]	RW1C	BUCK2_OV_EVENT	Indicates a CH2 Buck over-voltage event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH2 Buck no OV event 0x1 CH2 Buck OV event	0x0
[1]	RW1C	BUCK1_OV_EVENT	Indicates a CH1 Buck over-voltage event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH1 Buck no OV event 0x1 CH1 Buck OV event	0x0

Table 21: PMC_CH_UV (0x0003)

Bit	Type	Field Name	Description	Reset
[4]	RW1C	BUCK4_UV_EVENT	Indicates a CH4 Buck under-voltage (UV) event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH4 Buck no UV event 0x1 CH4 Buck UV event	0x0
[3]	RW1C	BUCK3_UV_EVENT	Indicates a CH3 Buck under-voltage event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH3 Buck no UV event 0x1 CH3 Buck UV event	0x0
[2]	RW1C	BUCK2_UV_EVENT	Indicates a CH2 Buck under-voltage event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH2 Buck no UV event 0x1 CH2 Buck UV event	0x0
[1]	RW1C	BUCK1_UV_EVENT	Indicates a CH1 Buck under-voltage event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 CH1 Buck no UV event	0x0

Bit	Type	Field Name	Description	Reset
			0x1 CH1 Buck UV event	
[0]	RW1C	LDO_UV_EVENT	Indicates an LDO UV event. Clear by a POR or writing 1 via I2C. **Value** **Description** 0x0 LDO no UV event 0x1 LDO UV event	0x0

Table 22: PMC_ADC_ENABLE (0x0004)

Bit	Type	Field Name	Description	Reset
[0]	RW	ADC_EN	ADC enable. **Value** **Description** 0x0 ADC disabled 0x1 ADC enabled	0x1

Table 23: PMC_CH_EN (0x0005)

Bit	Type	Field Name	Description	Reset
[5]	RW	FORCE_DISABLE	When this bit is set to 1 and the EN pin is high, a shutdown sequence starts. This bit is automatically cleared to 0 when the external EN pin is toggled low. **Value** **Description** 0x0 This function is off 0x1 This function is on	0x0
[4]	RW	EN4	CH4 Buck enable. **Value** **Description** 0x0 CH4 Buck disabled 0x1 CH4 Buck enabled	0x1
[3]	RW	EN3	CH3 Buck enable. **Value** **Description** 0x0 CH3 Buck disabled 0x1 CH3 Buck enabled	0x1
[2]	RW	EN2	CH2 Buck enable. **Value** **Description** 0x0 CH2 Buck disabled 0x1 CH2 Buck enabled	0x1
[1]	RW	EN1	CH1 Buck enable. **Value** **Description** 0x0 CH1 Buck disabled 0x1 CH1 Buck enabled	0x1

Bit	Type	Field Name	Description	Reset
[0]	RW	ENL	LDO enable. **Value** **Description** 0x0 LDO disabled 0x1 LDO enabled	0x1

Table 24: PMC_VOUT_BUCK1 (0x0007)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	VBUCK1	VBUCK1[7:0] CH1 Buck output voltage setting. 0x00 = 2.1 V, 0x3C = 3.3 V(Default), 20 mV resolution. Although this register will accept any value in its range of 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range stated in the electrical table.	0x3C

Table 25: PMC_VOUT_BUCK2 (0x0008)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	VBUCK2	VBUCK2[7:0] CH2 Buck output voltage setting. 0x00 = 1.5 V, 0x0F = 1.8 V(Default), 0x37 = 2.6 V, 20 mV resolution. Although this register will accept any value in its range of 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range stated in the electrical table.	0x0F

Table 26: PMC_VOUT_BUCK3 (0x0009)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	VBUCK3	VBUCK3[7:0] CH3 Buck output voltage setting. 0x00 = 0.9 V, 0x3C = 1.2 V (Default), 0x50 = 1.3 V, 5 mV resolution. Although this register will accept any value in its range of 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range stated in the electrical table.	0x3C

Table 27: PMC_VOUT_BUCK4 (0x000A)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	VBUCK4	VBUCK4[7:0] CH4 Buck output voltage setting. 0x00 = 0.8 V, 0x28 = 1.0 V (Default), 0 x 78 = 1.4 V, 5 mV resolution. Although this register will accept any value in its range of 0x00 to 0xFF, the output voltage accuracy is not guaranteed outside the range stated in the electrical table.	0x28

Table 28: PMC_PHASE_INTERLEAVING (0x000B)

Bit	Type	Field Name	Description	Reset
[7:6]	R	BUCK4_PHASE	CH4 Buck phase interleave. **Value** **Description** 0x0 CH4 Buck phase is 0 degrees 0x1 CH4 Buck phase is 90 degrees	0x3

Bit	Type	Field Name	Description	Reset
			0x2 CH4 Buck phase is 180 degrees 0x3 CH4 Buck phase is 270 degrees	
[5:4]	R	BUCK3_PHASE	CH3 Buck phase interleave. **Value Description** 0x0 CH3 Buck phase is 0 degrees 0x1 CH3 Buck phase is 90 degrees 0x2 CH3 Buck phase is 180 degrees 0x3 CH3 Buck phase is 270 degrees	0x2
[3:2]	R	BUCK2_PHASE	CH2 Buck phase interleave. **Value Description** 0x0 CH2 Buck phase is 0 degrees 0x1 CH2 Buck phase is 90 degrees 0x2 CH2 Buck phase is 180 degrees 0x3 CH2 Buck phase is 270 degrees	0x1
[1:0]	R	BUCK1_PHASE	BUCK1 phase interleave. **Value Description** 0x0 CH1 Buck phase is 0 degrees 0x1 CH1 Buck phase is 90 degrees 0x2 CH1 Buck phase is 180 degrees 0x3 CH1 Buck phase is 270 degrees	0x0

Table 29: PMC_BUCK_SEQ_GRP (0x000C)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	BUCK4_GRP	Assign CH4 Buck to a power-up / power-down sequencing slot. **Value Description** 0x0 CH4 Buck is assigned to slot 1 0x1 CH4 Buck is assigned to slot 2 0x2 CH4 Buck is assigned to slot 3 0x3 CH4 Buck is assigned to slot 4	0x3
[5:4]	RW	BUCK3_GRP	Assign CH3 Buck to a power-up / power-down sequencing slot. **Value Description** 0x0 CH3 Buck is assigned to slot 1 0x1 CH3 Buck is assigned to slot 2 0x2 CH3 Buck is assigned to slot 3 0x3 CH3 Buck is assigned to slot 4	0x3

Bit	Type	Field Name	Description	Reset
[3:2]	RW	BUCK2_GRP	Assign CH2 Buck to a power-up / power-down sequencing slot. **Value** **Description** 0x0 CH2 Buck is assigned to slot 1 0x1 CH2 Buck is assigned to slot 2 0x2 CH2 Buck is assigned to slot 3 0x3 CH2 Buck is assigned to slot 4	0x2
[1:0]	RW	BUCK1_GRP	Assign CH1 Buck to a power-up / power-down sequencing slot. **Value** **Description** 0x0 CH1 Buck is assigned to slot 1 0x1 CH1 Buck is assigned to slot 2 0x2 CH1 Buck is assigned to slot 3 0x3 CH1 Buck is assigned to slot 4	0x1

Table 30: PMC_LDO_SEQ_GRP (0x000D)

Bit	Type	Field Name	Description	Reset
[1:0]	RW	LDO_GRP	Assign LDO to a power-up / power-down sequencing slot. **Value** **Description** 0x0 LDO is assigned to slot 1 0x1 LDO is assigned to slot 2 0x2 LDO is assigned to slot 3 0x3 LDO is assigned to slot 4	0x0

Table 31: PMC_PG1 (0x000E)

Bit	Type	Field Name	Description	Reset
[4]	RW	BUCK4_PG1	Assign CH4 Buck to PG1 monitor group. **Value** **Description** 0x0 CH4 Buck is not assigned to PG1 group 0x1 CH4 Buck is assigned to PG1 group	0x0
[3]	RW	BUCK3_PG1	Assign CH3 Buck to PG1 monitor group. **Value** **Description** 0x0 CH3 Buck is not assigned to PG1 group 0x1 CH3 Buck is assigned to PG1 group	0x0
[2]	RW	BUCK2_PG1	Assign CH2 Buck to PG1 monitor group. **Value** **Description** 0x0 CH2 Buck is not assigned to PG1 group 0x1 CH2 Buck is assigned to PG1 group	0x1

Bit	Type	Field Name	Description	Reset
[1]	RW	BUCK1_PG1	Assign CH1 Buck to PG1 monitor group. **Value** **Description** 0x0 CH1 Buck is not assigned to PG1 group 0x1 CH1 Buck is assigned to PG1 group	0x0
[0]	RW	LDO_PG1	Assign LDO to PG1 monitor group. **Value** **Description** 0x0 LDO is not assigned to PG1 group 0x1 LDO is assigned to PG1 group	0x0

Table 32: PMC_PG2 (0x000F)

Bit	Type	Field Name	Description	Reset
[4]	RW	BUCK4_PG2	Assign CH4 Buck to PG2 monitor group. **Value** **Description** 0x0 CH4 Buck is not assigned to PG2 group 0x1 CH4 Buck is assigned to PG2 group	0x1
[3]	RW	BUCK3_PG2	Assign CH3 Buck to PG2 monitor group. **Value** **Description** 0x0 CH3 Buck is not assigned to PG2 group 0x1 CH3 Buck is assigned to PG2 group	0x1
[2]	RW	BUCK2_PG2	Assign CH2 Buck to PG2 monitor group. **Value** **Description** 0x0 CH2 Buck is not assigned to PG2 group 0x1 CH2 Buck is assigned to PG2 group	0x0
[1]	RW	BUCK1_PG2	Assign CH1 Buck to PG2 monitor group. **Value** **Description** 0x0 CH1 Buck is not assigned to PG2 group 0x1 CH1 Buck is assigned to PG2 group	0x1
[0]	RW	LDO_PG2	Assign LDO to PG2 monitor group. **Value** **Description** 0x0 LDO is not assigned to PG2 group 0x1 LDO is assigned to PG2 group	0x0

Table 33: PMC_DISCHARGE (0x0010)

Bit	Type	Field Name	Description	Reset
[4]	RW	BUCK4_DISCHARGE	CH4 Buck discharge resistor control. Connects resistor to ground when channel is shut down. When disabled, excessive charge may be left on output capacitors (NOT recommended). When enabled the resister will be connected after the	0x1

Bit	Type	Field Name	Description	Reset
			buck output voltage has completed ramping down to 0 V. **Value** **Description** 0x0 Disabled - NOT recommended 0x1 Enabled	
[3]	RW	BUCK3_DISCHARGE	CH3 Buck discharge resistor control. Connects resistor to ground when channel is shut down. When disabled, excessive charge may be left on output capacitors (NOT recommended). When enabled the resister will be connected after the buck output voltage has completed ramping down to 0 V. **Value** **Description** 0x0 Disabled - NOT recommended 0x1 Enabled	0x1
[2]	RW	BUCK2_DISCHARGE	CH2 Buck discharge resistor control. Connects resistor to ground when channel is shut down. When disabled, excessive charge may be left on output capacitors (NOT recommended). When enabled the resister will be connected after the buck output voltage has completed ramping down to 0 V. **Value** **Description** 0x0 Disabled - NOT recommended 0x1 Enabled	0x1
[1]	RW	BUCK1_DISCHARGE	CH1 Buck discharge resistor control. Connects resistor to ground when channel is shut down. When disabled, excessive charge may be left on output capacitors (NOT recommended). When enabled the resister will be connected after the buck output voltage has completed ramping down to 0 V. **Value** **Description** 0x0 Disabled - NOT recommended 0x1 Enabled	0x1
[0]	RW	LDO_DISCHARGE	LDO discharge resistor control. Connects resistor to ground when channel is shut down. When disabled, excessive charge may be left on output capacitors (NOT recommended). **Value** **Description** 0x0 Disabled - NOT recommended 0x1 Enabled	0x1

Table 34: PMC_TEMP (0x0011)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	TEMP	Indicates ADC TEMP value. Temperature, T (ºC) = -1.97*CODE + 349	0x0

Table 35: PMC_ADC0 (0x0012)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	ADC0	Indicates AN0 ADC value. VAN0 = 20 mV * CODE	0x0

Table 36: PMC_ADC1 (0x0013)

Bit	Type	Field Name	Description	Reset
[7:0]	RW	ADC1	Indicates AN1 ADC value. VAN1 = 20 mV * CODE	0x0

Table 37: PMC_REVISION_ID (0x0014)

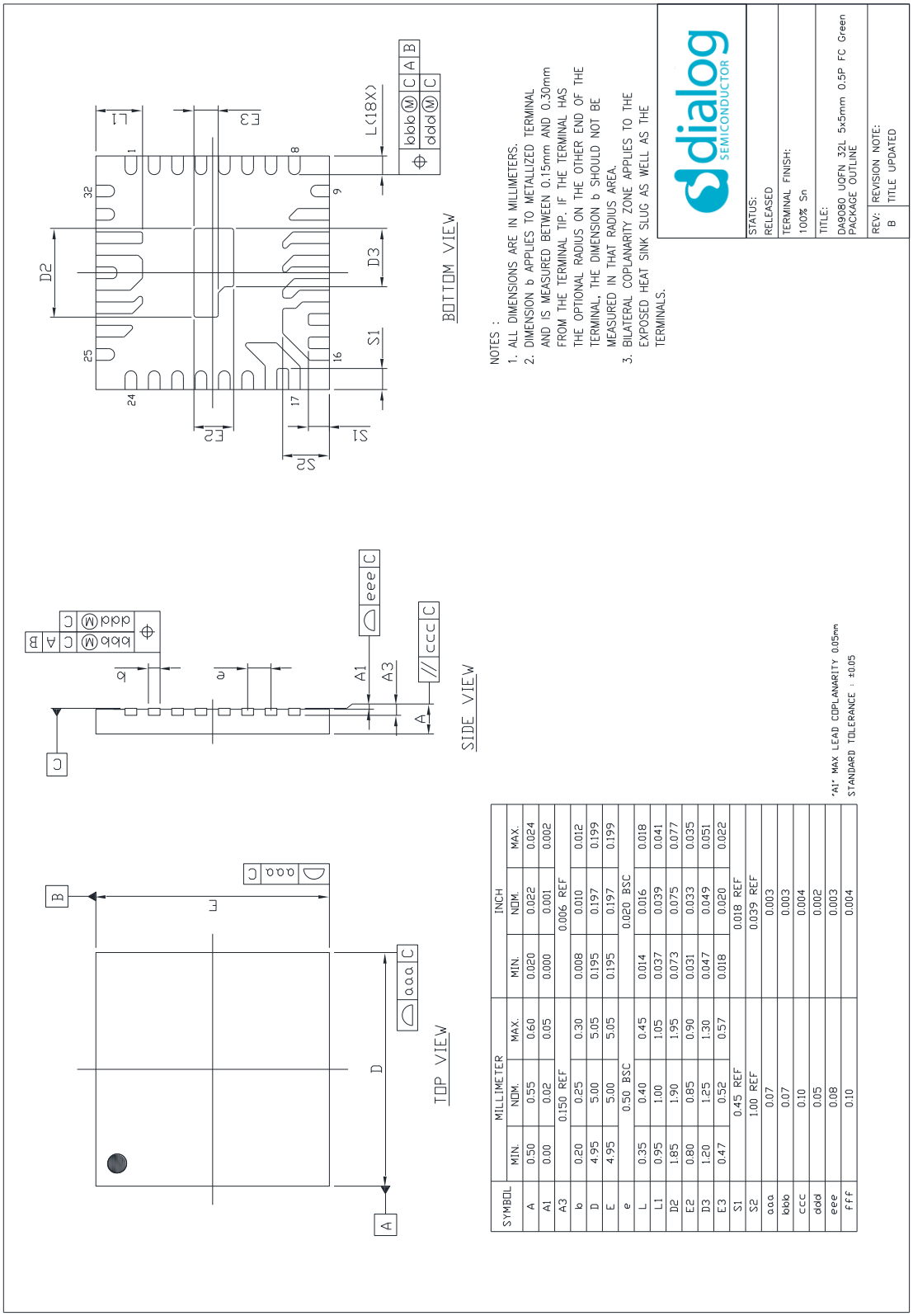
Bit	Type	Field Name	Description	Reset
[7:0]	RW	REVISION_ID	Scratch register for user.	0xE9

13.2.2 Chip ID

Table 38: OTP_CONFIG_ID (0x0062)

Bit	Type	Field Name	Description	Reset
[7:0]	R	CONFIG_REV	OTP variant code.	0x0

14 Package Information



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.150 REF			0.006 REF	
b	0.20	0.25	0.30	0.008	0.010	0.012
D	4.95	5.00	5.05	0.195	0.197	0.199
E	4.95	5.00	5.05	0.195	0.197	0.199
e		0.50 BSC			0.020 BSC	
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.95	1.00	1.05	0.037	0.039	0.041
D2	1.85	1.90	1.95	0.073	0.075	0.077
E2	0.80	0.85	0.90	0.031	0.033	0.035
D3	1.20	1.25	1.30	0.047	0.049	0.051
E3	0.47	0.52	0.57	0.018	0.020	0.022
S1		0.45 REF			0.018 REF	
S2		1.00 REF			0.039 REF	
aaa		0.07			0.003	
bbb		0.07			0.003	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

Figure 16: UQFN Package Outline Diagram

14.1 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 39.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The package is qualified for MSL 3.

Table 39: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

14.2 UQFN Handling

Manual handling of UQFN packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

14.3 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

15 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas Electronics local sales representative.

Table 40: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9080-xxFCB2	UQFN	5.0 x 5.0 by 0.5 mm pitch	Tape and Reel	4900

Part Number Legend:

xx: OTP number

16 Application Information

The following recommended components are references selected from requirements of a typical application.

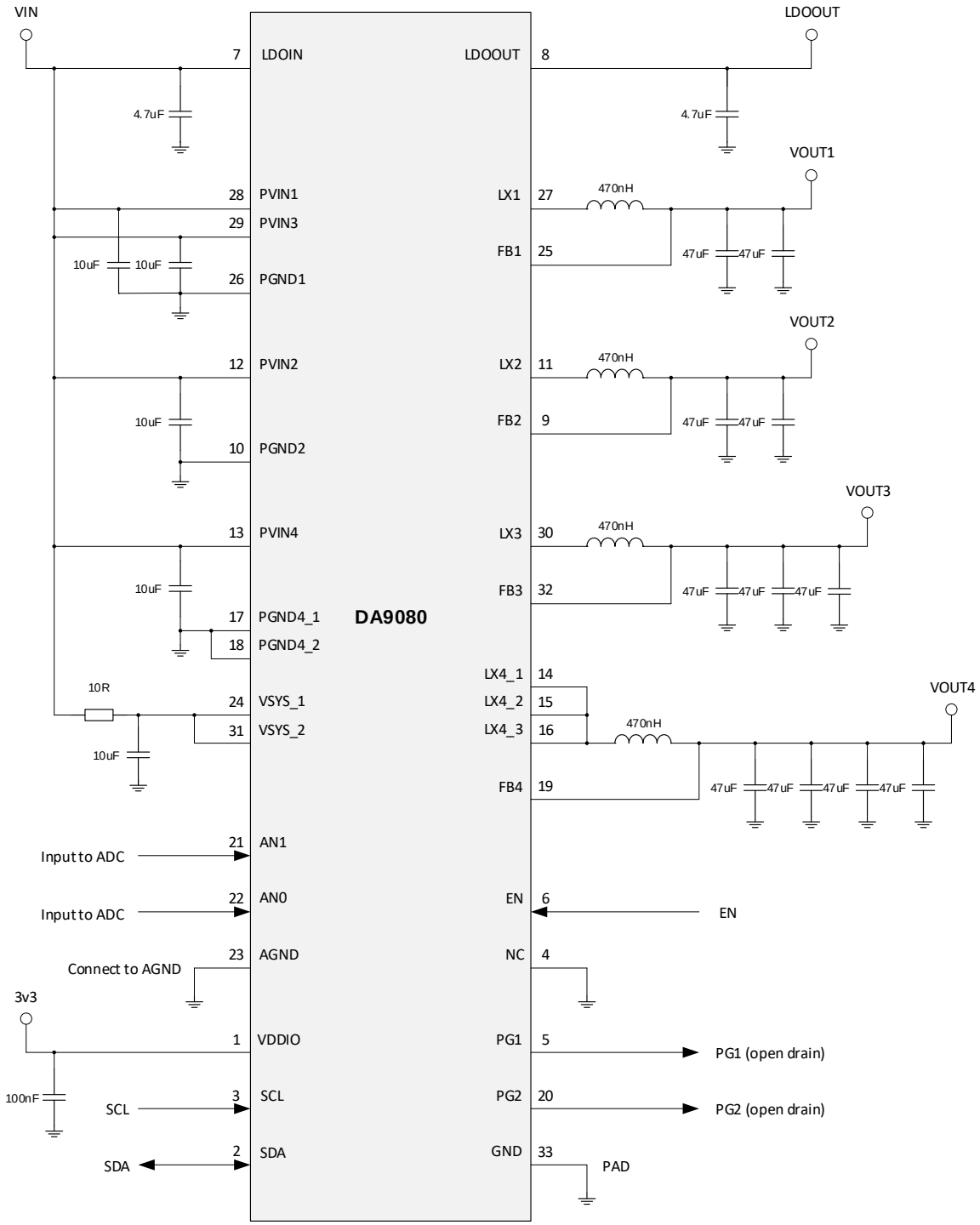


Figure 17: Application Diagram

16.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

Table 41: Recommended Capacitor Types

Application	Value	Size	Temp Char	Tol (%)	Rated (V)	Type
C_{VDDIO}	0.1 µF	0402	X7R ±15 %	±10	25 V	TDK CGA2B3X7R1E104K050BB
C_{LDOIN}, C_{LDOOUT}	4.7 µF	0402	JB ±10 %	±10	10 V	TDK C1005JB1A475K050BC
C_{VSYS}, $C_{PVIN<x>}$	10 µF	0402	X5R ±15 %	±20	10 V	AVX 0402ZD106MAT2A
$C_{VOUT<x>}$	47 µF	0603	X5R ±15 %	±20	6.3 V	Murata GRM188R60J476ME15D

16.2 Resistor Selection

Table 42: Recommended Resistor Type

Application	Value	Size	Tol (%)	Type
R_{VSYS}	10 Ω	0402	±1	Yageo RC0402FR-0710RL

16.3 Inductor Selection

Inductors should be selected based on the following parameters:

- Rated maximum current
- Usually a coil provides two current limits: ISAT specifies the maximum current at which the inductance drops by 30 % of the nominal value, and IMAX is defined by the maximum power dissipation and is applied to the effective current.
- DC resistance
- Critical for the converter efficiency and should therefore be minimized.

Fully shielded inductor is highly recommended to use. The typical recommended output inductance is 470 nH per output. Use of larger output inductance degrades the load transient performance of the buck converter.

Table 43: Recommended Inductor Type

Application	Value (nH)	Size (W*L*H) (mm)	I_{MAX}(DC) (A)	I_{SAT} (A)	Tol (%)	DC Resistance (mΩ)	Type
$L_{OUT<x>}$	470	2.5*2.0*1.0	4.3	5.6	±20	19	Cyntec HMLQ25201T-R47MSR

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.renesas.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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