1-Cell, 1.5 A Battery Charger PMIC with 20 mA Termination, Ultra-Low IQ Reverse Boost, and I2C

General Description

DA9168 is a configurable Battery Management IC (BMIC) with integrated dual LDOs and reverse boost to support USB-OTG. The extremely low quiescent current consumption in a very compact footprint makes it ideally suited for a multitude of space conscious, battery powered consumer applications. The fast-growing hearable segment for True Wireless Stereo (TWS), wearable segment for smart watches, and a range of smart home applications such as smart cameras are examples where the DA9168 is an extremely good fit.

The device comprises a high-efficiency switch mode charger with power path management capable of supporting up to 1.5 A charge current, dual LDOs that can be configured as load switches, and high-efficiency reverse boost functionality.

DA9168 has several power saving modes to increase battery life whether the product sits on the shelf or is in operation. Further savings in power are achieved with the ultra-low I_Q reverse boost converter that is efficient down to 60 µA load currents with low power LDOs.

Key Features

- High-efficiency, synchronous switch mode buck charger
  - 92 % charge efficiency at 0.5 A
  - Pulse frequency modulation (PFM) mode for light load operations
- Reverse current mode from VMID to VBUS
  - Reverse boost with up to 0.7 A output
  - 90% reverse boost efficiency at 1 mA to 10 mA; 95 % reverse boost efficiency at 10 mA to 100 mA output
  - PFM mode for light load operations
- Single input to support USB input and high voltage adapters
  - Supports 4.0 V to 10.0 V input voltage
  - Programmable input current limit (IINDPM) with I^2C (100 mA to 2.5 A, 100 mA/step) to support USB 2.0, USB 3.0 standards and high voltage adaptors
  - Programmable input voltage limit (VINDPM) range 3.8 V to 4.8 V
- Flexible I^2C configuration and autonomous charging for optimal system performance
- Integrates two LDOs / load switches
  - LDO output range 1.6 V to 5.2 V, 350 mA max load
  - Load switch 350 mA max load
- High integration includes all MOSFETs, current sensing, and loop compensation
- Low R_{DS_ON} < 19 mΩ (typ) BATFET to extend battery life
  - BATFET control to support Ship mode, wake up and full system reset
- 15 µA low battery leakage current with system voltage standby
- 0.1 µA (typ) leakage current in Ship mode
- High accuracy battery charging profile
- High integration and configurability
  - I^2C enabled battery temperature monitors
  - Watchdog feature and power cycling to prevent system stall
  - Reset input and Interrupt (INT_N) outputs
  - Compact, 30 pin, 2.5 mm x 2.1 mm x 0.4 mm WLCSP package
- Fast charge
  - Max 1500 mA, min 20 mA charge current
  - Programmable pre-charge, fast charge, and termination voltage
  - Dynamic power path balances
  - ±0.5 % accurate termination voltage
- ±5 % charge current regulation

Applications

- Wearable devices - fitness trackers, smart watches, wireless headphones
- Home automation devices - smoke detectors, smart thermostats, smart door locks
- Health monitoring medical accessories
- Rechargeable toys
- High efficiency, ultra-low power applications

System Diagram

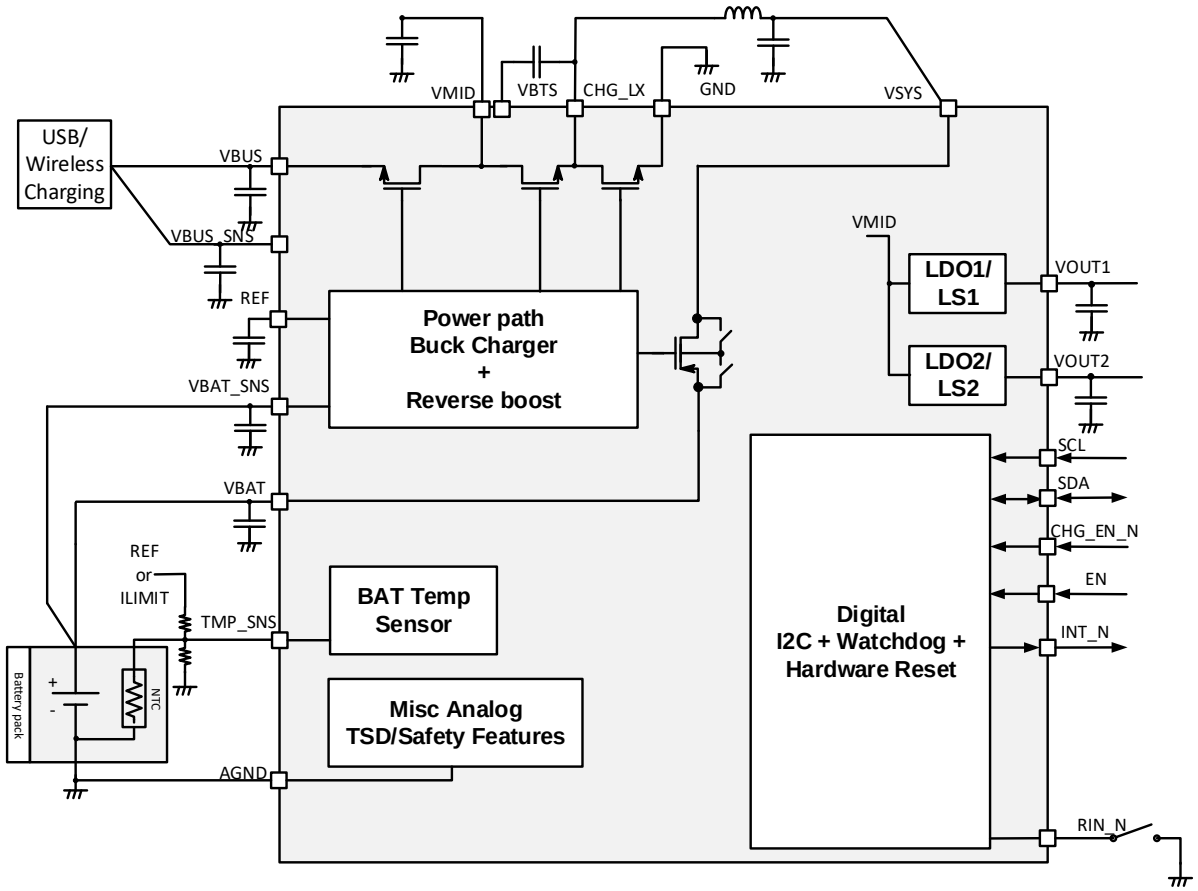

Figure 1: System Diagram

1-Cell, 1.5 A Battery Charger PMIC with 20 mA Termination, Ultra-Low IQ Reverse Boost, and I2C

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1 Terms and Definitions

BATFET	Battery field effect transistor
BMIC	Battery management IC
CHG	Charger or charge
FET	Field effect transistor
IC	Integrated circuit
I2C	Inter-integrated circuit
IINDPM	Dynamic power management input current
JEITA	Japan Electronics and Information Technology Industries Association
LDO	Low dropout regulator
MOSFET	Metal oxide semiconductor FET
OC	Over-current
OK	Okay (operating within specified range)
OV	Over voltage
PFM	Pulse frequency modulation
SPLMT	Supplement (mode)
TS	Temperature sensor
TSD	Temperature shutdown
USB	Universal Serial Bus
USB-PD	USB Power Delivery
USB-OTG	USB On-the-Go
UV	Under voltage
VINDPM	Dynamic power management input voltage
WLCSP	Wafer level chip scale package

2 Pinout

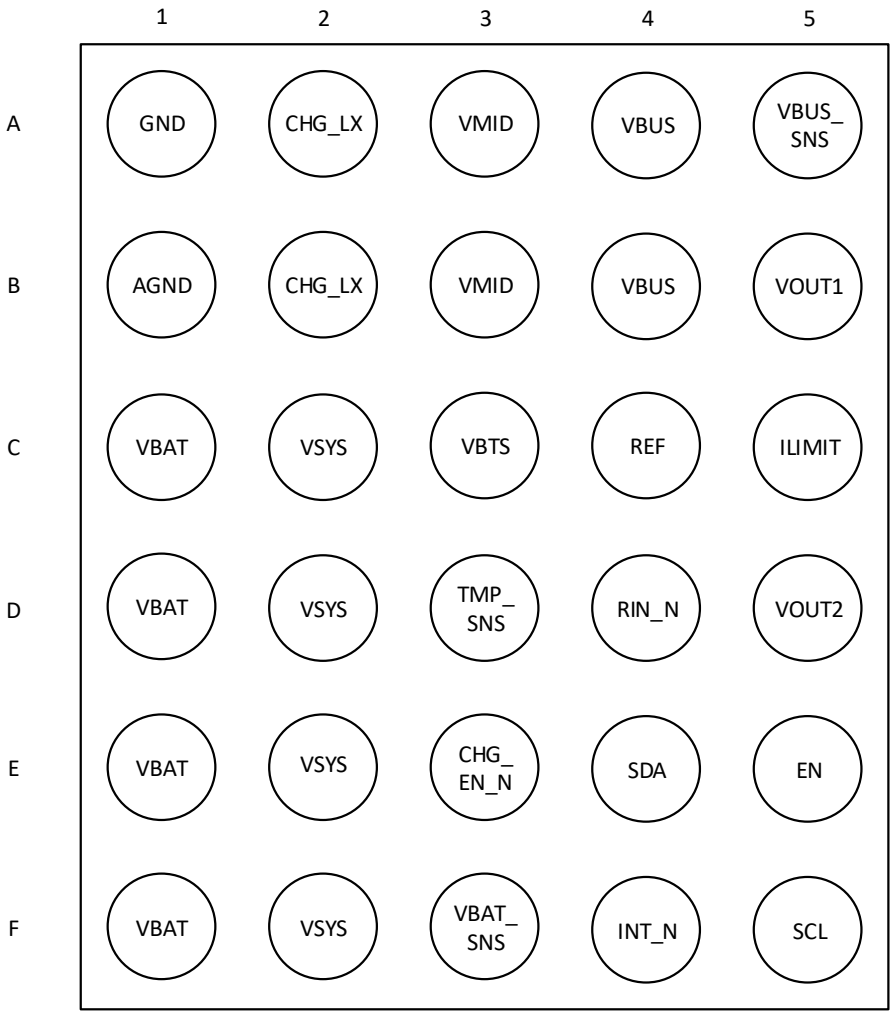


Figure 2: Pinout Diagram (Top View)

Table 1: Pin Description

Pin No.	Pin Name	Type (Table 2)	Description
A1, B1	GND, AGND	GND	Power ground for the buck charger. Connect to the buck input capacitor and ground plane.
A4, B4	VBUS	PWR	Input power supply.
A5	VBUS_SNS	PWR	VBUS voltage sense connection.
C2, D2, E2, F2	VSYS	PWR	VSYS is the intermediate rail.
C3	VBTS	PWR	High side driver positive supply. Internally, VBTS is connected to the cathode of the bootstrap diode.
A3, B3	VMID	PWR	Input of the buck charger.
A2, B2	CHG_LX	PWR	Buck charger switching node. Connect to the inductor.

C4	REF	PWR	Low side driver positive supply output. Internally, REF is connected to the anode of the bootstrap diode. The capacitor should be placed close to the IC.
C1, D1, E1, F1	VBAT	PWR	Battery connection. Connect to the positive terminal of the battery.
F3	VBAT_SNS	AI	Battery voltage sense connection. Connect to the positive battery terminal.
D3	TMP_SNS	AI	Battery pack NTC monitor. Connect to a resistive network and thermistor.
D4	RIN_N	DI	Manual reset input pin. RIN_N is internally pulled high. Pulling this pin low wakes up the device from Ship mode or performs a reset.
E4	SDA	DIO	I^2C interface data. Connect SDA to the logic rail through a 2 kΩ to10 kΩ pull-up resistor.
F5	SCL	DI	I^2C interface clock. Connect SCL to the logic rail through a 2 kΩ to10 kΩ pull-up resistor.
E3	CHG_EN_N	DI	Charger enable. Charing enable when CHG_EN_N is Low. Charing disable when CHG_EN_N is High.
F4	INT_N	DO	Open-drain interrupt output. Connect the INT_N to a logic rail through 10 kΩ resistor. The INT_N pin sends an active low, 256 µs pulse to host to report charger device status and fault.
C5	ILIMIT	AI	Input current limit setting pin. Connect a resistor between ILIMIT and ground to set the VBUS current limit (IINDPM). Alternatively, short this pin to ground to allow IINDPM to be programmed by register. Note: In the current OTP variant, ILIMIT pin is only used as TMP_SNS divider resistors power rail. Please refer to Figure 1.
D5	VOUT2	PWR	Load switch or LDO2 output. Bypass to ground.
B5	VOUT1	PWR	Load switch or LDO1 output. Bypass to ground.
E5	EN	DI	Enable pin for reverse boost, LDO1, and LDO2.

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	PWR	Power
DIO	Digital input/output	GND	Ground

3 Characteristics

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_S	Storage temperature		-55	150	°C
V_{BUS}	VBUS, VBUS_SNS	Device disabled	-6	22	V
V_{MID}	VMID supply voltage	Device disabled	-0.3	22	V
V_{MID_VBUS}	VMID to VBUS voltage	Device disabled	-0.3	18	V
V_{BAT}	VBAT, VBAT_SNS		-0.3	6	V
V_{SYS}	VSYS, VOUT1, VOUT2		-0.3	6	V
V_{IO}	All IO pins (unless otherwise stated)		-0.3	6	V
V_{BTS}	VBTS supply voltage	Not switching	V_{REF} -0.3	22	V
$V_{BTS\_VCHG\_LX}$	VBTS to CHG_LX voltage		-0.3	6	V
V_{CHG_LX}	CHG_LX		-2	16	V
V_{REF}	REF supply voltage		-0.3	6	V

3.2 Electrostatic Discharge Ratings

Table 4: Electrostatic Discharge Ratings

Parameter	Description	Conditions	Value	Unit
ESD_{HBM}	Maximum ESD protection	Human body model (HBM). All exposed pins.	2.0	kV
ESD_{CDM}	Maximum ESD protection	Charged device model (CDM)	0.5	kV

3.3 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Ambient temperature		-40	25	85	
T_J	Operating junction temperature		-40		105	°C
V_{BUS}	VBUS voltage	Including OV range	4	5	10.5	V
	VBUS operating voltage		4	5	10	V
V_{BAT}	Battery voltage	VBUS supplied	0	3.6	4.5	V
	Battery voltage	Active Battery mode	2.8	3.6	4.5	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
		VBUS not supplied				
V_{DDIO}	IO voltage	VDDIO < REF or VBAT, whichever is greater		1.8		V

3.4 Electrical Characteristics

T_J = -40 °C to +105 °C; T_A = -40 °C to +85 °C (typ = 25 °C) unless otherwise noted.

3.4.1 Power Consumption

Table 6: Power Consumption Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$I_{Q\_STANDBY\_BAT}$	Quiescent current from VBAT in Standby mode	V_{BAT} = 3.6 V STANDBY mode T_J < 85 °C			15	µA
$I_{Q\_BAT\_IDLE}$	Battery supply current	Reverse Boost mode No load V_{BUS} = 0 V, V_{BAT} = 4.0 V T_J < 85 °C REV_VBUS_EN = 0x0		25	60	µA
$I_{Q\_BUS\_IDLE}$	Supply current from VBUS	V_{BUS} = 5 V V_{BAT} = 3.7 V Charger disabled I_{SYS} = 0 A Average over 1 s T_J < 85 °C			3	mA
$I_{Q\_BAT\_SHIP}$	Ship mode current from VBAT	V_{BUS} = 0 V V_{BAT} = 3.6 V T_J < 85 °C		0.1	1	µA
$I_{Q\_BUS\_HIZ}$	I_Q from VBUS	V_{BUS} = 5 V V_{BAT} = 3.6 V V_{MID} =5.2 V V_{MID} > V_{BUS} T_J < 85 °C			60	µA

3.4.2 Supervisors

Table 7: Supervisors Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{BAT\_SHRT\_THR}$	Falling threshold voltage when charge profile changes from PRE CHARGE to TRICKLE CHARGE			2		V
$V_{BAT\_SHRT\_HYS}$	Hysteresis of V_{BAT_SHRT}			0.25		V
$V_{BAT\_UV\_FALL}$	Falling threshold range of V_{BAT} under-voltage protection			2.8		V
$V_{BAT\_UV\_RISE}$	Rising threshold range of V_{BAT} under-voltage protection			3		V
$V_{BAT\_UV\_HYS}$	Hysteresis of V_{BAT_UV}			200		mV
$V_{BAT\_OV\_RISE}$	Rising threshold range of V_{BAT} over-voltage protection			4.6		V
$V_{BAT\_OV\_HYS}$	Hysteresis of V_{BAT_OV}			50		mV
$V_{SYS\_UV\_FALL}$	Falling threshold range of V_{SYS} under-voltage protection			2.7		V
$V_{SYS\_UV\_HYS}$	Hysteresis of V_{SYS_UV}			200		mV
$V_{SYS\_OV\_RISE}$	Rising threshold range of V_{SYS} over-voltage protection			4.8		V
$V_{SYS\_OV\_HYS}$	Hysteresis of V_{SYS_OV}			50		mV
T_{CRIT_TSD}	Critical temperature where the system shuts down		115	125	135	°C
T_{WARN_TSD}	Warning temperature			90		°C
T_{HYS_TSD}	Hysteresis temperature			15		°C

3.4.3 Power Path

Table 8: Power Path Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$t_{RES\_VBUS\_OV\_RISE}$	V_{BUS} over-voltage response time, rise				200	ns
$t_{D\_VBUS\_UV\_RISE}$	V_{BUS} monitoring deglitch time (applies to V_{BUS_UV})	Selected by VBUS_DEB 10, 20, 100 (default) or 200 ms	10	100	200	ms
$t_{D\_VBUS\_OV\_FALL}$	V_{BUS} over-voltage deglitch time, fall	Selected by VBUS_DEB 10, 20, 100 (default) or 200 ms	10	100	200	ms
$V_{BUS\_UV\_FALL}$	Falling threshold of V_{BUS_UV}			4		V
$V_{BUS\_UV\_RISE}$	Rising threshold of V_{BUS_UV}			4.2		V
$V_{BUS\_UV\_HYS}$	Hysteresis of V_{BUS_UV}			200		mV
$V_{BUS\_OV\_RISE\_1}$	Rising threshold range of V_{BUS} over-voltage protection	Set VBUS_OVSEL = 0x0	5.6	5.8		V
$V_{BUS\_OV\_RISE\_2}$	Rising threshold range of V_{BUS} over-voltage protection	Set VBUS_OVSEL = 0x1	6.2	6.53		V
$V_{BUS\_OV\_RISE\_3}$	Rising threshold range of V_{BUS} over-voltage protection	Set VBUS_OVSEL = 0x2	8.5	8.95		V
$V_{BUS\_OV\_RISE\_4}$	Rising threshold range of V_{BUS} over-voltage protection	Set VBUS_OVSEL = 0x3	10.5	11.05		V
$V_{BUS\_OV\_RISE\_ACC}$	Accuracy of V_{BUS_OV}		-5		5	%
$V_{BUS\_OV\_HYS}$	Hysteresis of V_{BUS_OV}			200		mV
R_{ON_VBUS}	On resistance	V_{BUS} = 5 V		40		mΩ

3.4.4 Buck-Charger

Table 9: Buck Charger Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{SYS_REG}	Buck output voltage regulation	$V_{BAT} > V_{CHG\_FAST\_THR}$		VBAT + 50 mV		V
V_{SYS_MAX}	Maximum V_{SYS} operation voltage during charging				4.6	V
$V_{SYS\_MIN\_RNG}$	Minimum buck output voltage selectable range	$V_{BAT} < V_{CHG\_FAST\_THR}$ Set by bit VSYS_MIN in 100 mV/step	3.4		3.7	V
V_{INDPM_RNG}	VINDPM threshold when the input current is reduced.	Set by bit VINDPM in 100 mV/step	3.8		4.8	V
V_{INDPM_ACC}	Accuracy VINDPM threshold		-3		3	%
I_{INDPM_RNG}	Average VBUS current limit threshold range	VBUS = 5 V	0.1	0.5	2.5	A
$I_{INDPM\_ACC\_LO}$	Accuracy of average V_{BUS} current limit threshold	$I_{BUS} \leq 0.5$ A	-60		0	mA
$I_{INDPM\_ACC\_HI}$	Accuracy of average V_{BUS} current limit threshold	$I_{BUS} > 0.5$ A	-15		0	%
f_{BUCK}	Effective buck switching frequency			2.25		MHz
$I_{OUT\_MAX\_BUCK}$	Maximum output current	V_{BUS} = 5 V V_{SYS_MIN} = 3.7 V V_{BAT} = 0 V I_{INDPM} = 2.5 A (IINDPM = 0x18) VINDPM = 0x00 (disabled)	2			A
$\eta_{BUCK\_0.01A}$	Buck Efficiency1	V_{BUS} = 5 V V_{BAT} = 4 V I_{CHG} = 0.01 A I_{SYS} = 0 A Measured from VBUS to VBAT		40		%
$\eta_{BUCK\_0.5A}$	Buck Efficiency2	V_{BUS} = 5 V V_{BAT} = 4 V I_{CHG} = 0.5 A I_{SYS} = 0 A Measured from VBUS to VBAT		92		%

Parameter	Description	Conditions	Min	Typ	Max	Unit
$\eta_{BUCK\_1.5A}$	Buck Efficiency3	V_{BUS} = 5 V V_{BAT} = 4 V I_{CHG} = 1.5 A I_{SYS} = 0 A Measured from VBUS to VBAT		89		%

3.4.5 Reverse Boost Mode

Table 10: Reverse Boost Mode Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{OUT_RBST}	V_{MID} output voltage regulation			5		V
$V_{OUT\_RBST\_RNG}$	V_{MID} output voltage regulation range in Reverse Boost mode	3.3 V < V_{IN} < 4.45 V Set by bit BOOST_VOUT in 100 mV/step	4		5.5	V
$V_{OUT\_RBST\_ACC}$	V_{MID} output voltage regulation accuracy	V_{IN} = 4 V V_{OUT} = 5 V No load	-2.5		2.5	%
$I_{OUT\_MAX\_RBST}$	Maximum output current in Reverse Boost mode	V_{IN} = 3.8 V V_{OUT} = 5 V	700			mA
$V_{OUT\_REV\_VBUS}$	VBUS voltage regulation in REV_VBUS mode	BOOST_VOUT = 0xA (5.0 V Reverse Boost output) 0 < I_{OUT_VBUS} < 0.7 A	4.7		5.15	V
f_{RBST}	Effective reverse boost switching frequency			0.9		MHz
η_{RBST_1mA}	Boost efficiency	I_{REV} = 1 mA V_{IN} = 3.8 V V_{OUT} = 5 V		90		%
η_{RBST_10mA}	Boost efficiency	I_{REV} = 10 mA V_{IN} = 3.8 V V_{OUT} = 5 V		90		%
η_{RBST_100mA}	Boost efficiency	I_{REV} = 100 mA V_{IN} = 3.8 V V_{OUT} = 5 V		90		%
$t_{STARTUP\_EN}$	Total time for reverse-boost and load switch complete start-up from EN rise edge	V_{MID} = 5.0 V C_{VMID} = 20 µF C_{LDO} = 2.2 µF V_{BAT} > 3.3 V			1	ms

3.4.6 Charger

Table 11: Charger Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{BUS\_SLEEP\_THR}$	Sleep mode threshold (Force VBAT operation)	V_{BUS} falling Value = V_{BUS} - V_{BAT}		60		mV
$V_{BUS\_SLEEP\_HYS}$	Sleep mode hysteresis	V_{BUS} rising Value = V_{BUS} - V_{BAT}		160		mV
$V_{CHG\_FAST\_THR}$	Voltage threshold when charge profile changes from PRE CHARGE to FAST CHARGE(CC)	V_{BAT} rising	3	3.1	3.2	V
$V_{CHG\_FAST\_HYS}$	Fast charge hysteresis	V_{BAT} falling		300		mV
$V_{CHG\_RCHG\_THR\_0}$	Recharge threshold	CHG_VRCHG = 0x0 (default)		100		mV
$V_{CHG\_RCHG\_THR\_1}$	Recharge threshold	CHG_VRCHG = 0x1		200		mV
I_{CHG_RNG}	Charge range with 20 mA/step		20		1500	mA
$I_{CHG\_TER\_RNG\_0}$	Charge termination smaller current threshold range with 20 mA/step Set by CHG_ITERM	CHG_RANGE_TERM = 0x1	20		40	mA
$I_{CHG\_TER\_ACC\_0}$	Charge termination current accuracy of smaller current threshold range	CHG_RANGE_TERM = 0x1	-5		5	mA
$I_{CHG\_TER\_RNG\_1}$	Charge termination larger current threshold range with 20 mA/step Set by CHG_ITERM	CHG_RANGE_TERM = 0x1	60		100	mA
$I_{CHG\_TER\_ACC\_1}$	Charge termination current accuracy of larger current threshold range	CHG_RANGE_TERM = 0x1	-25		25	%
$I_{CHG\_FAST\_0}$	Fast charge current with 20 mA/step, smaller current threshold range Set by CHG_ICHG	CHG_RANGE = 0x1 $V_{BAT} > V_{CHG\_FAST\_THR}$	80		500	mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{CHG\_FAST\_ACC\_0}$	Fast charge current accuracy of smaller current threshold range	CHG_RANGE = 0x1 $V_{BAT} > V_{CHG\_FAST\_THR}$	-8		8	%
$I_{CHG\_FAST\_1}$	Fast charge current with 20 mA/step, larger current threshold range Set by CHG_ICHG	CHG_RANGE = 0x1 $V_{BAT} > V_{CHG\_FAST\_THR}$	520		1500	mA
$I_{CHG\_FAST\_ACC\_1}$	Fast charge current accuracy of larger current threshold range	CHG_RANGE = 0x1 $V_{BAT} > V_{CHG\_FAST\_THR}$	-5		5	%
$I_{CHG\_PRE\_RNG}$	Pre-charge current range with 20 mA step	CHG_RANGE = 0x1 AND CHG_RANGE_PRE = 0x1 $V_{BAT\_SHRT\_THR} < V_{BAT} < V_{CHG\_FAST\_THR}$ CHG_IPRE_MSB = 0x0, selectable range from 0 mA to 60 mA CHG_IPRE_MSB = 0x1, selectable range from 80 mA to 140 mA	0		140	mA
$I_{CHG\_PRE\_ACC}$	Pre-charge current accuracy	CHG_RANGE_PRE = 0x1 $V_{BAT\_SHRT\_THR} < V_{BAT} < V_{CHG\_FAST\_THR}$	-10		10	%
$I_{CHG\_RNG\_SMALL}$	Charge range with 5 mA/step		5		500	mA
$I_{CHG\_TER\_RNG\_SMALL\_0}$	Charge termination smaller current threshold range with 5 mA/step Set by CHG_ITERM	CHG_RANGE_TERM = 0x0	5		10	mA
$I_{CHG\_TER\_ACC\_SMALL\_0}$	Charge termination current accuracy of smaller current threshold range	CHG_RANGE_TERM = 0x0	-5		5	mA
$I_{CHG\_TER\_RNG\_SMALL\_1}$	Charge termination larger current threshold range with 5 mA/step Set by CHG_ITERM	CHG_RANGE_TERM = 0x0	15		25	mA
$I_{CHG\_TER\_ACC\_SMALL\_1}$	Charge termination current accuracy of larger current threshold range	CHG_RANGE_TERM = 0x0	-25		25	%

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{CHG\_FAST\_SMALL\_0}$	Fast charge current with 5 mA/step, smaller current threshold range Set by CHG_ICHG	CHG_RANGE = 0x0 $V_{BAT} > V_{CHG\_FAST\_THR}$	20		125	mA
$I_{CHG\_FAST\_ACC\_SMALL\_0}$	Fast charge current accuracy of smaller curreng threshold range	CHG_RANGE = 0x0 $_{BAT} > V_{CHG\_FAST\_THR}$	-8		8	%
$I_{CHG\_FAST\_SMALL\_1}$	Fast charge current with 5 mA/step, smaller current threshold range Set by CHG_ICHG	CHG_RANGE = 0x0 $_{BAT} > V_{CHG\_FAST\_THR}$	130		500	mA
$I_{CHG\_FAST\_ACC\_SMALL\_1}$	Fast charge current accuracy of smaller current threshold range	CHG_RANGE = 0x0 $_{BAT} > V_{CHG\_FAST\_THR}$	-5		5	%
$I_{CHG\_PRE\_RNG\_SMALL}$	Pre-charge current range with 5 mA step	CHG_RANGE = 0x0 OR CHG_RANGE_PRE = 0x0 $_{BAT\_SHRT\_THR} < V_{BAT} < V_{CHG\_FAST\_THR}$ CHG_IPRE_MSB = 0x0, selectable range from 0 mA to 15 mA CHG_IPRE_MSB = 0x1, selectable range from 20 mA to 35 mA	0		35	mA
$I_{CHG\_PRE\_ACC\_SMALL}$	Pre-charge current accuracy	CHG_RANGE_PRE = 0x0 $_{BAT\_SHRT\_THR} < V_{BAT} < V_{CHG\_FAST\_THR}$	-10		10	%
I_{CHG_TRI}	Average trickle charge current Selectable by CHG_TRICKLE: (2.5 / 7 / 19 / 32) mA with CHG_TRICKLE_CYC=1 (5 / 14 / 38 / 64) mA with CHG_TRICKLE_CYC=0	$V_{BAT} < V_{BAT\_SHRT\_THR}$	2.5	2.5	32	mA
$I_{CHG\_TRI\_ACC}$	Trickle-charge current accuracy	$V_{BAT} < V_{BAT\_SHRT\_THR}$	-20		20	%
$V_{CHG\_BAT\_REG}$	Battery regulation voltage range with 10 mV step Set by CHG_VBATREG		4	4.2	4.5	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{CHG\_BAT\_REG\_ACC}$	Battery regulation voltage accuracy	0 °C < T_A < 60 °C	-0.5		0.5	%
R_{ON_BATFET}	Battery switch on resistance	V_{BAT} = 4.2 V		19	29	mΩ
I_{BAT_OCP}	Discharge current limit with maximum setting		5			A
$t_{OUT\_CHG\_TOPOFF}$	TOPOFF charging timeout Set by CHG_TOPOFF		0		60	min
$t_{DEGLITCH\_CHG\_TER}$	Termination current deglitch delay			50		ms
$t_{DEGLITCH\_RCHG}$	Re-charge deglitch delay			30		ms

3.4.7 LDOs

3.4.7.1 REFLDO

Table 12: REFLDO Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
I_{LIM_REF}	Current limit for REFLDO			70		mA
$V_{OUT\_REF\_HI}$	REF voltage	V_{BUS} = 9 V I_{REF} = 20 mA	4.75	5	5.25	V
$V_{OUT\_REF\_LO}$	REF voltage	V_{BUS} = 5 V I_{REF} = 20 mA	4.45	4.85	4.95	V
V_{REFLDO_ACC}	Accuracy of REFLDO output voltage regulation		-5		5	%

3.4.7.2 LDO1

Table 13: LDO1 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
I_{LIM_LDO1}	Current limit in LDO mode			300		mA
V_{OUT_LDO1}	LDO1 voltage output	Set by LDO1_VOUT, step size = 100 mV	1.6		5.2	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OUT\_LDO1\_ACC}$	LDO1 voltage output accuracy	V_{IN_LDO} = 5.2 V V_{OUT_LDO} = 5.0 V I_{OUT} = 1 mA to 200 mA	-3		3	%
$I_{OUT\_LD\_SW1}$	Output current for load switch mode (LDO1)		350			mA
I_{OUT_LDO1}	Output current for LDO mode (LDO1)		200			mA

3.4.7.3 LDO2

Table 14: LDO2 Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
I_{LIM_LDO2}	Current limit in LDO mode			300		mA
V_{OUT_LDO2}	LDO2 voltage output	Set by LDO2_VOUT, step size = 100 mV	1.6		5.2	V
$V_{OUT\_LDO2\_ACC}$	LDO2 voltage output accuracy	V_{IN_LDO} = 5.2 V V_{OUT_LDO} = 5.0 V I_{OUT} = 1 mA to 200 mA	-3		3	%
$I_{OUT\_LD\_SW2}$	Output current for load switch mode (LDO2)		350			mA
I_{OUT_LDO2}	Output current for LDO mode (LDO2)		200			mA

3.4.8 Battery Temperature Sensor

Table 15: Battery Temp Sensor Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{TEMP_HI}	High temperature threshold	% of REF pin voltage	14.5	15	15.2	%
V_{TEMP_WARM}	Warm threshold	% of REF pin voltage	20.1	20.5	20.8	%
V_{TEMP_COOL}	Cool threshold	% of REF pin voltage	35.4	36	36.4	%
V_{TEMP_LO}	Low temperature threshold	% of REF pin voltage	39.3	39.8	40.2	%
$V_{OFF\_TEMP\_SNS}$	Temperature sensor disable threshold	% of REF pin voltage	55		60	%
$t_{TEMP\_SNS\_DEGLITCH}$	Temperature sensor deglitch time	Temperature sensor at any threshold		10		ms

3.4.9 Hardware Reset

Table 16: Hardware Reset Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t_{PRESS}	Pressing time to enter hardware reset	Selected by RST_TMR 4, 8, 12, or 20 s	4	12	20	s
t_{PRESS_ACC}	Pressing time accuracy			1		s
t_{SHDN}	Shut down time	Selected by SYS_WAIT 1, 2, 3, or 4 s	1	2	4	s
t_{SHDN_ACC}	Shut down time accuracy			0.5		s

3.4.10 Ship Mode

Table 17: Ship Mode Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t_D	Delay time to enter Ship mode	Selected by SHIP_DLY 2, 4, 7, or 10 s	2	10	10	s
t_{EXIT_USB}	Time to exit Ship mode after USB plug-in (including debounce time)	Selected by VBUS_DEB 10, 20, 100 (default), or 200 ms		100		ms
t_{EXIT_KEY1}	Time to exit Ship mode after key press (including debounce time)	RIN_N_SHIP_EXIT_TMR = 0x0 (default)		2		s
t_{EXIT_KEY2}	Time to exit Ship mode after key press (including debounce time)	RIN_N_SHIP_EXIT_TMR = 0x1		20	50	ms

3.4.11 Watchdog

Table 18: Watchdog Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t_{PWR_OFF}	Power off time	Selectable by SYS_WAIT Step 1 s	1		4	s
t_{WD}	Watchdog time duration	Selectable by WD_TMR 40 s, 80 s, or 160 s	40	160	160	s
I_Q	Watchdog power consumption			5		µA

3.4.12 Digital Interface

Table 19: Digital I/O Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
R_{PU}	RIN_N pull-up resistor			120		kΩ
V_{IL}	Maximum input voltage level detected as logic LOW				0.54	V
V_{IH}	Minimum input voltage level detected as logic HIGH		1.26			V
$t_{DEGLITCH\_GPI\_IN}$	Deglitch time. Low / high pulse width shorter than this deglitch time is ignored.			10		µs
$V_{OL\_INT\_N}$	Output low voltage for INT_N				0.32	V
V_{OL_SDA}	Output low voltage SDA				0.32	V

3.5 Thermal Characteristics

Table 20: Package Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
$R_{TH\_JA\_A}$	Junction-to-ambient thermal resistance	JEDEC 8-layer PCB, no airflow		34		°C/W
R_{PSI_JC}	Junction-to-case (top) thermal resistance	ΔJ_T		0.5		°C/W
R_{TH_JB}	Junction-to-board thermal resistance	1 mm from IC edge		10		°C/W
$R_{TH\_JA\_B}$	Junction-to-ambient thermal resistance	25 mm x 25 mm PCB, 8-layer, no airflow		79		°C/W

4 Functional Description

4.1 Overview

In a typical application, the DA9168 manages two power inputs: a battery at VBAT and a USB supply at VBUS. The larger of these supplies feeds the system output voltage at VSYS. VSYS in turn is used as the input supply to the charger.

When USB power is present, the buck charger is active and VSYS is controlled by the buck charger. When USB power is not connected, VSYS tracks the battery voltage. The DA9168 actively manages this power path, reducing charging current and input current as necessary, and allowing VSYS to draw current from both supplies during peak loads.

The DA9168 has multiple configurable protection features including battery and input supply over current. All settings can be controlled by I^2C.

As there are two input sources, the DA9168 has multiple regions of operation, see Figure 3.

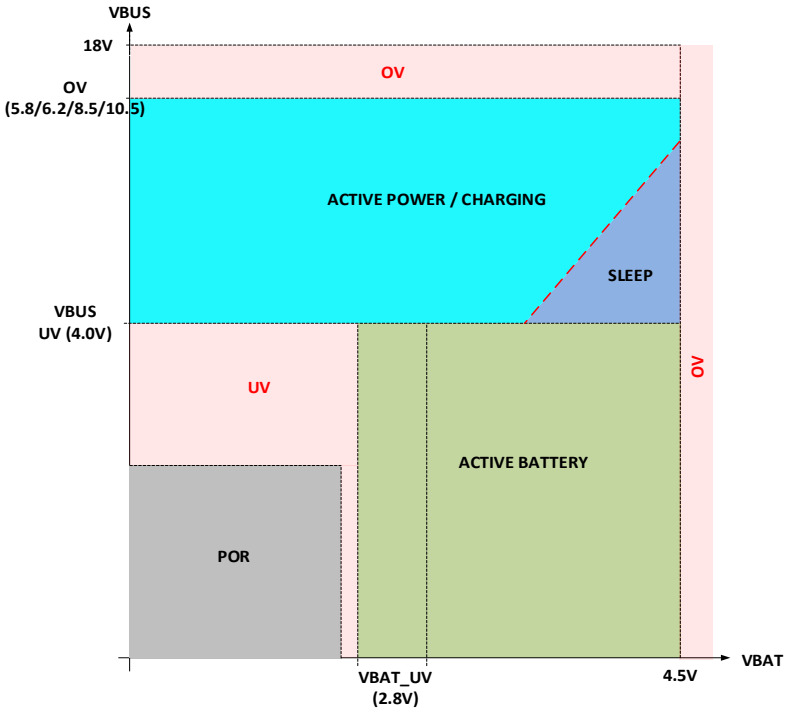


Figure 3: Regions of Operation

4.1.1 Power-On-Reset

During power-on-reset (PoR) the device powers internal bias circuits from the higher voltage of VBUS and VBAT. When V_{BUS} rises above the VBUS under-voltage threshold $V_{BUS\_UV\_RISE}$ or when V_{BAT} rises above the depletion threshold $V_{BAT\_UV\_RISE}$, the BATFET driver is active and the I^2C interface is ready for communication.

4.1.2 Active Battery Operation

When the battery is present, and the VBAT voltage is above $V_{BAT\_UV\_RISE}$, BATFET turns on and connects the battery to the system. REFLDO remains in Standby mode to minimize the quiescent current. The low R_{DS_ON} of BATFET and the low quiescent current on VBAT minimize the conduction loss and maximize the battery run time.

4.1.2.1 Ship Mode

Battery depletion can be minimized while the product sits on the shelf by placing the device into Ship mode, (an ultra-low leakage state), see Figure 4.

The device enters Ship mode when SHIP_MODE is set to 1, power source is unplugged ($V_{BUS} < V_{BUS\_UV\_FALL}$) and RIN_N pin is set to 1. There is programmable entry delay, t_D, which can be selected by SHIP_DLY bits, and disable the delay by SHIP_DLY_DIS bit.

If a power source is plugged in or the RIN_N pin is 0, entry is delayed until power is removed and the RIN_N pin is 1. In Ship mode, the entire device is in a low-leakage state, drawing only 1 µA (max).

To exit Ship mode, apply a valid power source ($V_{BUS} > V_{BUS\_UV\_RISE}$) or toggle RIN_N low for more than the programmable delay time of either t_{EXIT_KEY1} or t_{EXIT_KEY2}.

- Ship mode: $I_Q < 1$ µA
  - No I^2C access

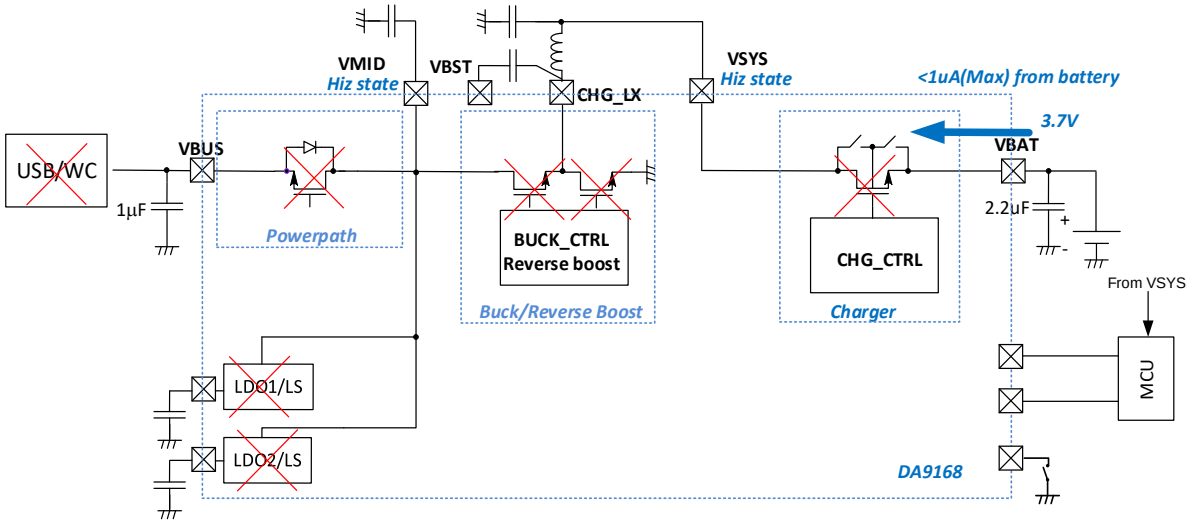


Figure 4: Ship Mode

The default delay time is t_{EXIT_KEY1}, (2 s, typical). If a quicker exit time from Ship mode (by using the RIN_N key) is required, the delay time can be set to t_{EXIT_KEY2} (20 ms, typical) by writing to bit RIN_N_SHIP_EXIT_TMR before entering Ship mode.

After configuring the delay time to t_{EXIT_KEY2} and entering Ship mode, the delay time remains set to t_{EXIT_KEY2} until Ship mode is exited. After Ship mode is exited, RIN_N_SHIP_EXIT_TMR resets to the OTP set time, t_{EXIT_KEY1}. It can be re-configured again to t_{EXIT_KEY2} ready for the next entry into Ship mode if required.

4.1.2.2 Standby Mode

When only the battery is powering the system and there is no load, the device enters Standby mode. In this mode BATFET turns on, see Figure 5.

- Standby mode with enabled Watchdog: I_Q < 15 µA

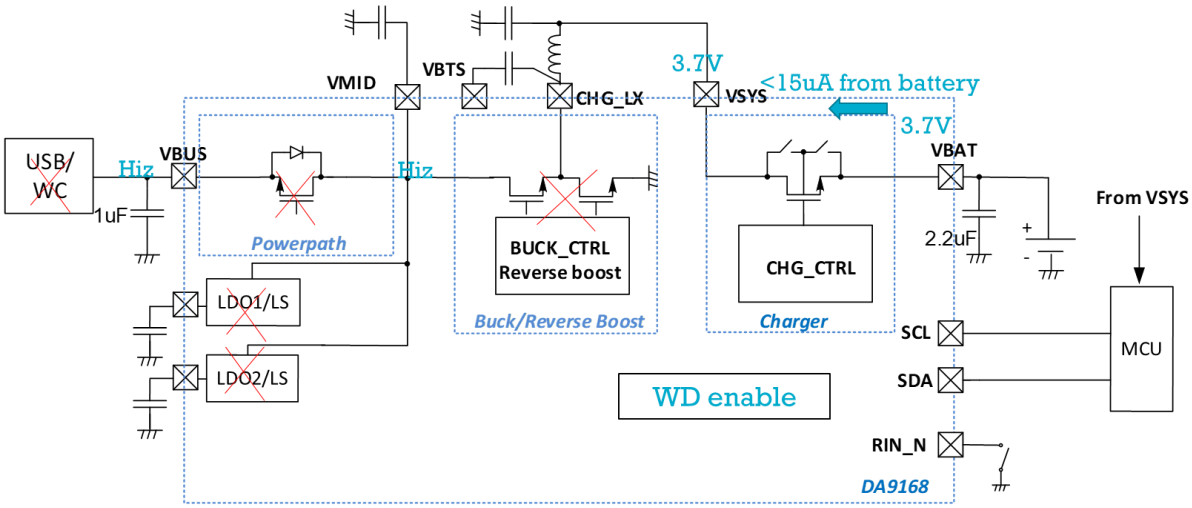


Figure 5: Standby Mode

4.1.2.3 Reverse Boost Mode

Reverse Boost mode is enabled by EN pin, see Figure 6. In this mode, the device regulates the VMID voltage between 4.0 V and 5.5 V (it is recommended that VMID voltage setting is set to 0.5 V higher than Reverse-Boost input, VBAT) and the two low-power LDOs are enabled. When an over-voltage event occurs at VMID, the device stops the reverse boost converter to protect accessory devices that are connected to the LDOs' outputs.

- Reverse boost converter and both LDOs enabled (no load) with enabled Watchdog: I_Q < 60 µA

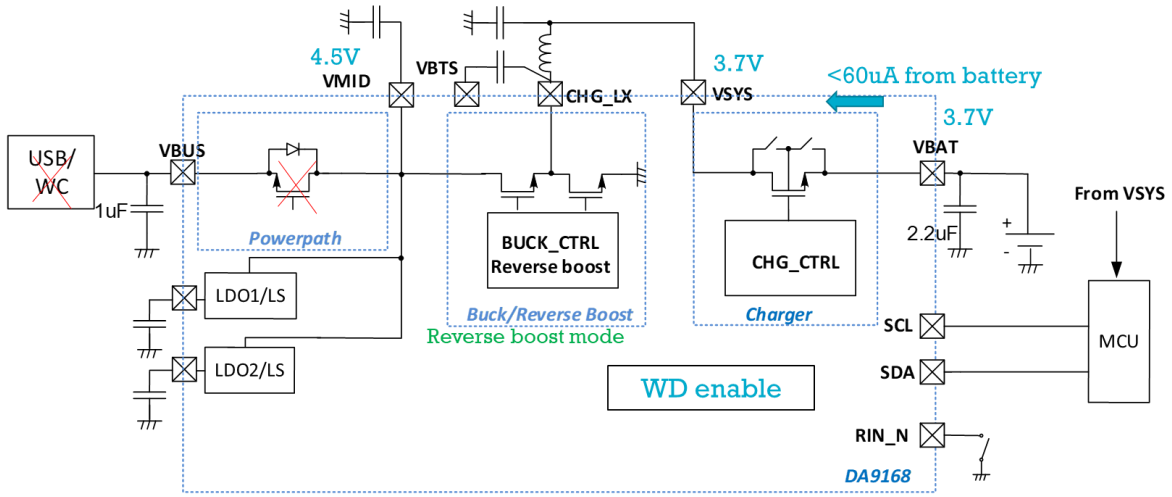


Figure 6: Reverse Boost Mode

In Reverse Boost mode, to turn on the power path and enable the Boost supply from VBUS, set REV_VBUS_EN = 0x1. The VBUS voltage depends on the Reverse Boost output setting and accuracy, and the IR-drop on the power path.

4.1.3 Active Power Operation

During USB-powered (Active Power) operation, when an input source is plugged in the device checks the input source voltage to turn on REFLDO and all the bias circuits. It detects and sets the input current limit (IINDPM) and input voltage limit (VINDPM) before the buck charger is started.

4.1.3.1 Powering Up REFLDO

The REFLDO supplies internal bias circuits as well as high-side and low-side FET gate drive. The REFLDO also provides bias to TMP_SNS external resistors. The REFLDO is enabled when the following conditions are valid:

1. $V_{BUS} > V_{BUS\_UV\_RISE}$
2. $V_{BUS} > V_{BAT} + V_{BUS\_SLEEP\_HYS}$ in Buck mode.
3. $V_{BUS} < V_{BAT} + V_{BUS\_SLEEP\_THR}$ in Reverse Boost mode.

4.1.3.2 Charge

When the charge function is available, VMID is supplied from VBUS and VSYS is regulated from VMID by the buck charger. Since VSYS is regulated by the buck charger, VSYS = VBAT +50 mV to maximize efficiency.

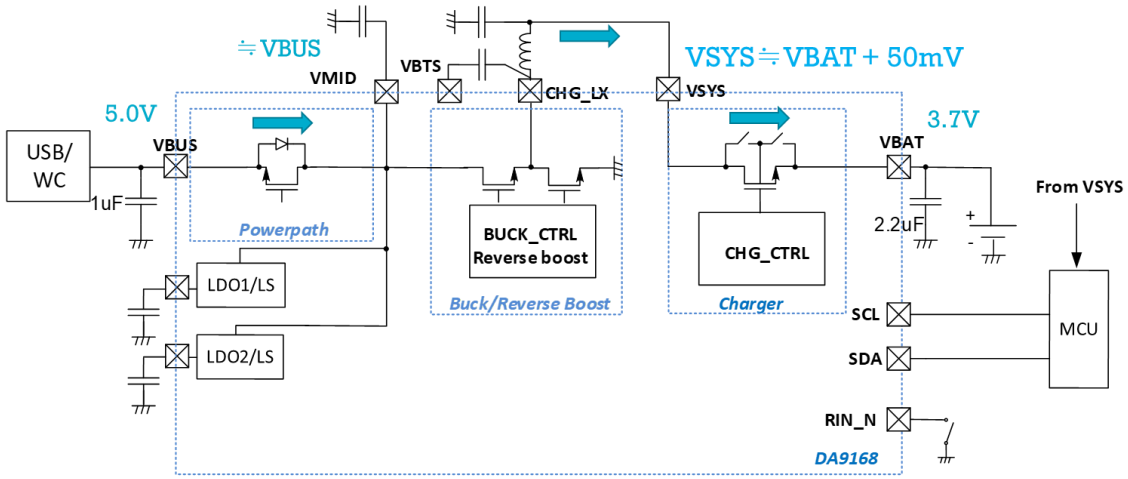


Figure 7: Active Power (Charge Case)

4.1.3.3 High Impedance Mode

In High Impedance (Hi-Z) mode the battery supplies the system power even if there is a VBUS power source, see Figure 8. This mode minimizes power consumption from VBUS to less than 60 µA and the device operates in the same way as in Active Battery operation. VMID voltage should be regulated by Reverse-Boost. However, if the VBUS voltage is higher than the VMID voltage, by enough margin, VBUS will charge to VMID through a body diode in the power path, instead of Reverse-Boost. In this case, VBUS instead of VBAT will contribute to the quiescent current.

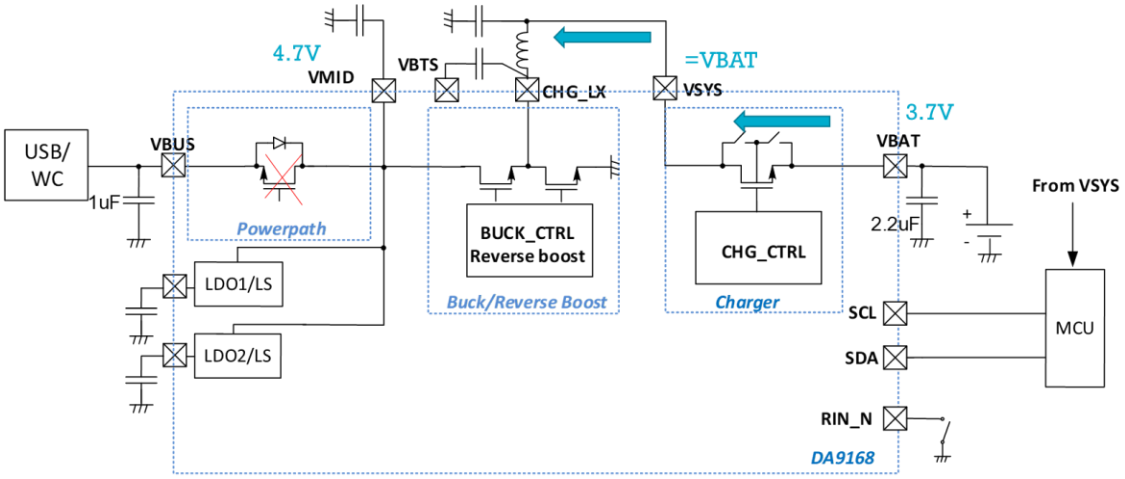


Figure 8: Hi-Z Mode

4.2 Battery Protection

The DA9168 includes battery protection. The battery is protected during discharge by the OC and UV functions. During charging, the battery voltage is sensed by VBAT_SNS to prevent battery over-voltage and the temperature sense (TMP_SNS) function protects against over-temperature, see Section 4.2.3. Highly accurate voltage regulation and charging current control prevent OV and OC conditions.

4.2.1 E_VBAT_UV Event

$V_{BAT\_UV\_FALL}$ protects the battery from over-discharge by disconnecting the discharge path when the battery voltage falls below the UV threshold.

When an E_VBAT_UV event occurs during active battery operation (VBUS not connected) the DA9168 outputs, including VSYS, shut down and all registers are reset to their default OTP values.

An E_VBAT_UV event generates an interrupt at INT_N.

4.2.2 E_VBAT_OV Event

The battery over-voltage threshold is $V_{BAT\_OV\_RISE}$. . When battery over-voltage occurs, $V_{BAT} > V_{BAT\_OV\_RISE}$, the charger device immediately stops switching and an event, E_VBAT_OV, is flag by an interrupt at INT_N.

During active batter operation, E_VBAT_OV event cause VSYS shut down. The VBAT_OV_CFG bit can mask the VBAT_OV caused shutdown behavior. In this case, VSYS still may shut down if $V_{BAT} = V_{SYS} > V_{SYS\_OV\_RISE}$

4.2.3 Battery Temperature Sensing

The temperature sense function uses the battery's NTC thermistor to monitor battery temperature, see Section 4.2.4. If the battery is too cold or hot, the fast charge current, or target voltage, is reduced or charging move to Halt status. Table 21 summarizes which protective measures will be applied in each temperature range.

Table 21: Battery Thermal Protection Measures

Temperature Range	Voltage at TMP_SNS	Charger Action	Interrupt Name
$T_{BAT} < T_{LO}$	$V_{TMP\_SNS} > V_{TEMP\_LO}$	Charging halt, device enters ship mode	E_TS COLD
$T_{LO} < T_{BAT} < T_{COOL}$	$V_{TEMP\_LO} > V_{TMP\_SNS} > V_{TEMP\_COOL}$	Charge current, I_{CHG} = TS_ICHG	E_TS COOL
$T_{COOL} < T_{BAT} < T_{WARM}$	$V_{TEMP\_COOL} > V_{TMP\_SNS} > V_{TEMP\_WARM}$	Normal charging	
$T_{WARM} < T_{BAT} < T_{HI}$	$V_{TEMP\_WARM} > V_{TMP\_SNS} > V_{TEMP\_HI}$	Target voltage V_{BAT_REG} (set by CHG_VBATREG) reduced by 100 mV or 200 mV (set by TS_VBATREG_SHIFT)	E_TS WARM
$T_{HI} < T_{BAT}$	$V_{TMP\_SNS} < V_{TEMP\_HI}$	Charging halt, device enters ship mode	E_TS HOT
	$V_{TEMP\_SNS} > V_{OFF\_TEMP\_SNS}$	Temperature sense disabled, optional fault	E_TS OFF

Charge status will move to Halt status when the junction temperature is above the warning level, T_{WARN_TSD}, see Section 3.4.2. An E_TSD_WARN event is observed (E_TSD_CRIT is system shut down), see Section 4.8.

4.2.4 TMP_SNS Pin Resistor Network

The four temperature thresholds, V_{TEMP_LO}, V_{TEMP_COOL}, V_{TEMP_WARM}, and V_{TEMP_HI} are fixed percentages of the voltage on the REF pin, see Section 3.4.8. The REF pin allows the battery temperature to be monitored through the resistor divider. V_{REF} is derived from the VMID voltage.

The TMP_SNS voltage is measured after a deglitch time of 10 ms, which precludes any need for filtering at TMP_SNS. To avoid measurement error, no filter capacitance larger than 10 nF should be added to TMP_SNS pin.

Temperature monitoring can be disabled (TS_OFF state) by the BTS_VBAT_EN and BTS_VBUS_EN bits, or by pulling TMP_SNS above the $V_{OFF\_TEMP\_SNS}$ threshold. The TS_OFF state disables temperature sensing and can optionally be flagged as a fault condition by setting bit E_TS_OFF to 1. When TMP_SNS is pulled high to enter TS_OFF, the off state is latched until TMP_SNS is disabled.

Each temperature sense threshold breach will generate an interrupt at INT_N.

The battery NTC interfaces to the TMP_SNS input through a resistive divider, see Figure 9.

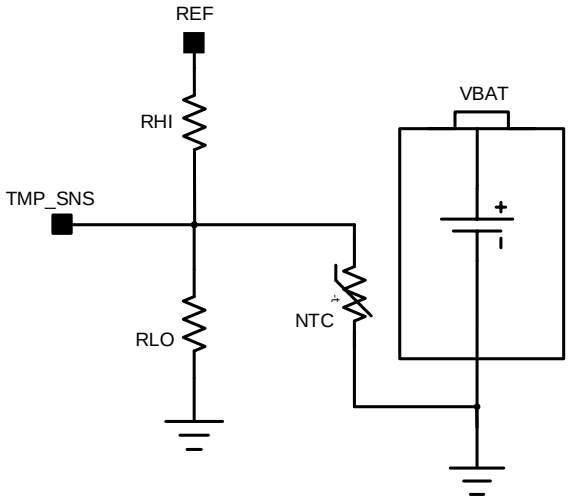


Figure 9: Battery Temperature Sensing with NTC

The resistor divider values (R_{HI} and R_{LO}) are selected as shown below so that the cold and hot TMP_SNS thresholds are reached at the corresponding NTC values.

Equation 1:

$$R_{(LO)} = \frac{R_{(COLD)} \times R_{(HOT)} \times \left(\frac{1}{0.398} - \frac{1}{0.15}\right)}{R_{(HOT)} \times \left(\frac{1}{0.15} - 1\right) - R_{(COLD)} \times \left(\frac{1}{0.398} - 1\right)}$$

Equation 2:

$$R_{(HI)} = \frac{\left(\frac{1}{0.398} - 1\right)}{\left(\frac{1}{R_{(LO)}} + \frac{1}{R_{(COLD)}}\right)}$$

Where:

- $R_{(HOT)}$ = the NTC resistance at the hot temperature, T_{HI}
- $R_{(COLD)}$ = the NTC resistance at the cold temperature, T_{LO}

4.3 Dynamic Power Management

The DA9168 continuously monitors input current and input voltage. When input source is overloaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the IINDPM or the input voltage rises above the VINDPM.

However, if the charge current is reduced to zero, the input source is still overloaded, then the system voltage starts to drop. Once the system voltage falls below the battery voltage (V_{SYS}<V_{BAT}), the device automatically enters the Supplement mode.

In Supplement mode, BATFET turns on and the battery starts discharging so that the system is supported from both the input source and battery.

4.3.1 VINDPM Threshold

Fixed dynamic power management input voltage (VINDPM) threshold. The default VINDPM threshold is 4.2 V (programmable from 3.8 V to 4.8 V by VINDPM bit).

4.4 Charging Operation

4.4.1 Battery Charging Process

When USB power is connected, (V_{BUS} > $V_{BUS\_UV\_RISE}$), the DA9168 is in one of four states, see Table 22. Charging is enabled and disabled with the CHG_EN_N pin and CHG_EN bit. This status is indicated by the PMC_STATUS_03 register.

Table 22: Charge Status

CHG_EN_N	CHG_EN	ICHG	VBAT	Status
H	*	N/A	N/A	Charge disabled
*	L	N/A	N/A	Charge disabled
L	H	> CHG_ITERM	≤ CHG_VBATREG	Charge in-progress
L	H	< CHG_ITERM	> CHG_VRCHG	Charge done

PMC_STATUS_03 is a read-only register which shows immediate charge status. The register does not hold status value and changes its value immediately when the charge status changes.

From the charge ready state, charging begins when the CHG_EN bit is high, and the CHG_EN_N input pin is pulled low.

The device charges the battery in three phases based on battery voltage: pre-charge, fast charge constant current (CC), and constant voltage (CV). These charge phases and status transitioning from the **charge ready** to **charge in progress** to **charge done** are shown in the typical charging profile in Figure 10.

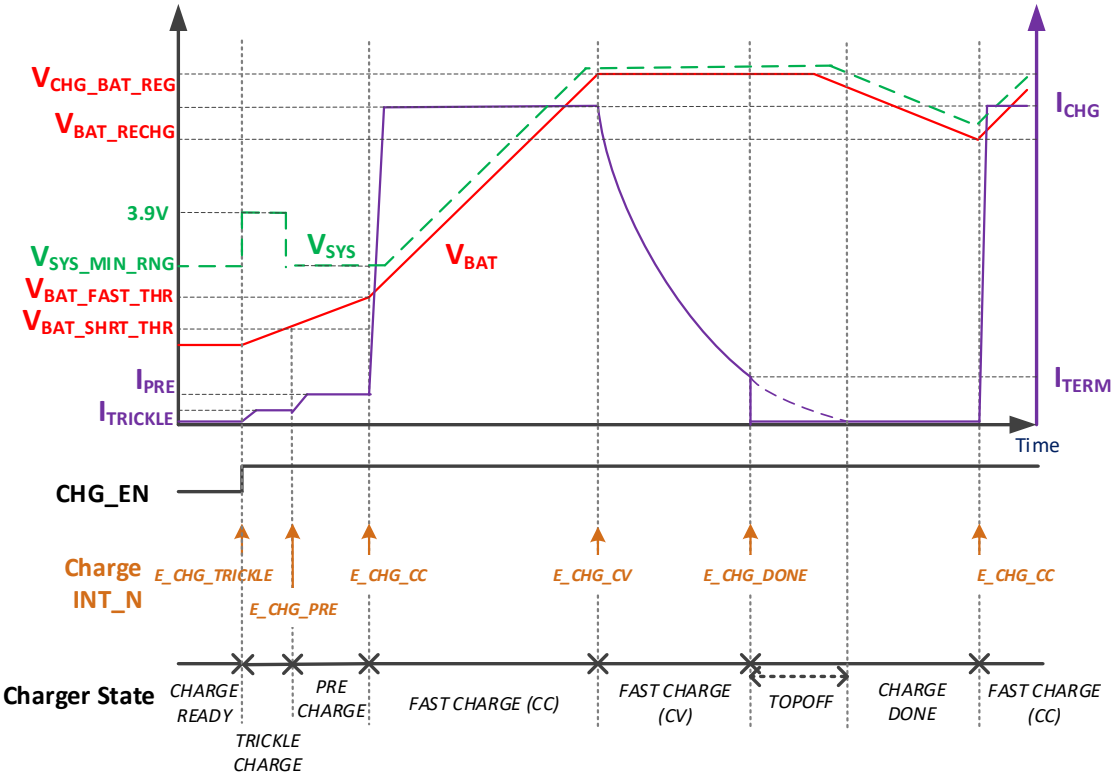


Figure 10: Charger Profile, State, and INT_N (Event)

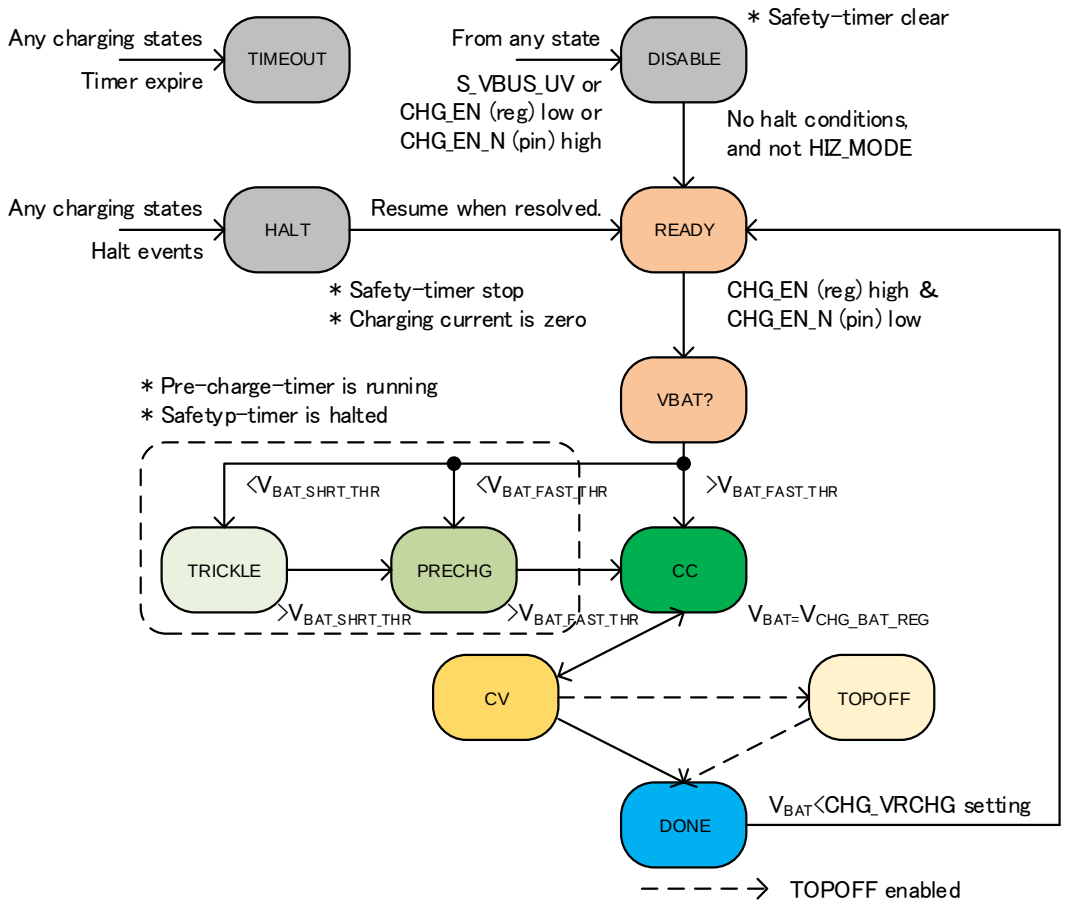


Figure 11: Charger Control, State

4.4.2 Trickle and Pre-Charge Low-Level Currents in Pre-Charge Mode

In Pre-Charge mode a constant low-level current is supplied to the battery.

- When V_{BAT} < 2.2 V, the low-level current is called the trickle charge current. Continuous operation mode and periodic operation mode can be selected by the CHG_TRICKLE_CYC bit. And trickle charge current setting is also selectable by the CHG_TRICKLE bits. The default setting is periodic operation mode with 5mA setting, means 2.5mA average trickle charge current, see Figure 12.

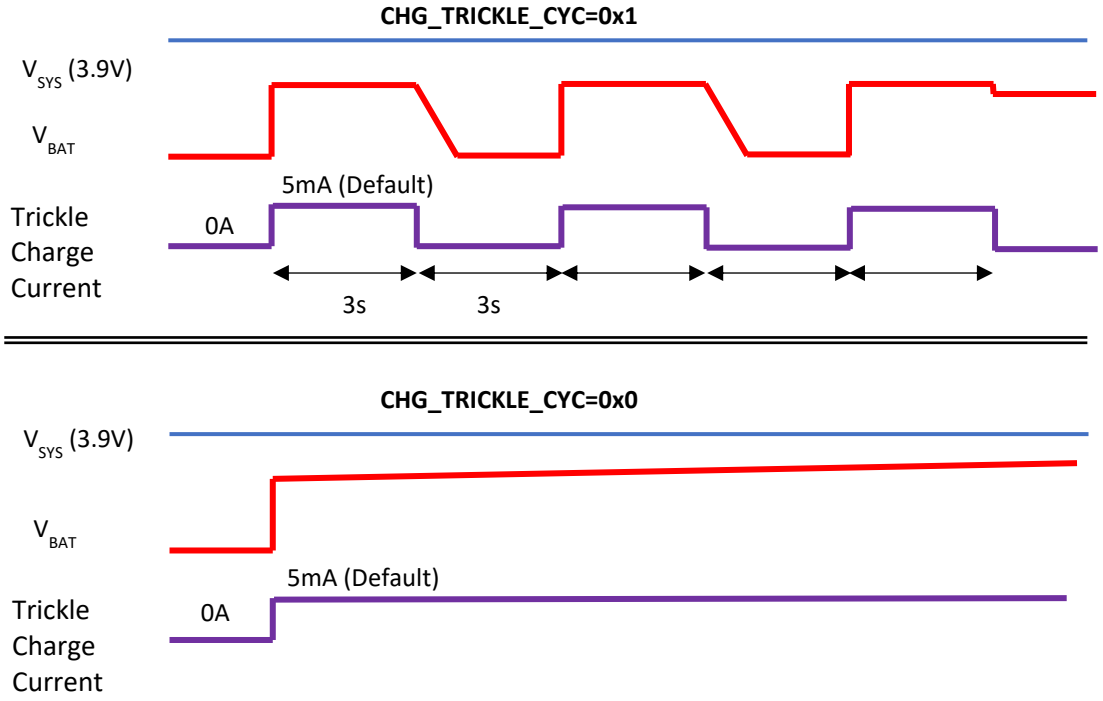


Figure 12: Trickle Charge Behavior

- When V_{BAT} > 2.2 V, the low-level current is called the pre-charge current. The maximum pre-charge current is140 mA.

Pre-charging is indicated by an INT_N interrupt and E_CHG_PRE.

4.4.3 Fast Charge Mode

Fast Charge mode can be split into two modes, Constant-Current (CC) mode, and Constant-Voltage (CV) mode.

4.4.3.1 CC Mode

In Constant-Current (CC) mode, a constant charging current is supplied to the battery. Charge current is selectable by the CHG_ICHG registers. When V_{BAT} reaches V_{BAT_REG} (set by CHG_VBATREG), the device ends Fast Charge mode and starts Constant Voltage mode operation.

4.4.3.2 CV Mode

Constant Voltage (CV) mode begins when the battery voltage rises into the regulation range. The regulated battery voltage, V_{BAT_REG}, is set by the CHG_VBATREG bits.

When the DA9168 enters CV mode, the charge current begins to decrease gradually, while the battery voltage remains regulated at V_{BAT_REG}. When the charge current decreases to the termination current level, charging is terminated and the charge status (PMIC_STATUS_03 register) changes to Charge Done.

Charge Done is indicated by an INT_N interrupt and E_CHG_DONE

After Charge Done, the charger can maintain CV mode charging behavior until the top off timer expires. The top off timer time is selected by bits CHG_TOPOFF and can be disabled by setting CHG_TOPOFF = 0x0.

4.4.4 Charge Halt

The DA9168 identifies multiple conditions to adjust or halt charging, indicated by the status bits. These conditions may reduce the charge current, reduce the target battery voltage, or take other actions. All are indicated by an interrupt and event bits.

When the charger is unable to provide the programmed charge current to the battery, such as when VBUS is in current limit, the termination current is ignored, CV charging continues until the charge current reaches 0 mA. Charge state remains as CV until the safety timer expires.

The system status affecting charge operation are summarized in Table 23. Also, by setting HIZ_MODE charging is halted and safety timers are stopped.

Table 23: System Status Affecting Charging

Status bits	Safety Timer	Charging Events
S_VBUS_UV	Cleared	Charging is disabled
S_VBUS_OV	Stopped	Charging is halted
S_VBUS_VINDPM	Half-rate (optional)	Charging is resumed
S_VBUS_IINDPM	Half-rate (optional)	Charging is resumed
S_VBAT_OV	Stopped	Charging is halted
S_VSYS_OV	Stopped	Charging is halted
S_CHG_SLEEP	Stopped	Charging is halted
S_CHG_SPLMT	Stopped	Charging is halted
S_TS_COLD	Stopped	Charging is halted. Device enters ship mode.
S_TS_HOT	Stopped	Charging is halted. Device enters ship mode.
S_TS_COOL	Half-rate (optional)	Charging is resumed. Charge current is optionally changed by TS_ICHG. Option enabled by CHG_TS_COOL_I.
S_TS_WARM	Half-rate (optional)	Charging is resumed. VBAT regulation voltage is optionally shifted by TS_VBATREG_SHIFT. Option enabled by CHG_TS_WARM_V.
S_CHG_TIMER	Cleared	Charging is latched-off. In order to re-start charging, it is required to disable charging first by unplugging VBUS, or setting bit CHG_EN = 0x0, or be connecting the CHG_EN_N input pin high.
S_WD_TIMER	Stopped	Charging is halted
S_TSD_WARN	Stopped	Charging is halted
S_TSD_CRIT	Stopped	Charging is halted
S_VSYS_OV	Stopped	Charging is halted

4.4.5 Power Cycling

The power-cycle function causes VSYS drop then restarts. Power-cycle can be initiated by a fault condition, RIN_N pushbutton or I2C command. The primary purpose of power-cycling is to clear a serious fault condition such as IC over-temperature or to reset the host.

A wait timer allows the host to act before power is shut down and can be set between 1 s and 4 s. The timer is programmable at register SYS_WAIT. The SYS_WAIT_CFG bit can shorten the timer as 1/10 of the default values.

4.4.6 Safety Timers

The safety timer starts counting as soon as a charge cycle begins, ensuring that the charge cycle is terminated even if the battery fails to reach the termination condition. There are two dedicated timers, one for pre-charge and another for the main timer. If the safety timers expire before charging is terminated, INT_N toggles.

The pre-charge timer counts during Pre-charge mode and is reset at the transition to Fast Charge mode. If the charger is still in Pre-Charge mode at the end of the pre-charge timer period, the charge cycle is terminated. The main safety timer stops in Pre-Charge mode and runs during Fast-Charge mode.

Table 24. Safety Timer Register Settings

CHG_TMR_SAFE and CHG_TMR_PRE	Main Charge Timer (h)	Pre-Charge Timer (min)
0x0	5	30
0x1	10	60
0x2	15	90
0x3	20	120

4.4.7 VMID OV

In active battery operation, when VMID rises above the VMID_OV threshold the reverse boost and the two LDOs will be latched-off.

This will create an E_VMID_OV event, and generate an interrupt on INT_N.

4.4.8 SLEEP

When VBUS - VBAT falls below $V_{BUS\_SLEEP\_THR}$ (i.e. when VBUS falls to within $V_{BUS\_SLEEP\_THR}$ of VBAT) the system enters SLEEP mode.

In this situation the system operation will change to active battery mode and charging will be halted.

This will create an E_CHG_SLEEP event, and generate an interrupt on INT_N.

To exit SLEEP mode, VBUS – VBAT must rise above $V_{BUS\_SLEEP\_HYS}$ (that is, VBUS rises at least $V_{BUS\_SLEEP\_THR}$ above VBAT).

4.4.9 SPLMT

As noted in section 4.3, the SPLMT mode will be entered when VSYS falls below VBAT due to pulling a load on VSYS that exceeds the IINDPM threshold.

In this situation the BATFET will automatically by turned on and allow the load current on VSYS to be simultaneously be supplied from VBUS and VBAT. This ensures larger currents can be sustained on VSYS above that which can be provided from VBUS alone and will prevent shutdown of VSYS.

This will create an E_CHG_SPLMT event, and generate an interrupt on INT_N.

4.4.10 TS_HOT / TS_COLD

When the battery temperature is detected to be above the TS_HOT threshold, or below the TS_COLD threshold using the battery temperature sensing block (see section 4.2.3), the device will enter ship mode (see section 4.1.2.1).

This will create an E_TS_HOT / E_TS_COLD event, and generate an interrupt on INT_N.

4.4.11 TS_COOL

When the battery temperature is detected to be below the TS_COLD threshold using the battery temperature sensing block (see section 4.2.3), there is an option to change the charge current using the TS_ICHG setting (register 0x1C). To enable this option set CHG_TS_COOL_I = 1 (register 0x1B).

During TS_COOL there is also an option to change to the safety timer to half-rate. This can be enabled by setting both CHG_TMR_HALF_EN = 1 (register 0x16) and CHG_TS_COOL_I = 1 (register 0x1B).

This will create an E_TS_COOL event, and generate an interrupt on INT_N.

4.4.12 TS_WARM

When the battery temperature is detected to be above the TS_WARM threshold using the battery temperature sensing block (see section 4.2.3), there is an option to change the battery regulation voltage by the amount specified in TS_VBATREG_SHIFT (register 0x1B). To enable this option set CHG_TS_WARM_V = 1 (also in register 0x1B).

If TS_VBATREF_SHIFT = 0, the battery regulation voltage is reduced by 100mV.

If TS_VBATREF_SHIFT = 1, the battery regulation voltage is reduced by 200mV.

During TS_WARM there is also an option to change to the safety timer to half-rate. This can be enabled by setting both CHG_TMR_HALF_EN = 1 (register 0x16) and CHG_TS_WARM_V = 1 (register 0x1B).

This will create an E_TS_WARM event, and generate an interrupt on INT_N.

4.4.13 LDO1 / LDO2 OC

When current larger than the ILIM_LDO1 (ILIM_LDO2) threshold is pulled from VOUT1 (VOUT2) then LDO1 (LDO2) is shutdown. It will then automatically restart after 10ms. If the fault still exists then LDO1 (LDO2) will shut down again, and this hiccup operation will continue until the fault is removed.

The LDO1 OCP (LDO2 OCP) can be disabled via the LDO1_OCP (LDO2_OCP) settings in register 0x1D.

This will create an E_LDO1_OC (E_LDO2_OC) event, and generate an interrupt on INT_N.

4.4.14 REF OC

When current larger than the ILIM_REF threshold is pulled from REFLDO, the reverse boost and the two LDOs will be latched-off.

This will create an E_REF_OC event, and generate an interrupt on INT_N.

4.5 LDOs / Load Switches

The DA9168 has two LDOs which are powered by VMID. Each LDO is configurable as either a load switch or an LDO. The LDO can deliver 200 mA and the load switch can deliver 350 mA.

In LDO mode, the output voltage for either LDO is programmable between 1.6 V and 5.2 V in 100 mV steps. Due to lower load capability with lower headroom, to ensure good regulation and full load capability, 200 mV or 300 mV of headroom is recommended at VLDO (VMID)

Each LDO is enabled and configured as load switch at register PMC_LDO_00. The output voltages are set at registers PMC_LDO_01 and PMC_LDO_02.

4.6 Host and Push Button Communication

The DA9168 features multiple digital pins for host and user communication, see Table 25. For connections, see Figure 13.

When the RIN_N pin is driven to logic low for t_{PRESS}, the BATFET reset process starts. The BATFET is turned off for t_{SHDN} and then it is re-enabled to reset system.

Table 25: Digital Pins for Host and Pushbutton Interface

Pin Name	Description
SCL / SDA	I^2C interface
RIN_N	Pushbutton interface Used for system reset or Ship mode exit.
INT_N	Interrupt output flag
EN	Enable reverse boost and LDOs

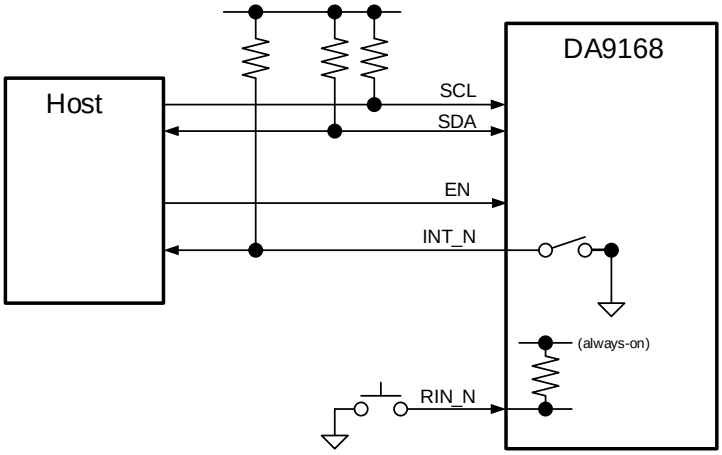


Figure 13: Digital Pin Connections

4.6.1 EN Pin Behavior

The EN pin is used for enabling Reverse Boost mode and both LDO/load switches.

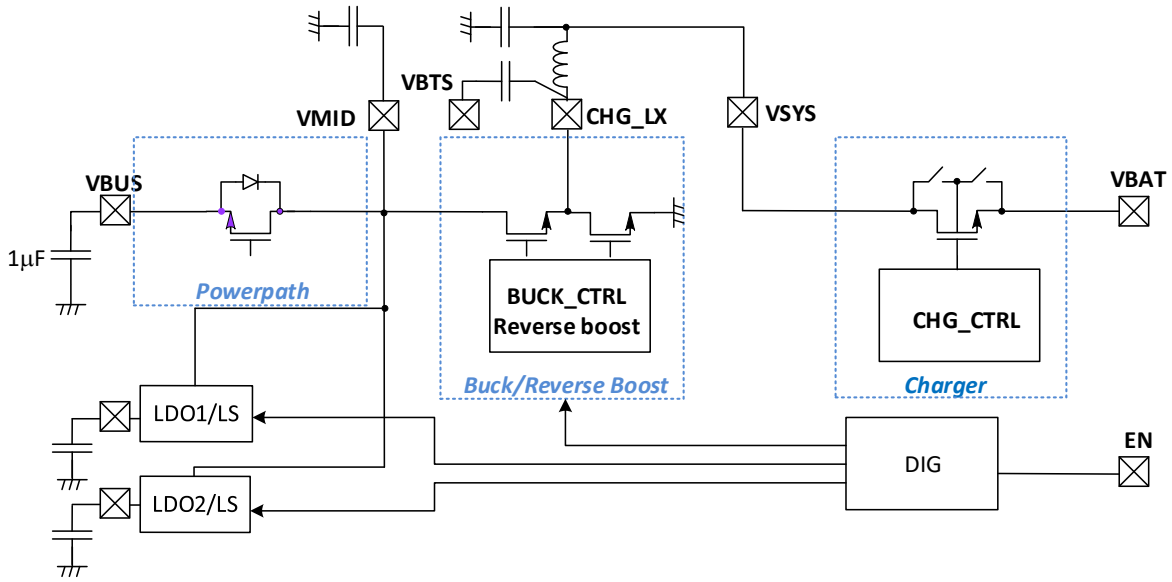


Figure 14: EN Pin Example

The EN pin is edge-triggered. A rising edge triggers an internal digital sequence which writes to BOOST_EN, LDO1_EN, and LDO2_EN high (selectively enabled and disabled by SEQ_BOOST).A falling edge immediately clears BOOST_EN, LDO1_EN, and LDO2_EN low (again, by the internal digital sequence, selectively).

LDO1 and LDO2 are enabled when LDO1_EN and LDO2_EN are high and VMID is available.

BOOST is enabled when BOOST_EN is high and VSYS is supplied from VBAT.

4.6.2 INT_N Pin Behavior

The INT_N output indicates interrupt events with a 256 µs pulse. The INT_N flag can be masked for each individual interrupt event by setting the corresponding mask bit to1. Event register fields can be found in PMC_EVENT_00 to PMC_EVENT_04, and corresponding INT_N mask bits in PMC_MASK_00 to PMC_MASK_04.

Event registers are configured as clear-on-read by default. They are set as soon as the corresponding event is detected and cleared as soon as they are read by I^2C. If E_RD_CLR_DIS is set, then the event registers behaves as clear-on-write 1.

Corresponding raw status bits are located in registers PMC_STATUS_00 to PMC_STATUS_04. Current status of the reported event can be checked by these registers.

4.6.3 RIN_N Behavior

When the Reset button, RIN_N, is pressed for longer than a set time, t_{PRESS}, VSYS power off till release RIN_N and wait a VSYS shutdown time, t_{SHDN}, the registers and VSYS reset.

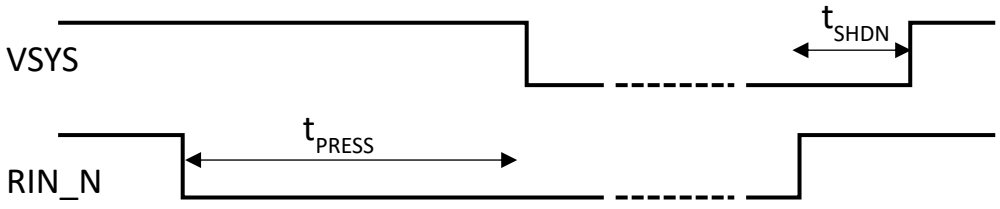


Figure 15: RIN_N reset Registers and VSYS

The press time, t_{PRESS}, and the VSYS shutdown times are programmable.

- The RIN_N button press time, $t_{PRESS,}$ is set by RST_TMR to (4, 8, 12, or 20) s, with a default of 12 s. It has an accuracy of ±1 s.
- The VSYS shutdown time, t_{SHDN}, is set by SYS_WAIT to (1, 2, 3, or 4) s, with a default of 2 s. It has an accuracy of ±0.5 s. This setting is common for *all* VSYS supplied features (for example, Watchdog).

RIN_N behavior can be masked by setting RST_OPT=0x0 and RST_OPT_PWRCYC=0x0 at the same time.

4.7 I²C Communication

The DA9168 includes an I²C-compatible 2-wire serial interface to access the internal registers. Through the I²C interface, the host processor can control each channel and read back system status. The DA9168 only operates as a slave device.

The host processor provides the serial clock at the SCL pin. The DA9168 supports I²C standard-mode (100 kHz) and up to 400 kHz fast-mode.

The DA9168 SLAVE address is 0x68.

The I²C data pin, SDA, is open drain, allowing multiple devices to share a communication line.

All transmissions begin with a START condition issued from the master while the bus is in an IDLE state (the bus is free). The START condition is initiated by a high to low transition on the SDA line while the SCL is in the high state. Alternately, a STOP condition is indicated by a low to high transition on the SDA line while the SCL line is in the high state as shown in Figure 16.

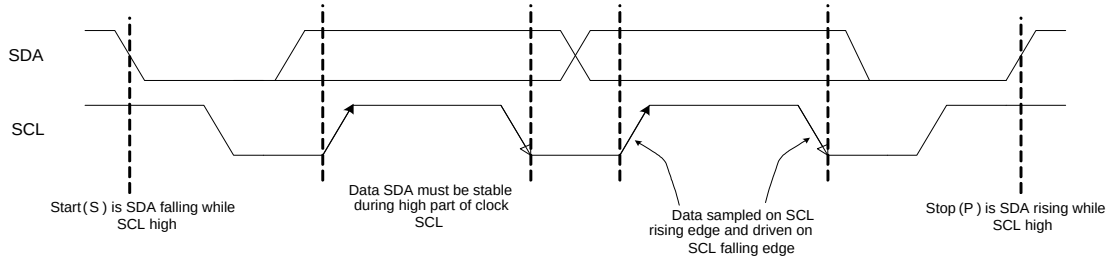


Figure 16: I²C Start (S) and Stop (P)

The I²C interface uses a two-byte serial protocol containing one byte for address and one byte for data. The data and address are transferred with MSB transmitted first for both read and write operations.

The DA9168 monitors the serial bus for a valid SLAVE address whenever the interface is enabled. When it receives its own slave address, the DA9168 immediately gives an Acknowledge signal to the host by pulling the SDA line low during the following clock cycle. A Not Acknowledge signal is given by the logic 1, not pulling down the SDA line.

A single byte WRITE is shown in Figure 17. Here the slave address is followed by a WRITE bit (low), the register address, and the WRITE data. Finally, the transaction is terminated with a STOP.

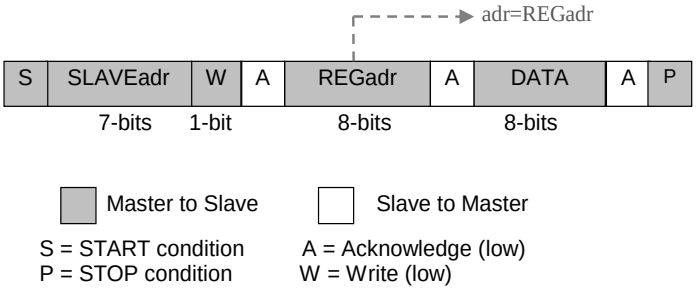


Figure 17: Single Write Command

The DA9168 also supports multiple byte writes, shown in Figure 18. By not sending the STOP command, data is written to consecutive addresses.

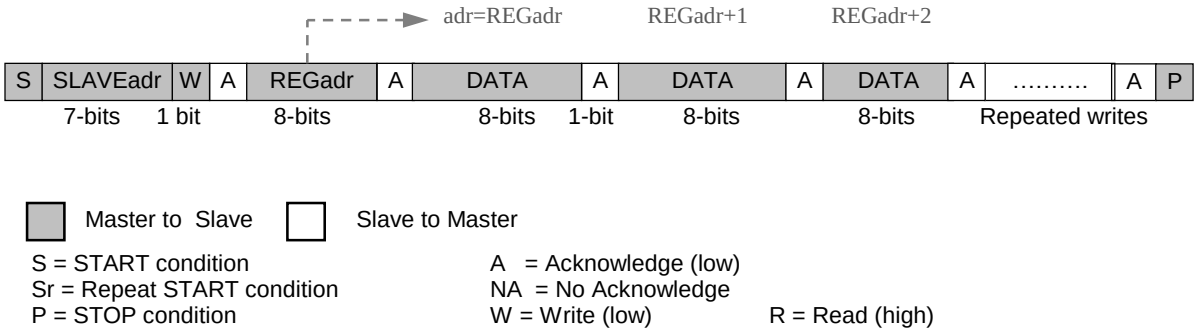


Figure 18: Consecutive Write Command

The data READ protocol is different in that a READ does not have a register address immediately preceding it. To READ from a specific address, the register address is given by using a write command followed by a Repeated START. A single byte READ is shown in Figure 19. A Repeated START is followed by the slave address and a READ bit. After the READ data is returned to the host, the host then responds with a Not Acknowledge and a STOP.

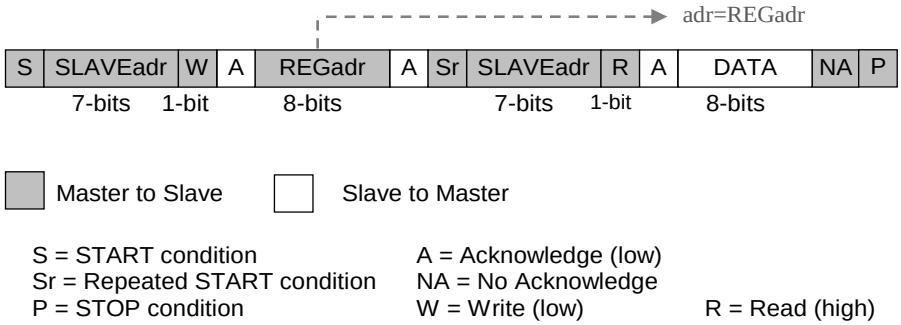


Figure 19: Single Read Command

The DA9168 also supports a multiple byte READ protocol. If the host responds to the returned data with an Acknowledge rather than Not Acknowledge and STOP, data will be read from sequential addresses until a Not Acknowledge and STOP command is given, as shown in Figure 20. If a READ address is given with a WRITE and Repeated START, consecutive addresses are read from the WRITE address.

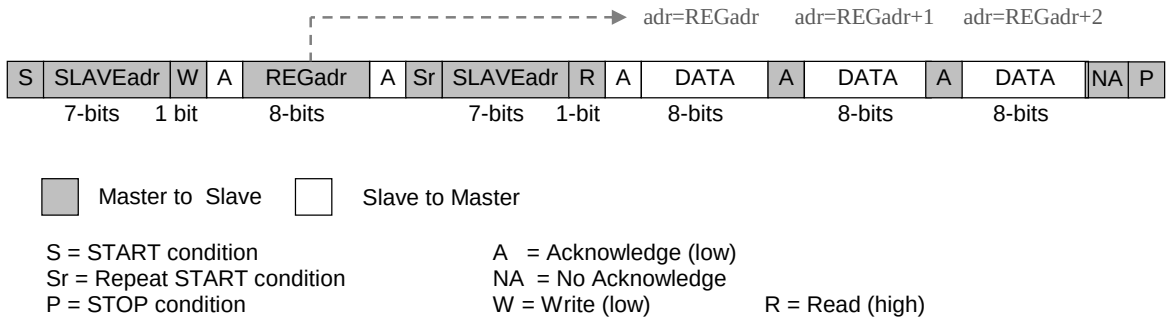


Figure 20: Consecutive Read Command

4.8 Thermal Protection

The DA9168 is protected from internal overheating by the over-temperature shutdown function.

When the power cycle ends, V_{SYS} will recover for several milliseconds; if the junction temperature is still above TSD_CRIT, the power cycle will be initiated again. In this way, the DA9168 continually attempts to restart with an active duty cycle of less than 1 %, enough to allow the IC to cool down. When the junction temperature has dropped below TSD_CRIT – THYS, power cycling will stop. When an over-temperature fault occurs, INT_N toggles.

To avoid tripping thermal shutdown, limit power dissipation to no more than:

$$P_{DISS} < \frac{118℃ - T_A}{R_{TH\_JA}}$$

Where T_A is the ambient temperature, R_{TH_JA} is the thermal resistance of the package and PCB.

4.9 Watchdog Behavior

The watchdog (WD) timer is reset either by I^2C communication or timer expiry. The expiration time of the watchdog is programmable as 40 s, 80 s , or 160 s by WD_TMR.

When the WD timer detects the expiration time, the following operation occurs.

1. INT_N
2. OTP reloads
3. VSYS restart, time can be set by SYS_WAIT

Restart WD timer after SYS_WAIT time

5 Register Definitions

5.1 Register Map

Table 26: Register Map

Addr	Register	7	6	5	4	3	2	1	0	Reset
functional registers										
System Status										
0x0000	PMC_STATUS_00	S_VBUS_VINDPM	S_VBUS_IINDPM	S_VMID_OC	S_VBAT_OC	S_VBUS_OK	S_VMID_OK	S_VSYS_OK	S_VBAT_OK	0x00
0x0001	PMC_STATUS_01	S_VBUS_OV	S_VMID_OV	S_VSYS_OV	S_VBAT_OV	S_VBUS_UV	S_VMID_UV	S_VSYS_UV	S_VBAT_UV	0x00
0x0002	PMC_STATUS_02	S_TSD_CRIT	S_TSD_WARN	S_WD_TIMER	S_TS_HOT	S_TS_WARM	S_TS_COOL	S_TS_COLD	S_TS_OFF	0x00
0x0003	PMC_STATUS_03	S_CHG_SLEEP	S_CHG_SPLMT	S_CHG_TIMER	S_CHG_TRICKLE	S_CHG_PRE	S_CHG_CC	S_CHG_CV	S_CHG_DONE	0x00
0x0004	PMC_STATUS_04	S_VSYS_SHUTDOWN	S_REF_OC	S_LDO2_IMON1	S_LDO2_IMON2	S_LDO2_OC	S_LDO1_IMON1	S_LDO1_IMON2	S_LDO1_OC	0x00
System Events										
0x0005	PMC_EVENT_00	E_VBUS_VINDPM	E_VBUS_IINDPM	E_VMID_OC	E_VBAT_OC	E_VBUS_OK	E_VMID_OK	E_VSYS_OK	E_VBAT_OK	0x00
0x0006	PMC_EVENT_01	E_VBUS_OV	E_VMID_OV	E_VSYS_OV	E_VBAT_OV	E_VBUS_UV	E_VMID_UV	E_VSYS_UV	E_VBAT_UV	0x00
0x0007	PMC_EVENT_02	E_TSD_CRIT	E_TSD_WARN	E_WD_TIMER	E_TS_HOT	E_TS_WARM	E_TS_COOL	E_TS_COLD	E_TS_OFF	0x00
0x0008	PMC_EVENT_03	E_CHG_SLEEP	E_CHG_SPLMT	E_CHG_TIMER	E_CHG_TRICKLE	E_CHG_PRE	E_CHG_CC	E_CHG_CV	E_CHG_DONE	0x00
0x0009	PMC_EVENT_04	E_VSYS_SHUTDOWN	E_REF_OC	E_LDO2_IMON1	E_LDO2_IMON2	E_LDO2_OC	E_LDO1_IMON1	E_LDO1_IMON2	E_LDO1_OC	0x00
Interrupt mask bits										
0x000A	PMC_MASK_00	M_VBUS_VINDPM	M_VBUS_IINDPM	M_VMID_OC	M_VBAT_OC	M_VBUS_OK	M_VMID_OK	M_VSYS_OK	M_VBAT_OK	0xFF

0x000B	PMC_MASK_01	M_VBUS_OV	M_VMID_OV	M_VSYS_OV	M_VBAT_OV	M_VBUS_UV	M_VMID_UV	M_VSYS_UV	M_VBAT_UV	0xFF
0x000C	PMC_MASK_02	M_TSD_CRIT	M_TSD_WARN	M_WD_TIMER	M_TS_HOT	M_TS_WARM	M_TS_COOL	M_TS_COLD	M_TS_OFF	0xFF
0x000D	PMC_MASK_03	M_CHG_SLEEP	M_CHG_SPLMT	M_CHG_TIMER	M_CHG_TRICKLE	M_CHG_PRE	M_CHG_CC	M_CHG_CV	M_CHG_DONE	0xFF
0x000E	PMC_MASK_04	M_VSYS_SHUTDOWN	M_REF_OC	M_LDO2_IMON1	M_LDO2_IMON2	M_LDO2_OC	M_LDO1_IMON1	M_LDO1_IMON2	M_LDO1_OC	0xFF
System settings										
0x000F	PMC_SYS_00	E_RD_CLR_DIS	VSYS_MIN<2:0>			VINDPM<3:0>				0x3B
0x0010	PMC_SYS_01	VSYS_OV_SHUTDOWN_DIS	VSYS_UV_SHUTDOWN_DIS	ILIMIT_EN	IINDPM<4:0>					0x44
0x0011	PMC_SYS_02	BTS_VBAT_RATE	BTS_VBAT_EN	BTS_VBUS_RATE	BTS_VBUS_EN	VBAT_DEB<1:0>		VBUS_DEB<1:0>		0x01
0x0012	PMC_SYS_03	SYS_WAIT<1:0>		WD_TMR<1:0>		WD_EN	RST_TMR<1:0>		RST_REG	0x34
0x0013	PMC_SYS_04	Reserved	BOOST_PWM	SEQ_BOOST	DLOAD_VMID_SEL<1:0>		DLOAD_VMID_EN	REV_VBUS_EN	BOOST_EN	0x38
0x0014	PMC_SYS_05	REV_VBUS_ILIM<3:0>				BOOST_VOUT<3:0>				0x9A
0x0015	PMC_SYS_06	RST_SYS	RIN_N_SHIP_EXIT_TMR	VBUS_OVSEL<1:0>		HIZ_MODE	SHIP_DLY<1:0>		SHIP_MODE	0x56
Charger Settings										
0x0016	PMC_CHG_00	Reserved	Reserved 0	BUCK_PWM	CHG_VRCHG	CHG_TMR_HALF_EN	CHG_TMR_EN	CHG_TERM_EN	CHG_EN	0x0E
0x0017	PMC_CHG_01	CHG_TMR_SAFE<1:0>		CHG_TMR_PRE<1:0>		CHG_TOPOFF<3:0>				0x00
0x0018	PMC_CHG_02	CHG_IPRE_MSB	CHG_RANGE_TERM	CHG_RANGE_PRE	CHG_ITERM<2:0>			CHG_IPRE<1:0>		0x0F
0x0019	PMC_CHG_03	CHG_RANGE	CHG_ICHG<6:0>							0x19
0x001A	PMC_CHG_04	Reserved	Reserved	CHG_VBATREG<5:0>						0x17

0x001B	PMC_CHG_05	IO_INT_N_PU	IO_EN_PD	IO_CHG_EN_N_PD	Reserved	Reserved	TS_VBATREG_SHIFT	CHG_TS_WARM_V	CHG_TS_COOL_I	0x00
0x001C	PMC_CHG_06	Reserved	TS_ICHG<6:0>							0x0C
LDO settings										
0x001D	PMC_LDO_00	LDO2_OCP	LDO2_PD	LDO2_LSW	LDO2_EN	LDO1_OCP	LDO1_PD	LDO1_LSW	LDO1_EN	0x44
0x001E	PMC_LDO_01	SEQ_LDO1<1:0>		LDO1_VOUT<5:0>						0x22
0x001F	PMC_LDO_02	SEQ_LDO2<1:0>		LDO2_VOUT<5:0>						0x22
0x0021	PMC_LDO_04	SYS_WAIT_CFG	RST_OPT_PWRCYC	SHIP_DLY_DIS	RST_OPT	VBAT_OV_CFG	CHG_TRICKLE_CYC	CHG_TRICKLE<1:0>		0x54
0x0022	PMC_LDO_05	LDO2_ILIM<3:0>				LDO1_ILIM<3:0>				0xAA
Options										
otp control										
Chip ID										
0x0042	OTP_DEVICE_ID	DEV_ID<7:0>								0xE7
0x0043	OTP_VARIANT_ID	MRC<3:0>				VRC<3:0>				0x30
0x0044	OTP_CONFIG_ID	CONFIG_REV<7:0>								0xDC

5.2 Register Descriptions

The Type column in the register description tables maps to the Access shown in Table 27.

Table 27: Register Access Type

Datasheet Type	Access
R	Read only
RW	Read / Write
RC	Clear on read
W1	Trigger by writing 1

5.2.1 System Status

Table 28: PMC_STATUS_00 (0x0000)

Bit	Type	Field Name	Description	Reset
[7]	R	S_VBUS_VINDPM	VBUS VINDPM Status **Value** **Description** **0x0** **VBUS not in VINDPM** 0x1 VBUS in VINDPM	0x0
[6]	R	S_VBUS_IINDPM	VBUS IINDPM Status **Value** **Description** **0x0** **VBUS not in IINDPM** 0x1 VBUS in IINDPM	0x0
[5]	R	S_VMID_OC	VMID OC Status during boost operation. **Value** **Description** **0x0** **VMID not in OC** 0x1 VMID in OC	0x0
[4]	R	S_VBAT_OC	VBAT OC Status during battery operation **Value** **Description** **0x0** **VBAT not in OC** 0x1 VBAT in OC	0x0
[3]	R	S_VBUS_OK	VBUS OK Status, above UV and below OV thresholds. **Value** **Description** **0x0** **VBUS not OK** 0x1 VBUS OK	0x0
[2]	R	S_VMID_OK	VMID OK Status during boost operation. **Value** **Description** **0x0** **VMID not OK**	0x0

Bit	Type	Field Name	Description	Reset
			0x1 VMID OK	
[1]	R	S_VSYS_OK	VSYS OK Status, above UV and below OV thresholds **Value Description** **0x0 VSYS not OK** 0x1 VSYS OK	0x0
[0]	R	S_VBAT_OK	VBAT OK Status, above UV and below OV thresholds. **Value Description** **0x0 VBAT not OK** 0x1 VBAT OK	0x0

Table 29: PMC_STATUS_01 (0x0001)

Bit	Type	Field Name	Description	Reset
[7]	R	S_VBUS_OV	VBUS OV Status. **Value Description** **0x0 VBUS not in OV** 0x1 VBUS in OV	0x0
[6]	R	S_VMID_OV	VMID OV Status during boost operation **Value Description** **0x0 VMID not in OV** 0x1 VMID in OV	0x0
[5]	R	S_VSYS_OV	VSYS OV Status **Value Description** **0x0 VSYS not in OV** 0x1 VSYS in OV	0x0
[4]	R	S_VBAT_OV	VBAT OV Status **Value Description** **0x0 VBAT not in OV** 0x1 VBAT in OV	0x0
[3]	R	S_VBUS_UV	VBUS UV Status **Value Description** **0x0 VBUS not in UV** 0x1 VBUS in UV	0x0
[2]	R	S_VMID_UV	VMID UV Status during boost operation **Value Description** **0x0 VMID not in UV** 0x1 VMID in UV	0x0

Bit	Type	Field Name	Description	Reset
[1]	R	S_VSYS_UV	VSYS UV Status **Value** **Description** **0x0** **VSYS not in UV** 0x1 VSYS in UV	0x0
[0]	R	S_VBAT_UV	VBAT UV Status **Value** **Description** **0x0** **VBAT not in UV** 0x1 VBAT in UV	0x0

Table 30: PMC_STATUS_02 (0x0002)

Bit	Type	Field Name	Description	Reset
[7]	R	S_TSD_CRIT	TSD CRIT Status **Value** **Description** **0x0** **Junction temperature below critical level.** 0x1 Junction temperature above critical level.	0x0
[6]	R	S_TSD_WARN	TSD WARN Status **Value** **Description** **0x0** **Junction temperature below warning level.** 0x1 Junction temperature above warning level.	0x0
[5]	R	S_WD_TIMER	WD TIMER Status **Value** **Description** **0x0** **Watch-dog timer not expired** 0x1 Watch-dog timer expired	0x0
[4]	R	S_TS_HOT	TS HOT Status **Value** **Description** **0x0** **Battery temperature sense not in HOT State** 0x1 Battery temperature sense in HOT State	0x0
[3]	R	S_TS_WARM	TS WARM Status **Value** **Description** **0x0** **Battery temperature sense not in WARM State** 0x1 Battery temperature sense in WARM State	0x0
[2]	R	S_TS_COOL	TS COOL Status **Value** **Description**	0x0

Bit	Type	Field Name	Description	Reset
			0x0 **Battery temperature sense not in COOL State** 0x1 Battery temperature sense in COOL State	
[1]	R	S_TS_COLD	TS COLD Status **Value** **Description** **0x0** **Battery temperature sense not in COLD State** 0x1 Battery temperature sense in COLD State	0x0
[0]	R	S_TS_OFF	TS OFF Status **Value** **Description** **0x0** **Battery temperature sense not in OFF State** 0x1 Battery temperature sense in OFF State	0x0

Table 31: PMC_STATUS_03 (0x0003)

Bit	Type	Field Name	Description	Reset
[7]	R	S_CHG_SLEEP	CHG SLEEP Status **Value** **Description** **0x0** **VBUS lower than SLEEP threshold** 0x1 VBUS higher than SLEEP threshold	0x0
[6]	R	S_CHG_SPLMT	CHG SPLMT Status **Value** **Description** **0x0** **VBAT** FET **not in supplement mode.** 0x1 VBAT FET in supplement mode.	0x0
[5]	R	S_CHG_TIMER	CHG TIMER Status **Value** **Description** **0x0** **Charge timer not expired** 0x1 Charge timer expired	0x0
[4]	R	S_CHG_TRICKLE	CHG TRICKLE Status **Value** **Description** **0x0** **Charger not in trickle charging** 0x1 Charger in trickle charging	0x0
[3]	R	S_CHG_PRE	CHG PRE Status **Value** **Description** **0x0** **Charger not in pre-charge** 0x1 Charger in pre-charge	0x0
[2]	R	S_CHG_CC	CHG CC Status	0x0

Bit	Type	Field Name	Description	Reset
			Value **Description** **0x0** **Charger not in constant-current state** 0x1 Charger in constant-current state	
[1]	R	S_CHG_CV	CHG CV Status **Value** **Description** **0x0** **Charger not in constant-voltage state** 0x1 Charger in constant-voltage state	0x0
[0]	R	S_CHG_DONE	CHG DONE Status **Value** **Description** **0x0** **Charge termination not completed** 0x1 Charge termination completed	0x0

Table 32: PMC_STATUS_04 (0x0004)

Bit	Type	Field Name	Description	Reset
[7]	R	S_VSYS_SHUTDOWN	VSYS SHUTDOWN Status **Value** **Description** **0x0** **VSYS not in SHUTDOWN** 0x1 VSYS in SHUTDOWN	0x0
[6]	R	S_REF_OC	REF OC Status **Value** **Description** **0x0** **REF not in OC** 0x1 REF in OC	0x0
[5]	R	S_LDO2_IMON1	LDO2 IMON1 Status **Value** **Description** **0x0** **LDO2 not in IMON1** 0x1 LDO2 in IMON1	0x0
[4]	R	S_LDO2_IMON2	LDO2 IMON2 Status **Value** **Description** **0x0** **LDO2 not in IMON2** 0x1 LDO2 in IMON2	0x0
[3]	R	S_LDO2_OC	LDO2 OC Status **Value** **Description** **0x0** **LDO2 not in OC** 0x1 LDO2 in OC	0x0
[2]	R	S_LDO1_IMON1	LDO1 IMON1 Status **Value** **Description** **0x0** **LDO1 not in IMON1**	0x0

Bit	Type	Field Name	Description	Reset
			0x1 LDO1 in IMON1	
[1]	R	S_LDO1_IMON2	LDO1 IMON2 Status **Value Description** **0x0 LDO1 not in IMON2** 0x1 LDO1 in IMON2	0x0
[0]	R	S_LDO1_OC	LDO1 OC Status **Value Description** **0x0 LDO1 not in OC** 0x1 LDO1 in OC	0x0

5.2.2 System Events

Table 33: PMC_EVENT_00 (0x0005)

Bit	Type	Field Name	Description	Reset
[7]	RC	E_VBUS_VINDPM	VBUS VINDPM Event register. Clear on read. **Value Description** **0x0 VBUS not in VINDPM** 0x1 VBUS in VINDPM	0x0
[6]	RC	E_VBUS_IINDPM	VBUS IINDPM Event register. Clear on read. **Value Description** **0x0 VBUS not in IINDPM** 0x1 VBUS in IINDPM	0x0
[5]	RC	E_VMID_OC	VMID OC Event register. Clear on read. **Value Description** **0x0 VMID not in OC** 0x1 VMID in OC	0x0
[4]	RC	E_VBAT_OC	VBAT OC Event register. Clear on read. **Value Description** **0x0 VBAT not in OC** 0x1 VBAT in OC	0x0
[3]	RC	E_VBUS_OK	VBUS OK Event register. Clear on read. **Value Description** **0x0 VBUS not OK** 0x1 VBUS OK	0x0
[2]	RC	E_VMID_OK	VMID OK Event register. Clear on read. **Value Description** **0x0 VMID not OK** 0x1 VMID OK	0x0

Bit	Type	Field Name	Description	Reset
[1]	RC	E_VSYS_OK	VSYS OK Event register. Clear on read. **Value Description** **0x0 VSYS not OK** 0x1 VSYS OK	0x0
[0]	RC	E_VBAT_OK	VBAT OK Event register. Clear on read. **Value Description** **0x0 VBAT not OK** 0x1 VBAT OK	0x0

Table 34: PMC_EVENT_01 (0x0006)

Bit	Type	Field Name	Description	Reset
[7]	RC	E_VBUS_OV	VBUS OV Event register. Clear on read. **Value Description** **0x0 VBUS not in OV** 0x1 VBUS in OV	0x0
[6]	RC	E_VMID_OV	VMID OV Event register. Clear on read. **Value Description** **0x0 VMID not in OV** 0x1 VMID in OV	0x0
[5]	RC	E_VSYS_OV	VSYS OV Event register. Clear on read. **Value Description** **0x0 VSYS not in OV** 0x1 VSYS in OV	0x0
[4]	RC	E_VBAT_OV	VBAT OV Event register. Clear on read. **Value Description** **0x0 VBAT not in OV** 0x1 VBAT in OV	0x0
[3]	RC	E_VBUS_UV	VBUS UV Event register. Clear on read. **Value Description** **0x0 VBUS not in UV** 0x1 VBUS in UV	0x0
[2]	RC	E_VMID_UV	VMID UV Event register. Clear on read. **Value Description** **0x0 VMID not in UV** 0x1 VMID in UV	0x0
[1]	RC	E_VSYS_UV	VSYS UV Event register. Clear on read. **Value Description**	0x0

Bit	Type	Field Name	Description	Reset
			0x0 VSYS not in UV 0x1 VSYS in UV	
[0]	RC	E_VBAT_UV	VBAT UV Event register. Clear on read. **Value Description** **0x0 VBAT not in UV** 0x1 VBAT in UV	0x0

Table 35: PMC_EVENT_02 (0x0007)

Bit	Type	Field Name	Description	Reset
[7]	RC	E_TSD_CRIT	TSD CRIT Event register. Clear on read. **Value Description** **0x0 Junction temperature below critical level.** 0x1 Junction temperature above critical level.	0x0
[6]	RC	E_TSD_WARN	TSD WARN Event register. Clear on read. **Value Description** **0x0 Junction temperature below warning level.** 0x1 Junction temperature above warning level.	0x0
[5]	RC	E_WD_TIMER	WD TIMER Event register. Clear on read. **Value Description** **0x0 Watch-dog timer not expired** 0x1 Watch-dog timer expired	0x0
[4]	RC	E_TS_HOT	TS HOT Event register. Clear on read. **Value Description** **0x0 Battery temperature sense not in HOT State** 0x1 Battery temperature sense in HOT State	0x0
[3]	RC	E_TS_WARM	TS WARM Event register. Clear on read. **Value Description** **0x0 Battery temperature sense not in WARM State** 0x1 Battery temperature sense in WARM State	0x0
[2]	RC	E_TS_COOL	TS COOL Event register. Clear on read. **Value Description** **0x0 Battery temperature sense not in COOL State** 0x1 Battery temperature sense in COOL State	0x0

Bit	Type	Field Name	Description	Reset
[1]	RC	E_TS_COLD	TS COLD Event register. Clear on read. **Value** **Description** **0x0** **Battery temperature sense not in COLD State** 0x1 Battery temperature sense in COLD State	0x0
[0]	RC	E_TS_OFF	TS OFF Event register. Clear on read. **Value** **Description** **0x0** **Battery temperature sense not in OFF State** 0x1 Battery temperature sense in OFF State	0x0

Table 36: PMC_EVENT_03 (0x0008)

Bit	Type	Field Name	Description	Reset
[7]	RC	E_CHG_SLEEP	CHG SLEEP Event register. Clear on read. **Value** **Description** **0x0** **VBUS lower than SLEEP threshold** 0x1 VBUS higher than SLEEP threshold	0x0
[6]	RC	E_CHG_SPLMT	CHG SPLMT Event register. Clear on read. **Value** **Description** **0x0** **VBAT** FET **not in supplement mode.** 0x1 VBAT FET in supplement mode.	0x0
[5]	RC	E_CHG_TIMER	CHG TIMER Event register. Clear on read. **Value** **Description** **0x0** **Charge timer not expired** 0x1 Charge timer expired	0x0
[4]	RC	E_CHG_TRICKLE	CHG TRICKLE Event register. Clear on read. **Value** **Description** **0x0** **Charger not in trickle charging** 0x1 Charger in trickle charging	0x0
[3]	RC	E_CHG_PRE	CHG PRE Event register. Clear on read. **Value** **Description** **0x0** **Charger not in pre-charge** 0x1 Charger in pre-charge	0x0
[2]	RC	E_CHG_CC	CHG CC Event register. Clear on read. **Value** **Description** **0x0** **Charger not in constant-current state** 0x1 Charger in constant-current state	0x0
[1]	RC	E_CHG_CV	CHG CV Event register. Clear on read.	0x0

Bit	Type	Field Name	Description	Reset
			Value **Description** **0x0** **Charger not in constant-voltage state** 0x1 Charger in constant-voltage state	
[0]	RC	E_CHG_DONE	CHG DONE Event register. Clear on read. **Value** **Description** **0x0** **Charge termination not completed** 0x1 Charge termination completed	0x0

Table 37: PMC_EVENT_04 (0x0009)

Bit	Type	Field Name	Description	Reset
[7]	RC	E_VSYS_SHUTDOWN	VSYS SHUTDOWN Event register. Clear on read. **Value** **Description** **0x0** **VSYS not in SHUTDOWN** 0x1 VSYS in SHUTDOWN	0x0
[6]	RC	E_REF_OC	REF OC Event register. Clear on read. **Value** **Description** **0x0** **REF not in OC** 0x1 REF in OC	0x0
[5]	RC	E_LDO2_IMON1	LDO2 IMON1 Event register. Clear on read. **Value** **Description** **0x0** **LDO2 not in IMON1** 0x1 LDO2 in IMON1	0x0
[4]	RC	E_LDO2_IMON2	LDO2 IMON2 Event register. Clear on read. **Value** **Description** **0x0** **LDO2 not in IMON2** 0x1 LDO2 in IMON2	0x0
[3]	RC	E_LDO2_OC	LDO2 OC Event register. Clear on read. **Value** **Description** **0x0** **LDO2 not in OC** 0x1 LDO2 in OC	0x0
[2]	RC	E_LDO1_IMON1	LDO1 IMON1 Event register. Clear on read. **Value** **Description** **0x0** **LDO1 not in IMON1** 0x1 LDO1 in IMON1	0x0
[1]	RC	E_LDO1_IMON2	LDO1 IMON2 Event register. Clear on read. **Value** **Description** **0x0** **LDO1 not in IMON2**	0x0

Bit	Type	Field Name	Description	Reset
			0x1 LDO1 in IMON2	
[0]	RC	E_LDO1_OC	LDO1 OC Event register. Clear on read. **Value Description** **0x0 LDO1 not in OC** 0x1 LDO1 in OC	0x0

5.2.3 Interrupt Masks

Table 38: PMC_MASK_00 (0x000A)

Bit	Type	Field Name	Description	Reset
[7]	RW	M_VBUS_VINDPM	INT_N Mask bit for VBUS VINDPM Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[6]	RW	M_VBUS_IINDPM	INT_N Mask bit for VBUS IINDPM Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[5]	RW	M_VMID_OC	INT_N Mask bit for VMID OC Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[4]	RW	M_VBAT_OC	INT_N Mask bit for VBAT OC Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[3]	RW	M_VBUS_OK	INT_N Mask bit for VBUS OK Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[2]	RW	M_VMID_OK	INT_N Mask bit for VMID OK Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[1]	RW	M_VSYS_OK	INT_N Mask bit for VSYS OK Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1

Bit	Type	Field Name	Description	Reset
[0]	RW	M_VBAT_OK	INT_N Mask bit for VBAT OK Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1

Table 39: PMC_MASK_01 (0x000B)

Bit	Type	Field Name	Description	Reset
[7]	RW	M_VBUS_OV	INT_N Mask bit for VBUS OV Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[6]	RW	M_VMID_OV	INT_N Mask bit for VMID OV Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[5]	RW	M_VSYS_OV	INT_N Mask bit for VSYS OV Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[4]	RW	M_VBAT_OV	INT_N Mask bit for VBAT OV Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[3]	RW	M_VBUS_UV	INT_N Mask bit for VBUS UV Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[2]	RW	M_VMID_UV	INT_N Mask bit for VMID UV Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[1]	RW	M_VSYS_UV	INT_N Mask bit for VSYS UV Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[0]	RW	M_VBAT_UV	INT_N Mask bit for VBAT UV Event **Value** **Description**	0x1

Bit	Type	Field Name	Description	Reset
			0x0 Not masked **0x1 Masked**	

Table 40: PMC_MASK_02 (0x000C)

Bit	Type	Field Name	Description	Reset
[7]	RW	M_TSD_CRIT	INT_N Mask bit for TSD CRIT Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[6]	RW	M_TSD_WARN	INT_N Mask bit for TSD WARN Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[5]	RW	M_WD_TIMER	INT_N Mask bit for WD TIMER Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[4]	RW	M_TS_HOT	INT_N Mask bit for TS HOT Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[3]	RW	M_TS_WARM	INT_N Mask bit for TS WARM Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[2]	RW	M_TS_COOL	INT_N Mask bit for TS COOL Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[1]	RW	M_TS_COLD	INT_N Mask bit for TS COLD Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1
[0]	RW	M_TS_OFF	INT_N Mask bit for TS OFF Event **Value Description** 0x0 Not masked **0x1 Masked**	0x1

Table 41: PMC_MASK_03 (0x000D)

Bit	Type	Field Name	Description	Reset
[7]	RW	M_CHG_SLEEP	INT_N Mask bit for CHG SLEEP Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[6]	RW	M_CHG_SPLMT	INT_N Mask bit for CHG SPLMT Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[5]	RW	M_CHG_TIMER	INT_N Mask bit for CHG TIMER Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[4]	RW	M_CHG_TRICKLE	INT_N Mask bit for CHG TRICKLE Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[3]	RW	M_CHG_PRE	INT_N Mask bit for CHG PRE Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[2]	RW	M_CHG_CC	INT_N Mask bit for CHG CC Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[1]	RW	M_CHG_CV	INT_N Mask bit for CHG CV Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[0]	RW	M_CHG_DONE	INT_N Mask bit for CHG DONE Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1

Table 42: PMC_MASK_04 (0x000E)

Bit	Type	Field Name	Description	Reset
[7]	RW	M_VSYS_SHUTDOWN	INT_N Mask bit for VSYS SHUTDOWN Event	0x1

Bit	Type	Field Name	Description	Reset
			Value **Description** 0x0 Not masked **0x1** **Masked**	
[6]	RW	M_REF_OC	INT_N Mask bit for REF OC Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[5]	RW	M_LDO2_IMON1	INT_N Mask bit for LDO2 IMON1 Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[4]	RW	M_LDO2_IMON2	INT_N Mask bit for LDO2 IMON2 Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[3]	RW	M_LDO2_OC	INT_N Mask bit for LDO2 OC Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[2]	RW	M_LDO1_IMON1	INT_N Mask bit for LDO1 IMON1 Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[1]	RW	M_LDO1_IMON2	INT_N Mask bit for LDO1 IMON2 Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1
[0]	RW	M_LDO1_OC	INT_N Mask bit for LDO1 OC Event **Value** **Description** 0x0 Not masked **0x1** **Masked**	0x1

5.2.4 System Settings

Table 43: PMC_SYS_00 (0x000F)

Bit	Type	Field Name	Description	Reset
[7]	RW	E_RD_CLR_DIS	Interrupt event register read-on-clear disable	0x0
[6:4]	RW	VSYS_MIN	VSYS MIN settings (V)	0x3

Bit	Type	Field Name	Description	Reset
			Value **Description** 0x4 Reserved 0x5 Reserved 0x6 Reserved 0x7 Reserved 0x0 3.4 0x1 3.5 0x2 3.6 **0x3 3.7**	
[3:0]	RW	VINDPM	VINDPM threshold setting (V) **Value** **Description** 0x00 Disable 0x01 Reserved 0x02 Reserved 0x03 Reserved 0x04 3.8 0x05 3.9 0x06 4.0 0x07 4.1 0x08 4.2 0x09 4.3 0x0A 4.4 **0x0B 4.5** 0x0C 4.6 0x0D 4.7 0x0E 4.8 0x0F Reserved	0x0B

Table 44: PMC_SYS_01 (0x0010)

Bit	Type	Field Name	Description	Reset
[7]	RW	VSYS_OV_SHUTDOWN_DIS	**Disable VSYS shut-down by VSYS_OV Value** **Description** **0x0 System shutdown by VSYS_OV** 0x1 No system shutdown by VSYS_OV	0x0
[6]	RW	VSYS_UV_SHUTDOWN_DIS	Disable VSYS shut-down by VSYS_UV	0x1

Bit	Type	Field Name	Description	Reset
			Value **Description** 0x0 System shutdown by VSYS_UV **0x1** **No system shutdown by VSYS_UV**	
[5]	RW	ILIMIT_EN	ILIMIT pin function enable **Value** **Description** **0x0** **No IINDPM update** 0x1 Set IINDPM by ILIMIT pin on VBUS plug-in.	0x0
[4:0]	RW	IINDPM	Input current limit setting (A). **Value** **Description** 0x00 0.1 0x01 0.2 0x02 0.3 0x03 0.4 **0x04** **0.5** 0x05 0.6 0x06 0.7 0x07 0.8 0x08 0.9 0x09 1.0 0x0A 1.1 0x0B 1.2 0x0C 1.3 0x0D 1.4 0x0E 1.5 0x0F 1.6 0x10 1.7 0x11 1.8 0x12 1.9 0x13 2.0 0x14 2.1 0x15 2.2 0x16 2.3 0x17 2.4 0x18 2.5 0x19 Reserved 0x1A Reserved	0x04

Bit	Type	Field Name	Description	Reset
			0x1B Reserved 0x1C Reserved 0x1D Reserved 0x1E Reserved 0x1F Reserved	

Table 45: PMC_SYS_02 (0x0011)

Bit	Type	Field Name	Description	Reset
[7]	RW	BTS_VBAT_RATE	Battery temperature sense interval while in battery operation, must set BTS_VBAT_EN == BTS_VBUS_EN == 0 to update **Value Description** **0x0 50 ms** 0x1 2 sec	0x0
[6]	RW	BTS_VBAT_EN	Battery temperature sense enable while in battery operation **Value Description** **0x0 Disable** 0x1 Enable	0x0
[5]	RW	BTS_VBUS_RATE	Battery temperature sense interval while VBUS supply present, must set BTS_VBAT_EN == BTS_VBUS_EN == 0 to update **Value Description** **0x0 50 ms** 0x1 2 sec	0x0
[4]	RW	BTS_VBUS_EN	Battery temperature sense enable while VBUS supply present **Value Description** **0x0 Disable** 0x1 Enable	0x0
[3:2]	RW	VBAT_DEB	VBAT detection debounce time (ms) **Value Description** **0x0 10** 0x1 20 0x2 100 0x3 200	0x0
[1:0]	RW	VBUS_DEB	VBUS detection debounce time (ms) **Value Description** 0x0 10 **0x1 20**	0x1

Bit	Type	Field Name	Description	Reset
			0x2 100 0x3 200	

Table 46: PMC_SYS_03 (0x0012)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	SYS_WAIT	VSYS power-off time for system power recovery cycle (s) **Value Description** **0x0 1** 0x1 2 0x2 3 0x3 4	0x0
[5:4]	RW	WD_TMR	Watch-dog timer expire time (s). Write-blocked when WD_EN is High. **Value Description** 0x0 OFF 0x1 40 0x2 80 **0x3 160**	0x3
[3]	RW	WD_EN	Watchdog enable **Value Description** **0x0 No action** 0x1 Watchdog enabled	0x0
[2:1]	RW	RST_TMR	RIN_N button press time (s) **Value Description** 0x0 4 0x1 8 **0x2 12** 0x3 20	0x2
[0]	W1	RST_REG	Triggers register initialization. **Value Description** **0x0 No action** 0x1 Register reset	0x0

Table 47: PMC_SYS_04 (0x0013)

Bit	Type	Field Name	Description	Reset
[6]	RW	BOOST_PWM	BOOST force-PWM **Value Description**	0x0

Bit	Type	Field Name	Description	Reset
			0x0 Auto-mode 0x1 Force-PWM mode	
[5]	RW	SEQ_BOOST	BOOST_EN bit to be controlled by EN pin **Value Description** 0x0 EN pin toggle has no effect on BOOST_EN **0x1 BOOST_EN is set when EN pin toggles high, and cleared when toggles low**	0x1
[4:3]	RW	DLOAD_VMID_SEL	Select dummy-load value on VMID (mA) **Value Description** 0x0 5 0x1 10 0x2 20 **0x3 30**	0x3
[2]	RW	DLOAD_VMID_EN	Enable dummy-load on VMID **Value Description** **0x0 Disable** 0x1 Enable	0x0
[1]	RW	REV_VBUS_EN	Enable BOOST supply output from VBUS **Value Description** **0x0 Disable** 0x1 Enable	0x0
[0]	RW	BOOST_EN	Boost enable during battery operation **Value Description** **0x0 Disable** 0x1 Enable	0x0

Table 48: PMC_SYS_05 (0x0014)

Bit	Type	Field Name	Description	Reset
[7:4]	RW	REV_VBUS_ILIM	Boost current limit setting when REV_VBUS_EN = 1 (A) **Value Description** 0x00 0.1 0x01 0.2 0x02 0.3 0x03 0.4 0x04 0.5 0x05 0.6	0x09

Bit	Type	Field Name	Description	Reset
			0x06 0.7 0x07 0.8 0x08 0.9 **0x09 1.0** 0x0A Reserved 0x0B Reserved 0x0C Reserved 0x0D Reserved 0x0E Reserved 0x0F Reserved	
[3:0]	RW	BOOST_VOUT	Boost output voltage settings (V) **Value Description** 0x0 4.0 0x1 4.1 0x2 4.2 0x3 4.3 0x4 4.4 0x5 4.5 0x6 4.6 0x7 4.7 0x8 4.8 0x9 4.9 **0xA 5.0** 0xB 5.1 0xC 5.2 0xD 5.3 0xE 5.4 0xF 5.5	0xA

Table 49: PMC_SYS_06 (0x0015)

Bit	Type	Field Name	Description	Reset
[7]	W1	RST_SYS	Triggers VSYS power-cycle **Value Description** **0x0 No action** 0x1 Trigger VSYS power-cycle	0x0
[6]	RW	RIN_N_SHIP_EXIT_TMR	RIN_N debounce time to exit from SHIP_MODE **Value Description**	0x1

Bit	Type	Field Name	Description	Reset
			0x0 20 ms **0x1 2 s**	
[5:4]	RW	VBUS_OVSEL	VBUS OV settings (V) **Value Description** 0x0 5.8 **0x1 6.2** 0x2 8.5 0x3 10.5	0x1
[3]	RW	HIZ_MODE	Hi-Z mode enable. **Value Description** **0x0 Supply from VBUS when available** 0x1 Supply from battery, even when VBUS present	0x0
[2:1]	RW	SHIP_DLY	Ship-mode entry delay time (s) **Value Description** 0x0 2 0x1 4 0x2 7 **0x3 10**	0x3
[0]	RW	SHIP_MODE	Ship-mode entry **Value Description** **0x0 No action** 0x1 Enter ship-mode. VBATFET is off.	0x0

5.2.5 Charger Settings

Table 50: PMC_CHG_00 (0x0016)

Bit	Type	Field Name	Description	Reset
[5]	RW	BUCK_PWM	BUCK PWM threshold reduction during charge **Value Description** **0x0 PWM threshold unchanged while charging** 0x1 Lower PWM threshold while charging	0x0
[4]	RW	CHG_VRCHG	Charger recharge threshold offset settings (mV) **Value Description** **0x0 100** 0x1 200	0x0
[3]	RW	CHG_TMR_HALF_EN	Charger safty timer rate reduced to half on selected events.	0x1

Bit	Type	Field Name	Description	Reset
			Value **Description** 0x0 Disable **0x1** **Enable**	
[2]	cfg OTP	CHG_TMR_EN	Charger safty timer enable. **Value** **Description** 0x0 Disable **0x1** **Enable**	0x1
[1]	RW	CHG_TERM_EN	Charger enable termination. Charger state transition to DONE state is enabled. **Value** **Description** 0x0 Disable **0x1** **Enable**	0x1
[0]	RW	CHG_EN	Charger enable register. CHG_EN_N pin level also needs to be low for charging to be enabled. **Value** **Description** **0x0** **Disable** 0x1 Enable	0x0

Table 51: PMC_CHG_01 (0x0017)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	CHG_TMR_SAFE	Charger safety timer setting (h) **Value** **Description** **0x0** **5** 0x1 10 0x2 15 0x3 20	0x0
[5:4]	RW	CHG_TMR_PRE	Pre-charge safety timer setting (min) **Value** **Description** **0x0** **30** 0x1 60 0x2 90 0x3 120	0x0
[3:0]	RW	CHG_TOPOFF	Top off timer (min) **Value** **Description** **0x0** **Disable TOPOFF** 0x1 0.25 0x2 0.5 0x3 1	0x0

Bit	Type	Field Name	Description	Reset
			0x4 5 0x5 10 0x6 15 0x7 20 0x8 25 0x9 30 0xA 35 0xB 40 0xC 45 0xD 50 0xE 55 0xF 60	

Table 52: PMC_CHG_02 (0x0018)

Bit	Type	Field Name	Description	Reset
[7]	RW	CHG_IPRE_MSB	Adds offset to pre-charge current setting (mA) **Value Description** **0x0 +0** 0x1 CHG_RANGE = 0 : +20, CHG_RANGE = 1 : +80	0x0
[6]	RW	CHG_RANGE_TERM	Charging current range settings for CHG_ITERM. Only effective when CHG_RANGE = 1. **Value Description** **0x0 Termination 5-25 mA, in 5 mA steps** 0x1 Termination 20 mA to 100 mA, in 20 mA steps	0x0
[5]	RW	CHG_RANGE_PRE	Charging current range settings for CHG_IPRE. Only effective when CHG_RANGE = 1. **Value Description** **0x0 Pre-charge 5-15 mA, in 5 mA steps** 0x1 Pre-charge 20 mA to 60 mA, in 20 mA steps	0x0
[4:2]	RW	CHG_ITERM	Termination charge current setting. (mA) **Value Description** 0x0 Reserved 0x1 CHG_RANGE = 0 : 5, CHG_RANGE = 1 : 20 0x2 CHG_RANGE = 0 : 10, CHG_RANGE = 1 : 40	0x3

Bit	Type	Field Name	Description	Reset
			0x3 **CHG_RANGE = 0 : 15, CHG_RANGE = 1 : 60** 0x4 CHG_RANGE = 0 : 20, CHG_RANGE = 1 : 80 0x5 CHG_RANGE = 0 : 25, CHG_RANGE = 1 : 100 0x6 Reserved 0x7 Reserved	
[1:0]	RW	CHG_IPRE	Pre-charge current setting. (mA) **Value** **Description** 0x0 0, Use only when CHG_IPRE_MSB=1 0x1 CHG_RANGE = 0 : 5, CHG_RANGE = 1 : 20 0x2 CHG_RANGE = 0 : 10, CHG_RANGE = 1 : 40 **0x3** **CHG_RANGE = 0 : 15, CHG_RANGE = 1 : 60**	0x3

Table 53: PMC_CHG_03 (0x0019)

Bit	Type	Field Name	Description	Reset
[7]	RW	CHG_RANGE	Charging current range settings **Value** **Description** **0x0** **Fast-charge 5 mA to 500 mA in 5 mA steps, also forces CHG_RANGE for CHG_ITERM and CHG_IPRE to 0** 0x1 Fast charge 20 mA to 2000 mA in 20 mA steps. CHG_RANGE_PRE and CHG_RANGE_TERM are effective	0x0
[6:0]	RW	CHG_ICHG	Fast charge current setting. (mA) **Value** **Description** 0x00 Reserved 0x01 CHG_RANGE = 0 : 5, CHG_RANGE = 1 : 20 0x02 CHG_RANGE = 0 : 10, CHG_RANGE = 1 : 40 0x03 CHG_RANGE = 0 : 15, CHG_RANGE = 1 : 60 0x04 CHG_RANGE = 0 : 20, CHG_RANGE = 1 : 80 0x05 CHG_RANGE = 0 : 25, CHG_RANGE = 1 : 100 0x06 CHG_RANGE = 0 : 30, CHG_RANGE = 1 : 120	0x19

Bit	Type	Field Name	Description		Reset
			0x07	CHG_RANGE = 0 : 35, CHG_RANGE = 1 : 140	
			0x08	CHG_RANGE = 0 : 40, CHG_RANGE = 1 : 160	
			0x09	CHG_RANGE = 0 : 45, CHG_RANGE = 1 : 180	
			0x0A	CHG_RANGE = 0 : 50, CHG_RANGE = 1 : 200	
			0x0B	CHG_RANGE = 0 : 55, CHG_RANGE = 1 : 220	
			0x0C	CHG_RANGE = 0 : 60, CHG_RANGE = 1 : 240	
			0x0D	CHG_RANGE = 0 : 65, CHG_RANGE = 1 : 260	
			0x0E	CHG_RANGE = 0 : 70, CHG_RANGE = 1 : 280	
			0x0F	CHG_RANGE = 0 : 75, CHG_RANGE = 1 : 300	
			0x10	CHG_RANGE = 0 : 80, CHG_RANGE = 1 : 320	
			0x11	CHG_RANGE = 0 : 85, CHG_RANGE = 1 : 340	
			0x12	CHG_RANGE = 0 : 90, CHG_RANGE = 1 : 360	
			0x13	CHG_RANGE = 0 : 95, CHG_RANGE = 1 : 380	
			0x14	CHG_RANGE = 0 : 100, CHG_RANGE = 1 : 400	
			0x15	CHG_RANGE = 0 : 105, CHG_RANGE = 1 : 420	
			0x16	CHG_RANGE = 0 : 110, CHG_RANGE = 1 : 440	
			0x17	CHG_RANGE = 0 : 115, CHG_RANGE = 1 : 460	
			0x18	CHG_RANGE = 0 : 120, CHG_RANGE = 1 : 480	
			0x19	**CHG_RANGE = 0 : 125, CHG_RANGE = 1 : 500**	
			0x1A	CHG_RANGE = 0 : 130, CHG_RANGE = 1 : 520	
			0x1B	CHG_RANGE = 0 : 135, CHG_RANGE = 1 : 540	
			0x1C	CHG_RANGE = 0 : 140, CHG_RANGE = 1 : 560	
			0x1D	CHG_RANGE = 0 : 145, CHG_RANGE = 1 : 580	

Bit	Type	Field Name	Description		Reset
			0x1E	CHG_RANGE = 0 : 150, CHG_RANGE = 1 : 600	
			0x1F	CHG_RANGE = 0 : 155, CHG_RANGE = 1 : 620	
			0x20	CHG_RANGE = 0 : 160, CHG_RANGE = 1 : 640	
			0x21	CHG_RANGE = 0 : 165, CHG_RANGE = 1 : 660	
			0x22	CHG_RANGE = 0 : 170, CHG_RANGE = 1 : 680	
			0x23	CHG_RANGE = 0 : 175, CHG_RANGE = 1 : 700	
			0x24	CHG_RANGE = 0 : 180, CHG_RANGE = 1 : 720	
			0x25	CHG_RANGE = 0 : 185, CHG_RANGE = 1 : 740	
			0x26	CHG_RANGE = 0 : 190, CHG_RANGE = 1 : 760	
			0x27	CHG_RANGE = 0 : 195, CHG_RANGE = 1 : 780	
			0x28	CHG_RANGE = 0 : 200, CHG_RANGE = 1 : 800	
			0x29	CHG_RANGE = 0 : 205, CHG_RANGE = 1 : 820	
			0x2A	CHG_RANGE = 0 : 210, CHG_RANGE = 1 : 840	
			0x2B	CHG_RANGE = 0 : 215, CHG_RANGE = 1 : 860	
			0x2C	CHG_RANGE = 0 : 220, CHG_RANGE = 1 : 880	
			0x2D	CHG_RANGE = 0 : 225, CHG_RANGE = 1 : 900	
			0x2E	CHG_RANGE = 0 : 230, CHG_RANGE = 1 : 920	
			0x2F	CHG_RANGE = 0 : 235, CHG_RANGE = 1 : 940	
			0x30	CHG_RANGE = 0 : 240, CHG_RANGE = 1 : 960	
			0x31	CHG_RANGE = 0 : 245, CHG_RANGE = 1 : 980	
			0x32	CHG_RANGE = 0 : 250, CHG_RANGE = 1 : 1000	
			0x33	CHG_RANGE = 0 : 255, CHG_RANGE = 1 : 1020	
			0x34	CHG_RANGE = 0 : 260, CHG_RANGE = 1 : 1040	

Bit	Type	Field Name	Description		Reset
			0x35	CHG_RANGE = 0 : 265, CHG_RANGE = 1 : 1060	
			0x36	CHG_RANGE = 0 : 270, CHG_RANGE = 1 : 1080	
			0x37	CHG_RANGE = 0 : 275, CHG_RANGE = 1 : 1100	
			0x38	CHG_RANGE = 0 : 280, CHG_RANGE = 1 : 1120	
			0x39	CHG_RANGE = 0 : 285, CHG_RANGE = 1 : 1140	
			0x3A	CHG_RANGE = 0 : 290, CHG_RANGE = 1 : 1160	
			0x3B	CHG_RANGE = 0 : 295, CHG_RANGE = 1 : 1180	
			0x3C	CHG_RANGE = 0 : 300, CHG_RANGE = 1 : 1200	
			0x3D	CHG_RANGE = 0 : 305, CHG_RANGE = 1 : 1220	
			0x3E	CHG_RANGE = 0 : 310, CHG_RANGE = 1 : 1240	
			0x3F	CHG_RANGE = 0 : 315, CHG_RANGE = 1 : 1260	
			0x40	CHG_RANGE = 0 : 320, CHG_RANGE = 1 : 1280	
			0x41	CHG_RANGE = 0 : 325, CHG_RANGE = 1 : 1300	
			0x42	CHG_RANGE = 0 : 330, CHG_RANGE = 1 : 1320	
			0x43	CHG_RANGE = 0 : 335, CHG_RANGE = 1 : 1340	
			0x44	CHG_RANGE = 0 : 340, CHG_RANGE = 1 : 1360	
			0x45	CHG_RANGE = 0 : 345, CHG_RANGE = 1 : 1380	
			0x46	CHG_RANGE = 0 : 350, CHG_RANGE = 1 : 1400	
			0x47	CHG_RANGE = 0 : 355, CHG_RANGE = 1 : 1420	
			0x48	CHG_RANGE = 0 : 360, CHG_RANGE = 1 : 1440	
			0x49	CHG_RANGE = 0 : 365, CHG_RANGE = 1 : 1460	
			0x4A	CHG_RANGE = 0 : 370, CHG_RANGE = 1 : 1480	
			0x4B	CHG_RANGE = 0 : 375, CHG_RANGE = 1 : 1500	

Bit	Type	Field Name	Description		Reset
			0x4C	CHG_RANGE = 0 : 380, CHG_RANGE = 1 : 1520	
			0x4D	CHG_RANGE = 0 : 385, CHG_RANGE = 1 : 1540	
			0x4E	CHG_RANGE = 0 : 390, CHG_RANGE = 1 : 1560	
			0x4F	CHG_RANGE = 0 : 395, CHG_RANGE = 1 : 1580	
			0x50	CHG_RANGE = 0 : 400, CHG_RANGE = 1 : 1600	
			0x51	CHG_RANGE = 0 : 405, CHG_RANGE = 1 : 1620	
			0x52	CHG_RANGE = 0 : 410, CHG_RANGE = 1 : 1640	
			0x53	CHG_RANGE = 0 : 415, CHG_RANGE = 1 : 1660	
			0x54	CHG_RANGE = 0 : 420, CHG_RANGE = 1 : 1680	
			0x55	CHG_RANGE = 0 : 425, CHG_RANGE = 1 : 1700	
			0x56	CHG_RANGE = 0 : 430, CHG_RANGE = 1 : 1720	
			0x57	CHG_RANGE = 0 : 435, CHG_RANGE = 1 : 1740	
			0x58	CHG_RANGE = 0 : 440, CHG_RANGE = 1 : 1760	
			0x59	CHG_RANGE = 0 : 445, CHG_RANGE = 1 : 1780	
			0x5A	CHG_RANGE = 0 : 450, CHG_RANGE = 1 : 1800	
			0x5B	CHG_RANGE = 0 : 455, CHG_RANGE = 1 : 1820	
			0x5C	CHG_RANGE = 0 : 460, CHG_RANGE = 1 : 1840	
			0x5D	CHG_RANGE = 0 : 465, CHG_RANGE = 1 : 1860	
			0x5E	CHG_RANGE = 0 : 470, CHG_RANGE = 1 : 1880	
			0x5F	CHG_RANGE = 0 : 475, CHG_RANGE = 1 : 1900	
			0x60	CHG_RANGE = 0 : 480, CHG_RANGE = 1 : 1920	
			0x61	CHG_RANGE = 0 : 485, CHG_RANGE = 1 : 1940	
			0x62	CHG_RANGE = 0 : 490, CHG_RANGE = 1 : 1960	

Bit	Type	Field Name	Description		Reset
			0x63	CHG_RANGE = 0 : 495, CHG_RANGE = 1 : 1980	
			0x64	CHG_RANGE = 0 : 500, CHG_RANGE = 1 : 2000	
			0x65	Reserved	
			0x7F	Reserved	

Table 54: PMC_CHG_04 (0x001A)

Bit	Type	Field Name	Description		Reset
[5:0]	RW	CHG_VBATREG	Battery voltage regulation setting (V). 10 mV step.		0x17
			Value	**Description**	
			0x00	Reserved	
			0x01	Reserved	
			0x02	Reserved	
			0x03	4.00	
			0x04	4.01	
			0x05	4.02	
			0x06	4.03	
			0x07	4.04	
			0x08	4.05	
			0x09	4.06	
			0x0A	4.07	
			0x0B	4.08	
			0x0C	4.09	
			0x0D	4.10	
			0x0E	4.11	
			0x0F	4.12	
			0x10	4.13	
			0x11	4.14	
			0x12	4.15	
			0x13	4.16	
			0x14	4.17	
			0x15	4.18	
			0x16	4.19	
			0x17	**4.20**	
			0x18	4.21	
			0x19	4.22	
			0x1A	4.23	

Bit	Type	Field Name	Description	Reset
			0x1B 4.24 0x1C 4.25 0x1D 4.26 0x1E 4.27 0x1F 4.28 0x20 4.29 0x21 4.30 0x22 4.31 0x23 4.32 0x24 4.33 0x25 4.34 0x26 4.35 0x27 4.36 0x28 4.37 0x29 4.38 0x2A 4.39 0x2B 4.40 0x2C 4.41 0x2D 4.42 0x2E 4.43 0x2F 4.44 0x30 4.45 0x31 4.46 0x32 4.47 0x33 4.48 0x34 4.49 0x35 4.50 0x36 Reserved 0x37 Reserved 0x38 Reserved 0x39 Reserved 0x3A Reserved 0x3B Reserved 0x3C Reserved 0x3D Reserved 0x3E Reserved	

Bit	Type	Field Name	Description	Reset
			0x3F Reserved	

Table 55: PMC_CHG_05 (0x001B)

Bit	Type	Field Name	Description	Reset
[7]	RW	IO_INT_N_PU	INT_N pin internal pull-up **Value Description** **0x0 Disable** 0x1 Enable	0x0
[6]	RW	IO_EN_PD	EN pin internal pull-down **Value Description** **0x0 Disable** 0x1 Enable	0x0
[5]	RW	IO_CHG_EN_N_PD	CHG_EN_N pin internal pull-down **Value Description** **0x0 Disable** 0x1 Enable	0x0
[2]	RW	TS_VBATREG_SHIFT	Battery voltage regulation setting down-shift during TS event (mV). **Value Description** **0x0 100** 0x1 200	0x0
[1]	RW	CHG_TS_WARM_V	Charger VBATREG is shifted by TS_VBATREG_SHIFT, and termination disabled during TS_WARM. **Value Description** **0x0 Disable** 0x1 Enable	0x0
[0]	RW	CHG_TS_COOL_I	Charger ICHG is set to TS_ICHG on TS_COOL. Charge termination disabled during TS_COOL. **Value Description** **0x0 Disable** 0x1 Enable	0x0

Table 56: PMC_CHG_06 (0x001C)

Bit	Type	Field Name	Description	Reset
[6:0]	RW	TS_ICHG	Fast charge current setting during TS event. (mA) **Value Description** 0x00 Reserved 0x01 CHG_RANGE = 0 : 5, CHG_RANGE = 1 : 20	0x0C

Bit	Type	Field Name	Description		Reset
			0x02	CHG_RANGE = 0 : 10, CHG_RANGE = 1 : 40	
			0x03	CHG_RANGE = 0 : 15, CHG_RANGE = 1 : 60	
			0x04	CHG_RANGE = 0 : 20, CHG_RANGE = 1 : 80	
			0x05	CHG_RANGE = 0 : 25, CHG_RANGE = 1 : 100	
			0x06	CHG_RANGE = 0 : 30, CHG_RANGE = 1 : 120	
			0x07	CHG_RANGE = 0 : 35, CHG_RANGE = 1 : 140	
			0x08	CHG_RANGE = 0 : 40, CHG_RANGE = 1 : 160	
			0x09	CHG_RANGE = 0 : 45, CHG_RANGE = 1 : 180	
			0x0A	CHG_RANGE = 0 : 50, CHG_RANGE = 1 : 200	
			0x0B	CHG_RANGE = 0 : 55, CHG_RANGE = 1 : 220	
			0x0C	**CHG_RANGE = 0 : 60, CHG_RANGE = 1 : 240**	
			0x0D	CHG_RANGE = 0 : 65, CHG_RANGE = 1 : 260	
			0x0E	CHG_RANGE = 0 : 70, CHG_RANGE = 1 : 280	
			0x0F	CHG_RANGE = 0 : 75, CHG_RANGE = 1 : 300	
			0x10	CHG_RANGE = 0 : 80, CHG_RANGE = 1 : 320	
			0x11	CHG_RANGE = 0 : 85, CHG_RANGE = 1 : 340	
			0x12	CHG_RANGE = 0 : 90, CHG_RANGE = 1 : 360	
			0x13	CHG_RANGE = 0 : 95, CHG_RANGE = 1 : 380	
			0x14	CHG_RANGE = 0 : 100, CHG_RANGE = 1 : 400	
			0x15	CHG_RANGE = 0 : 105, CHG_RANGE = 1 : 420	
			0x16	CHG_RANGE = 0 : 110, CHG_RANGE = 1 : 440	
			0x17	CHG_RANGE = 0 : 115, CHG_RANGE = 1 : 460	
			0x18	CHG_RANGE = 0 : 120, CHG_RANGE = 1 : 480	

Bit	Type	Field Name	Description		Reset
			0x19	CHG_RANGE = 0 : 125, CHG_RANGE = 1 : 500	
			0x1A	CHG_RANGE = 0 : 130, CHG_RANGE = 1 : 520	
			0x1B	CHG_RANGE = 0 : 135, CHG_RANGE = 1 : 540	
			0x1C	CHG_RANGE = 0 : 140, CHG_RANGE = 1 : 560	
			0x1D	CHG_RANGE = 0 : 145, CHG_RANGE = 1 : 580	
			0x1E	CHG_RANGE = 0 : 150, CHG_RANGE = 1 : 600	
			0x1F	CHG_RANGE = 0 : 155, CHG_RANGE = 1 : 620	
			0x20	CHG_RANGE = 0 : 160, CHG_RANGE = 1 : 640	
			0x21	CHG_RANGE = 0 : 165, CHG_RANGE = 1 : 660	
			0x22	CHG_RANGE = 0 : 170, CHG_RANGE = 1 : 680	
			0x23	CHG_RANGE = 0 : 175, CHG_RANGE = 1 : 700	
			0x24	CHG_RANGE = 0 : 180, CHG_RANGE = 1 : 720	
			0x25	CHG_RANGE = 0 : 185, CHG_RANGE = 1 : 740	
			0x26	CHG_RANGE = 0 : 190, CHG_RANGE = 1 : 760	
			0x27	CHG_RANGE = 0 : 195, CHG_RANGE = 1 : 780	
			0x28	CHG_RANGE = 0 : 200, CHG_RANGE = 1 : 800	
			0x29	CHG_RANGE = 0 : 205, CHG_RANGE = 1 : 820	
			0x2A	CHG_RANGE = 0 : 210, CHG_RANGE = 1 : 840	
			0x2B	CHG_RANGE = 0 : 215, CHG_RANGE = 1 : 860	
			0x2C	CHG_RANGE = 0 : 220, CHG_RANGE = 1 : 880	
			0x2D	CHG_RANGE = 0 : 225, CHG_RANGE = 1 : 900	
			0x2E	CHG_RANGE = 0 : 230, CHG_RANGE = 1 : 920	
			0x2F	CHG_RANGE = 0 : 235, CHG_RANGE = 1 : 940	

Bit	Type	Field Name	Description		Reset
			0x30	CHG_RANGE = 0 : 240, CHG_RANGE = 1 : 960	
			0x31	CHG_RANGE = 0 : 245, CHG_RANGE = 1 : 980	
			0x32	CHG_RANGE = 0 : 250, CHG_RANGE = 1 : 1000	
			0x33	CHG_RANGE = 0 : 255, CHG_RANGE = 1 : 1020	
			0x34	CHG_RANGE = 0 : 260, CHG_RANGE = 1 : 1040	
			0x35	CHG_RANGE = 0 : 265, CHG_RANGE = 1 : 1060	
			0x36	CHG_RANGE = 0 : 270, CHG_RANGE = 1 : 1080	
			0x37	CHG_RANGE = 0 : 275, CHG_RANGE = 1 : 1100	
			0x38	CHG_RANGE = 0 : 280, CHG_RANGE = 1 : 1120	
			0x39	CHG_RANGE = 0 : 285, CHG_RANGE = 1 : 1140	
			0x3A	CHG_RANGE = 0 : 290, CHG_RANGE = 1 : 1160	
			0x3B	CHG_RANGE = 0 : 295, CHG_RANGE = 1 : 1180	
			0x3C	CHG_RANGE = 0 : 300, CHG_RANGE = 1 : 1200	
			0x3D	CHG_RANGE = 0 : 305, CHG_RANGE = 1 : 1220	
			0x3E	CHG_RANGE = 0 : 310, CHG_RANGE = 1 : 1240	
			0x3F	CHG_RANGE = 0 : 315, CHG_RANGE = 1 : 1260	
			0x40	CHG_RANGE = 0 : 320, CHG_RANGE = 1 : 1280	
			0x41	CHG_RANGE = 0 : 325, CHG_RANGE = 1 : 1300	
			0x42	CHG_RANGE = 0 : 330, CHG_RANGE = 1 : 1320	
			0x43	CHG_RANGE = 0 : 335, CHG_RANGE = 1 : 1340	
			0x44	CHG_RANGE = 0 : 340, CHG_RANGE = 1 : 1360	
			0x45	CHG_RANGE = 0 : 345, CHG_RANGE = 1 : 1380	
			0x46	CHG_RANGE = 0 : 350, CHG_RANGE = 1 : 1400	

Bit	Type	Field Name	Description		Reset
			0x47	CHG_RANGE = 0 : 355, CHG_RANGE = 1 : 1420	
			0x48	CHG_RANGE = 0 : 360, CHG_RANGE = 1 : 1440	
			0x49	CHG_RANGE = 0 : 365, CHG_RANGE = 1 : 1460	
			0x4A	CHG_RANGE = 0 : 370, CHG_RANGE = 1 : 1480	
			0x4B	CHG_RANGE = 0 : 375, CHG_RANGE = 1 : 1500	
			0x4C	CHG_RANGE = 0 : 380, CHG_RANGE = 1 : 1520	
			0x4D	CHG_RANGE = 0 : 385, CHG_RANGE = 1 : 1540	
			0x4E	CHG_RANGE = 0 : 390, CHG_RANGE = 1 : 1560	
			0x4F	CHG_RANGE = 0 : 395, CHG_RANGE = 1 : 1580	
			0x50	CHG_RANGE = 0 : 400, CHG_RANGE = 1 : 1600	
			0x51	CHG_RANGE = 0 : 405, CHG_RANGE = 1 : 1620	
			0x52	CHG_RANGE = 0 : 410, CHG_RANGE = 1 : 1640	
			0x53	CHG_RANGE = 0 : 415, CHG_RANGE = 1 : 1660	
			0x54	CHG_RANGE = 0 : 420, CHG_RANGE = 1 : 1680	
			0x55	CHG_RANGE = 0 : 425, CHG_RANGE = 1 : 1700	
			0x56	CHG_RANGE = 0 : 430, CHG_RANGE = 1 : 1720	
			0x57	CHG_RANGE = 0 : 435, CHG_RANGE = 1 : 1740	
			0x58	CHG_RANGE = 0 : 440, CHG_RANGE = 1 : 1760	
			0x59	CHG_RANGE = 0 : 445, CHG_RANGE = 1 : 1780	
			0x5A	CHG_RANGE = 0 : 450, CHG_RANGE = 1 : 1800	
			0x5B	CHG_RANGE = 0 : 455, CHG_RANGE = 1 : 1820	
			0x5C	CHG_RANGE = 0 : 460, CHG_RANGE = 1 : 1840	
			0x5D	CHG_RANGE = 0 : 465, CHG_RANGE = 1 : 1860	

Bit	Type	Field Name	Description		Reset
			0x5E	CHG_RANGE = 0 : 470, CHG_RANGE = 1 : 1880	
			0x5F	CHG_RANGE = 0 : 475, CHG_RANGE = 1 : 1900	
			0x60	CHG_RANGE = 0 : 480, CHG_RANGE = 1 : 1920	
			0x61	CHG_RANGE = 0 : 485, CHG_RANGE = 1 : 1940	
			0x62	CHG_RANGE = 0 : 490, CHG_RANGE = 1 : 1960	
			0x63	CHG_RANGE = 0 : 495, CHG_RANGE = 1 : 1980	
			0x64	CHG_RANGE = 0 : 500, CHG_RANGE = 1 : 2000	
			0x65	Reserved	
			0x7F	Reserved	

5.2.6 LDO Settings

Table 57: PMC_LDO_00 (0x001D)

Bit	Type	Field Name	Description		Reset
[7]	RW	LDO2_OCP	LDO2 OCP mode.		0x0
			Value	**Description**	
			0x0	**Disable**	
			0x1	Enable hiccup of 10 ms interval.	
[6]	RW	LDO2_PD	LDO2 pull-down enable		0x1
			Value	**Description**	
			0x0	Disable	
			0x1	**Enable**	
[5]	RW	LDO2_LSW	LDO2 load-switch mode, write-blocked when LDO2 is High		0x0
			Value	**Description**	
			0x0	**LDO mode**	
			0x1	Load-switch mode	
[4]	RW	LDO2_EN	LDO2 enable		0x0
			Value	**Description**	
			0x0	**Disable**	
			0x1	Enable	
[3]	RW	LDO1_OCP	LDO1 OCP mode.		0x0
			Value	**Description**	
			0x0	**Disable**	

Bit	Type	Field Name	Description	Reset
			0x1 Enable hiccup of 10 ms interval.	
[2]	RW	LDO1_PD	LDO1 pull-down enable **Value Description** 0x0 Disable **0x1 Enable**	0x1
[1]	RW	LDO1_LSW	LDO1 load-switch mode, write-blocked when LDO1 is High **Value Description** **0x0 LDO mode** 0x1 Load-switch mode	0x0
[0]	RW	LDO1_EN	LDO1 enable **Value Description** **0x0 Disable** 0x1 Enable	0x0

Table 58: PMC_LDO_01 (0x001E)

Bit	Type	Field Name	Description	Reset
[7:6]	RW	SEQ_LDO1	LDO1 enable by EN pin. **Value Description** **0x0 LDO1 not enabled by EN pin** 0x1 EnableLDO1 ASAP after EN pin rise. 0x2 Enable LDO1 0.25 ms after EN pin rise. 0x3 Enable LDO1 0.5 ms after EN pin rise.	0x0
[5:0]	RW	LDO1_VOUT	LDO1 output voltage setting (V), when LDO1_LSW is 0. **Value Description** 0x00 1.6 0x01 1.7 0x02 1.8 0x03 1.9 0x04 2.0 0x05 2.1 0x06 2.2 0x07 2.3 0x08 2.4 0x09 2.5 0x0A 2.6 0x0B 2.7	0x22

Bit	Type	Field Name	Description		Reset
			0x0C	2.8	
			0x0D	2.9	
			0x0E	3.0	
			0x0F	3.1	
			0x10	3.2	
			0x11	3.3	
			0x12	3.4	
			0x13	3.5	
			0x14	3.6	
			0x15	3.7	
			0x16	3.8	
			0x17	3.9	
			0x18	4.0	
			0x19	4.1	
			0x1A	4.2	
			0x1B	4.3	
			0x1C	4.4	
			0x1D	4.5	
			0x1E	4.6	
			0x1F	4.7	
			0x20	4.8	
			0x21	4.9	
			0x22	**5.0**	
			0x23	5.1	
			0x24	5.2	
			0x25	Reserved	
			0x3F	Reserved	

Table 59: PMC_LDO_02 (0x001F)

Bit	Type	Field Name	Description		Reset
[7:6]	RW	SEQ_LDO2	LDO2 enable by EN pin.		0x0
			Value	**Description**	
			0x0	**LDO2 not enabled by EN pin**	
			0x1	EnableLDO2 ASAP after EN pin rise.	
			0x2	Enable LDO2 0.25 ms after EN pin rise.	
			0x3	Enable LDO2 0.5 ms after EN pin rise.	

Bit	Type	Field Name	Description	Reset
[5:0]	RW	LDO2_VOUT	LDO2 output voltage setting (V), when LDO2_LSW is 0. **Value** **Description** 0x00 1.6 0x01 1.7 0x02 1.8 0x03 1.9 0x04 2.0 0x05 2.1 0x06 2.2 0x07 2.3 0x08 2.4 0x09 2.5 0x0A 2.6 0x0B 2.7 0x0C 2.8 0x0D 2.9 0x0E 3.0 0x0F 3.1 0x10 3.2 0x11 3.3 0x12 3.4 0x13 3.5 0x14 3.6 0x15 3.7 0x16 3.8 0x17 3.9 0x18 4.0 0x19 4.1 0x1A 4.2 0x1B 4.3 0x1C 4.4 0x1D 4.5 0x1E 4.6 0x1F 4.7 0x20 4.8 0x21 4.9	0x22

Bit	Type	Field Name	Description		Reset
			0x22	**5.0**	
			0x23	5.1	
			0x24	5.2	
			0x25	Reserved	
			0x3F	Reserved	

Table 60: PMC_LDO_04 (0x0021)

Bit	Type	Field Name	Description		Reset
[7]	RW	SYS_WAIT_CFG	Configuration for SYS_WAIT		0x0
			Value	**Description**	
			0x0	**Default setting**	
			0x1	Wait time is 1/10 of default values	
[6]	RW	RST_OPT_PWRCYC	RIN_N long-press to trigger power-cycle (only when RST_OPT=0)		0x1
			Value	**Description**	
			0x0	RIN_N long-press does not trigger power-cycle when RST_OPT=0	
			0x1	**RIN_N long-press triggers power-cycle**	
[5]	RW	SHIP_DLY_DIS	Disable SHIP_MODE entry delay		0x0
			Value	**Description**	
			0x0	**SHIP_MODE entry after SHIP_DLY**	
			0x1	SHIP_MODE entry with minimum delay	
[4]	RW	RST_OPT	RIN_N operation options		0x1
			Value	**Description**	
			0x0	VSYS recovery after SYS_WAIT regardless of RIN_N state	
			0x1	**VSYS recovery after SYS_WAIT on RIN_N rise**	
[3]	RW	VBAT_OV_CFG	Disables system shutdown by VBAT_OV		0x0
			Value	**Description**	
			0x0	**Shut-down VSYS on VBAT_OV**	
			0x1	Do not shut-down VSYS on VBAT_OV	
[2]	RW	CHG_TRICKLE_CYC	Trickle charge 50% duty cyclic mode		0x1
			Value	**Description**	
			0x0	Cyclic mode disabled	
			0x1	**Cyclic mode enabled**	
[1:0]	RW	CHG_TRICKLE	Trickle charge current (CHG_TRICKLE_CYC=0/CHG_TRICKLE_CYC=1) (mA)		0x0

Bit	Type	Field Name	Description	Reset
			Value **Description** **0x0** **5 / 2.5** 0x1 14 / 7 0x2 38 / 19 0x3 64 / 32	

Table 61: PMC_LDO_05 (0x0022)

Bit	Type	Field Name	Description	Reset
[7:4]	RW	LDO2_ILIM	VOUT2 current limit (mA) **Value** **Description** 0x0 37 0x1 82 0x2 127 0x3 172 0x4 217 0x5 262 0x6 307 0x7 352 0x8 397 0x9 442 **0xA** **487** 0xB 532 0xC 577 0xD 622 0xE 667 0xF 712	0xA
[3:0]	RW	LDO1_ILIM	VOUT1 current limit (mA) **Value** **Description** 0x0 37 0x1 82 0x2 127 0x3 172 0x4 217 0x5 262 0x6 307 0x7 352 0x8 397	0xA

Bit	Type	Field Name	Description	Reset
			0x9 442 **0xA 487** 0xB 532 0xC 577 0xD 622 0xE 667 0xF 712	

5.2.7 Chip ID

Table 62: OTP_DEVICE_ID (0x0042)

Bit	Type	Field Name	Description	Reset
[7:0]	R	DEV_ID	Device ID	0xE7

Table 63: OTP_VARIANT_ID (0x0043)

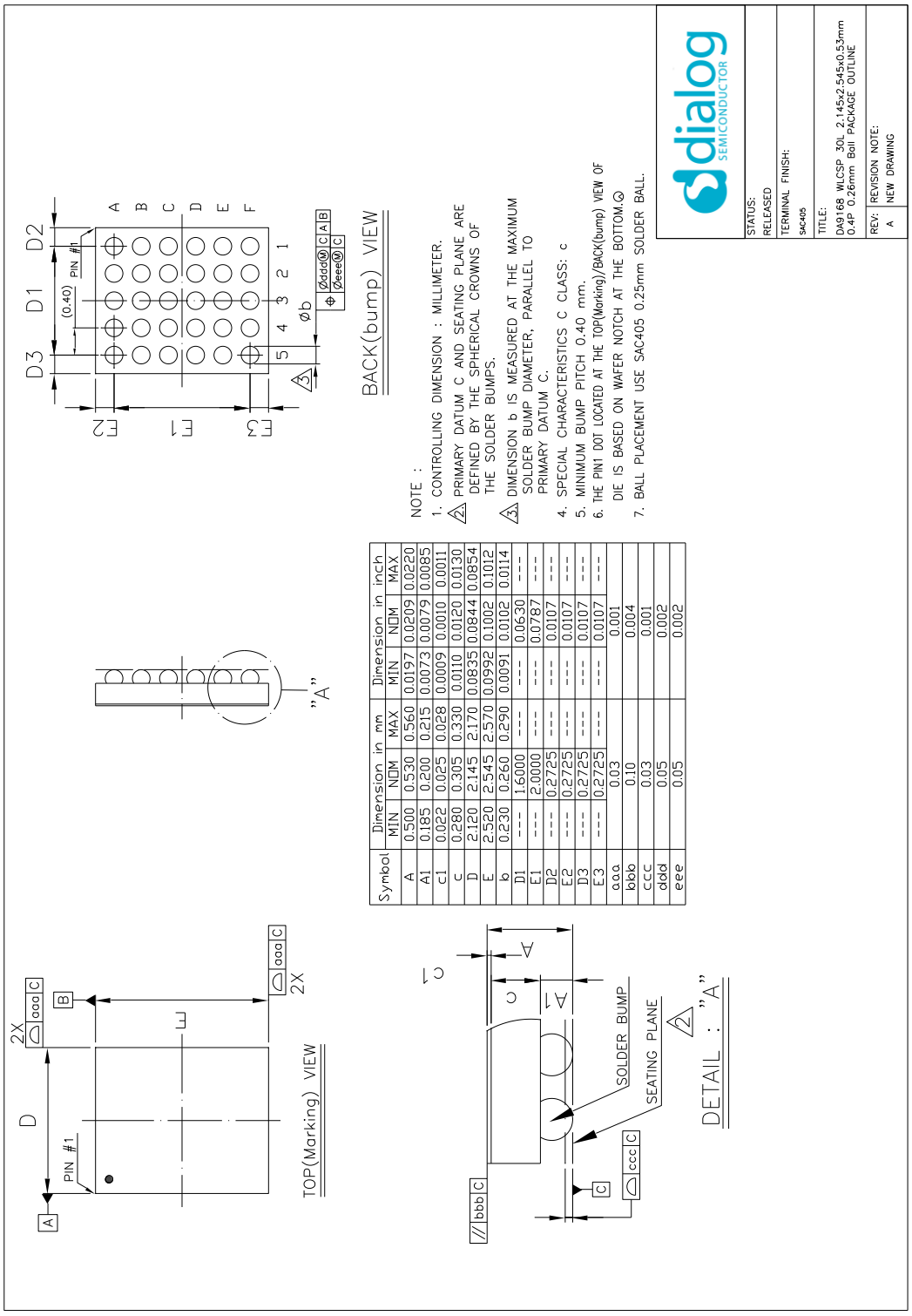
Bit	Type	Field Name	Description	Reset
[7:4]	R	MRC	Mask revision code	0x3
[3:0]	R	VRC	Chip variant code	0x0

Table 64: OTP_CONFIG_ID (0x0044)

Bit	Type	Field Name	Description	Reset
[7:0]	R	CONFIG_REV	OTP variant code	0xDC

6 Package Information

6.1 Package Outlines



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.500	0.530	0.560	0.0197	0.0209	0.0220
A1	0.185	0.200	0.215	0.0073	0.0079	0.0085
c1	0.022	0.025	0.028	0.0009	0.0010	0.0011
c	0.280	0.305	0.330	0.0110	0.0120	0.0130
D	2.120	2.145	2.170	0.0835	0.0844	0.0854
E	2.520	2.545	2.570	0.0992	0.1002	0.1012
b	0.230	0.260	0.290	0.0091	0.0102	0.0114
D1	---	1.6000	---	---	0.0630	---
E1	---	2.0000	---	---	0.0787	---
D2	---	0.2725	---	---	0.0107	---
E2	---	0.2725	---	---	0.0107	---
D3	---	0.2725	---	---	0.0107	---
E3	---	0.2725	---	---	0.0107	---
aaa		0.03			0.001	
bbb		0.10			0.004	
ccc		0.03			0.001	
ddd		0.05			0.002	
eee		0.05			0.002	

Figure 21: WLCSP Package Outline Diagram

7 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

Table 65: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9168-xxU72	WLCSP 30L	2.145 x 2.545 x 0.53	Tape and Reel	6000
DA9168-xxU76	WLCSP 30L	2.145 x 2.545 x 0.53	Waffle Pack	550

Where xx represents the OTP variant.

8 Application Information

8.1 Recommended External Components

Component values shown are typical values (not de-rated). For capacitors assume X5R type or better with a DC voltage rating of twice the maximum applied voltage. For inductors, the saturation current rating is equal or greater than the current limit value. The Electrical Specifications are based on the typical values where applicable.

Table 66: Recommended External Components

Parameter	Description	Conditions	Min	Typ	Max	Unit
C_{VBUS}	VBUS capacitance			1.0		µF
C_{VBUS_SNS}	VBUS_SNS capacitance			1.0		µF
C_{VMID}	VMID capacitance			10*2		µF
L_{CHG_LX}	Inductor Buck charger			2.2		µH
C_{BTS}	VBTS capacitance			47		nF
C_{VSYS}	VSYS capacitance			10*2		µF
C_{VBAT}	VBAT capacitance			2.2		µF
C_{VBAT_SNS}	VBAT_SNS capacitance			0.1		µF
C_{REF}	REF output capacitance			4.7		µF
C_{LDO1}	LDO1 output capacitance			2.2		µF
C_{LDO2}	LDO2 output capacitance			2.2		µF

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

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1-Cell, 1.5 A Battery Charger PMIC with 20 mA Termination, Ultra-Low IQ Reverse Boost, and I2C

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(Rev.1.0 Mar 2020)

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