EL7566

Monolithic 6A DC/DC Step-Down Regulator

FN7102
Rev 7.00
May 8, 2006

The EL7566 is a full-feature synchronous step-down regulator capable of up to 6A and 96% efficiency. The device operates from 3V to 6V input supply (V_{IN}). With internal CMOS power FETs, the device can operate at up to 100% duty ratio, allowing for an output voltage range of 0.8V to nearly V_{IN}. An adjustable switching frequency up to 1MHz enables the use of small components, thereby reducing board area consumption to under 0.72sq-in on one side of a PCB. The EL7566 operates in constant frequency PWM mode, making external synchronization possible. A soft-start feature is integrated in the EL7566 to limit in-rush currents and allow for a smooth voltage ramp from zero to regulation. Other start-up features are integrated to add flexibility for synchronizing many supplies in multiple configurations. The EL7566 also offers a voltage margining capability that shifts the output voltage ±5% for validation of system card performance and reliability during manufacturing tests. A junction temperature indicator conveniently monitors the silicon die temperature, saving time in thermal characterization.

An easy-to-use simulation tool is available for download and can be used to modify design parameters such as switching frequency, voltage ripple, ambient temperature, as well as view schematics waveforms, efficiency graphs, and complete BOM with Gerber layout.

Features

- Integrated MOSFETs
- 6A continuous output current
- Up to 96% efficiency
- Multiple supply start-up tracking
- Built-in ±5% voltage margining
- 3V to 6V input voltage
- 0.72 in^2 footprint with components on one side of PCB
- Adjustable switching frequency to 1MHz
- Oscillator synchronization possible
- 100% duty ratio
- Junction temperature indicator
- Over-temperature protection
- Internal soft-start
- Variable output voltage down to 0.8V
- Power-good indicator
- 28 Ld HTSSOP package
- Pb-free plus anneal available (RoHS compliant)

Applications

- Point-of-regulation power supplies
- FPGA Core and I/O supplies
- DSP, CPU Core, and IO supplies
- Logic/Bus supplies
- Portable equipment

Related Documentation

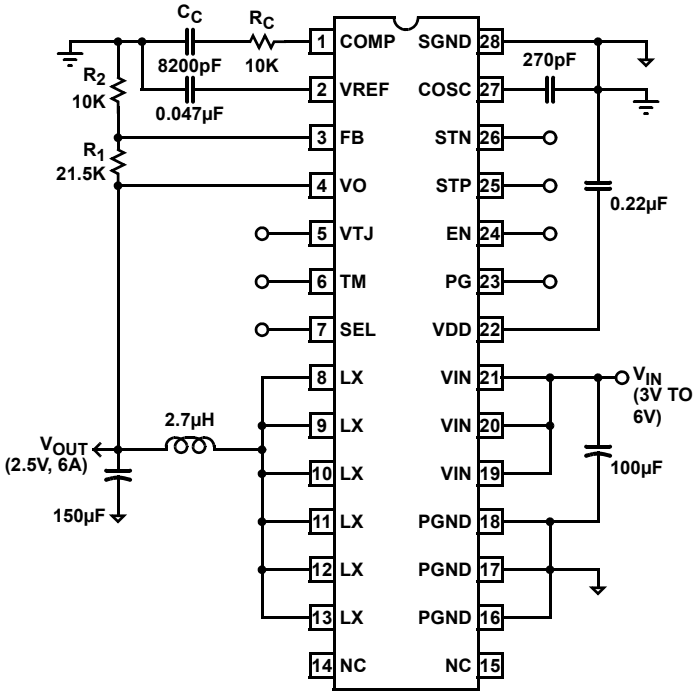
- Technical Brief 415 - Using the EL7566 Demo Board
- Easy-to-use applications software simulation tool available at www.intersil.com/dc-dc

Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
EL7566DRE	7566DRE	-	0 to 85	28 Ld HTSSOP	MDP0048
EL7566DRE-T7	7566DRE	7”	0 to 85	28 Ld HTSSOP	MDP0048
EL7566DRE-T13	7566DRE	13”	0 to 85	28 Ld HTSSOP	MDP0048
EL7566DREZ (Note)	7566DREZ	-	0 to 85	28 Ld HTSSOP (Pb-free)	MDP0048
EL7566DREZ-T7 (Note)	7566DREZ	7”	0 to 85	28 Ld HTSSOP (Pb-free)	MDP0048
EL7566DREZ-T13 (Note)	7566DREZ	13”	0 to 85	28 Ld HTSSOP (Pb-free)	MDP0048
EL7566AIREZ (Note)	7566AIREZ		-40 to 85	28 Ld HTSSOP (Pb-free)	MDP0048
EL7566AIREZ-T7 (Note)	7566AIREZ	7”	-40 to 85	28 Ld HTSSOP (Pb-free)	MDP0048
EL7566AIREZ-T13 (Note)	7566AIREZ	13”	-40 to 85	28 Ld HTSSOP (Pb-free)	MDP0048

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Typical Application Diagram



Absolute Maximum Ratings (T_A = 25°C)

V_{IN}, V_{DD} to SGND . . . . . -0.3V to +6.5V
VX to PGND . . . . . -0.3V to V_{IN} +0.3V
SGND to PGND . . . . . -0.3V to +0.3V
COMP, V_{REF}, FB, V_O, V_{TJ}, TM,
SEL, PG, EN, STP, STN, C_{OSC} to SGND . . . . . -0.3V to V_{DD} +0.3V

Storage Temperature . . . . . -65°C to +150°C
Junction Temperature . . . . . +125°C
Operating Ambient Temperature DRE . . . . . 0°C to +85°C
Operating Ambient Temperatute AIRE . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Specifications

$V_{DD} = V_{IN}$ = 3.3V, $T_A = T_J$ = 25°C, C_{OSC} = 390pF, Unless Otherwise Specified

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		3		6	V
V_{REF}	Reference Accuracy		1.24	1.26	1.28	V
V_{REFTC}	Reference Temperature Coefficient			50		ppm/°C
$V_{REFLOAD}$	Reference Load Regulation	$0 < I_{REF} < 50\mu A$	-1			%
V_{RAMP}	Oscillator Ramp Amplitude			1.15		V
I_{OSC_CHG}	Oscillator Charge Current	$0.1V < V_{OSC} < 1.25V$		200		µA
I_{OSC_DIS}	Oscillator Discharge Current	$0.1V < V_{OSC} < 1.25V$		8		mA
I_{VDD}	V_{DD} Supply Current	V_{EN} = 1 (L disconnected)	2	2.7	5	mA
I_{VDD_OFF}	V_{DD} Standby Current	EN = 0		1	1.5	mA
V_{DD_OFF}	V_{DD} for Shutdown		2.4		2.65	V
V_{DD_ON}	V_{DD} for Startup		2.6		2.95	V
T_{OT}	Over-temperature Threshold			135		°C
T_{HYS}	Over-temperature Hysteresis			20		°C
I_{LEAK}	Internal FET Leakage Current	EN = 0, L_X = 6V (low FET), L_X = 0V (high FET)			10	µA
I_{LMAX}	Peak Current Limit		7.8			A
R_{DSON1}	PMOS On Resistance			29	50	mΩ
$R_{DSONTC2}$	NMOS On Resistance			25		mΩ
R_{DSONTC}	R_{DSON} Tempco			0.2		mΩ/°C
I_{STP}	STP Pin Input Pull-down Current	$V_{STP} = V_{IN}/2$	-4	2.5		µA
I_{STN}	STN Pin Input Pull-up Current	$V_{STN} = V_{IN}/2$		2.5	4	µA
V_{PGP}	Positive Power Good Threshold	With respect to target output voltage	6		14	%
V_{PGN}	Negative Power Good Threshold	With respect to target output voltage	-14		-6	%
V_{PG_HI}	Power Good Drive High	I_{PG} = 1mA	2.6			V
V_{PG_LO}	Power Good Drive Low	I_{PG} = -1mA			0.5	V
V_{OVP}	Output Overvoltage Protection			10		%
V_{FB}	Output Initial Accuracy	I_{LOAD} = 0A	0.79	0.8	0.81	V
V_{FB_LINE}	Output Line Regulation	V_{IN} = 3.3V, ΔV_{IN} = 10%, I_{LOAD} = 0A		0.2	0.5	%
GM_{EA}	Error Amplifier Transconductance	V_{CC} = 0.65V	85	125	165	µs
V_{FB_TC}	Output Temperature Stability	$0°C < T_A < 85°C$, I_{LOAD} = 3A		±1		%
F_S	Switching Frequency		300	370	440	kHz
I_{FB}	Feedback Input Pull-up Current	V_{FB} = 0V		100	200	nA

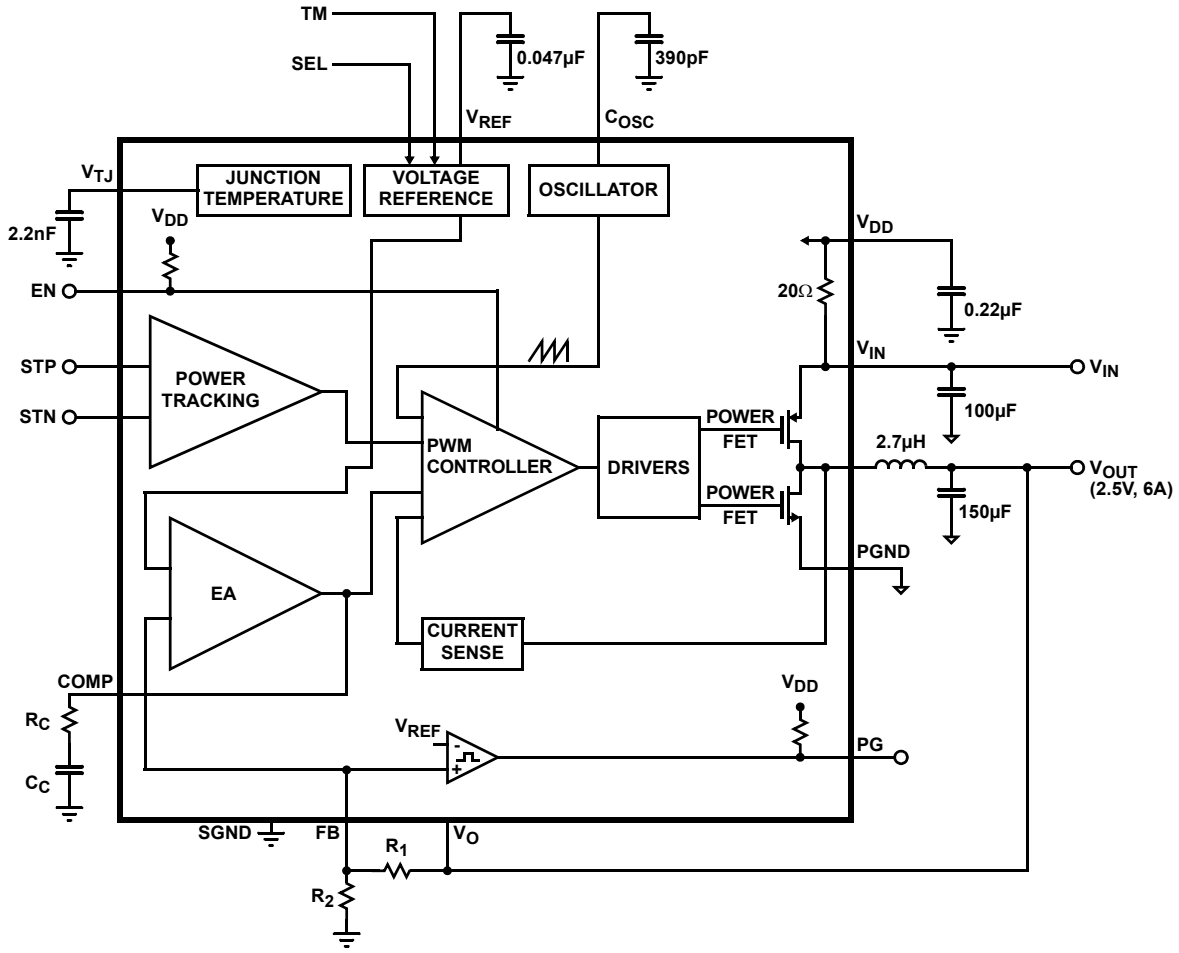
DC Electrical Specifications $V_{DD} = V_{IN} = 3.3V$, $T_A = T_J = 25°C$, $C_{OSC} = 390pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{EN_HI}	EN Input High Threshold		2.6			V
V_{EN_LO}	EN Input Low Threshold				1	V
I_{EN}	Enable Pull-up Current	$V_{EN} = 0$	-4	-2.5		µA
TM, S_{EL_HI}	Input High Level		2.6			V
TM, S_{EL_LO}	Input Low Level				1	V

Pin Descriptions

PIN NUMBER	PIN NAME	PIN FUNCTION
1	COMP	Error amplifier output; place loop compensation components here
2	VREF	Bandgap reference bypass capacitor; typically 0.022µF to 0.047µF to SGND
3	FB	Voltage feedback input; connected to external resistor divider between V_{OUT} and SGND for adjustable output; also used for speed-up capacitor connection
4	VO	Output sense for fixed output option. This pin can be open for EL7566
5	VTJ	Junction temperature monitor output
6	TM	Stress test enable; allows ±5% output movement; connect to SGND if function is not used
7	SEL	Positive or negative stress select; see text
8, 9, 10, 11, 12, 13	LX	Inductor drive pin; high current output whose average voltage equals the regulator output voltage
14, 15	NC	Not used
16, 17, 18	PGND	Ground return of the regulator; connected to the source of the low-side synchronous NMOS Power FET
19, 20, 21	VIN	Power supply input of the regulator; connected to the drain of the high-side PMOS Power FET
22	VDD	Control circuit positive supply; connected to V_{IN} through an internal 20Ω resistor
23	PG	Power-good window comparator output; logic 1 when regulator output is within ±10% of target output voltage
24	EN	Chip enable, active high; a 2.5µA internal pull-up current enables the device if the pin is left open; a capacitor can be added at this pin to delay the start of a converter
25	STP	Auxilliary supply tracking positive input; tied to regulator output to synchronize start-up with a second supply; leave open for standalone operation; 2µA internal pull-up current
26	STN	Auxiliary supply tracking negative input; connect to output of a second supply to synchronize start-up; leave open for standalone operation; 2µA internal pull-up current
27	COSC	Oscillator timing capacitor (see performance curves)
28	SGND	Control circuit negative supply or signal ground

Block Diagram



Typical Performance Curves

$V_{IN} = V_D = 5V$, $V_O = 2.5V$, $I_O = 6A$, $f_S = 500kHz$, L = 2.7µH, $C_{IN} = 100µF$, $C_{OUT} = 150µF$, $T_A = 25°C$ unless otherwise noted.

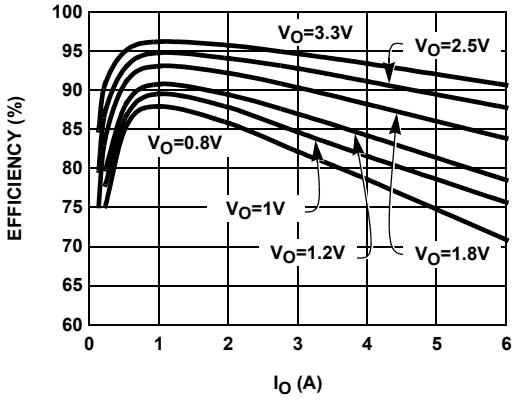


FIGURE 1. EFFICIENCY (V_{IN} = 5V)

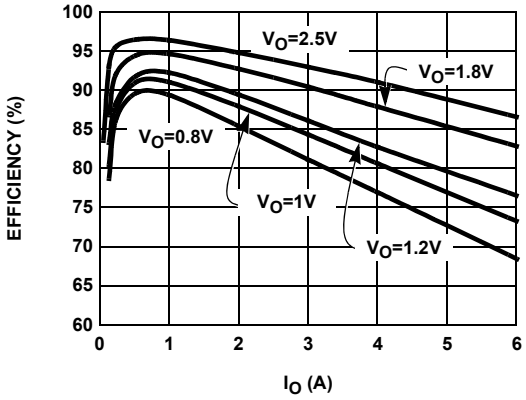


FIGURE 2. EFFICIENCY (V_{IN} = 3.3V)

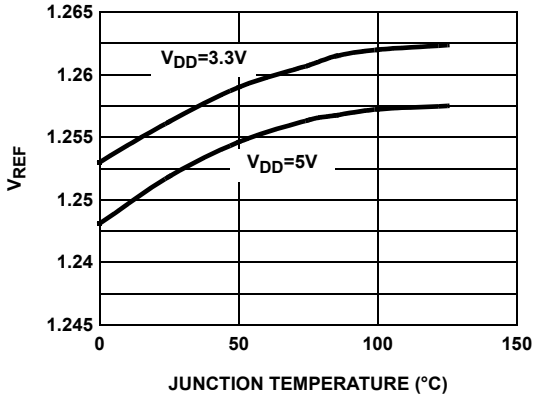


FIGURE 3. V_{REF} vs TEMPERATURE

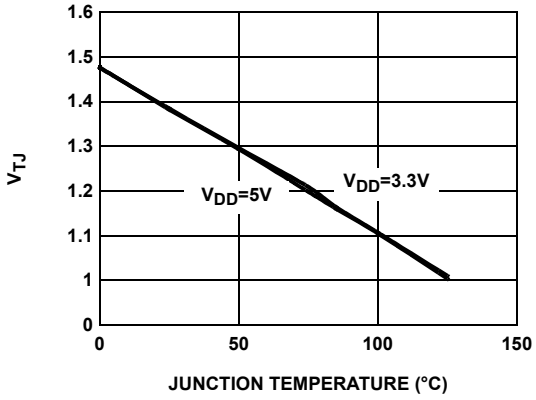


FIGURE 4. V_{TJ} vs TEMPERATURE

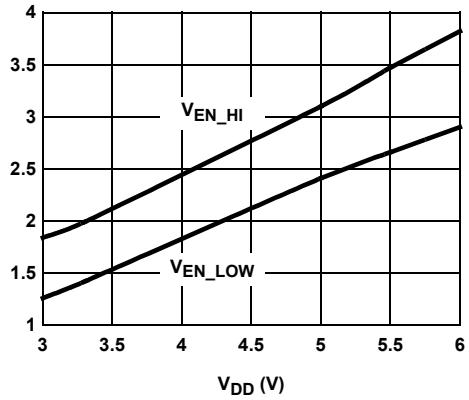


FIGURE 5. V_{EN_HI} & V_{EN_LOW} vs V_{DD}

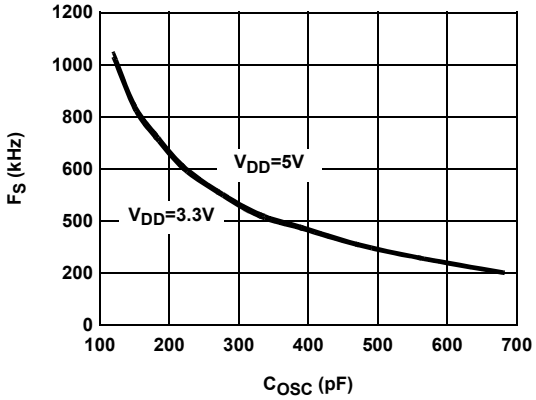


FIGURE 6. F_S vs C_{OSC}

Typical Performance Curves

$V_{IN} = V_D = 5V$, $V_O = 2.5V$, $I_O = 6A$, $f_S = 500kHz$, L = 2.7µH, $C_{IN} = 100µF$, $C_{OUT} = 150µF$, $T_A = 25°C$ unless otherwise noted. **(Continued)**

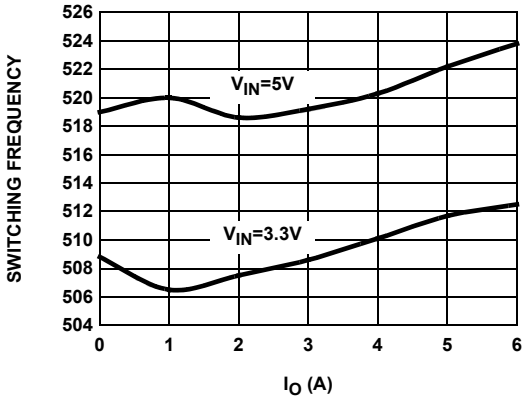


FIGURE 7. F_S vs LOAD CURRENT

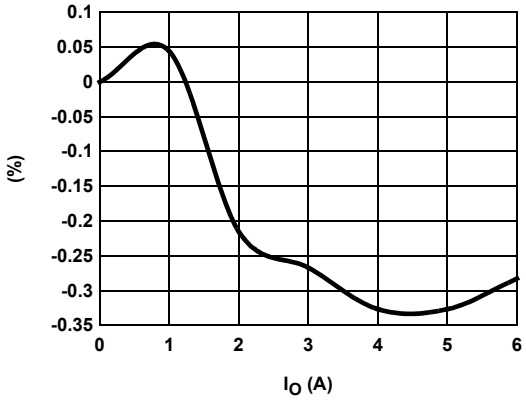


FIGURE 8. LOAD REGULATIONS

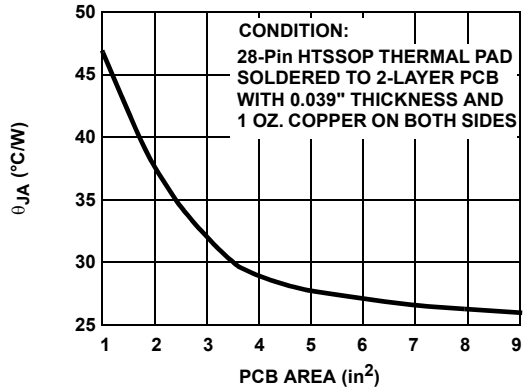


FIGURE 9. HTSSOP THERMAL RESISTANCE vs PCB AREA (NO AIR FLOW)

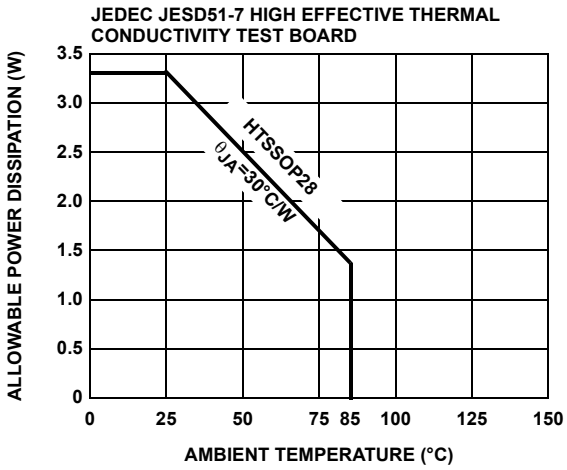


FIGURE 10. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

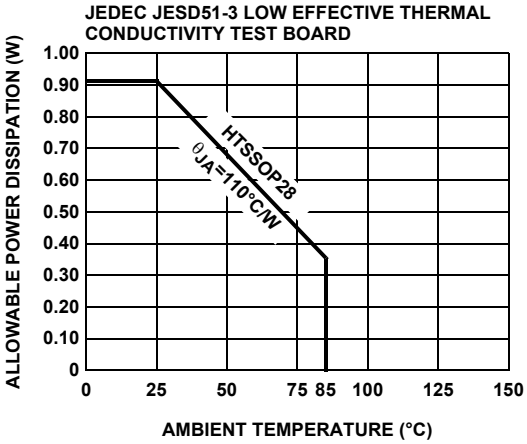


FIGURE 11. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Waveforms

V_{IN} = V_D = 5V, V_O = 2.5V, I_O = 6A, f_S = 500kHz, L = 2.7µH, C_{IN} = 100µF, C_{OUT} = 150µF, T_A = 25°C unless otherwise noted.

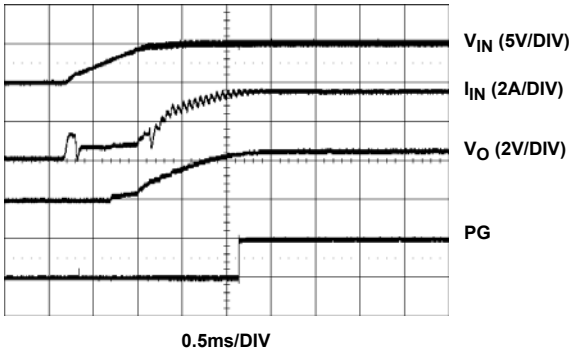


FIGURE 12. START-UP

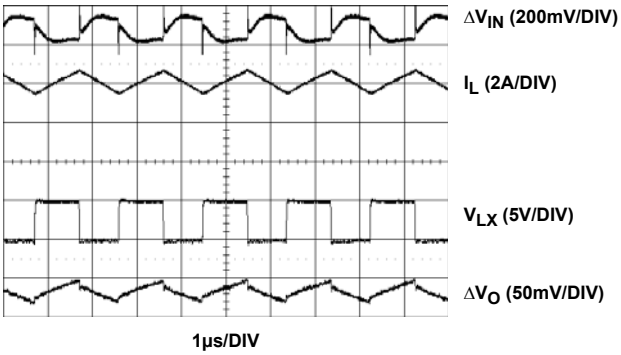


FIGURE 13. STEADY-STATE OPERATION

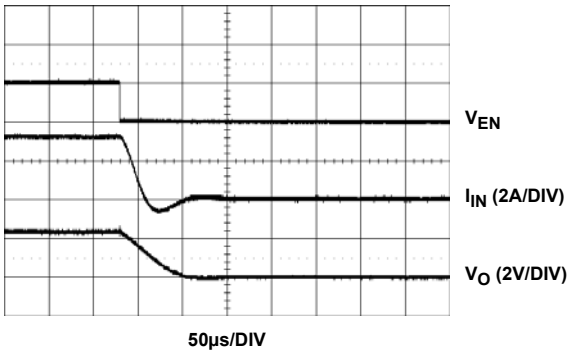


FIGURE 14. SHUT-DOWN

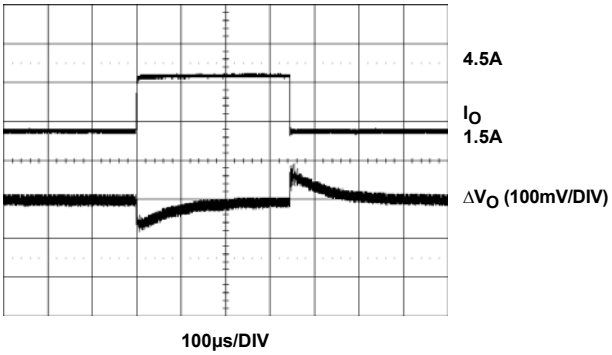


FIGURE 15. TRANSIENT RESPONSE

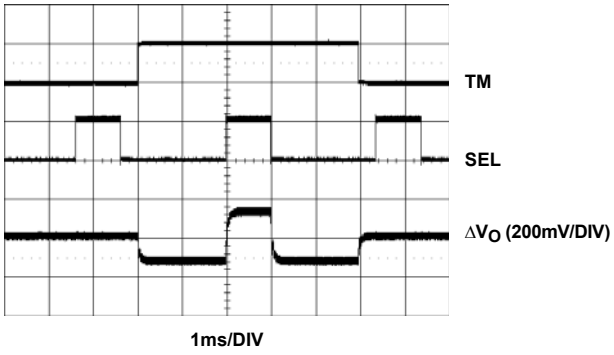


FIGURE 16. VOLTAGE MARGINING

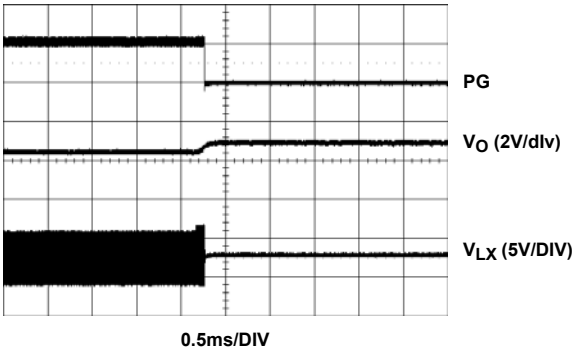


FIGURE 17. OVERVOLTAGE SHUT-DOWN

Waveforms

V_{IN} = V_D = 5V, V_O = 2.5V, I_O = 6A, f_S = 500kHz, L = 2.7µH, C_{IN} = 100µF, C_{OUT} = 150µF, T_A = 25°C unless otherwise noted. **(Continued)**

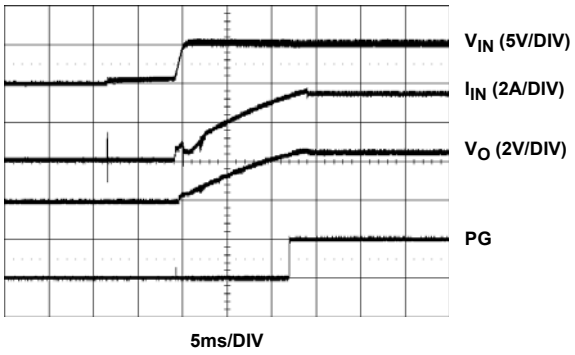


FIGURE 18. ADJUSTABLE START-UP

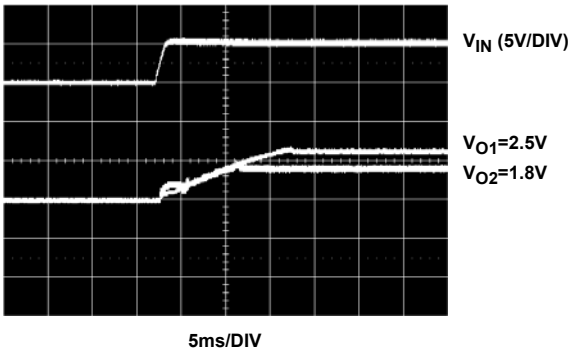


FIGURE 19. TRACKING START-UP

Detailed Description

The EL7566 is a 6A capable buck regulator operating from an input voltage range of 3V to 6V. The duty cycle can be adjusted from 0% to 100% allowing for a wide range of programmable output voltages. Patented on-chip resistorless current-sensing enables current mode control for excellent step load response. Overcurrent, Overvoltage, input Undervoltage, and thermal protection is integrated along with soft-start and power-up sequencing features to produce an overall robust power solution for general purpose applications.

EL7566DRE vs. EL7566AIRE

The EL7566AIRE includes the following feature changes from the EL7566DRE:

- Up to 6A Current *Sinking* Capability
- Expanded Temperature Range: -40°C to 85°C
- No Overvoltage Protection

Start-Up

The EL7566 employs a digital soft-start feature to suppress the in-rush current needed to charge the output capacitance and smoothly ramp the output voltage to regulation (See Figure 12). The normal start-up process begins when the input voltage reaches the rising POR threshold (~2.8V) and EN pin is transitioned HIGH by an internal 2.5µA current source. The output voltage is then digitally ramped to regulation over a 2ms period. The 2ms soft start-up time can be extended if needed by configuring the STP and STN pins. (refer to Full Start-Up Control section).

If the input voltage is ramped slowly, soft-start may be initiated before the input supply has reached regulation. The lower input voltage will have increased current demand during start-up and may risk an overcurrent event. To prevent such an event from occurring, a capacitor can be placed from the EN pin to GND to program a delay between when the rising POR threshold for VIN is met and when soft-start begins. The programmable delay time, T_D, is governed by Equation 1.

$$T_D = C_{EN} \times \frac{V_{EN\_HI}}{I_{EN}}$$

where:

- C_{EN} is the capacitance at EN pin
- V_{EN_HI} is the EN input high level (function of V_{DD} voltage, see Figure 5)
- I_{EN} is the EN pin pull-up current, nominal 2.5µA

Steady-State Operation

Under all steady-state conditions the converter will operate in fixed frequency continuous-conduction mode. For fast transient response and ease of controllability, a peak current-mode control method is employed. The inductor current is sensed from the upper PMOS. This current signal serves as the ramp to the PWM comparator and is compared against the difference signal generated by the transconductance error amplifier. Slope compensation for the ramp is used to allow for 100% duty cycle operation (see Figure 20). The pulse-width modulated square wave output of the PWM comparator is amplified and serves as the gate drive signals for the switching power FETs.

100% DUTY RATIO

EL7566 uses CMOS as internal synchronous power switches. The upper and lower switches are PMOS and NMOS respectively. The upper PMOS saves the need for a boot capacitor normally seen in NMOS/NMOS half-bridges.

It also allows 100% turn-on of the upper PMOS switch, achieving V_O close to V_{IN}. The maximum achievable V_O is:

$$V_O = V_{IN} - (R_L + R_{DSON1}) \times I_O$$

Where R_L is the DC resistance on the inductor and R_{DSON1} is the PMOS on-resistance, nominally 30mΩ at room temperature with a temperature coefficient of 0.2mΩ/°C.

OUTPUT VOLTAGE SELECTION

The output voltage can be as high as the input voltage minus the PMOS and inductor voltage drops (as seen previously in Equation 2). Referring to the Typical Application Circuit on page 2, use R_1 and R_2 to set the output voltage according to the following formula:

$$V_O = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Some standard values of R_1 and R_2 are listed in Table 1.

TABLE 1.

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	2	Open
1	2.49	10
1.2	4.99	10
1.5	10	11.5
1.8	12.7	10.2
2.5	21.5	10
3.3	36	11.5

It is important that the series combination of R1 and R2 is large enough as to not draw excessive current from the output.

VOLTAGE MARGINING

The EL7566 has built-in 5% load stress test (commonly called voltage margining) function. Combinations of TM and SEL set the margins shown in Table 2. When this function is not used, both pins should be connected to SGND, either directly or through a 10kΩ resister. Figure 16 shows this feature.

TABLE 2.

CONDITION	TM	SEL	V_O
Normal	0	X	Nominal
High Margin	1	1	Nominal + 5%
Low Margin	1	0	Nominal - 5%

SWITCHING FREQUENCY

The regulator has a programmable switching frequency of 200kHz to 1MHz. The switching frequency is generated by a relaxation comparator and adjusted by a capacitor from the OSC pin to GND (C_{OSC}). The triangle waveform has 95% duty ratio and runs from 0.2V to 1.2V. Refer to the curve in Figure 6 for the appropriate value of C_{OSC} for the desired frequency. If external synchronization is desired, the circuit in Figure 21 can be used.

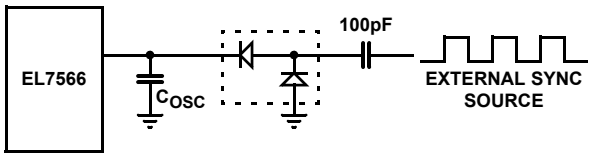


FIGURE 20. EXTERNAL SYNC CIRCUIT

Always choose the converter self-switching frequency 20% lower than the sync frequency to accommodate component variations.

Protection Features

The EL7566 features a wide range of protective measures to prevent the persistence of damaging system conditions. These features are overvoltage, overcurrent, Power-On-Reset (POR), and Thermal Shutdown protection.

OVERVOLTAGE PROTECTION (OVP)

The EL7566 monitors the output voltage and will shut down if it exceeds 110% of the set regulation point. This is accomplished by comparing the reference to the FB pin voltage. If an overvoltage condition is met, the controller will turn the high-side switch off, the low-side switch on, and pull PGOOD low. The converter will not latch off and will proceed with a soft-start as soon as the fault condition is cleared.

OVERCURRENT PROTECTION (OCP)

The current information for PWM ramp generation is also used for overcurrent protection. The measured current is compared against a preset Overcurrent threshold (~7-10A). If the output current exceeds the threshold, the output will shut down by turning off the high-side switch and turning the low-side switch on. This event, like OVP, will not latch the converter off. A soft-start will be initiated when the fault is cleared.

POWER-ON RESET (POR)

To ensure proper regulator operation, a power-on reset feature monitors the input voltage. When adequate input voltage is achieved (V_{DD} > 2.8V), the converter is allowed to soft-start. However, if V_{DD} falls below 2.5V, the regulator will shut down in the same manner as OVP or OCP.

THERMAL PROTECTION AND JUNCTION TEMPERATURE INDICATOR

An internal temperature sensor continuously monitors the junction temperature. If the junction temperature exceeds 135°C, the regulator is in a fault condition and will shut down. When the temperature falls back below 110°C, the regulator goes through the soft-start procedure again.

The V_{TJ} pin reports a voltage proportional to the junction temperature. Equation 3 illustrates the relationship and can be used to accurately evaluate thermal design points.

$$T_J = 75 + \frac{1.2 - V_{TJ}}{0.00384}$$

Full Start-Up Control

The EL7566 offers full start-up control. The core of this control is a start-up comparator in front of the main PWM controller. The STP and STN are the inputs to the comparator, whose HI output forces the PWM comparator to skip switching cycles. The user can choose any of the following control configurations:

ADJUSTABLE SOFT-START

In this configuration, the ramp-up time is adjustable to any time longer than the building soft-start time of 2ms. The approximate ramp-up time, T_{ST}, is:

$$T_{ST} = RC\left(\frac{V_O}{V_{IN}}\right)$$

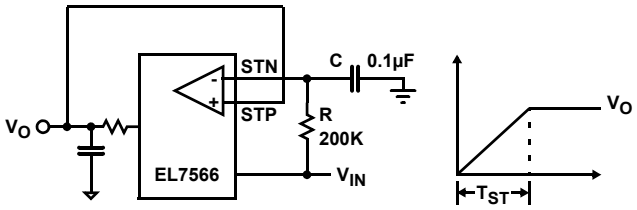


FIGURE 21. ADJUSTABLE START-UP

CASCADE START-UP

In this configuration, EN pin of Regulator 2 is connected to the PG pin of Regulator 1 (Figure 22). V_{O2} will only start after V_{O1} is good.

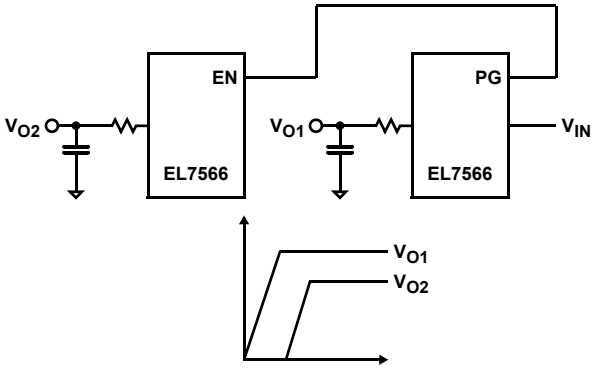


FIGURE 22. CASCADE START-UP

LINEAR START-UP

In the linear start-up tracking configuration, the regulator with lower output voltage, V_{O2}, tracks the one with higher output voltage, V_{O1}.

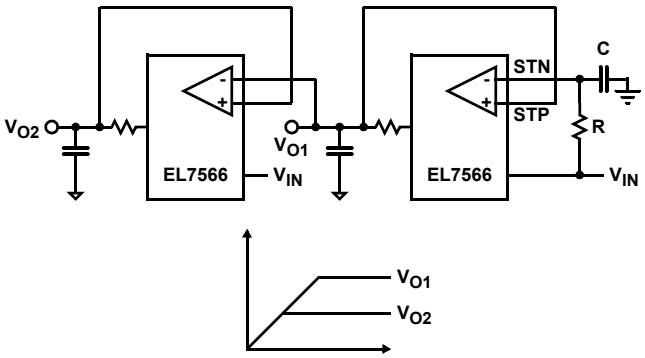


FIGURE 23. LINEAR START-UP TRACKING

OFFSET START-UP

Compared with the cascade start-up, this configuration allows Regulator 2 to begin the start-up process when V_{O1} reaches a particular value of $V_{REF}*(1+R_B/R_A)$ before PG goes HI, where V_{REF} is the regulator reference voltage. V_{REF}=1.26.

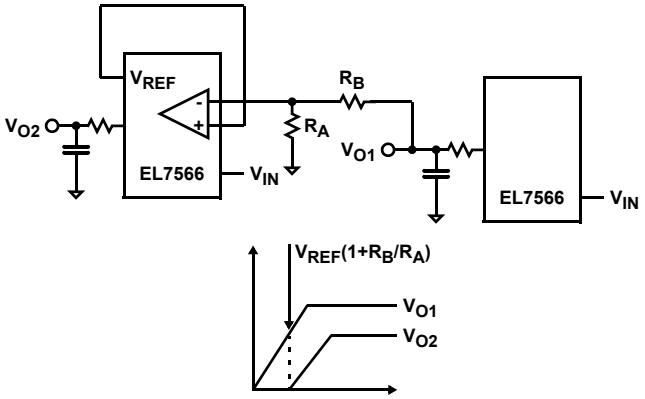


FIGURE 24. OFFSET START-UP TRACKING

Component Selection

INPUT CAPACITOR

The main functions of the input capacitor(s) are to maintain the input voltage steady and to filter out the pulse current passing through the upper switch. The root-mean-square value of this current is:

$$I_{IN,RMS} = \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}} \times I_O \approx 1/2(I_O)$$

for a wide range of V_{IN} and V_O.

For long-term reliability, the input capacitor or combination of capacitors must have the current rating higher than $I_{IN,RMS}$. Use X5R or X7R type ceramic capacitors, or SPCAP or POSCAP types of Polymer capacitors for their high current handling capability.

INDUCTOR

The NMOS positive current limit is set at about 8A. For optimal operation, the peak-to-peak inductor current ripple ΔI_L should be less than 1A. The following equation gives the inductance value:

$$L = \frac{(V_{IN} - V_O) \times V_O}{V_{IN} \times \Delta I_L \times F_S}$$

The peak current the inductor sees is:

$$I_{LPK} = I_O + \frac{\Delta I_L}{2}$$

When inductor is chosen, it must be rated to handle the peak current and the average current of I_O.

OUTPUT CAPACITOR

Output voltage ripple and transient response are the predominant factors when choosing the output capacitor. Initially, output capacitance should be sized with an ESR to satisfy the output ripple ΔV_O requirement:

$$\Delta V_O = \Delta I_L \times ESR$$

When a step load change, ΔI_O, is applied to the converter, the initial voltage drop can be approximated by ESR*ΔI_O. The output voltage will continue to drop until the control loop begins to correct the output voltage error. Increasing the output capacitance will lessen the impact of load steps on output voltage. Increasing loop bandwidth will also reduce output voltage deviation under step load conditions. Some experimentation with converter bandwidth and output filtering will be necessary to generate a good transient response (Reference Figure 15).

As with the input capacitor, it is recommended to use X5R or X7R type of ceramic capacitors. SPCAP or POSCAP type Polymer capacitors can also be used for the low ESR and high capacitance requirements of these converters.

Generally, the AC current rating of the output capacitor is not a concern because the RMS current is only 1/8 of ΔI_L.

LOOP COMPENSATION

Current-mode control in system forces the inductor current to be proportional to the error signal. This has the advantage of eliminating the double pole response of the output filter, and reducing complexity in the overall loop compensation. A simple Type 1 compensator is adequate to generate a stable, high-bandwidth converter. The compensation resister is decided by:

$$R_C = \frac{I_O}{VFB} \times \frac{F_C \times 2 \times \pi \times (ESR + R_{OUT}) \times C_{OUT}}{GM_{PWM} \times GM_{EA}}$$

where:

- GM_{PWM} is the transconductance of the PWM comparator, GM_{PWM} = 120S

$$R_{OUT} = \frac{V_O}{I_O}$$

- ESR is the ESR of the output capacitor
- C_{OUT} is output capacitance
- GM_{EA} is the transconductance of the error amplifier, GM_{EA} = 120µS
- F_C is the intended crossover frequency of the loop. For best performance, set this value to about one-tenth of the switching frequency.
- Once R_C is chosen, C_C is decided by:

$$C_C = 1.5 \times C_{OUT} \times \frac{R_{OUT}}{R_C}$$

Design Example

A 5V to 2.5V converter with a 6A load requirement.

1. Choose the input capacitor

The input capacitor or combination of capacitors has to be able to take about 1/2 of the output current, e.g., 3A. Panasonic EEFUD0J101XR is rated at 3.3A, 6.3V, meeting the above criteria.

2. Choose the inductor. Set the converter switching frequency at 500kHz:

$$L = \frac{(V_{IN} - V_O) \times V_O}{V_{IN} \times \Delta I_L \times F_S}$$

ΔI_L = 1A yields 2.3µH. Leave some margin and choose L = 2.7µH. Coilcraft's DO3316P-272HC has the required current rating.

3. Choose the output capacitor

L = 2.7µH yields about 1A inductor ripple current. If 25mV of ripple is desired, C_{OUT}'s ESR needs to be less than 25mΩ. Panasonic's EEFUD0G151XR 150µF has an ESR of 12mΩ and is rated at 4V.

ESR is not the only factor deciding the output capacitance. As discussed earlier, output voltage droops less with more capacitance when converter is in load transient. Multiple iterations may be needed before final components are chosen.

4. Loop compensation

50kHz is the intended crossover frequency. With the conditions R_C and C_C are calculated as:

R_C = 10.5kΩ and C_C = 8900pF, round to standard value of 8200pF.

For convenience, Table 3 lists the compensation values for frequently used output voltages.

TABLE 3. COMPENSATION VALUES

V_O (V)	R_C (kΩ)	C_C (pF)
3.3	13.7	8200
2.5	10.5	8200
1.8	7.68	8200
1.5	6.49	8200
1.2	5.23	8200
1	4.42	8200
0.8	3.57	8200

Thermal Management

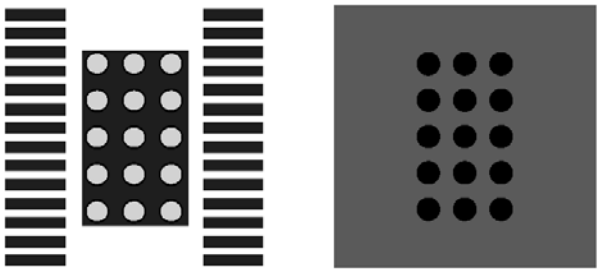
The EL7566 is packaged in a thermally-efficient HTSSOP-28 package, which utilizes the exposed thermal pad at the bottom to spread heat through PCB metal.

Therefore:

1. The thermal pad must be soldered to the PCB.
2. Maximize the PCB area.
3. If a multiple layer PCB is used, thermal vias (13 to 25 mil) must be placed underneath the thermal pad to connect to ground plane(s). Do not place thermal reliefs on the vias. Figure 25 shows a typical connection.

The thermal resistance for this package is as low as 26°C/W for 2 layer PCB of 0.39" thickness (See Figure 9). The actual junction temperature can be measured at V_{TJ} pin.

The thermal performance of the IC is heavily dependent on the layout of the PCB. The user should exercise care during the design phase to ensure the IC will operate within the recommended environmental conditions.



COMPONENT SIDE CONNECTION **GROUND PLANE CONNECTION**

FIGURE 25. PCB LAYOUT - 28-PIN HTSSOP PACKAGE

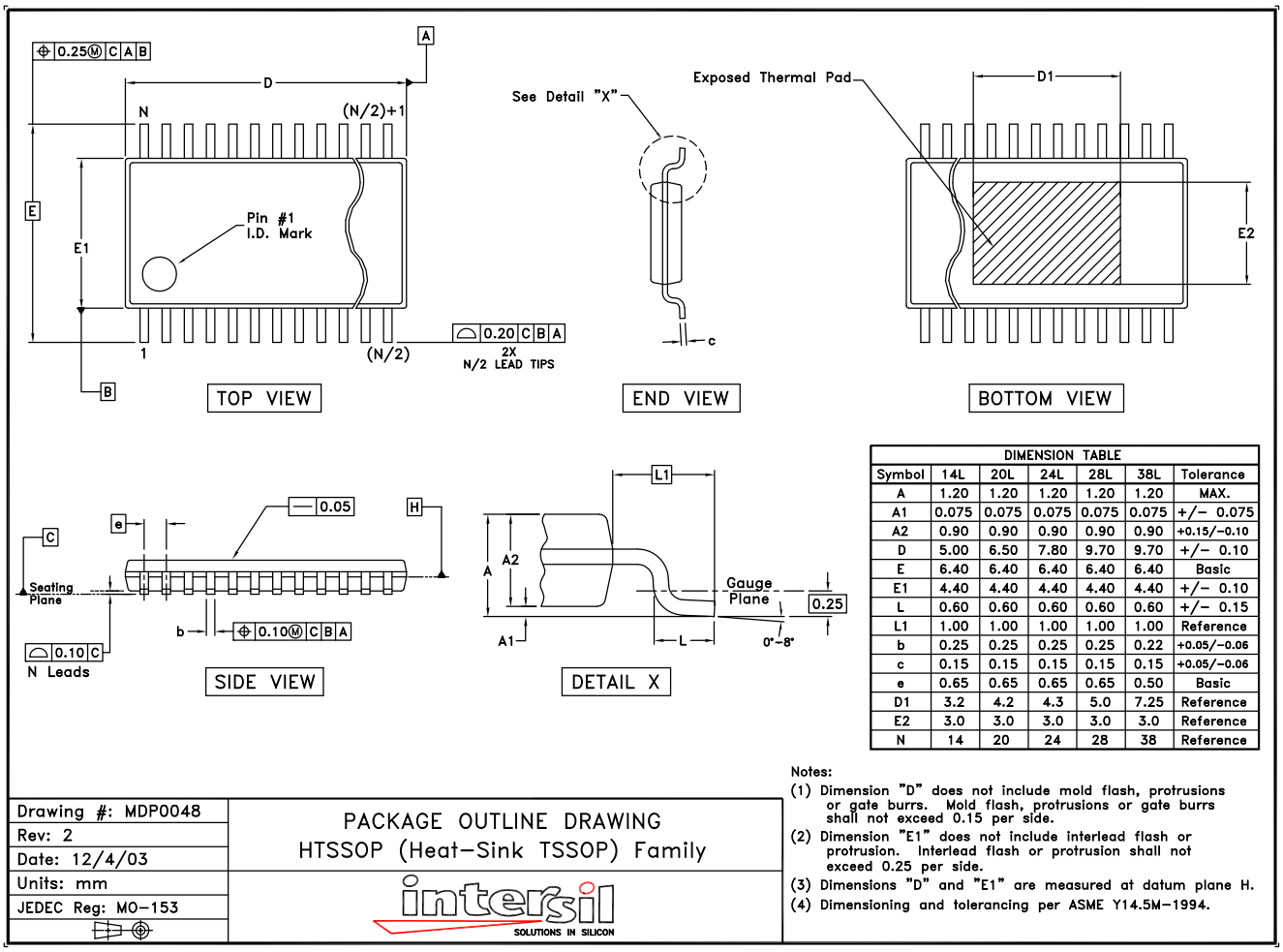
Layout Considerations

The layout is very important for the converter to function properly. Follow these tips for best performance:

1. Separate the Power Ground (⏚) and Signal Ground (⏚); connect them only at one point right at the SGND pin
2. Place the input capacitor(s) as close to V_{IN} and PGND pins as possible
3. Make as small as possible the loop from LX pins to L to C_O to PGND pins
4. Place R_1 and R_2 pins as close to the FB pin as possible
5. Maximize the copper area around the PGND pins; do not place thermal relief around them
6. Thermal pad should be soldered to PCB. Place several via holes under the chip to the ground plane to help heat dissipation

The demo board is a good example of layout based on this outline. Please refer to the EL7566 Application Brief.

Package Outline Drawing



DIMENSION TABLE						
Symbol	14L	20L	24L	28L	38L	Tolerance
A	1.20	1.20	1.20	1.20	1.20	MAX.
A1	0.075	0.075	0.075	0.075	0.075	+/− 0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/−0.10
D	5.00	6.50	7.80	9.70	9.70	+/− 0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	+/− 0.10
L	0.60	0.60	0.60	0.60	0.60	+/− 0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
b	0.25	0.25	0.25	0.25	0.22	+0.05/−0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/−0.06
e	0.65	0.65	0.65	0.65	0.50	Basic
D1	3.2	4.2	4.3	5.0	7.25	Reference
E2	3.0	3.0	3.0	3.0	3.0	Reference
N	14	20	24	28	38	Reference

Notes:
(1) Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
(2) Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
(3) Dimensions "D" and "E1" are measured at datum plane H.
(4) Dimensioning and tolerancing per ASME Y14.5M−1994.

Drawing #: MDP0048	PACKAGE OUTLINE DRAWING HTSSOP (Heat−Sink TSSOP) Family
Rev: 2	
Date: 12/4/03	
Units: mm	
JEDEC Reg: MO−153	

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp