

Description

The F1421 is a high gain / high linearity RF amplifier used in high-performance RF applications. The F1421 provides 20.3dB gain with a +40dBm OIP3 and 5.5dB noise figure at 1.9GHz. This device uses a single 5V supply and 138mA of I_{CC} .

In typical base stations, RF amplifiers are used in the RX and TX traffic paths to boost signal levels. The F1421 amplifier offers very high reliability due to its construction using silicon die in a QFN package.

Typical Applications

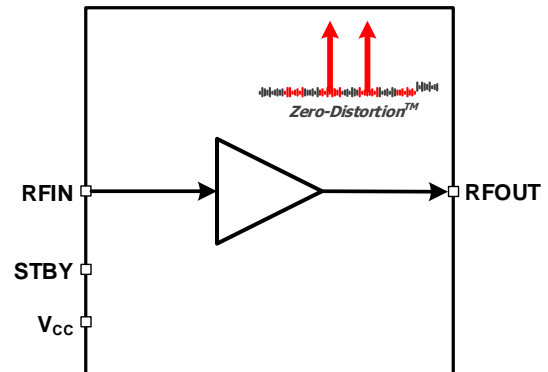
- Multi-mode, multi-carrier transmitters
- PCS1900 base stations
- DCS1800 base stations
- WiMAX and LTE base stations
- UMTS/WCDMA 3G base stations
- PHS/PAS base stations
- Public safety infrastructure

Features

- Broadband 1.7GHz to 2.2GHz
- 20.3dB typical gain at 1.9GHz
- 5.5dB noise figure at 1.9GHz
- +40dBm OIP3 at 1.9GHz
- +23dBm output P1dB at 1.9GHz
- Single 5V supply voltage
- $I_{CC} = 138\text{mA}$
- -40°C to $+105^{\circ}\text{C}$ operating temperature
- 50Ω single-ended input / output impedances
- Standby mode for power savings
- 4mm x 4mm, 24-pin QFN package

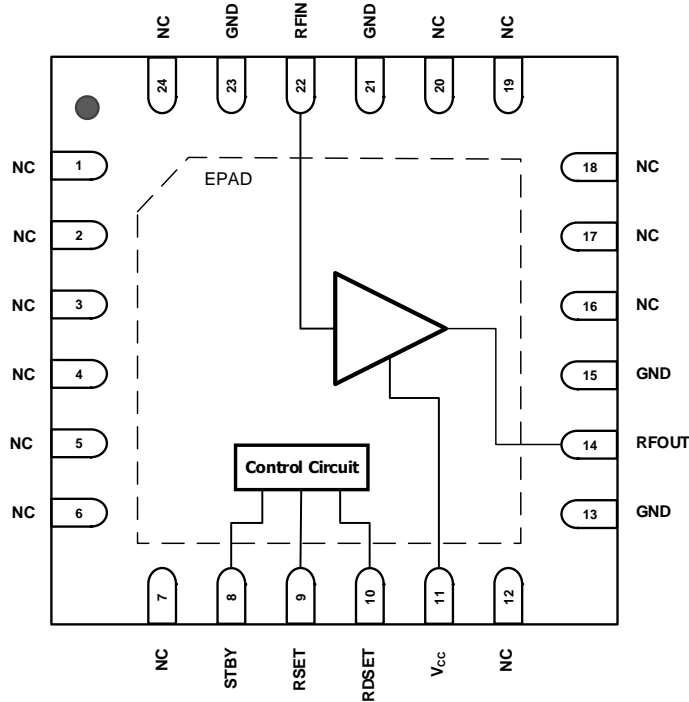
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 4mm x 4mm x 0.9mm QFN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

| Number | Name | Description |
|------------------------|-----------------|---|
| 1 - 7, 12, 16 - 20, 24 | NC | No internal connection. These pins can be left unconnected, have a voltage applied, or be connected to ground (recommended). |
| 8 | STBY | Standby (HIGH = device power OFF, LOW/Open = device power ON). Internally this pin has a pull-down resistor that is connected to GND. |
| 9 | RSET | Amplifier bias current setting resistor. Connect a 2.26kΩ resistor to ground. |
| 10 | RDSET | Amplifier second bias current setting resistor. Connect a 5.76kΩ resistor to ground. |
| 11 | V _{CC} | Power supply for the amplifier. |
| 13, 15, 21, 23 | GND | Internally grounded. These pins must be grounded as close to the device as possible. |
| 14 | RFOUT | RF output. Must use an external DC block as close to the pin as possible. |
| 22 | RFIN | RF input internally matched to 50Ω. Must use an external DC block. The DC block should be placed as close to the pin as possible for best RF performance. |
| | - EPAD | Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance. |

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F1421 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

| Parameter | Symbol | Minimum | Maximum | Units |
|---|---------------|-----------------|-------------------|-------|
| Supply Voltage | V_{CC} | -0.3 | +5.5 | V |
| STBY | V_{STBY} | -0.3 | $V_{CC} + 0.25$ | V |
| RFIN Externally Applied DC Voltage | V_{RFIN} | -0.3 | +0.3 | V |
| RFOUT Externally Applied DC voltage | V_{RFOUT} | $V_{CC} - 0.15$ | $V_{CC} + 0.15$ | V |
| Maximum RF CW Input Power | P_{MAX_IN} | | +18 | dBm |
| Continuous Power Dissipation | P_{DISS} | | 1.5 | W |
| Junction Temperature | T_{JMAX} | | +150 | °C |
| Storage Temperature Range | T_{STOR} | -65 | +150 | °C |
| Lead Temperature (soldering, 10s) | T_{LEAD} | | +260 | °C |
| Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012) | V_{ESDHMB} | | 2000 (Class 2) | V |
| Electrostatic Discharge – CDM (JEDEC 22-C101F) | V_{ESDCDM} | | 500 (Class C2) | V |

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|--------------------------------------|---------------|-----------------|---------|---------|---------|----------|
| Supply Voltage | V_{CC} | | 4.75 | | 5.25 | V |
| Operating Temperature Range | T_{EP} | Exposed Paddle | -40 | | +105 | °C |
| RF Frequency Range | f_{RF} | Operating Range | 1.7 | | 2.2 | GHz |
| Maximum Operating Input RF Power [a] | P_{IN_MAX} | | | | +10 | dBm |
| RF Source Impedance | Z_{RFI} | Single Ended | | 50 | | Ω |
| RF Load Impedance | Z_{RFO} | Single Ended | | 50 | | Ω |

[a] Input / output load impedance < 2:1 VSWR any phase based in a 50 Ω system.

Electrical Characteristics

See the F1421 Typical Application Circuit. Specifications apply when operated at $V_{CC} = +5.0V$, $f_{RF} = 1.9GHz$, $T_{EP} = +25^{\circ}C$, $Z_S = Z_L = 50\Omega$, tone spacing = 5MHz, $P_{OUT} = +4dBm/$ tone, evaluation board (EVKit) traces and connectors are de-embedded, unless otherwise stated.

Table 4. Electrical Characteristics

| Parameter | Symbol | Condition | Minimum | Typical | Maximum | Units |
|------------------------------------|------------------|---|----------------|---------|-------------|---------|
| Logic Input High Threshold | V_{IH} | | 1.1 [a] | | V_{CC} | V |
| Logic Input Low Threshold | V_{IL} | | | | 0.8 | V |
| Logic Current | I_{IL}, I_{IH} | Standby Pin | -10 | | 10 | μA |
| Supply Current | I_{CC} | Standby = LOW or open | | 138 | 153 | mA |
| | I_{CC_STBY} | Standby = HIGH | | 0.6 | 1.2 | mA |
| Gain | $G_{1.7}$ | $f_{RF} = 1.7GHz$ | | 19.6 | | dB |
| | $G_{1.9}$ | $f_{RF} = 1.9GHz$ | 18.8 | 20.3 | 21.8 | |
| | $G_{2.2}$ | $f_{RF} = 2.2GHz$ | | 21.0 | | |
| Input Return Loss | RL_{IN} | | | 15 | | dB |
| Output Return Loss | RL_{OUT} | | | 15 | | dB |
| Gain Flatness | G_{FLAT} | $f_{RF} = 1.7GHz$ to $2.2GHz$ | | 1.3 | | dB |
| Gain Ripple | G_{RIPPLE} | In any 20MHz range over RF Band | | 0.06 | | dB |
| Noise Figure | NF | $f_{RF} = 1.7GHz$ | | 5.6 | | dB |
| | | $f_{RF} = 1.9GHz$ | | 5.5 | | |
| | | $f_{RF} = 2.2GHz$ | | 5.6 | | |
| | | $f_{RF} = 1.9GHz, T_{EP} = +105^{\circ}C$ | | 6.3 | | |
| Output Third Order Intercept Point | OIP3 | $P_{OUT} = +4dBm/$ tone 5MHz tone delta | 36 | 40 | | dBm |
| Output 1dB Compression | OP1dB | | 21 | 23 | | dBm |
| Power ON Switching Time | t_{ON} | 50% STBY control to within 0.2dB of the on state final gain value | | 120 | | ns |
| Power OFF Switching Time | t_{OFF} | 50% STBY control to 30dB below on state gain value | | 80 | | ns |

[a] Specifications in the minimum/maximum columns that are shown in **bold italics** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

Thermal Characteristics

Table 5. Package Thermal Characteristics

| Parameter | Symbol | Value | Units |
|--|-------------------|-------|-------|
| Junction to Ambient Thermal Resistance | θ_{JA} | 45 | °C/W |
| Junction to Case Thermal Resistance (Case is defined as the exposed paddle) | θ_{JC-BOT} | 36 | °C/W |
| Moisture Sensitivity Rating (Per J-STD-020) | | MSL 1 | |

Typical Operating Conditions (TOC)

- $V_{CC} = 5.0V$
- $Z_L = Z_S = 50\Omega$ Single Ended
- $f_{RF} = 1.9GHz$
- $T_{EP} = 25^\circ C$ (All temperatures are referenced to the exposed paddle)
- STBY = LOW (0V)
- $P_{OUT} = +4dBm/Tone$
- 5MHz Tone Spacing
- Evaluation Kit traces and connector losses are de-embedded

Typical Performance Characteristics

Figure 3. Gain vs Frequency

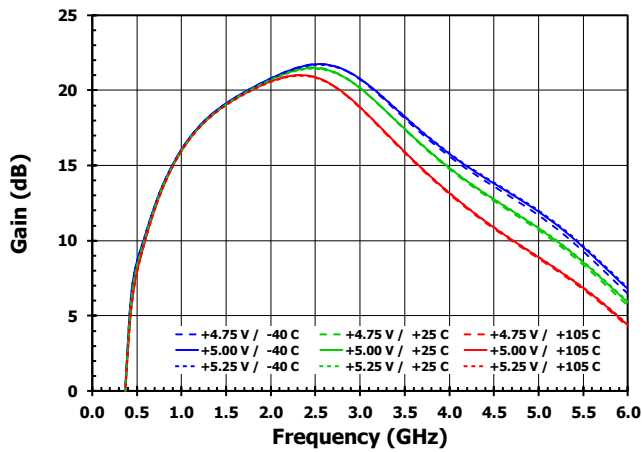


Figure 4. Reverse Isolation vs Frequency

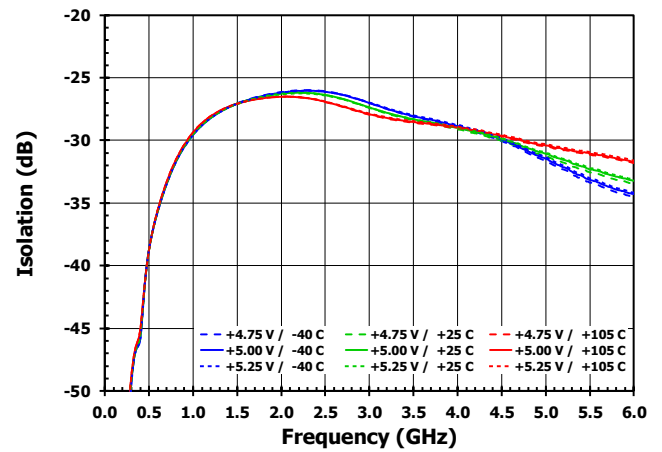


Figure 5. Input Return Loss vs Frequency

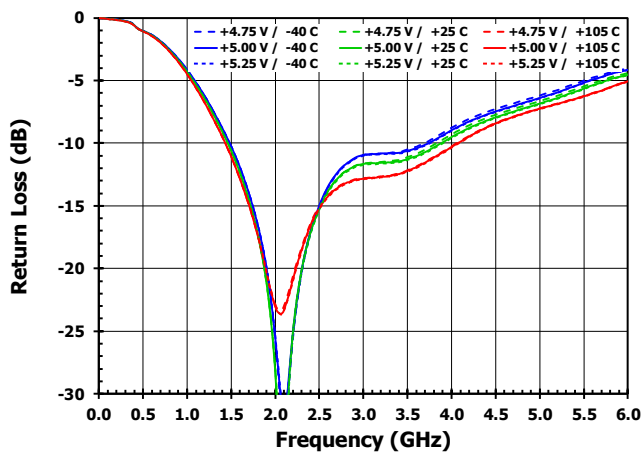


Figure 6. Output Return Loss vs Frequency

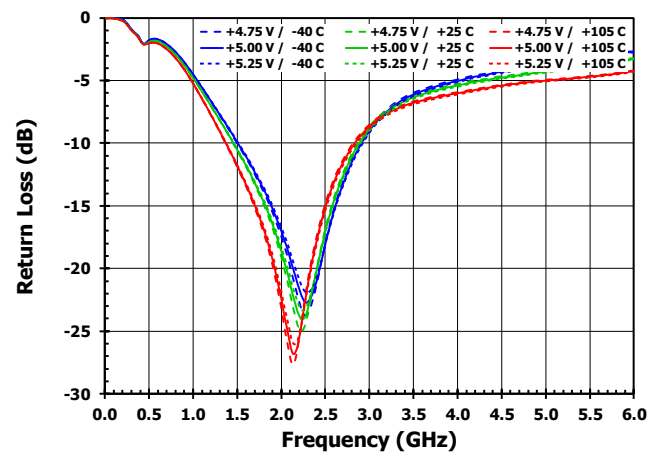


Figure 7. Gain vs Frequency

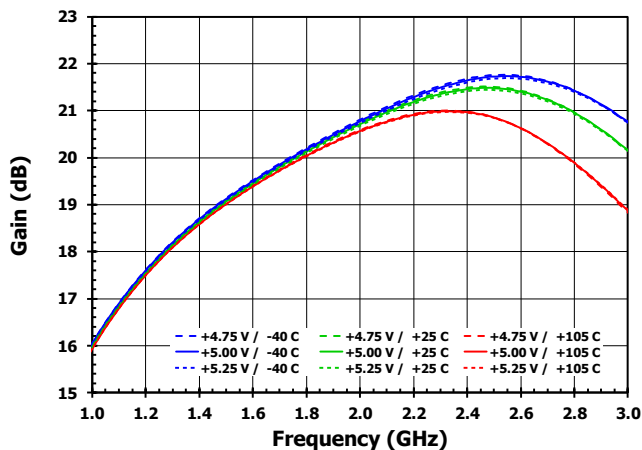
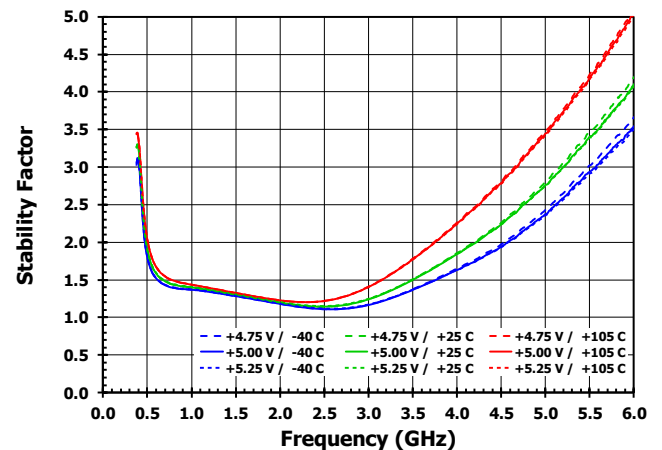


Figure 8. Stability vs Frequency



Typical Performance Characteristics

Figure 9. Output IP3 versus Frequency

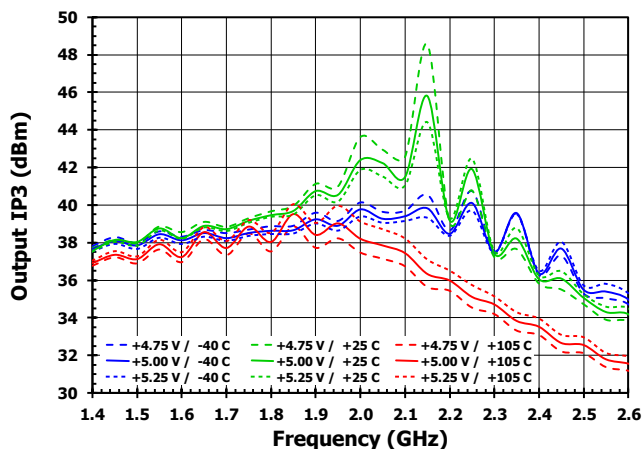


Figure 10. Output P1dB versus Frequency

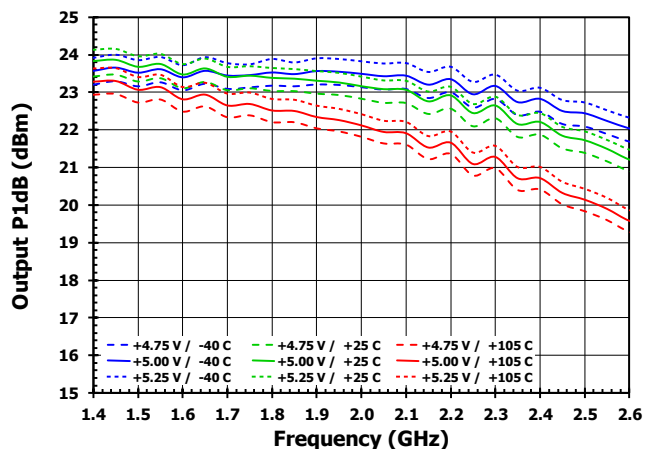


Figure 11. Second Harmonic versus Frequency

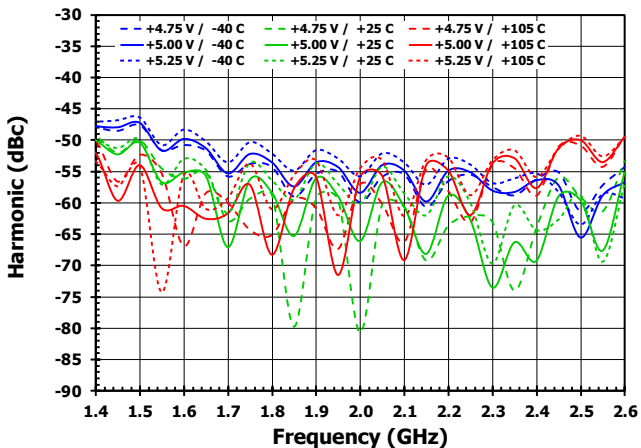


Figure 12. Third Harmonic versus Frequency

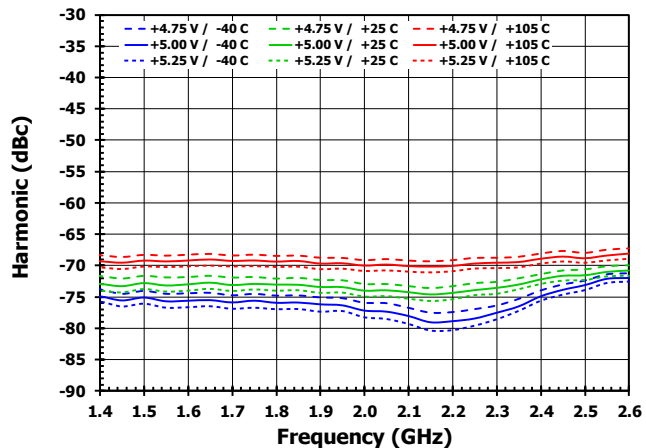


Figure 13. Noise Figure versus Frequency

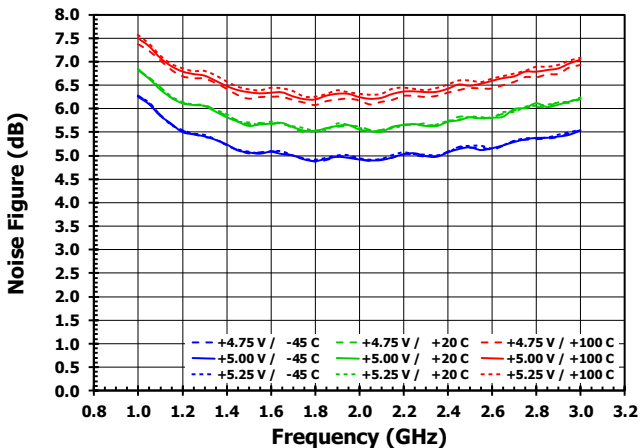
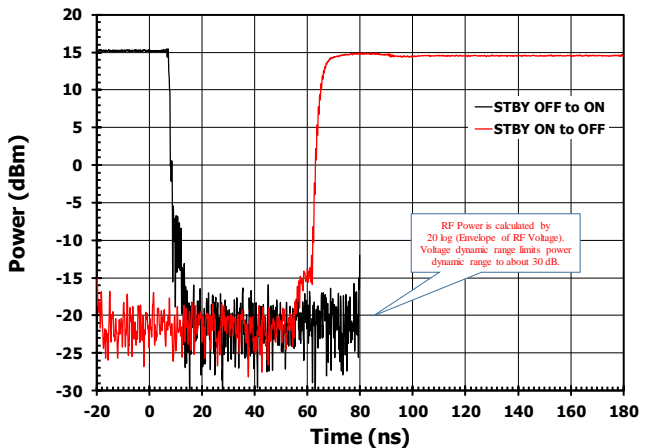


Figure 14. Standby Switching Speed



Evaluation Kit Picture

Note: The evaluation board is used for multiple devices.

Figure 15. Top View

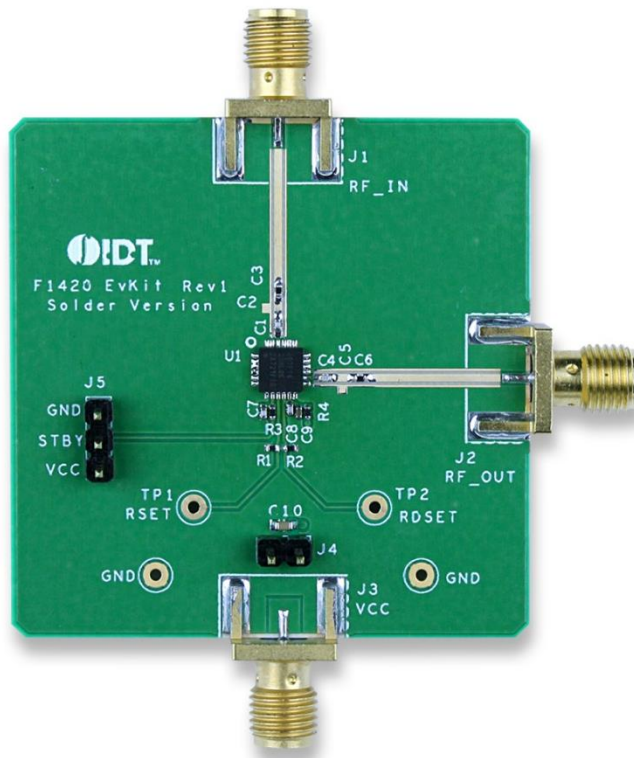
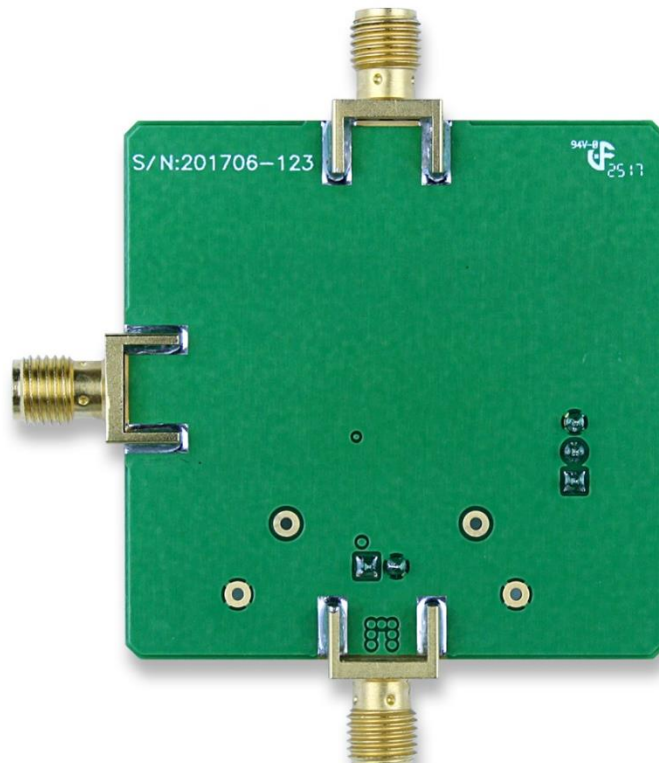


Figure 16. Bottom View



Evaluation Kit / Applications Circuit

Figure 17. Electrical Schematic

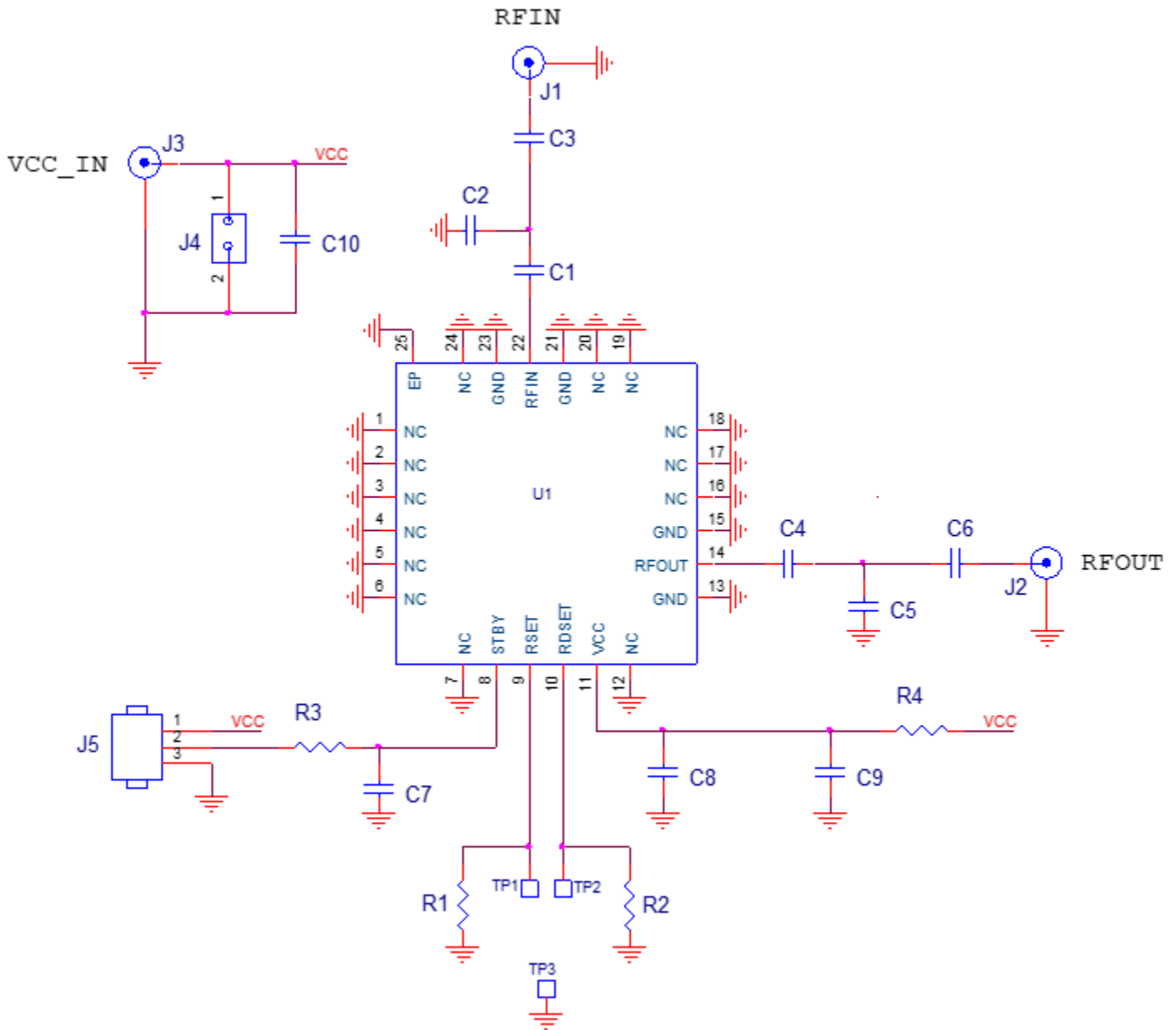


Table 6. Bill of Material (BOM)

| Part Reference | QTY | Description | Manufacturer Part # | Manufacturer |
|----------------|-----|--|---------------------|-----------------|
| C1 | 2 | 2.2pF \pm 0.1, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H2N20J | Murata |
| C4 | 2 | 4.0pF \pm 0.1, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H470J | Murata |
| C7 | 1 | 2pF \pm 0.1pF, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H2R0B | Murata |
| C8 | 1 | 1000pF \pm 5%, 50V, C0G Ceramic Capacitor (0402) | GRM1555C1H102J | Murata |
| C9 | 1 | 0.1 μ F \pm 10%, 16V, X7R Ceramic Capacitor (0402) | GRM155R71C104K | Murata |
| C10 | 1 | 10 μ F \pm 20%, 16V, X6S Ceramic Capacitor (0603) | GRM188C81C106M | Murata |
| R1 | 1 | 1.87k Ω \pm 1%, 1/10W, Resistor (0402) | ERJ-2RKF2001X | Panasonic |
| R2 | 1 | 5.11k Ω \pm 1%, 1/10W, Resistor (0402) | ERJ-2RKF3401X | Panasonic |
| R3 | 1 | 1k Ω \pm 1%, 1/10W, Resistor (0402) | ERJ-2RKF1001X | Panasonic |
| C3, C6, R4 | 3 | 0 Ω Resistors (0402) | ERJ-2GE0R00X | Panasonic |
| J4 | 1 | CONN HEADER VERT SGL 2 X 1 POS GOLD | 961102-6404-AR | 3M |
| J5 | 1 | CONN HEADER VERT SGL 3 X 1 POS GOLD | 961103-6404-AR | 3M |
| J1, J2, J3 | 3 | Edge Launch SMA (0.375 inch pitch ground, tab) | 142-0701-851 | Emerson Johnson |
| U1 | 1 | AMP | F1421NLGK | IDT |
| | 1 | Printed Circuit Board | F1420 EVKit REV 1 | IDT |
| C2, C5 | | DNP | | |

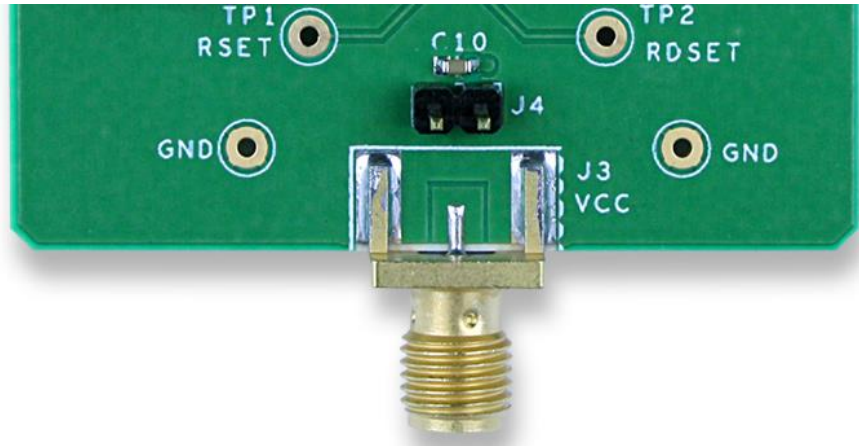
Evaluation Kit Operation

Power Supply Setup

Set up a power supply in the voltage range of 3.0V to 5.25V with the power supply output disabled. The voltage can be applied via one of the following connections (see Figure 18):

- J3 connector
- J4 header connection (GND is the pin farthest away from the J4 label)

Figure 18. Power Supply Connections



Standby (STBY) Pin

The Evaluation Board has the ability to control the F1421 for standby operation. The logic voltage is applied to the J5 header connection as shown in Figure 19.

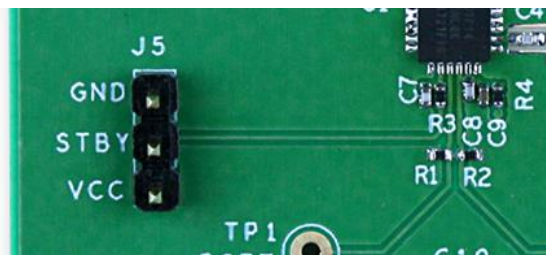
To place the amplifier in the active mode (on) use one of these options:

- Make no connections on J5
- Apply a logic LOW signal to STBY (pin 2 of J5 or the middle pin).
- Make a connection between pin 3 (GND) and pin 2 (STBY, the middle pin) of J5.

To place the amplifier in the standby mode (off), use one of these options:

- Apply a logic HIGH signal to the STBY (pin 2 of J5 or the middle pin).
- Make a connection between pin 1 (VCC) and pin 2 (STBY, the middle pin) of J5.

Figure 19. Standby Pin Connection



Power-On Procedure

Set up the voltage supplies and Evaluation Board as described in the "Power Supply Setup" section with the "Standby Pin" set for logic LOW.

- Enable the power supply.
- The STBY pin now can now be exercised.

Power-Off Procedure

- Set the STBY pin to logic LOW.
- Disable the power supply.

Application Information

The F1421 has been optimized for use in high-performance RF applications from 1.7GHz to 2.2GHz.

Standby Mode (STBY)

The F1421 has a standby pin which allows the amplifier to be turned off to decrease overall power requirements. The pin uses simple logic levels and is compatible with both JEDEC 1.8V and JEDEC 3.3V logic. Table 7 lists the amplifier state for the logic. An internal pull-down resistor causes the amplifier to default to the on state.

Table 7. Standby Truth Table

| STBY (pin 8) | Condition |
|--------------|---------------|
| LOW or Open | Amplifier On |
| HIGH | Amplifier Off |

RSET and RDSET

The F1421 has been optimized for gain and intermodulation products by adjusting the bias resistors RSET and RDSET. For the optimized setting, RSET (R1) is 1.87kΩ and RDSET (R2) is 5.11kΩ.

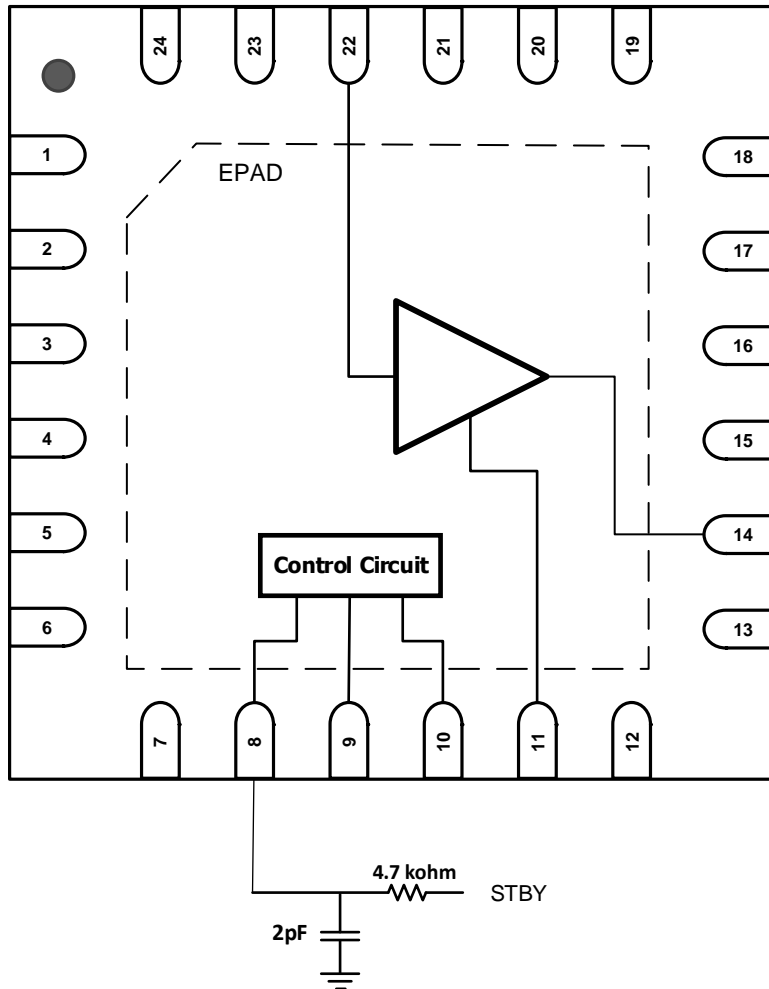
Power Supplies

The power supply pin should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure, and fast transients can trigger ESD clamps and cause them to fail. Supply voltage changes or transients should have a slew rate less than 1V/20μs.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pin 8 (STBY). Note the recommended resistor and capacitor values do not necessarily match the EVKit BOM for the case of poor control signal integrity.

Figure 20. Control Pin Interface for Signal Integrity



Digital Pin Voltage and Resistance Values

Table 8 provides the open-circuit DC voltage referenced to ground and resistance value for the control pin listed.

Table 8. Digital Pin Voltages and Resistance

| Pin | Name | Open Circuit DC Voltage | Internal Connection |
|-----|------|-------------------------|--------------------------|
| 8 | STBY | 0V | 580kΩ resistor to ground |

Package Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

<https://www.idt.com/document/psc/nlnlg24p1-package-outline-40-x-40-mm-body-05-mm-pitch-qfn-epad-size-245-x-245-mm>

Ordering Information

| Orderable Part Number | Package | MSL Rating | Carrier Type | Temperature |
|-----------------------|------------------------------|------------|--------------|----------------|
| F1421NLGK | 4mm x 4mm x 0.9mm 24-pin QFN | 1 | Tray | -40° to +105°C |
| F1421NLGK8 | 4mm x 4mm x 0.9mm 24-pin QFN | 1 | Reel | -40° to +105°C |
| F1421EVBI | Evaluation Board | | | |

Marking Diagram



Line 1 and 2 are the part number.
 Line 3 “ZA” is for die version.
 Line 3 “721” is one digit for the year and week that the part was assembled.
 Line 3 “FTG” denotes the production process.

Revision History

| Revision | Revision Date | Description of Change |
|----------|---------------|-----------------------|
| 0 | May 11, 2018 | Initial Release. |

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