GENERAL DESCRIPTION

The F2250 is a low insertion loss **V**oltage **V**ariable RF **A**ttenuator (VVA) designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 50MHz to 6000MHz. In addition to providing low insertion loss, the F2250 provides excellent linearity performance over its entire voltage control and attenuation range.

The F2250 uses a single positive supply voltage of 3.15V to 5.25V. Other features include the V_{MODE} pin allowing either positive or negative voltage control slope vs attenuation and multi-directional operation meaning the RF input can be applied to either RF1 or RF2 pins. Control voltage ranges from 0V to 3.6V using either positive or negative control voltage slope.

COMPETITIVE ADVANTAGE

F2250 provides extremely low insertion loss and superb IP3, IP2, Return Loss and Slope Linearity across the control range. Comparing to the previous state-of-the-art for silicon VVAs this device is better as follows:

- ✓ Insertion Loss @ 2000MHz: 1.4dB vs. 2.8dB
- ✓ Insertion Loss @ 6000MHz: 2.7dB vs. 7dB
- ✓ Maximum Attenuation Slope: 33dB/Volt vs. 53dB/Volt
- ✓ Minimum Return Loss up to 6000MHz: 12.5dB vs. 7dB
- ✓ Minimum Output IP3: 31dBm vs. 15dBm
- ✓ Minimum Input IP2: 87dBm vs. 80dBm
- ✓ Maximum Operating Temperature: +105°C vs. +85°C

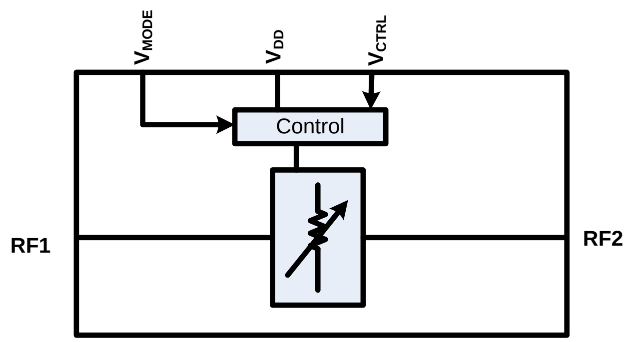
APPLICATIONS

- Base Station 2G, 3G, 4G
- Portable Wireless
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID handheld and portable readers
- Cable Infrastructure
- Wireless LAN
- Test / ATE Equipment

FEATURES

- Low Insertion Loss: 1.4dB @ 2000MHz
- Typical / Min IIP3: 65dBm / 47dBm
- Typical / Min IIP2: 95dBm / 87dBm
- 33.6dB Attenuation Range
- Bi-directional RF ports
- +34.4dBm Input P1dB compression
- V_{MODE} pin allows either positive or negative attenuation control response
- Linear-in-dB attenuation characteristic
- Supply voltage: 3.15V to 5.25V
- V_{CTRL} range: 0V to 3.6V using 5V supply
- +105°C max operating temperature
- 3mm x 3mm, 16-pin QFN package

DEVICE BLOCK DIAGRAM



ORDERING INFORMATION

PART# MATRIX

Part#	RF Freq Range (MHz)	Insertion Loss (dB)	IIP3 (dBm)	Pinout Compatibility
F2250	50 - 6000	1.4 (at 2GHz)	+65	RFMD
F2255	1 - 3000	1.1 (at 500MHz)	+60	
F2258	50 - 6000	1.4 (at 2GHz)	+65	Hittite

ABSOLUTE MAXIMUM RATINGS

Parameter / Condition		Symbol	Min	Max	Units
V_{DD} to GND		V_{DD}	-0.3	5.5	V
V_{MODE} to GND		V_{MODE}	-0.3	Minimum (V_{DD}, 3.9)	V
V_{CTRL} to GND	V_{DD} = 0V to 5.25V	V_{CTRL}	-0.3	Minimum (V_{DD}, 4.0)	V
RF1, RF2 to GND		V_{RF}	-0.3	0.3	V
RF1 or RF2 Input Power applied for 24 hours maximum (V_{DD} applied @ 2GHz and +85°C)		P_{MAX24}		30	dBm
RF1 or RF2 Continuous Operating Power		P_{MAX_OP}		See Figure 1	dBm
Maximum Junction Temperature		T_{JMAX}		+150	°C
Storage Temperature Range		T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)		T_{LEAD}		+260	°C
ESD Voltage– HBM (Per ESD STM5.1-2007)		V_{ESDHBM}		Class 1C	
ESD Voltage – CDM (Per ESD STM5.3.1-2009)		V_{ESDCDM}		Class C3	

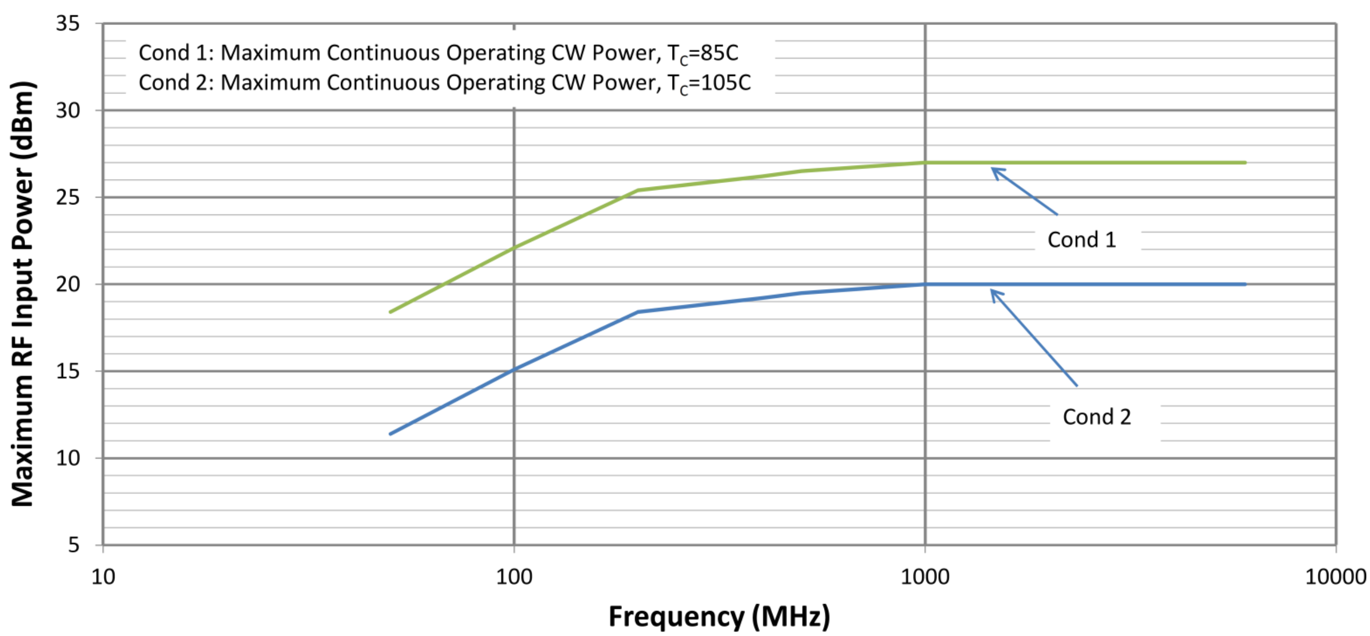


FIGURE 1: MAXIMUM RF INPUT POWER VS. RF FREQUENCY

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

Θ_{JA} (Junction – Ambient)	80.6°C/W
Θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	5.1°C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL 1

F2250 Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating Freq Range	F_{RF}		50		6000	MHz
Supply Voltage	V_{DD}		3.15		5.25	V
V_{MODE} Logic	V_{IH}	V_{DD} > 3.9V	1.17		3.6 [2]	V
		V_{DD} = 3.15V to 3.9V	1.17		V_{DD} -0.3	
	V_{IL}		0		0.63	
V_{CTRL} Range	V_{CTRL}	V_{DD} = 3.9V to 5.25V	0		3.6	V
		V_{DD} = 3.15V to 3.9V	0		V_{DD}-0.3	
Supply Current	I_{DD}		***0.5*** [1]	1.17	***2***	mA
Logic Current	I_{MODE}		***-1***		***38***	µA
I_{CTRL} Current	I_{CTRL}		***-1***		***14***	µA
RF Operating Power [3]	$P_{MAX,\ CW}$				See Figure 1	dBm
RF1 Port Impedance	Z_{RF1}			50		Ω
RF2 Port Impedance	Z_{RF2}			50		
Operating Temperature Range	T_{CASE}	Exposed Paddle Temperature	-40		+105	°C

Operating Conditions Notes:
1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test.
2 – Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
3 – Refer to the Maximum **Operating** RF Input Power vs. RF Frequency curves in Figure 1.

F2250 Specification

Refer to EVKit / Applications Circuit, V_{DD} = +3.3V, T_C = +25°C, signals applied to RF1 input, F_{RF} = 2000MHz, minimum attenuation, P_{IN} = 0dBm for small signal parameters, +20dBm for single tone linearity tests, +20dBm per tone for two tone tests, two tone delta frequency = 50MHz, PCB board traces and connector losses are de-embedded unless otherwise noted. Refer to Typical Operating Curves for performance over entire frequency band.

Parameter	Symbol	Comment	Min	Typ	Max	Units
Insertion Loss, IL (Minimum Attenuation)	A_{MIN}	2GHz		1.4	***1.9*** [1]	dB
		3GHz		1.6		
		6GHz		2.6	3.1	
Maximum Attenuation	A_{MAX}		34 [2]	35		dB
Insertion Phase Δ	$\Phi_{\Delta MAX}$	At 36dB attenuation relative to Insertion Loss		27		deg
	$\Phi_{\Delta MID}$	At 18dB attenuation relative to Insertion Loss		10		
Input 1dB Compression [3]	P1dB			34.4		dBm
Minimum RF1 Return Loss over control voltage range	S11	50MHz [4]		16		dB
		700MHz		17		
		2000MHz		17		
		6000MHz		15		
Minimum RF2 Return Loss over control voltage range	S22	50MHz [4]		16		dB
		700MHz		15		
		2000MHz		16		
		6000MHz		13		
Input IP3	IIP3			65		dBm
Input IP3 over Attenuation	$IIP3_{ATTEN}$	All attenuation settings	44	47		
Minimum Output IP3	$OIP3_{MIN}$	Maximum attenuation		35		
Input IP2	IIP2	P_{IN} + $IM2_{dBC}$, IM2 term is F1+F2		95		dBm
Minimum Input IP2	$IIP2_{MIN}$	All attenuation settings		87		dBm
Input IH2	HD2	P_{IN} + $H2_{dBc}$		90		dBm
Input IH3	HD3	P_{IN} + ($H3_{dBc}$/2)		54		dBm
Settling Time	$T_{SETTL0.1dB}$	Any 1dB step in the 0dB to 33dB control range 50% V_{CTRL} to RF settled to within ± 0.1dB		15		µsec

Specification Notes:

1 – Items in min/max columns in ***bold italics*** are Guaranteed by Test.

2 – Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.

3 – The input 1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section. along with Figure 1 for the maximum RF input power vs. RF frequency.

4 – Set blocking capacitors C7 & C8 to 0.01uF to achieve best return loss performance at 50MHz.

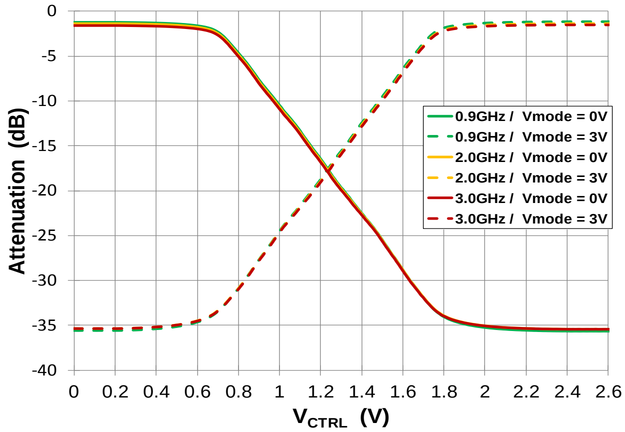
TYPICAL OPERATING CONDITIONS

Unless otherwise noted, the following conditions apply:

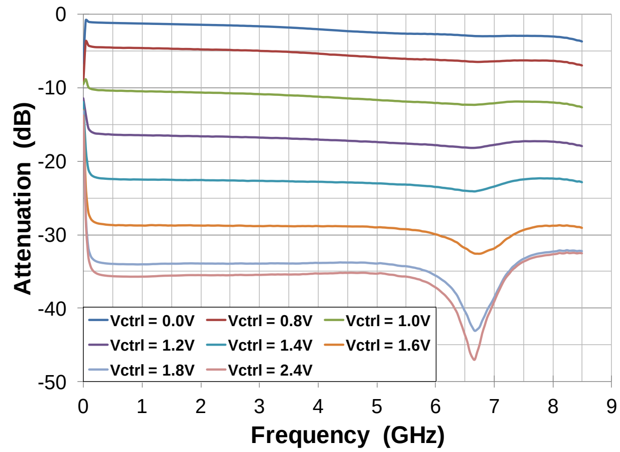
- V_{DD} = +3.3V or +5.0V
- T_C = +25ºC
- V_{MODE} = 0V
- RF trace and connector losses are de-embedded for S-parameters
- Pin = 0dBm for all small signal tests
- Pin = +20dBm for single tone linearity tests (RF1 port driven)
- Pin = +20dBm/tone for two tone linearity tests (RF1 port driven)
- Two tone frequency spacing = 50MHz

TYPICAL OPERATING CONDITIONS [S2P BROADBAND PERFORMANCE] (-1-)

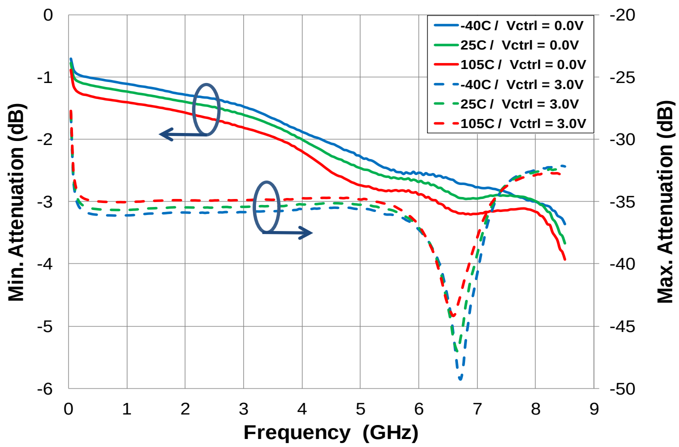
Attenuation vs. V_{CTRL}



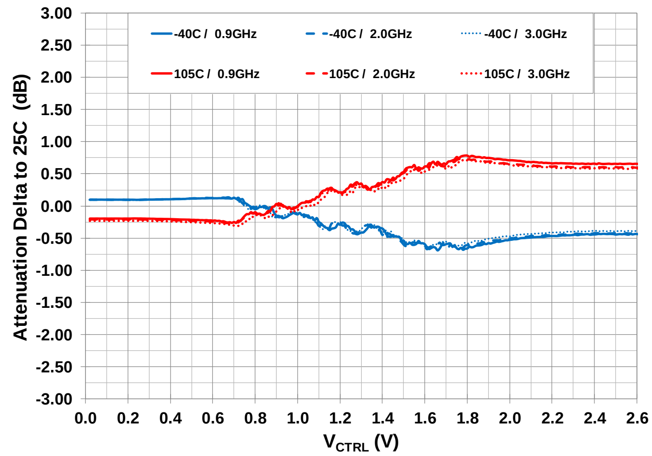
Attenuation vs. Frequency



Min. & Max. Attenuation vs. Frequency

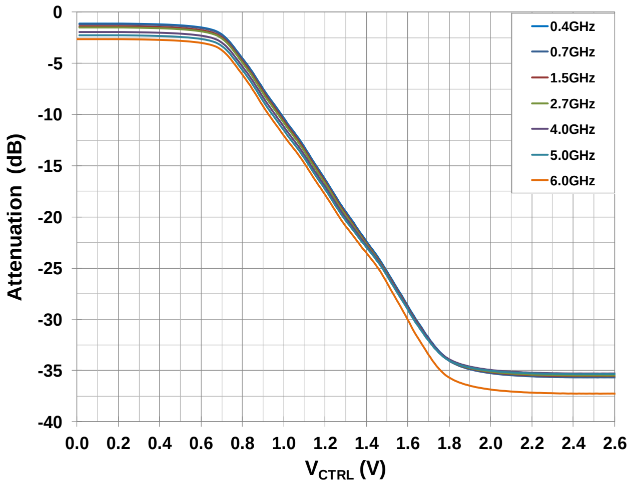


Attenuation Delta to 25C vs. Frequency

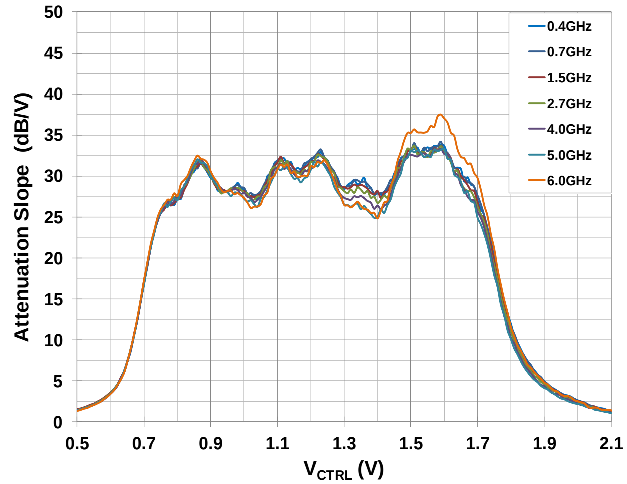


TYPICAL OPERATING CURVES [S2P vs. V_{CTRL}] (-2-)

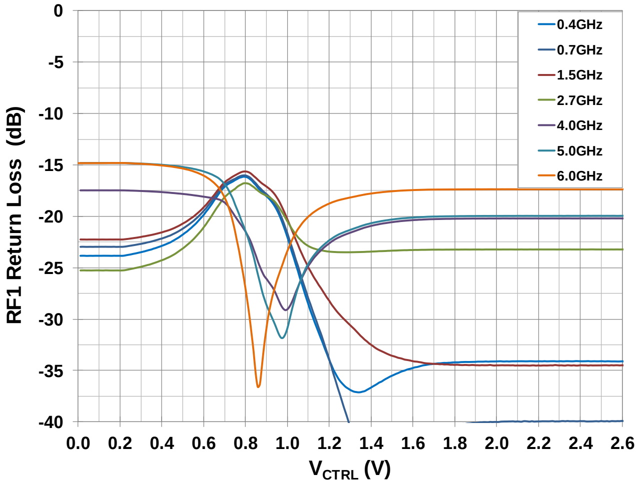
Attenuation vs. V_{CTRL}



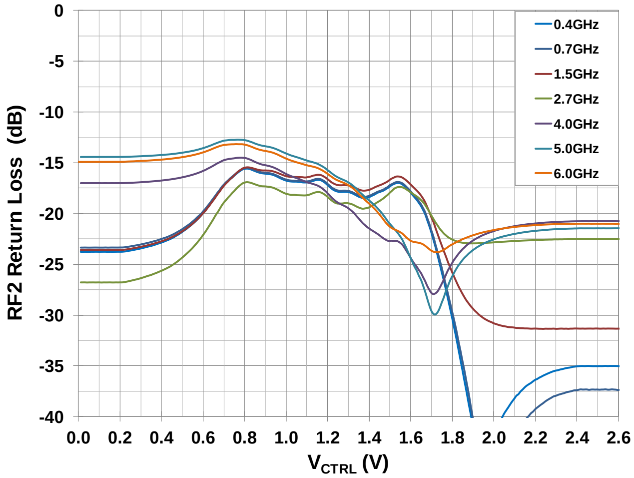
Attenuation Slope vs. V_{CTRL}



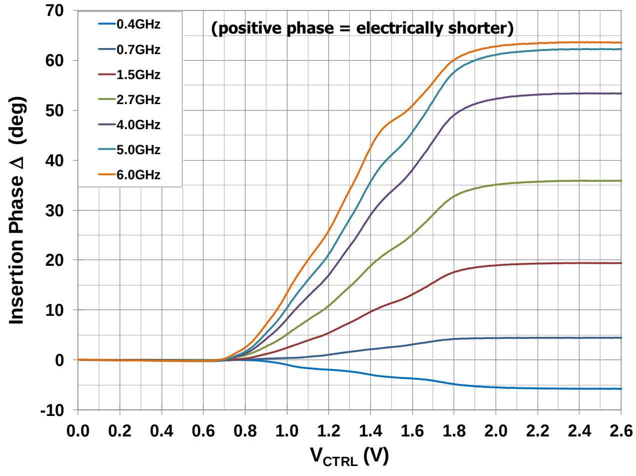
RF1 Return Loss vs. V_{CTRL}



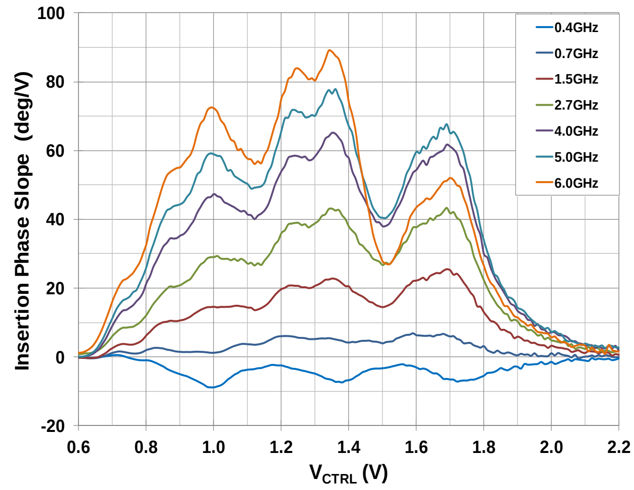
RF2 Return Loss vs. V_{CTRL}



Insertion Phase Δ vs. V_{CTRL}

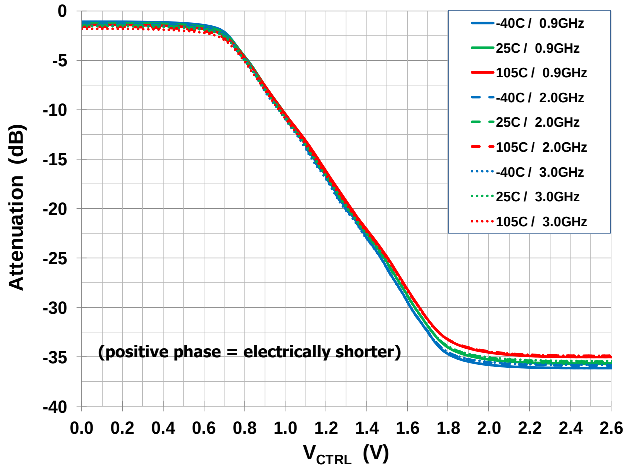


Insertion Phase Slope vs. V_{CTRL}

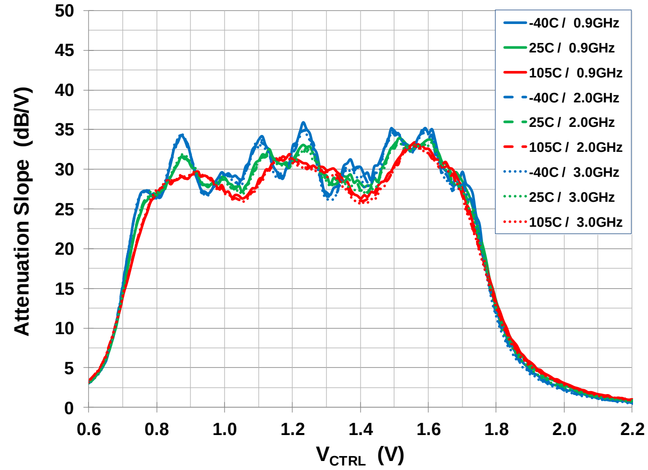


TYPICAL OPERATING CONDITIONS [S2P VS. V_{CTRL} & TEMPERATURE] (-3-)

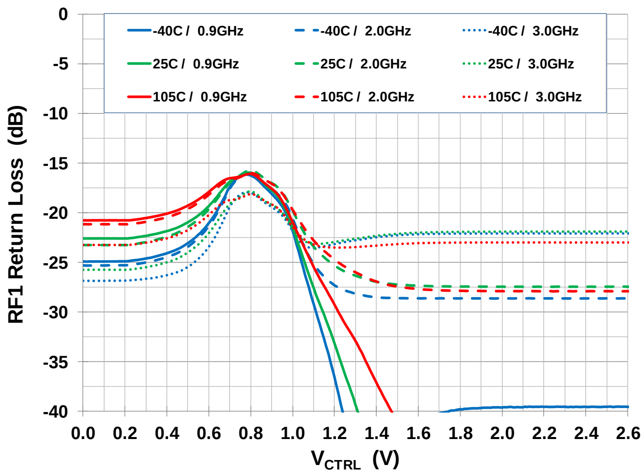
Attenuation Response vs. V_{CTRL}



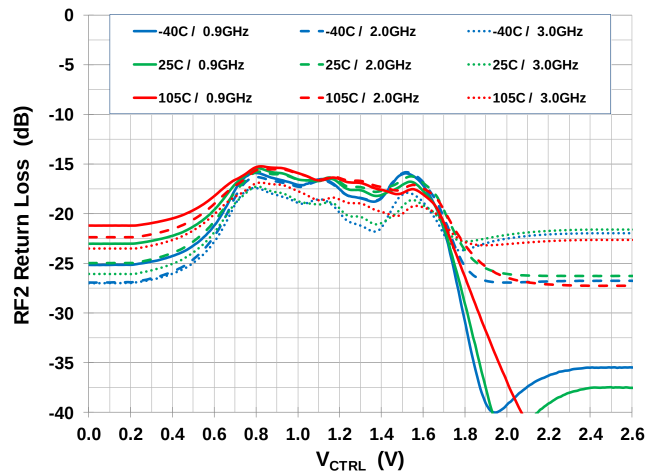
Attenuation Slope vs. V_{CTRL}



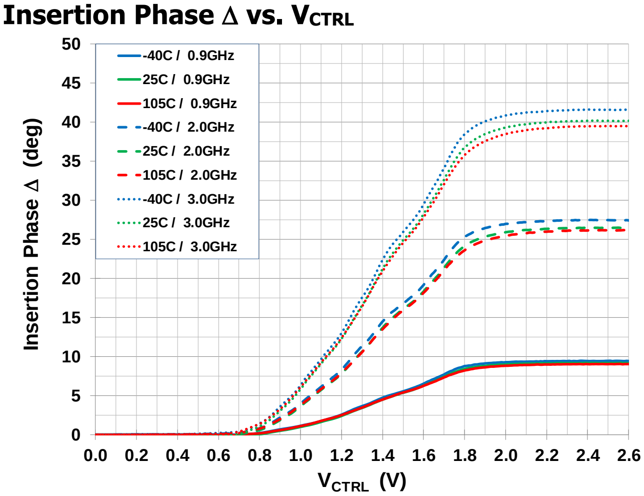
RF1 Return Loss vs. V_{CTRL}



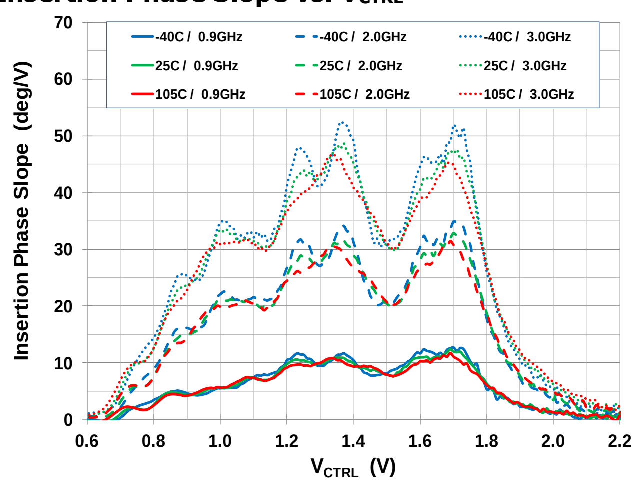
RF2 Return Loss vs. V_{CTRL}



Insertion Phase Δ vs. V_{CTRL}

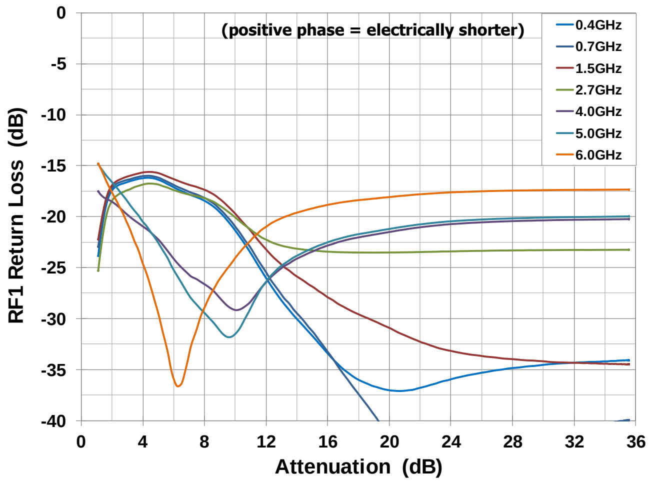


Insertion Phase Slope vs. V_{CTRL}

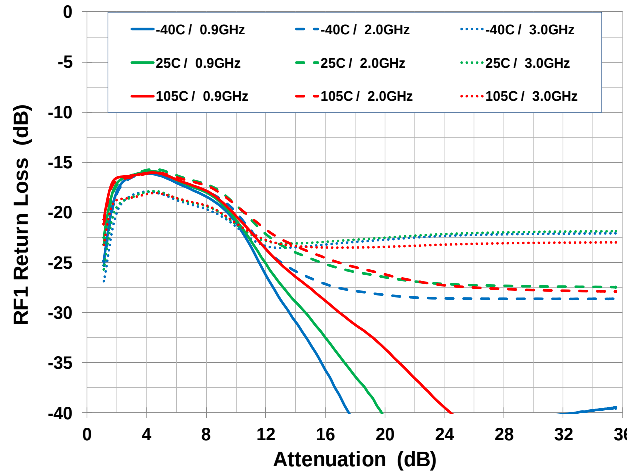


Typical Operating Conditions [S2P vs. Attenuation & Temperature] (-4-)

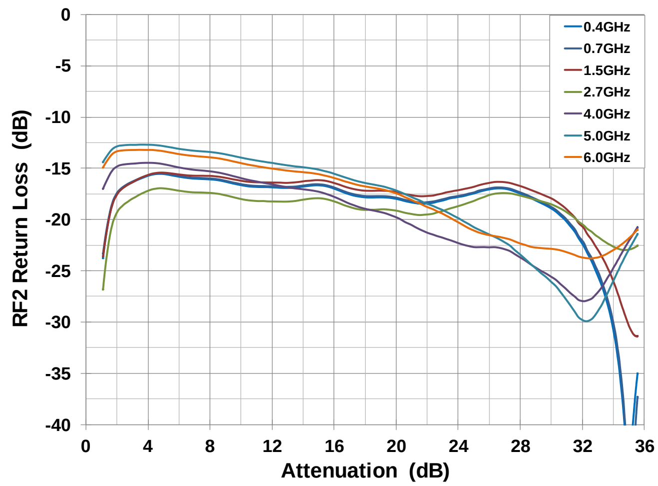
RF1 Return Loss vs. Attenuation



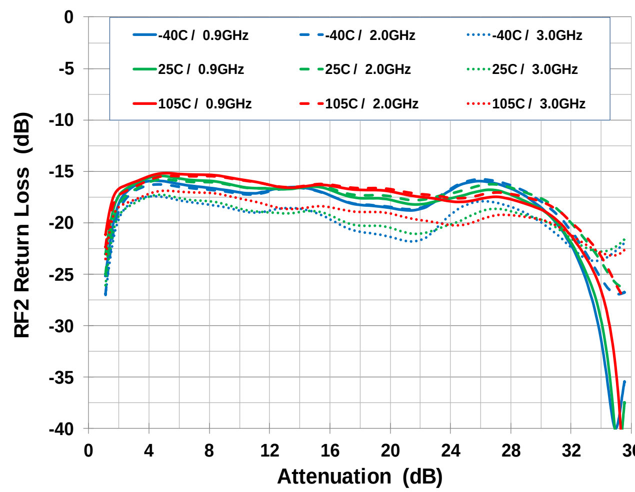
RF1 Return Loss vs. Attenuation



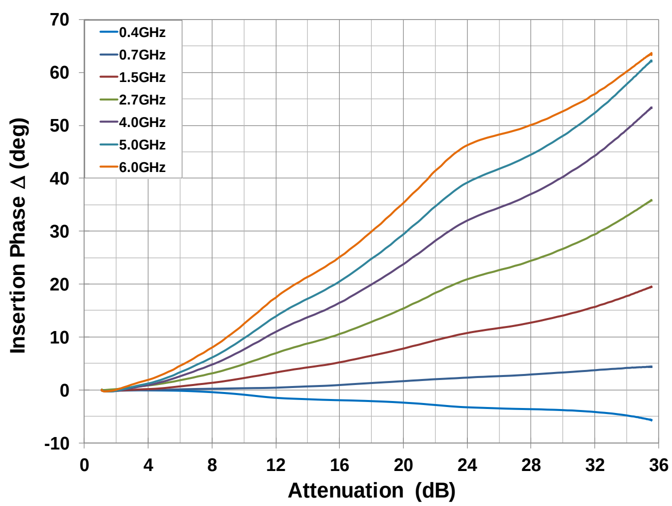
RF2 Return Loss vs. Attenuation



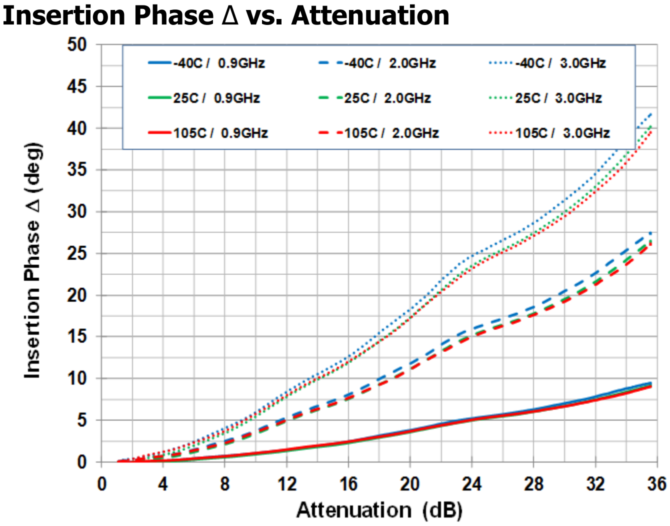
RF2 Return Loss vs. Attenuation



Insertion Phase Δ vs. Attenuation

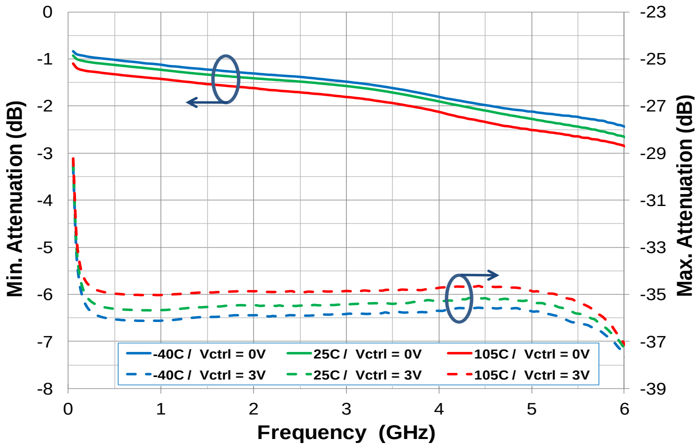


Insertion Phase Δ vs. Attenuation

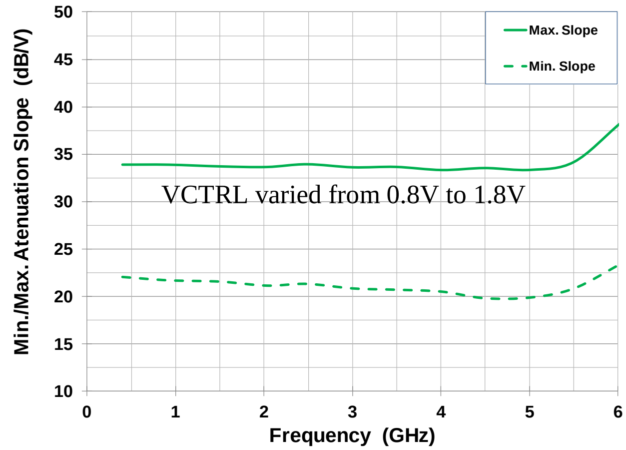


Typical Operating Conditions [S2P vs. Frequency] (-5-)

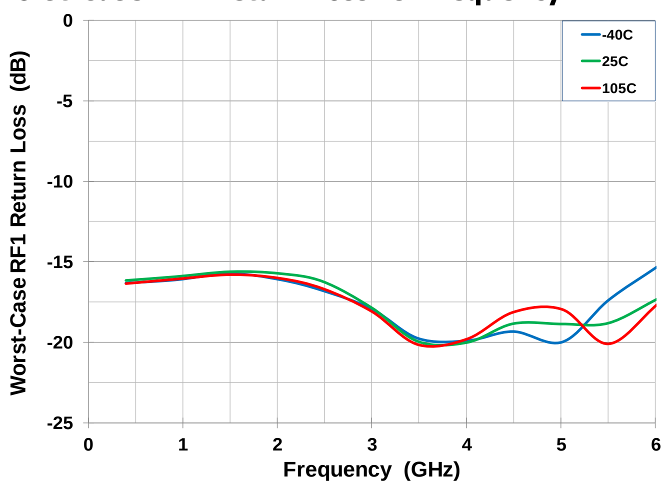
Min. & Max. Attenuation vs. Frequency



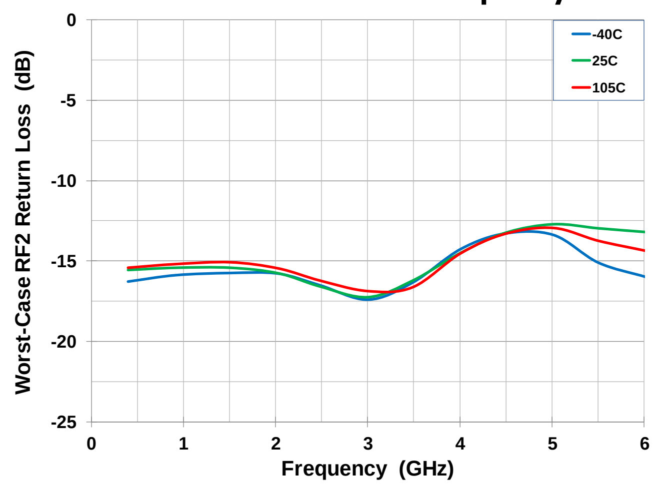
Min. & Max. Attenuation Slope vs. Frequency



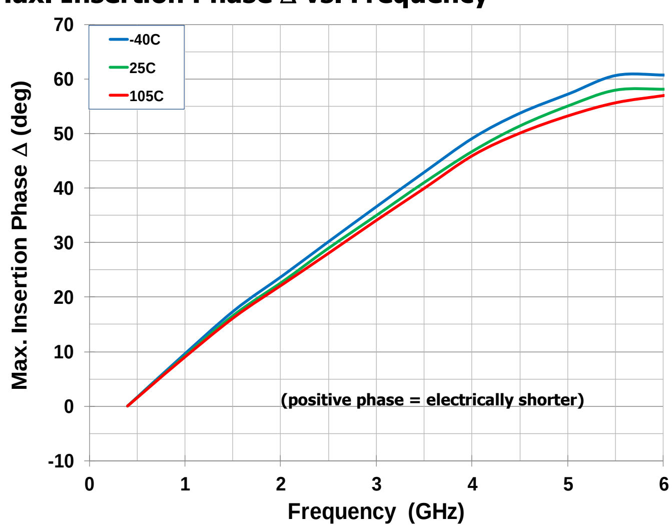
Worst-Case RF1 Return Loss vs. Frequency



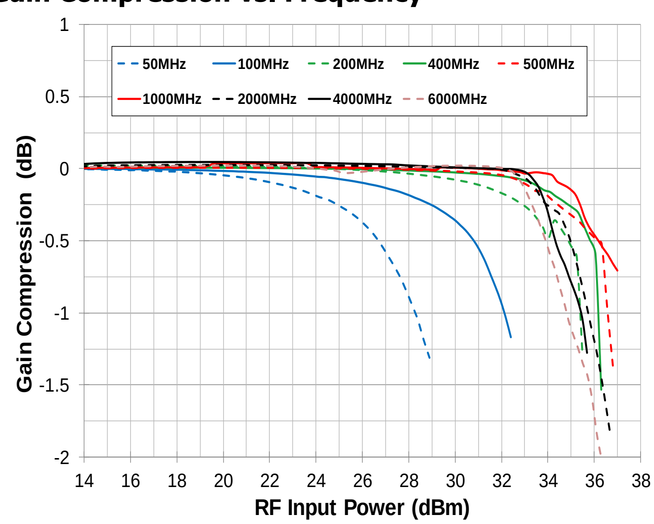
Worst-Case RF2 Return Loss vs. Frequency



Max. Insertion Phase Δ vs. Frequency

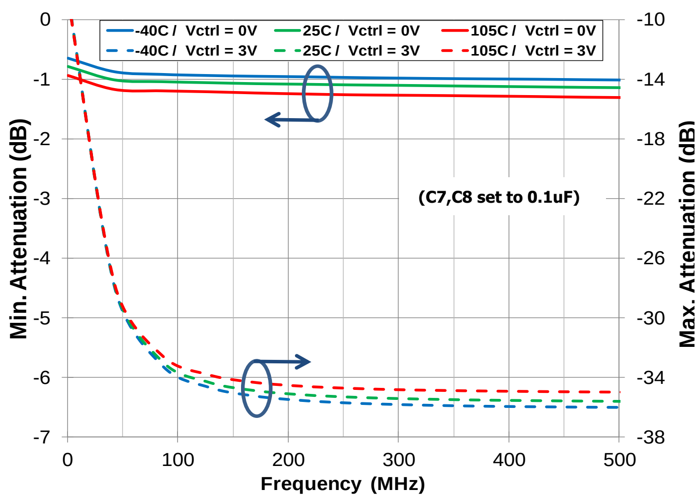


Gain Compression vs. Frequency

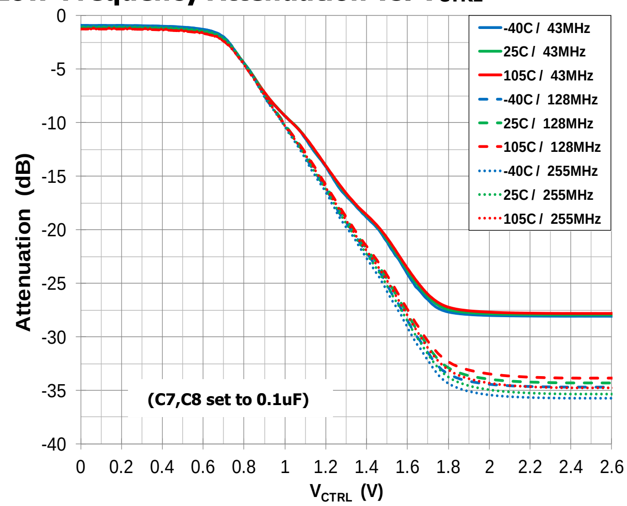


TYPICAL OPERATING CONDITIONS [S2P @ LOW FREQUENCY, GROUP DELAY] (-6-)

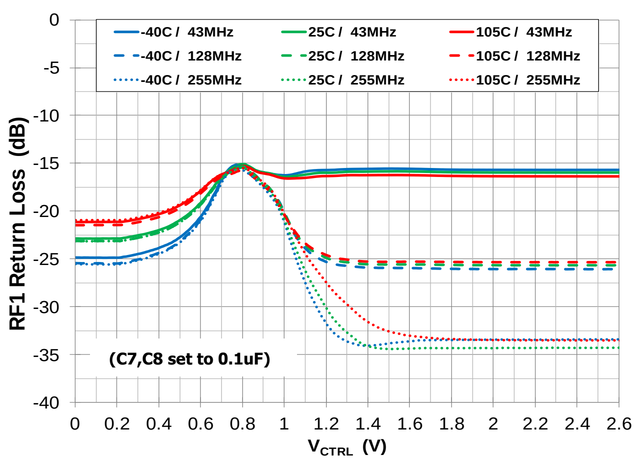
Min. & Max. Attenuation vs. Low Frequency



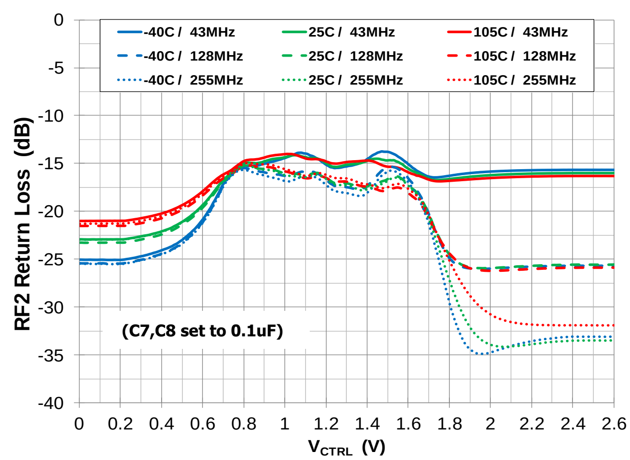
Low-Frequency Attenuation vs. V_{CTRL}



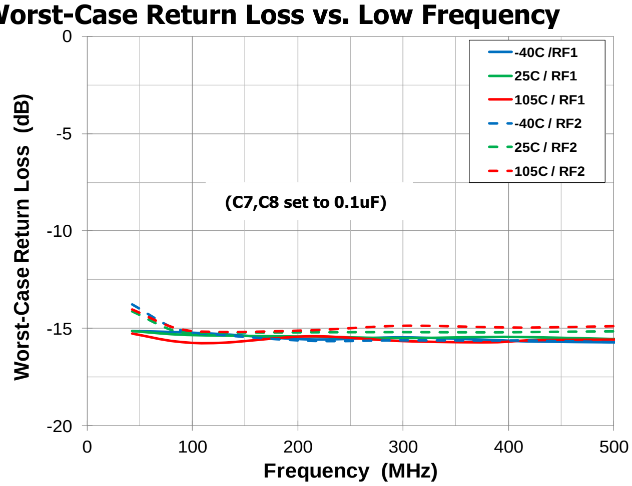
Low-Frequency RF1 Return Loss vs. V_{CTRL}



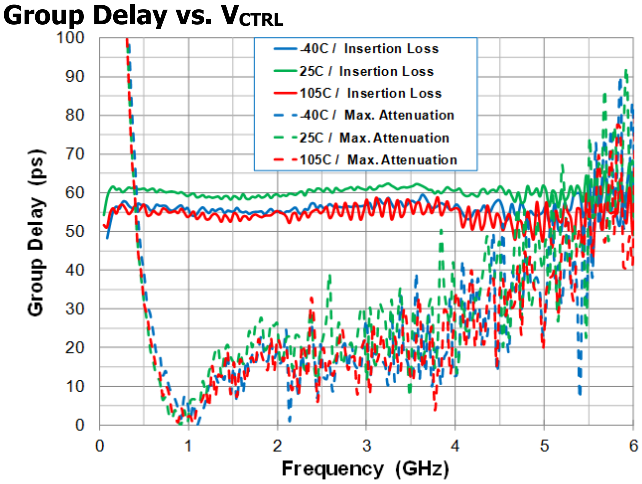
Low-Frequency RF2 Return Loss vs. V_{CTRL}



Worst-Case Return Loss vs. Low Frequency

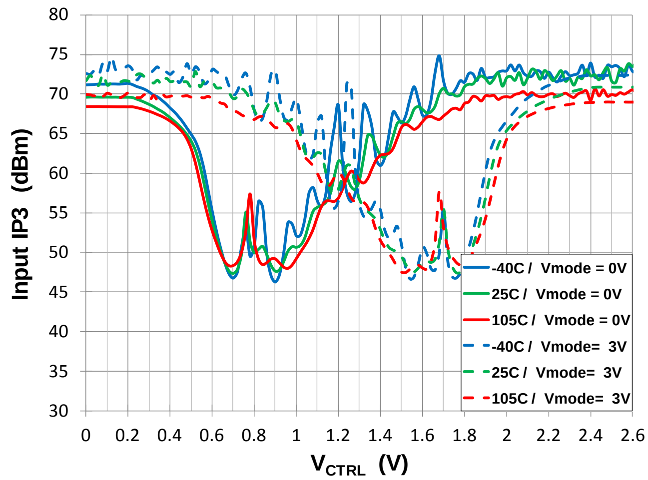


Group Delay vs. V_{CTRL}

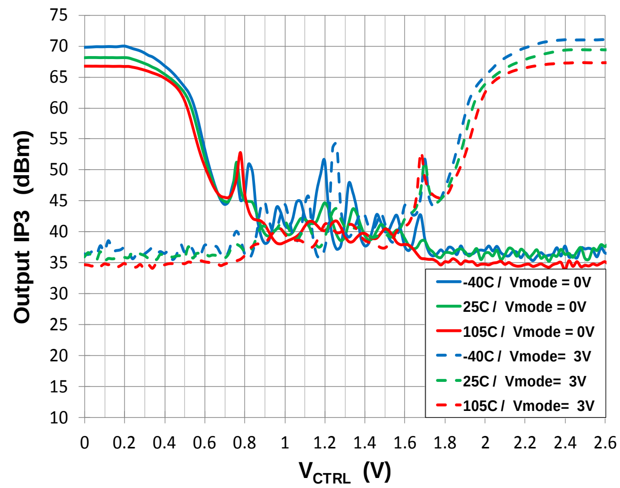


Typical Operating Conditions 2GHz, V_{DD}=3.3V [IP3, IP2, IH2, IH3 vs. V_{CTRL}, V_{MODE}] (-7-)

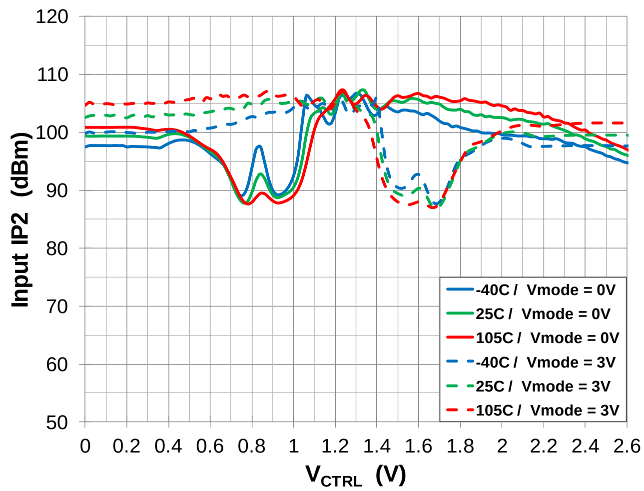
Input IP3 vs. V_{CTRL}



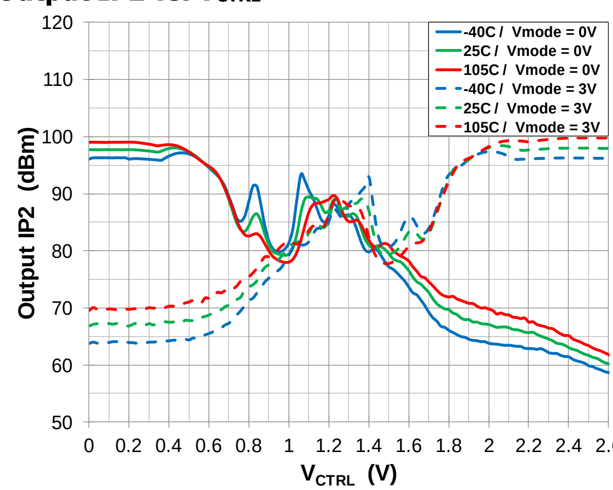
Output IP3 vs. V_{CTRL}



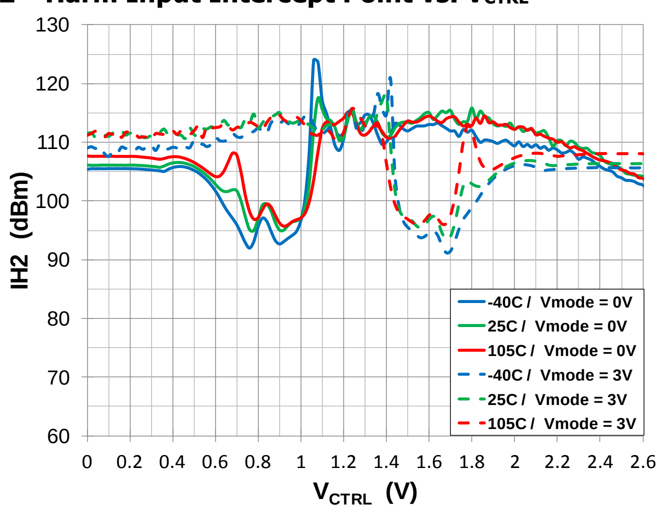
Input IP2 vs. V_{CTRL}



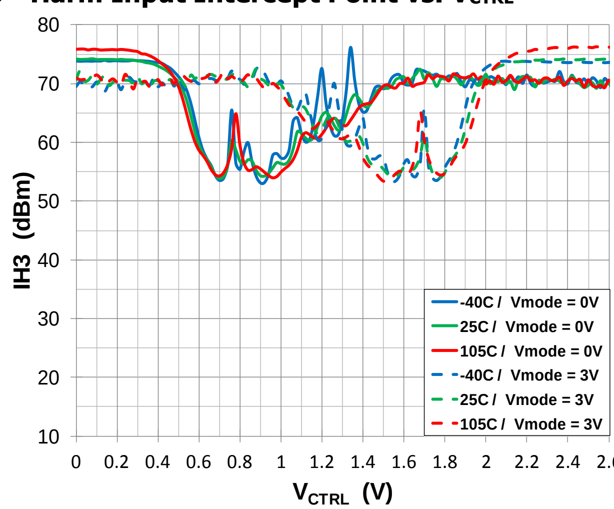
Output IP2 vs. V_{CTRL}



2nd Harm Input Intercept Point vs. V_{CTRL}

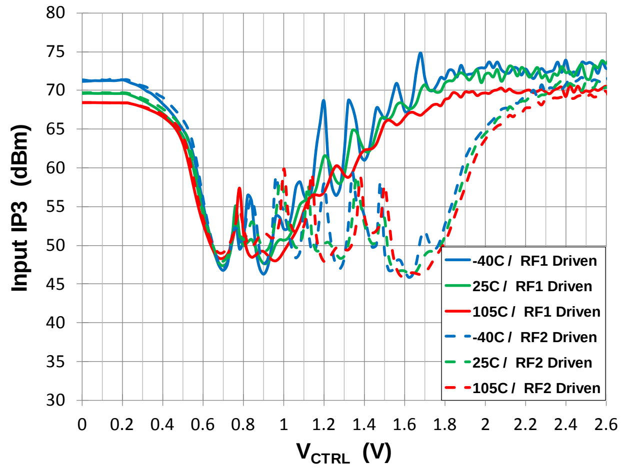


3rd Harm Input Intercept Point vs. V_{CTRL}

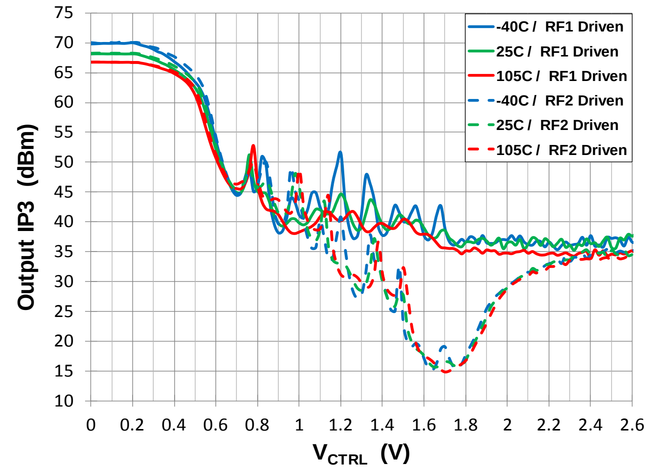


TYPICAL OPERATING CONDITIONS 2GHz, V_{DD}=3.3V [IP3, IP2, IH2, IH3 VS. V_{CTRL}, RF1/RF2 DRIVEN] (-8-)

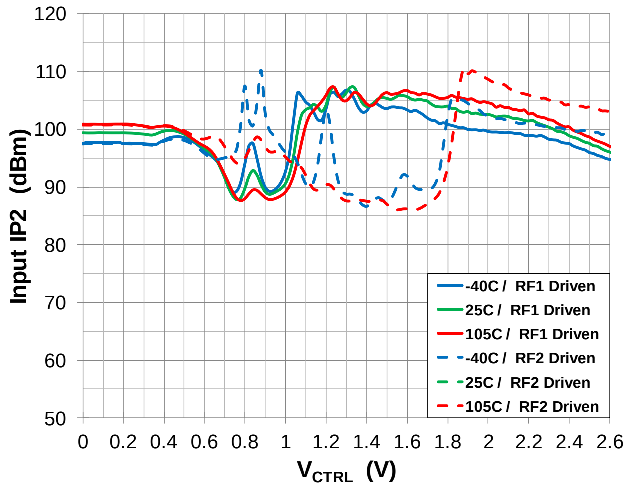
Input IP3 vs. V_{CTRL}



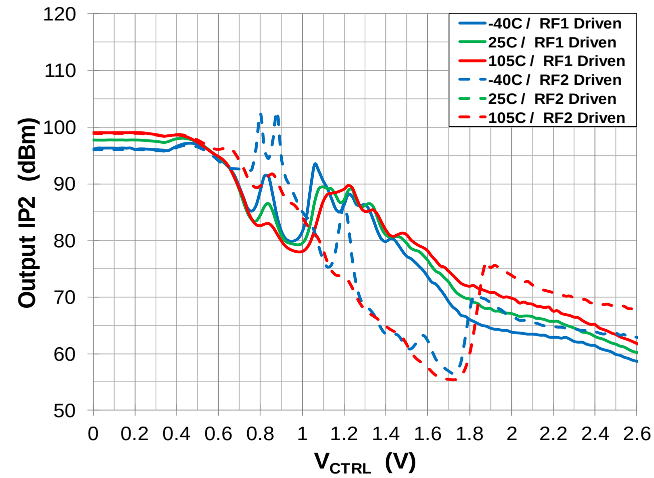
Output IP3 vs. V_{CTRL}



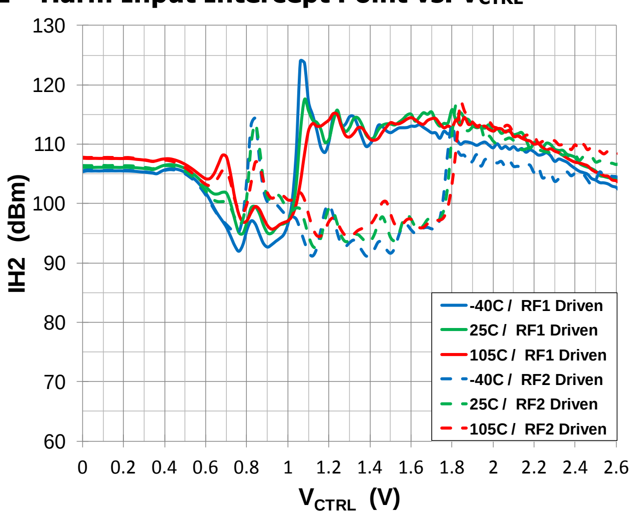
Input IP2 vs. V_{CTRL}



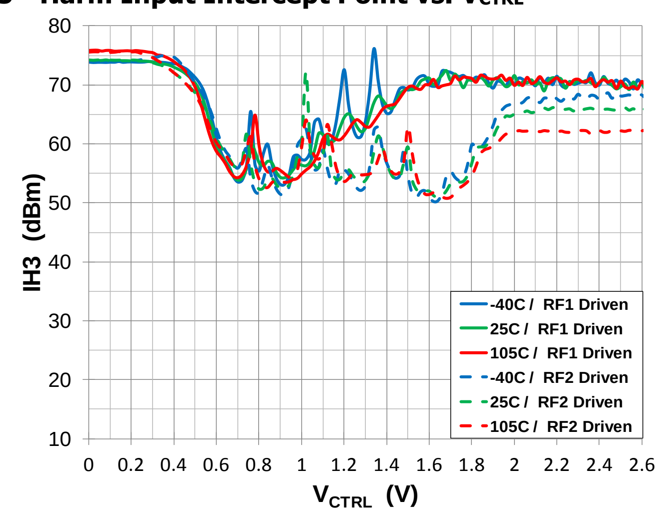
Output IP2 vs. V_{CTRL}



2nd Harm Input Intercept Point vs. V_{CTRL}

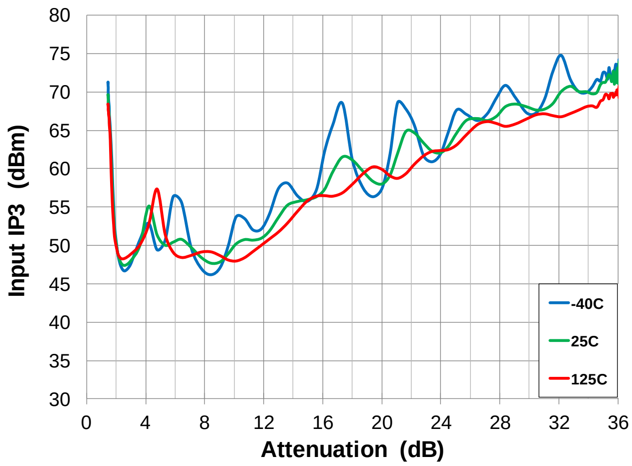


3rd Harm Input Intercept Point vs. V_{CTRL}

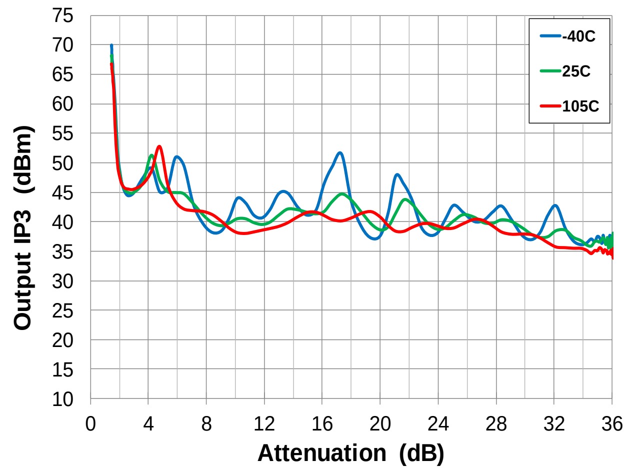


Typical Operating Conditions 2GHz, V_{DD}=3.3V [IP3, IP2, IH2, IH3 vs. Attenuation] (-9-)

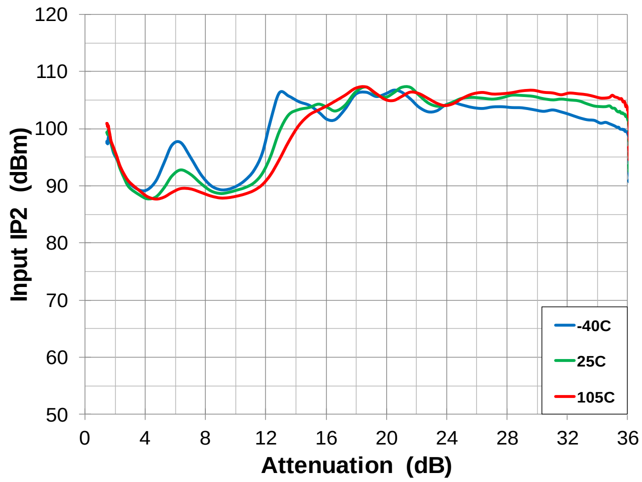
Input IP3 vs. Attenuation



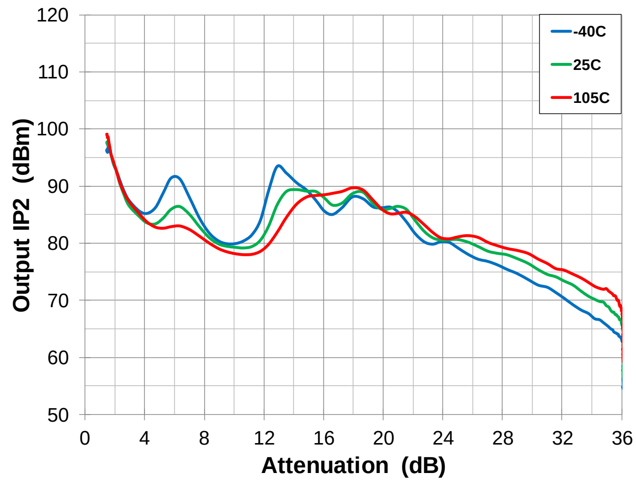
Output IP3 vs. Attenuation



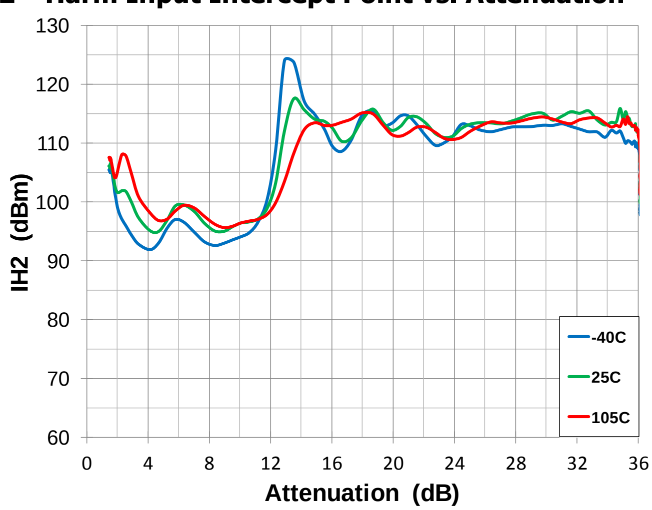
Input IP2 vs. Attenuation



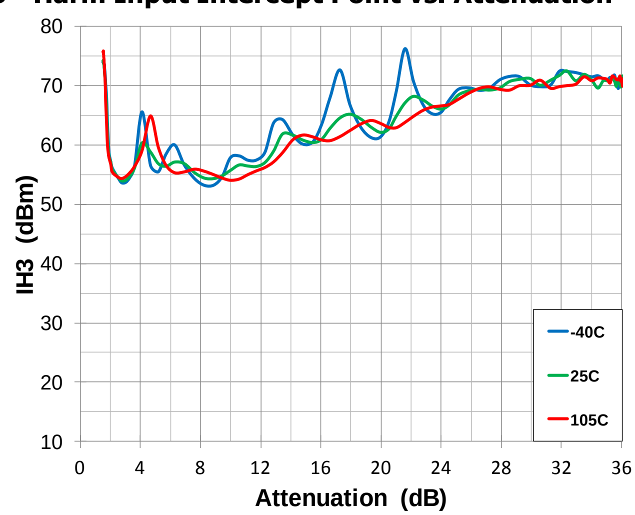
Output IP2 vs. Attenuation



2nd Harm Input Intercept Point vs. Attenuation

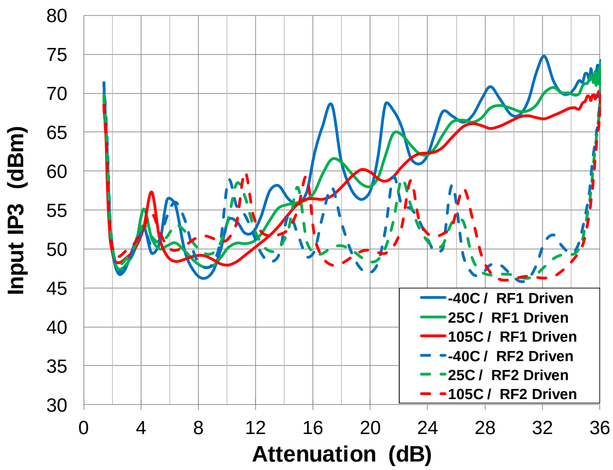


3rd Harm Input Intercept Point vs. Attenuation

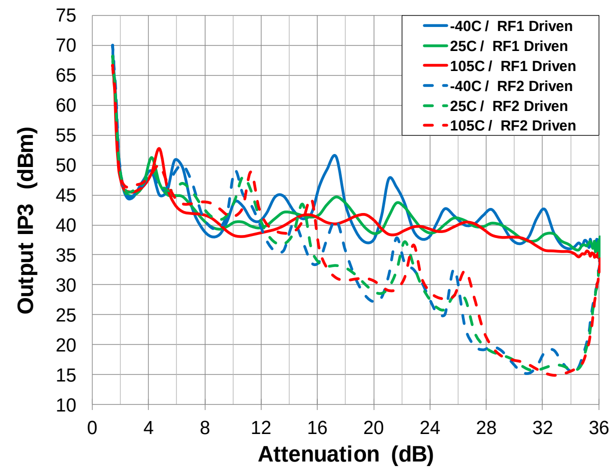


TYPICAL OPERATING CONDITIONS 2GHz, V_{DD}=3.3V [IP3, IP2, IH2, IH3 VS. ATTEN, RF1/RF2 DRIVEN] (-10-)

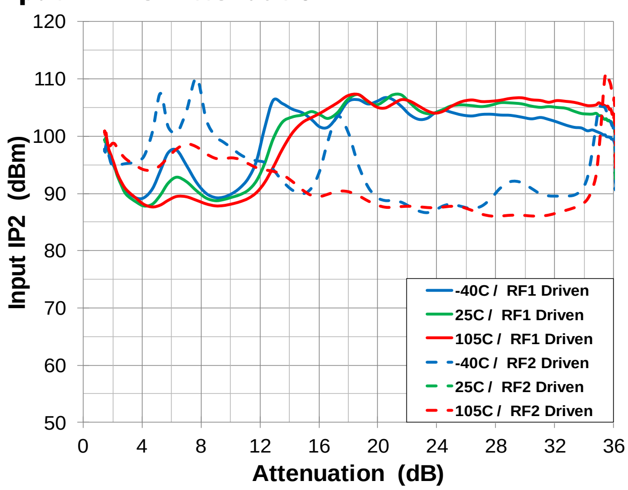
Input IP3 vs. Attenuation



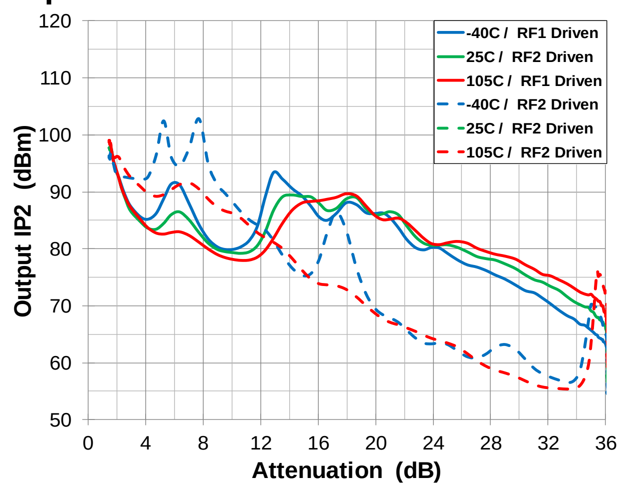
Output IP3 vs. Attenuation



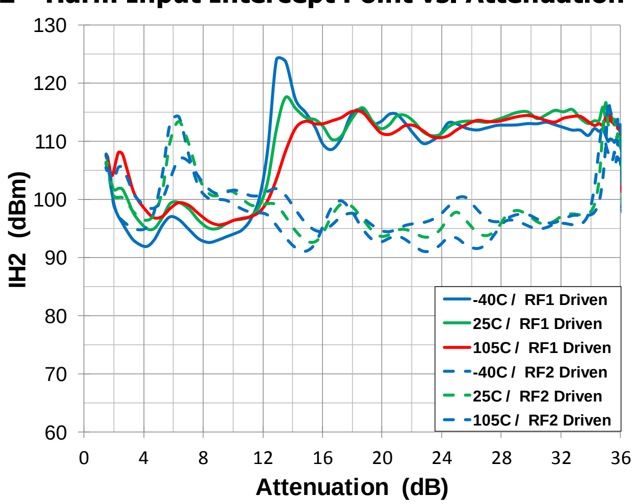
Input IP2 vs. Attenuation



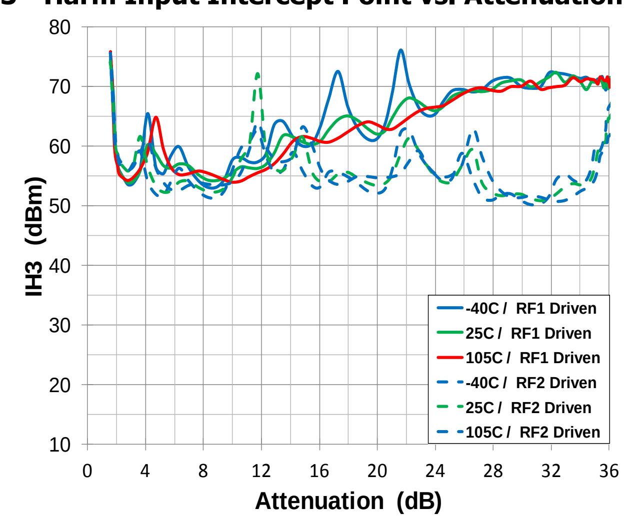
Output IP2 vs. Attenuation



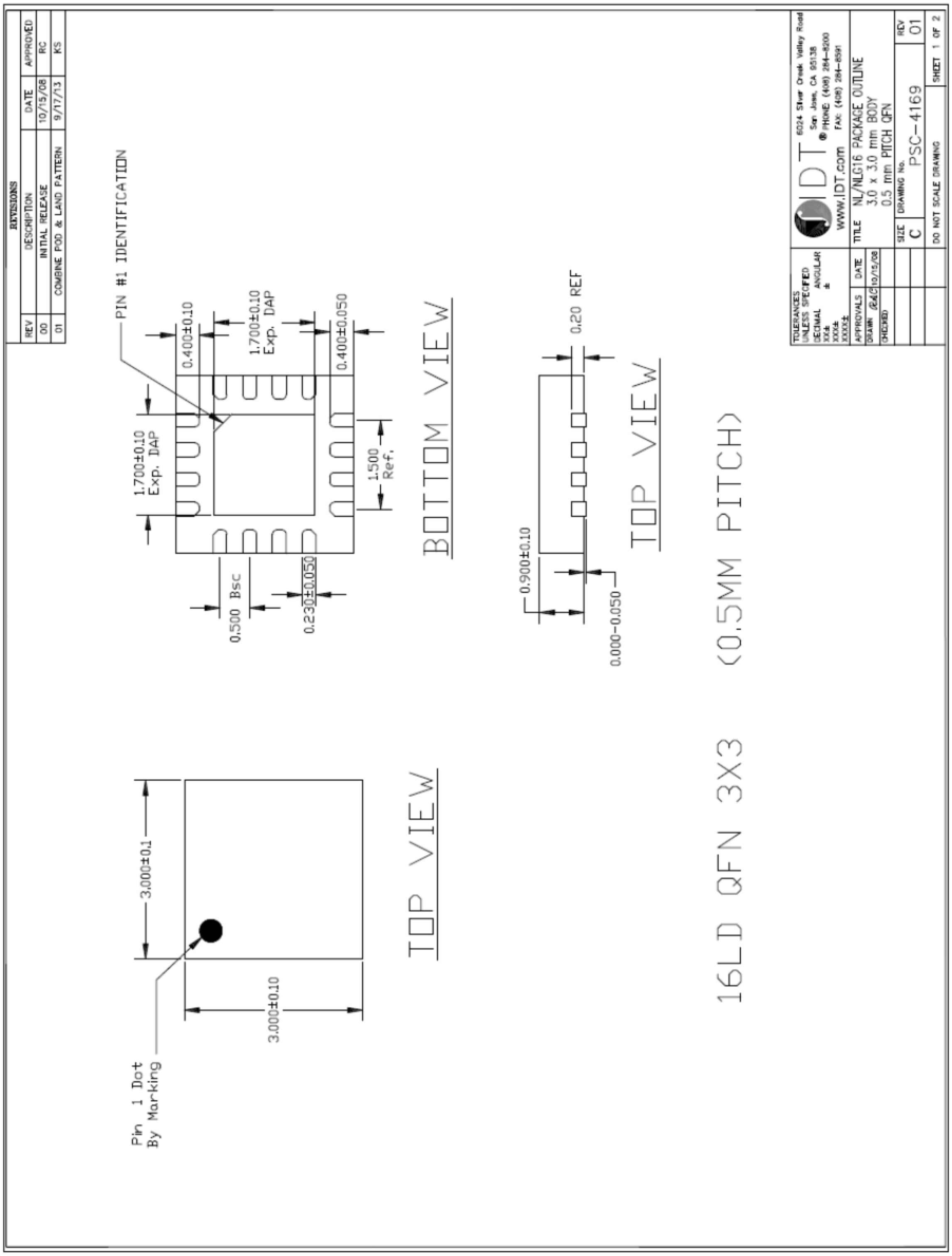
2nd Harm Input Intercept Point vs. Attenuation



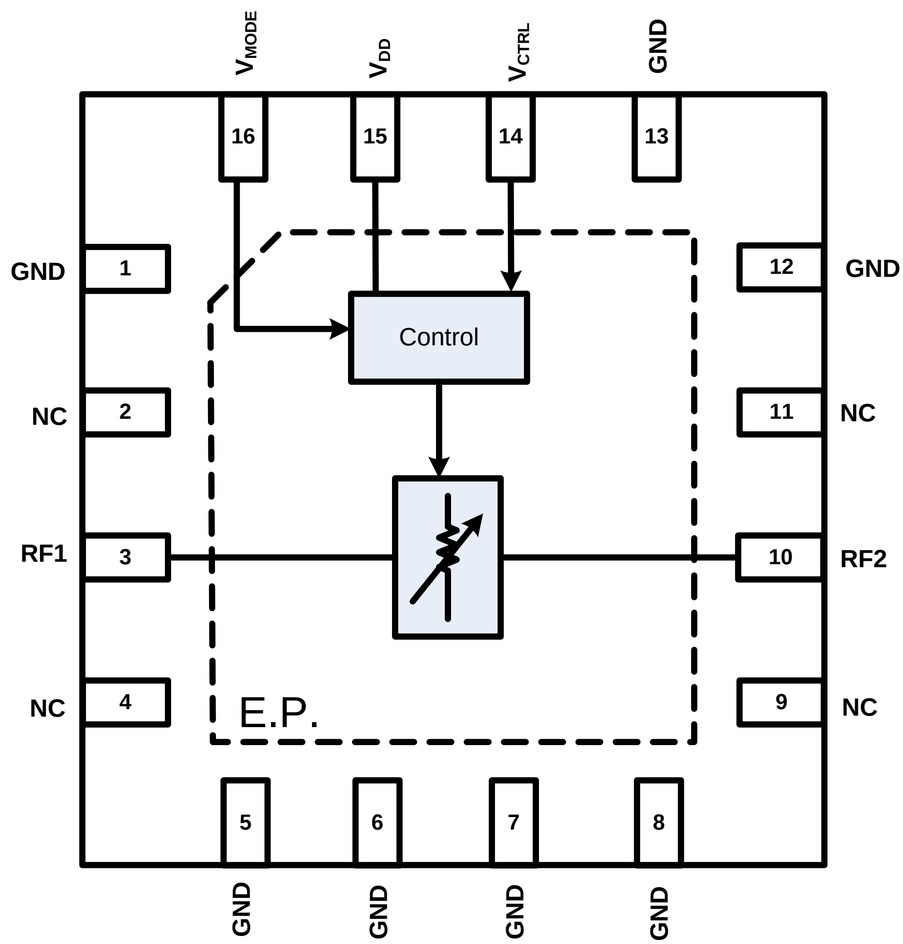
3rd Harm Input Intercept Point vs. Attenuation



PACKAGE DRAWING (3X3 16 PIN)



PINOUT & BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1, 5, 6, 7, 8, 12, 13	GND	Ground these pins as close to the device as possible.
2, 4, 9, 11	NC	No internal connection. These pins can be left unconnected or connected to ground (recommended).
3	RF1	RF Port 1. Matched to 50 ohms. Must use an external AC coupling capacitor as close to the device as possible. For low frequency operation increase the capacitor value to result in a low reactance at the frequency of interest.
10	RF2	RF Port 2. Matched to 50 ohms. Must use an external AC coupling capacitor as close to the device as possible. For low frequency operation increase the capacitor value to result in a low reactance at the frequency of interest.
14	V_{CTRL}	Attenuator control voltage. Apply a voltage in the range as specified in the Operating Conditions. See application section for details about V_{CTRL}.
15	V_{DD}	Power supply input. Bypass to GND with capacitors close as possible to pin.
16	V_{MODE}	Attenuator slope control. Set to logic LOW to enable negative attenuation slope. Set to logic HIGH to enable positive attenuation slope.
	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to achieve the specified RF performance.

APPLICATIONS INFORMATION

Default Start-up

V_{MODE} must be tied to either GND or Logic HIGH. If V_{CTRL} pin is left floating, the part will power up in the minimum attenuation state when V_{MODE} = GND, or the maximum attenuation state when V_{MODE} = High.

V_{CTRL}

The V_{CTRl} pin is used to control the attenuation of the F2250. With V_{MODE} set to a logic low (high) this places the device in a negative (positive) slope mode where increasing (decreasing) voltage produces an increasing (a decreasing) attenuation from min attenuation (max attenuation) to max attenuation (min attenuation) respectively. The V_{CTRl} pin has an on-chip pullup ESD diode so V_{DD} should be applied before V_{CTRl} is applied. If this sequencing is not possible, then resistor R2 should be set for 1kΩ to limit the current into the V_{CTRL} pin.

V_{MODE}

The V_{MODE} pin is used to set the attenuation vs. V_{CTRl} slope. With V_{MODE} set to logic low (high) this will set the attenuation slope to be negative (positive). A negative (positive) slope is defined as increased (decreased) attenuation with increasing (decreasing) V_{CTRl} voltage. The EVKIT provides and on-board jumper to manually set the $V_{MODE.}$ Installing a jumper on header J2 from VMODE to GND (VHI) to set the device for a negative (positive) slope.

RF1 and RF2 Ports

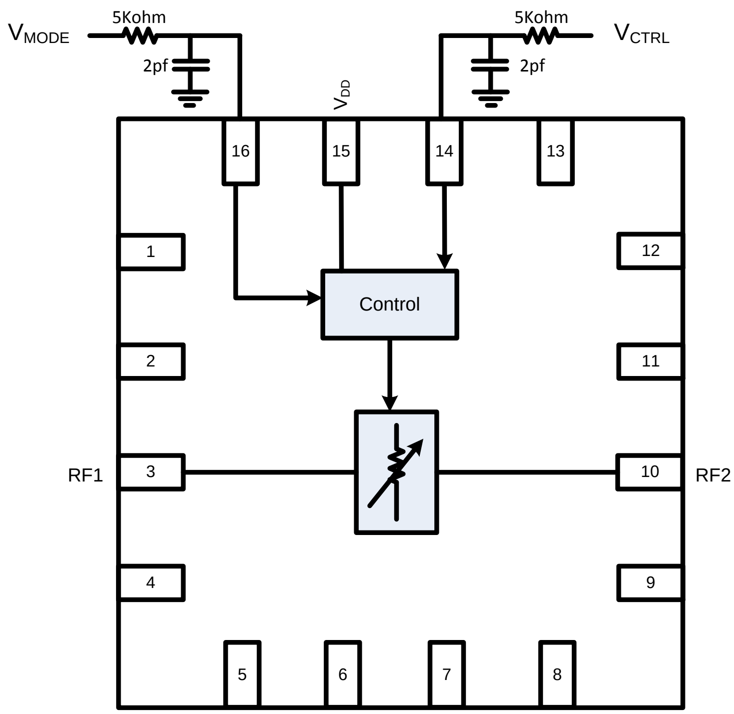
The F2250 is a bi-directional device thus allowing RF1 or RF2 to be used as the RF input. As displayed in the Typical Operating Conditions curves, RF1 shows some enhanced linearity performance and therefore should be used as the RF input, if possible, for best results. This F2250 has been designed to accept high RF input power levels, therefore V_{DD} must be applied prior to the application of RF power to ensure reliability. DC blocking capacitors are required on the RF pins and should be set to a value that results in a low reactance over the frequency range of interest.

Power Supplies

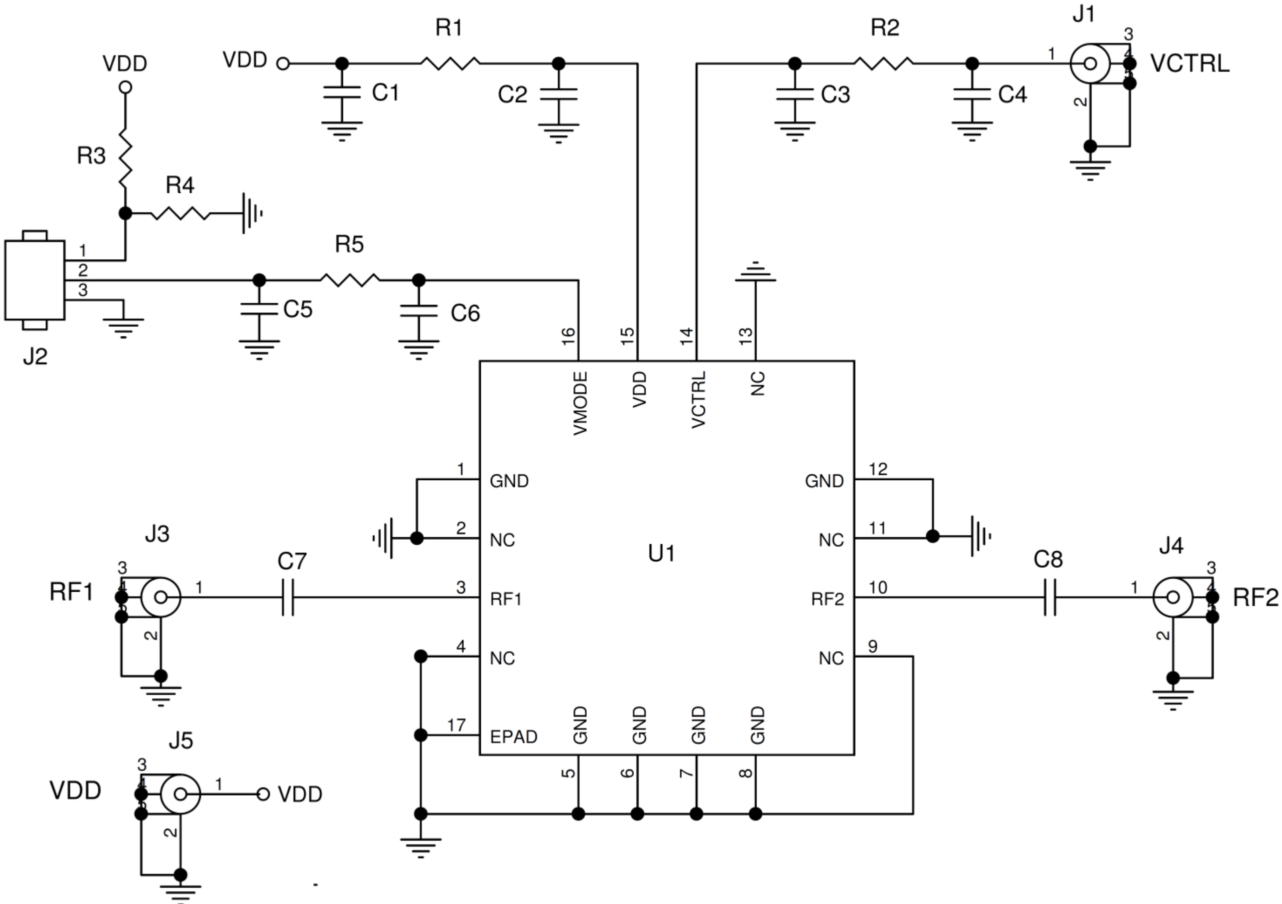
The supply pin should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

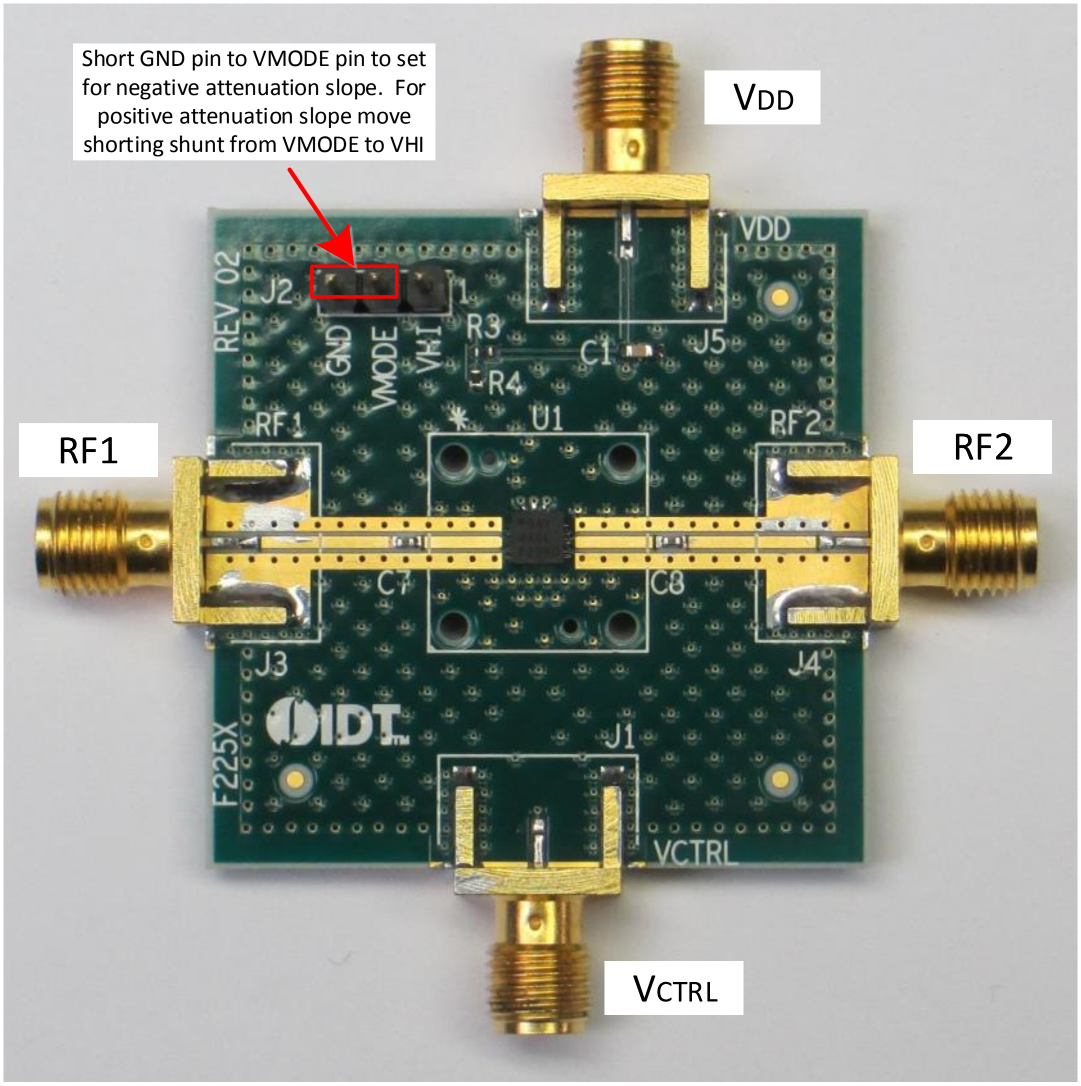
If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of control pins 14 and 16 is recommended as shown below.



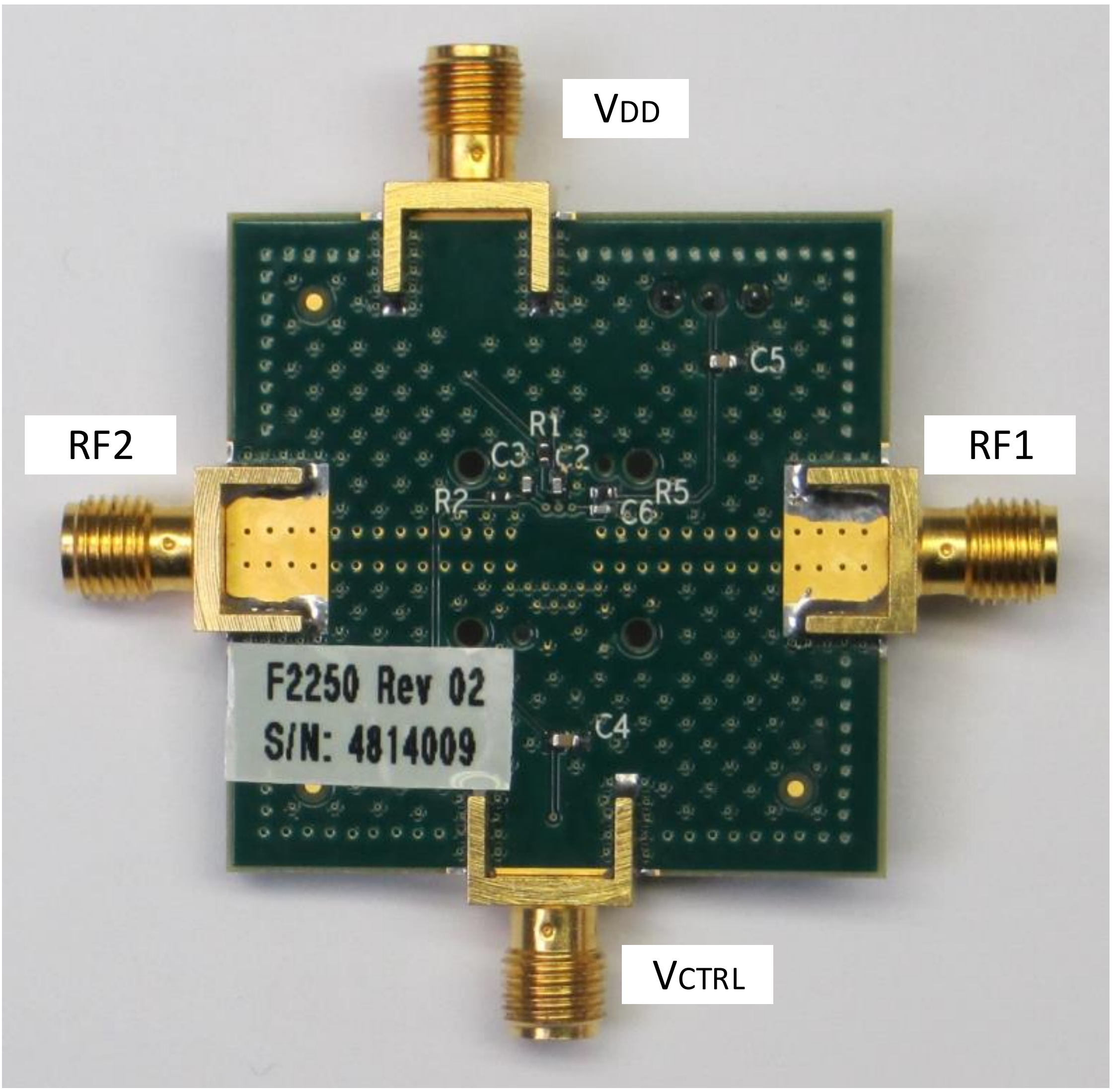
EVKIT/ APPLICATIONS CIRCUIT



EVKIT PICTURE / LAYOUT (TOP SIDE)



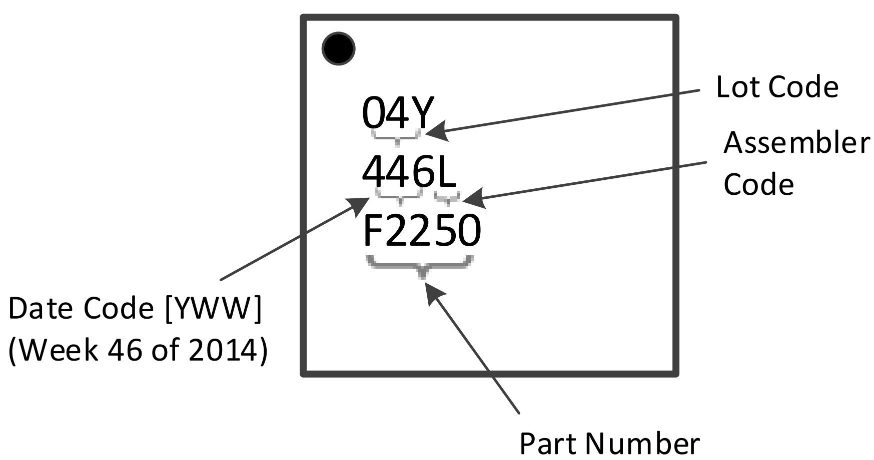
EVKIT PICTURE / LAYOUT (BOTTOM SIDE)



EVKIT BOM

Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
C1, C4, C5	3	10nF ±5%, 50V, X7R Ceramic Capacitors (0603)	GRM188R71H103J	Murata
C2, C3, C6	3	1000pF ±5%, 50V, C0G Ceramic Capacitors (0402)	GRM1555C1H102J	Murata
C7, C8	2	100pF ±5%, 50V, C0G Ceramic Capacitors (0402)	GRM1555C1H101J	Murata
R1, R2, R5	3	0Ω Resistors (0402)	ERJ-2GE0R00X	Panasonic
R3, R4	2	100kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1003X	Panasonic
J1, J3-J5	4	Edge Launch SMA (0.375 inch pitch ground tabs)	142-0701-851	Emerson Johnson
J2	1	CONN HEADER VERT SGL 3 X 1 POS GOLD	961103-6404-AR	3M
U1	1	Voltage Variable Attenuator	F2250NLGK	IDT
	1	Printed Circuit Board	F225x REV (02)	IDT

TOP MARKINGS



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