Description

The F4481 is a 400MHz to 1100MHz Quad Path TX DVGA outfitted with 100Ω differential inputs and 50Ω single-ended outputs. The device is part of a complete family of VGAs targeting FDD and TDD applications within the 400MHz to 4200MHz frequency range.

Using a single 3.3V power supply and only 520mA of ICC, the F4481 provides four independent transmit paths, each with 28dB maximum gain, +40dBm OIP3, +16dBm output P1dB, and 5.5dB NF at 900MHz under typical conditions. Each channel includes a glitch-free digital step attenuator that reduces gain by up to 31.5dB in precise 0.5dB steps.

The F4481 is packaged in an 8 × 8 mm 56-LGA, with matched 100Ω differential input and 50Ω single-ended output impedances for ease of integration into the signal path.

Competitive Advantage

- Combines four independent TX channels consisting of an LPF, LNA, DSA, and Driver in a compact 8 × 8 mm LGA package
- Low DC power
- High linearity
- High reliability
- Uses Renesas' patented *Zero-Distortion™* and *Glitch-Free™* technologies, providing superior performance and PA damage protection over the entire RF gain range

Typical Applications

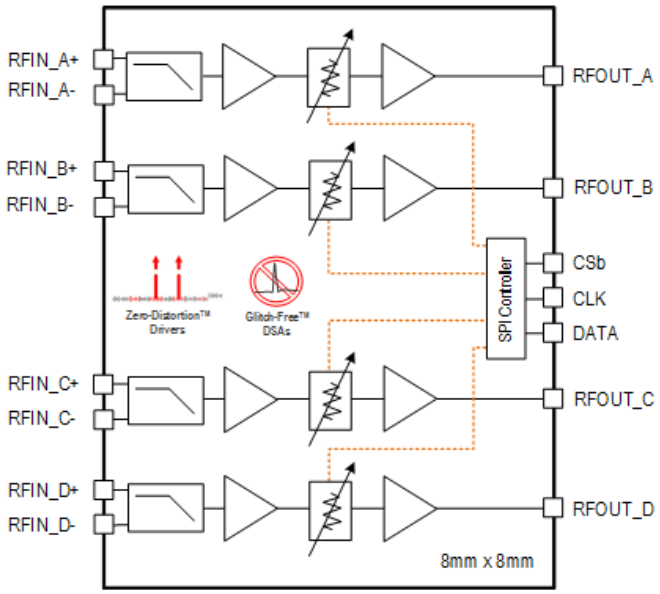
- 4G and 5G multi-mode, multi-carrier transmitters
- LTE and UMTS/WCDMA base stations
- Active antenna systems
- Digital radio

Features

- Independent quad channels for FDD TX applications
- RF range: 400MHz to 1100MHz
  - F4482: 1300MHz to 2800MHz
- 28dB typical max gain at 900MHz
- Precise SPI-controlled *Glitch-Free™* gain adjustment
  - 31.5dB gain range with 0.5dB step size
- 5.5dB NF at 900MHz
- +40dBm OIP3 at 900MHz
- +16dBm output P1dB at 900MHz
- 3.3V supply voltage
- I_{CC} = 520mA
- 100Ω differential input impedances
- 50Ω single-ended output impedances
- 1.8V and 3.3V logic support
- Independent Channel Standby modes for power savings
- Operating temperature (T_{EP}) range: -40°C to +105°C
- 8 × 8 mm, 56-LGA package

Block Diagram

Figure 1. Block Diagram



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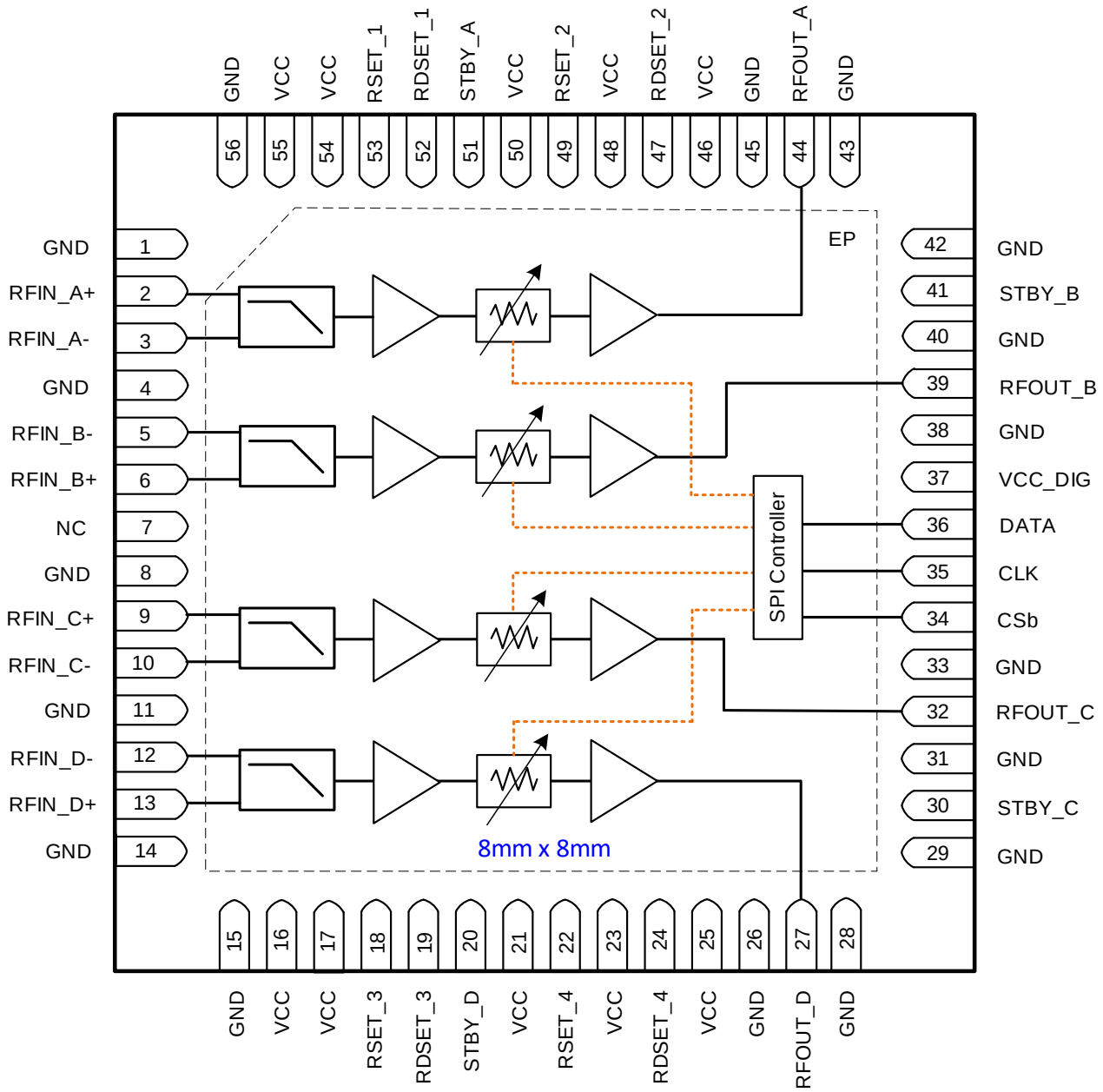
Pin Assignments

Figure 2. Pin Assignments for 8.0 × 8.0 × 0.65 mm 56-LGA Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 4, 8, 11, 14, 15, 26, 28, 29, 31, 33, 38, 40, 42, 43, 45, 56	GND	Internally grounded. These pins must be grounded as close to the device as possible.
2	RFIN_A+	Channel A RF differential input. Internally matched to 100Ω. Must use external DC blocks.
3	RFIN_A-	
5	RFIN_B-	Channel B RF differential input. Internally matched to 100Ω. Must use external DC blocks.
6	RFIN_B+	
7	NC	No internal connection. It is highly recommended that this pin be connected to a ground via that is located as close to the pin as possible.
9	RFIN_C+	Channel C RF differential input. Internally matched to 100Ω. Must use external DC blocks.
10	RFIN_C-	
12	RFIN_D-	Channel D RF differential input. Internally matched to 100Ω. Must use external DC blocks.
13	RFIN_D+	
16, 17, 21, 23, 25, 46, 48, 50, 54, 55	V_{CC}	Power supply. Must place the bypass capacitor as close to the pin as possible.
18	RSET_3	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
19	RDSET_3	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
20	STBY_D	Standby channel D. With Logic LOW applied to this pin (or if the pin is left unconnected), channel D enters STBY mode and is powered off. With Logic HIGH applied to this pin, channel D is powered on and is fully operational.
22	RSET_4	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
24	RDSET_4	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
27	RFOUT_D	RF output D internally matched to 50Ω. Must use external DC block.
30	STBY_C	Standby channel C. With Logic LOW applied to this pin (or if the pin is left unconnected), channel C enters STBY mode and is powered off. With Logic HIGH applied to this pin, channel C is powered on and is fully operational.
32	RFOUT_C	RF output C internally matched to 50Ω. Must use external DC block.
34	CSb	Serial chip select. CSb pin can be pulled up to V_{CC} and down to GND. 1.8 V and 3.3 V logic compatible.

Number	Name	Description
35	CLK	Serial clock input. 1.8 V and 3.3 V logic compatible.
36	DATA	Data write for the 3-wire serial interface. 1.8V and 3.3V logic compatible.
37	V_{CC_DIG}	Digital power supply. Must place the bypass capacitor as close to the pin as possible.
39	RFOUT_B	RF output B internally matched to 50Ω. Must use external DC block.
41	STBY_B	Standby channel B. With Logic LOW applied to this pin (or if the pin is left unconnected), channel B enters STBY mode and is powered off. With Logic HIGH applied to this pin, channel B is powered on and is fully operational.
44	RFOUT_A	RF output A internally matched to 50Ω. Must use external DC block.
47	RDSET_2	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
49	RSET_2	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
51	STBY_A	Standby channel A. With Logic LOW applied to this pin (or if the pin is left unconnected), channel A enters STBY mode and is powered off. With Logic HIGH applied to this pin, channel A is powered on and is fully operational.
52	RDSET_1	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
53	RSET_1	Connect external resistor to GND to optimize amplifier performance. Refer to Table 12, Bill of Materials (BOM).
	– EPAD	Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F4481 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
V_{CC} to GND	V_{CC}	-0.3	+3.6	V
DATA, CSb, CLK	V_{CTL}	-0.3	V_{CC} + 0.25	V
STBY	V_{CTL}	-0.3	V_{CC} + 0.25	V
STBY Minus V_{CC} Voltage (voltage difference)	$V_{STBY-VCC}$		0.3	V
RSET_1, RSET_2, RSET_3, RSET_4 Pin Maximum Output DC Current [a]	I_{RSET}		+1	mA
RDSET_1, RDSET_2, RDSET_3, RDSET_4 Pin Maximum Output DC Current [a]	I_{RDSET}		+1	mA
RFIN_A, RFIN_B, RFIN_C, RFIN_D to GND Externally Applied DC Voltage	V_{RFIN}	-0.3	+0.3	V
RFOUT_A, RFOUT_B, RFOUT_C, RFOUT_D to GND Externally Applied DC Voltage	V_{RFOUT}	V_{CC} - 0.15	V_{CC} + 0.15	V
RF Input Power (RFIN_A, RFIN_B, RFIN_C, RFIN_D) applied for 24 Hours Maximum [b]	P_{IN_MAX24}		+17	dBm
Storage Temperature Range	T_{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)	T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V_{ESDHBM}		2000 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)	V_{ESDCDM}		250 (Class C1)	V

[a] RSET_1, RSET_2, RSET_3, RSET_4, RDSET_1, RDSET_2, RDSET_3 and RDSET_4 pins MUST be connected to ground with resistors; otherwise, damage to the part may result. For suggested resistor values, see Table 12.

[b] Exposure to these maximum RF levels can result in significant VCC current draw due to overdriving the amplifier stages.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Supply Voltage [a]	V_{CC}	All V_{CC} pins.	3.15	3.3	3.45	V
Operating Temperature Range	T_{EP}	Exposed paddle temperature.	-40		+105	°C
Junction Temperature	T_J				125	°C
RF Frequency Range	f_{RF}	Band 1	400		500	MHz
		Band 2	570		1100	
Maximum CW Input Power	P_{IN_MAX}	Z_S = 100Ω, Z_L = 50Ω.			Note [b]	dBm
RF Input Port Impedance	Z_{RFI}	Differential impedance.		100		Ω
RF Output Port Impedance	Z_{RFO}	Single-ended impedance.		50		Ω

[a] Power-on resets will only occur for V_{CC} < 3V. Device is designed to function with any supply voltage ≥ 3V, although performance may be degraded when operated outside the recommended voltage range.

[b] Level = Lower of (-7.5dBm + attenuation setting) or 5dBm.

Electrical Characteristics

See the F4481 Applications Circuit. Unless stated otherwise, specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, f_{RF} = 900MHz, STBY_A = STBY_B = STBY_C = STBY_D = HIGH, Z_S = 100Ω differential, Z_L = 50Ω single-ended, maximum gain setting, and output power = 0dBm/tone. EVKit trace and connector losses are de-embedded.

Table 4. Electrical Characteristics – General

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input HIGH	V_{IH}	Supports both 1.8V and 3.3V logic.	*1.07* [a]			V
Logic Input LOW	V_{IL}				*0.63*	V
SPI Logic Current (CSb, CLK, DATA)	I_{CTL}	3.3V logic.	*-5*		*5*	µA
		1.8V logic.	*-5*		*5*	
Standby Logic Current (STBY_A, STBY_B, STBY_C, STBY_D)	I_{IH}, I_{IL}	3.3V logic.	*5*		*40*	µA
		1.8V logic.	*5*		*40*	
Supply Current [b]	I_{CC_4}	4 channels on.		520	*630*	mA
	I_{CC_3}	3 channels on.		400		
	I_{CC_2}	2 channels on.		270		
	I_{CC_1}	1 channel on.		150		
Standby Current	I_{CC_STBY}	All channels off.		20	*30*	mA
Power ON Switching Time	t_{ON}	50% STBY to RF output settled to within ±0.1dB.			1 [c]	µs
Power OFF Switching Time	t_{OFF}	50% STBY to 35dBc reduction of output power.			1 [c]	µs
Lineup Out-of-Band Rejection at Max Gain [c]	$f_{REJECTION}$	Total gain variation over f_{RF} = 400MHz to 500MHz. Referred to f_{RF} = 450MHz. DSA 0dB attenuation.			3	dBc
		Total gain variation over f_{RF} = 570MHz to 1100MHz. Referred to f_{RF} = 900MHz. DSA 0dB attenuation.			3	
		4800MHz < f_{RF} < 7000MHz. Referred to f_{RF} = 900MHz. DSA 0dB attenuation.	40			
Gain Settling Time [c]	G_{ST}	Any 2dB step in the 0dB to 31.5dB range. 50% of CSb to 1% / 99% RF.		0.4	1	µs
DSA Adjustment Range	G_{RANGE}			31.5		dB
DSA Step Resolution	G_{STEP}	LSB		0.5		dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Adjacent State Attenuator Glitching	$ATTN_G$	DSA step: 5.5dB to 6dB.		0.8		dB
		DSA step: 6dB to 5.5dB.		0.9		
		DSA step: 11.5dB to 12dB.		1.5		
		DSA step: 12dB to 11.5dB.		1		
		DSA step: 17.5dB to 18dB.		1.2		
		DSA step: 18dB to 17.5dB.		0.8		
		DSA step: 23.5dB to 24dB.		1.3		
		DSA step: 24dB to 23.5dB.		0.8		
		DSA step: 29.5dB to 30dB.		0.5		
		DSA step: 30dB to 29.5dB.		1		
		All Other 0.5dB DSA steps.		0.6		
		All Other 2dB DSA steps.		1		
Common Mode Rejection	CMR	f_{RF} = 450MHz to 650MHz	30			dB
		f_{RF} = 400MHz to 1100MHz	20			
Amplitude Imbalance	$IMBAL_{AMP}$	Measures RFIN- to RFOUT and compares RFOUT to RFIN+ amplitude.		1		dB
Phase Imbalance	$IMBAL_{PH}$	Measures RFIN- to RFOUT and compares RFOUT to RFIN+ phase. Deviation is from ideal 180 degrees.		5		deg

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Serial Clock Speed	f_{CLK}				*50*	MHz
CSb to First Serial Clock Rising Edge	t_{LS}	SPI 3-wire Bus. 50% of CSb falling edge to 50% of CLK rising edge.	*10* [c]			ns
Serial Data Hold Time	t_H	SPI 3-wire Bus. 50% of CLK rising edge to 50% of DATA falling edge.	*10* [c]			ns
Final Serial Clock Rising Edge to CSb	t_{LCS}	SPI 3-wire Bus. 50% of CLK rising edge to 50% of CSb rising edge.	*10* [c]			ns
Stability K Factor	K_{FACTOR}	T_{EP} = -40˚C to +105˚C. V_{CC} = 3.15V to 3.45V. f_{RF} = 10MHz to 9GHz.	1			

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

[b] For input signal power level equal to P1dB, expect DC current to increase above typical value.

[c] Speeds are measured after SPI programming is completed (data latched with CSb = HIGH).

Table 5. Electrical Characteristics – Band 1 (400MHz to 500MHz)

See the F4481 Applications Circuit. Unless stated otherwise, specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, f_{RF} = 450MHz, STBY_A = STBY_B = STBY_C = STBY_D = HIGH, Z_S = 100Ω differential, Z_L = 50Ω single-ended, maximum gain setting, and output power = 0dBm/tone. EVKit trace and connector losses are de-embedded.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN}		15 [a]	25		dB
RF Output Return Loss	RL_{OUT}		11	13		dB
Maximum Gain	G_{MAX}	DSA 0dB attenuation.	*24.5*	27	*30*	dB
Mid-Range Gain	G_{MID}	DSA 14dB attenuation.	*10.5*	13	*16*	dB
Minimum Gain	G_{MIN}	DSA 31.5dB attenuation.	*-7.5*	-4.5	*-1.8*	dB
Gain Variation Over Temperature	G_{TEMP}	DSA 0dB attenuation. Over T_{EP} = -40°C to +105°C, and relative to 25°C.		+1.6 / -2.4		dB
		DSA 14dB attenuation. Over T_{EP} = -40°C to +105°C, and relative to 25°C.		+1.4 / -2.1		
Gain Flatness	G_{FLAT}	Any 100MHz BW.		1		dB
Gain Ripple	G_{RIPPLE}	In any 20MHz range.		0.4		dB
Intra-die Channel-to-Channel Differences in Gain	G_A - G_B	Worst case difference in Gain for any 2dB step over the 0dB to 30dB attenuation range (with channels A and B both set to identical DSA attenuation levels).		0.2		dB
Reverse Isolation	G_{REV}	DSA 0dB attenuation.		45		dB
		DSA 31.5dB attenuation.		75		
Intra-Die Channel Isolation [b]	$ISOL_{A-B}$	Any RF input/output combination involving channel A paired with channel B. DSA = 0dB.	40	45		dB
Inter-Die Channel Isolation [b]	$ISOL_{B-C}$	Any RF input / output combination involving channel B (die 1) paired with channel C (die 2). DSA = 0dB.	50	55		dB
Filter Group Delay in Passband	τ	f_{RF} = 400MHz to 500MHz.		2.5		ns
Filter Group Delay Ripple	τ_{RIPPLE}	f_{RF} = 400MHz to 500MHz.		1.1		ns

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Intra-die Channel-to-Channel Differences in Group Delay	$\tau_A - \tau_B$	Worst case difference in Group Delay for any 2dB step over the 0dB to 30dB attenuation range (with channels A and B both set to identical DSA attenuation levels).			0.02		ns
Cross Channel Group Delay in Passband vs. Channel Group Delay in Passband	$\tau_{XCHANNEL} - \tau$	f_{RF} = 400MHz to 500MHz Worst case cross-channel leakage combinations (A to B) - B; (B to A) - A; (B to C) - C; (C to B) - B; (C to D) - D; (D to C) - C	DSA = 0dB		2		ns
			DSA = 14dB		2		
			DSA = 28dB		2		
Step Error (DNL)	$ERROR_{STEP}$	Maximum error between adjacent steps.			+0.16 /-0.26		dB
Maximum Absolute Error (INL) [c]	$ERROR_{ABS}$	Over attenuation range referenced to maximum gain state.			± 0.8		dB
Phase Shift Over Any 5ºC Temperature Change Over the -40ºC to 105ºC Range	$\Phi_{\Delta Temp\ @\ 0dB}$	DSA = 0dB			0.6		deg
	$\Phi_{\Delta Temp\ @\ 14dB}$	DSA = 14dB			0.3		
	$\Phi_{\Delta Temp\ @\ 28dB}$	DSA = 28dB			0.3		
Phase Shift Between Startups	$\Phi_{ON-OFF-ON}$	Channel A or Channel B Phase Shifts. Measuring “On State” phase shifts occurring over time as the device is powered on/off via STBY mode or via PORs (power-on resets).				2	deg
	$[\Phi_A - \Phi_B]_{ON-OFF-ON}$	Channel A - Channel B Phase Shifts. Measuring “On State” phase shifts occurring over time as the device is powered on/off via STBY mode or via PORs (power-on resets).				10	
Phase Shift Between Any 2dB Step	$\Phi_{2dB\ Step}$	Worst case, any 2dB step.			+0.15 / -0.7		deg
Phase Shift Between Any 8dB Step	$\Phi_{8dB\ Step}$	Worst case, any 8dB step.			4		deg

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Phase Shift Relative to 0dB Attenuation State	$\Phi_{\Delta MAX}$	DSA 31.5dB attenuation.			-18		deg
	$\Phi_{\Delta MID}$	DSA 14dB attenuation.			-12		
Intra-die Channel-to-Channel Differences in Phase	$\Phi_A - \Phi_B$	$\Phi_{A\ @\ 16dB} - \Phi_{B\ @\ 16dB}$ Worst case difference in phase with channels A and B both set to DSA = 16dB attenuation levels.			10		deg
		$[\Phi_{A\ @\ XdB} - \Phi_{B\ @\ XdB}] - [\Phi_{A\ @\ 16dB} - \Phi_{B\ @\ 16dB}]$ Worst case difference in phase between the 16dB DSA attenuation case and any other state when the DSAs are set to XdB. X = 16 ± 2N, where N is an integer ranging from 1 to 8.			2		
Noise Figure at Room (25˚C) [d]	NF_{ROOM}	T_{EP} = 25˚C	DSA = 0dB		7.3	9 [a]	dB
			DSA = 14dB		10.2		
			DSA = 28dB		21.5		
Noise Figure at Hot (105˚C) [d]	NF_{HOT}	T_{EP} = 105˚C	DSA = 0dB		9.2		dB
			DSA = 14dB		12.5		
			DSA = 28dB		24		
Noise Figure at Cold (-40˚C) [d]	NF_{COLD}	T_{EP} = -40˚C	DSA = 0dB		5.7		dB
			DSA = 14dB		8.3		
			DSA = 28dB		19.4		

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Output Third Order Intercept Point [d]	OIP3	DSA = 0dB. T_{EP} = 105˚C. P_{OUT} = 0dBm / tone. 5MHz tone separation.		34		dBm
		DSA = 4dB. T_{EP} = 105˚C. P_{OUT} = 0dBm / tone. 5MHz tone separation.		34		
		DSA = 14dB. T_{EP} = 25°C. P_{OUT} = -3dBm / tone. 5MHz tone separation.	27 [a]	33		
		DSA = 28dB. T_{EP} = -40˚C. P_{OUT} = -10dBm / tone. 5MHz tone separation.		17		
Output 1dB Compression Point [d]	OP1dB	DSA = 0dB		15		dBm
		DSA = 14dB	12	14		
		DSA = 28dB		0.9		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

[b] Signal applied to RFIN_X. Measure desired signal at RFOUT_X and compare to undesired leakage signal level at RFOUT_Y.

[c] Absolute Error = ± [0.05 + 0.05*(DSA attenuator setting)]

[d] Measured by terminating one differential RFIN port to 50Ω load and applying RF signal to second RFIN port.

Table 6. Electrical Characteristics – Band 2 (570MHz to 1100MHz)

See the F4481 Applications Circuit. Unless stated otherwise, specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, f_{RF} = 900MHz, STBY_A = STBY_B = STBY_C = STBY_D = HIGH, Z_S = 100Ω differential, Z_L = 50Ω single-ended, maximum gain setting, and output power = 0dBm/tone. EVKit trace and connector losses are de-embedded.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN}		12 [a]	16		dB
RF Output Return Loss	RL_{OUT}		10	20		dB
Maximum Gain	G_{MAX}	DSA 0dB attenuation.	*25.5*	28	*30.5*	dB
Mid-Range Gain	G_{MID}	DSA 14dB attenuation.	*11.5*	14	*16.5*	dB
Minimum Gain	G_{MIN}	DSA 31.5dB attenuation.	*-1.5*	-3.5	*-6.5*	dB
Gain Variation Over Temperature	G_{TEMP}	DSA 0dB attenuation. Over T_{EP} = -40°C to +105°C, and relative to 25°C.		+1 / -1.5		dB
		DSA 14dB attenuation. Over T_{EP} = -40°C to +105°C, and relative to 25°C.		+1 / -1.4		
Gain Flatness	G_{FLAT}	Any 200MHz BW.		0.5		dB
Gain Ripple	G_{RIPPLE}	In any 20MHz range.		0.2		dB
Intra-die Channel-to-Channel Differences in Gain	G_A - G_B	Worst case difference in Gain for any 2dB step over the 0dB to 30dB attenuation range (with channels A and B both set to identical DSA attenuation levels).		0.1		dB
Reverse Isolation	G_{REV}	DSA 0dB attenuation		45		dB
		DSA 31.5dB attenuation		80		
Intra-Die Channel Isolation [b]	$ISOL_{A-B}$	Any RF input/output. DSA 0dB Attenuation	40	45		dB
Inter-Die Channel Isolation [b]	$ISOL_{B-C}$	Any RF input / output combination involving channel B (die 1) paired with channel C (die 2). DSA = 0dB.	50	55		dB
Filter Group Delay in Passband	τ	f_{RF} = 570MHz to 1100MHz		2	4	ns
Filter Group Delay Ripple	τ_{RIPPLE}	Any 280MHz band within f_{RF} = 570MHz to 1100MHz		1.5	2.5	ns

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Intra-die Channel-to-Channel Differences in Group Delay	$\tau_A - \tau_B$	Worst case difference in Group Delay for any 2dB step over the 0dB to 30dB attenuation range (with channels A and B both set to identical DSA attenuation levels).			0.02		ns
Cross Channel Group Delay in Passband vs. Channel Group Delay in Passband	$\tau_{XCHANNEL} - \tau$	f_{RF} = 570MHz to 1100MHz Worst case cross-channel leakage combinations (A to B) - B; (B to A) - A; (B to C) - C; (C to B) - B; (C to D) - D; (D to C) - C	DSA = 0dB		2		ns
			DSA = 14dB		2		
			DSA = 28dB		2		
Step Error (DNL)	$ERROR_{STEP}$	Maximum error between adjacent steps			+0.05 /-0.15		dB
Absolute Error (INL)	$ERROR_{ABS}$	Over attenuation range referenced to maximum gain state			Note [c]		dB
Phase Shift Over Any 5ºC Temperature Change Over the -40ºC to 105ºC Range	$\Phi_{\Delta Temp\ @\ 0dB}$	DSA = 0dB			0.6		deg
	$\Phi_{\Delta Temp\ @\ 14dB}$	DSA = 14dB			0.5		
	$\Phi_{\Delta Temp\ @\ 28dB}$	DSA = 28dB			0.5		
Phase Shift Between Startups	$\Phi_{ON-OFF-ON}$	Channel A or Channel B Phase Shifts. Measuring “On State” phase shifts occurring over time as the device is powered on/off via STBY mode or via PORs (power-on resets).				2	deg
	$[\Phi_A - \Phi_B]_{ON-OFF-ON}$	Channel A - Channel B Phase Shifts. Measuring “On State” phase shifts occurring over time as the device is powered on/off via STBY mode or via PORs (power-on resets).				10	
Phase Shift Between Any 2dB Step	$\Phi_{2dB\ Step}$	Worst case, any 2dB step.			+0.25 / -0.6		deg
Phase Shift Between Any 8dB Step	$\Phi_{8dB\ Step}$	Worst case, any 8dB step.			1.1		deg

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Phase Shift Relative to 0dB Attenuation State	$\Phi_{\Delta MAX}$	DSA 31.5dB attenuation			-6		deg
	$\Phi_{\Delta MID}$	DSA 14dB attenuation			-4		
Intra-die Channel-to-Channel Differences in Phase	$\Phi_A - \Phi_B$	Φ_A at 16dB - Φ_B at 16dB Worst case difference in phase with channels A and B both set to DSA = 16dB attenuation levels.			10		deg
		[Φ_A at XdB - ΦB at XdB] - [Φ_A at 16dB - Φ_B at 16dB] Worst case difference in phase between the 16dB DSA attenuation case and any other state when the DSAs are set to XdB. X = 16 ± 2N, where N is an integer ranging from 1 to 8.			2		
Noise Figure at Room (25˚C) [d]	NF_{ROOM}	T_{EP} = 25˚C	DSA = 0dB		5.5	7 [a]	dB
			DSA = 14dB		8.7		
			DSA = 28dB		20		
Noise Figure at Hot (105˚C) [d]	NF_{HOT}	T_{EP} = 105˚C	DSA = 0dB		7		dB
			DSA = 14dB		10.5		
			DSA = 28dB		22		
Noise Figure at Cold (-40˚C) [d]	NF_{COLD}	T_{EP} = -40˚C	DSA = 0dB		4.2		dB
			DSA = 14dB		7.3		
			DSA = 28dB		20		

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Output Third Order Intercept Point [d]	OIP3 0dB Attn	DSA = 0dB. T_{EP} = 105˚C. P_{OUT} = 0dBm / tone. 5MHz tone separation.	f_{RF} = 900MHz		35		dBm
	OIP3 4dB Attn	DSA = 4dB. T_{EP} = 105˚C. P_{OUT} = 0dBm / tone. 5MHz tone separation.	f_{RF} = 900MHz		35		
	OIP3 14dB Attn	DSA = 14dB. T_{EP} = 25˚C P_{OUT} = -3dBm / tone. 5MHz tone separation.	f_{RF} = 900MHz	27	33		
	OIP3 28dB Attn	DSA = 28dB. T_{EP} = -40˚C P_{OUT} = -10dBm / tone. 5MHz tone separation.	f_{RF} = 900MHz		19		
Output 1dB Compression Point [d]	OP1dB 0dB Attn	DSA = 0dB. T_{EP} = 105˚C.	f_{RF} = 900MHz		16		dBm
	OP1dB 4dB Attn	DSA = 4dB. T_{EP} = 105˚C.	f_{RF} = 900MHz		16		
	$OP1dB_{14dB\ Attn}$	DSA = 14dB. T_{EP} = 25˚C.	f_{RF} = 900MHz	12	15		
	$OP1dB_{28dB\ Attn}$	DSA = 28dB. T_{EP} = -40˚C.	f_{RF} = 900MHz		0.13		

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

[b] Signal applied to RFIN_X. Measure desired signal at RFOUT_X and compare to undesired leakage signal level at RFOUT_Y.

[c] Absolute Error = ± [0.05 + 0.05*(DSA Attenuator Setting)]

[d] Measured by terminating one differential RFIN port to 50Ω load and applying RF signal to second RFIN port.

Thermal Characteristics

Table 7. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	26.89	°C/W
Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)	$\theta_{JC\text{-}BOT}$	3.33	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 3	

Typical Operating Conditions (TOC)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- Vcc = 3.3V
- Z_S = 100Ω differential
- Z_L = 50Ω Single-ended
- f_{RF} = 450MHz
- f_{RF} = 900MHz
- T_{EP} = +25 °C
- STBY_A = STBY_B = STBY_C = STBY_D = HIGH (All channels enabled)
- P_{OUT} = 0dBm / Tone unless otherwise specified for multi-tone tests
- 5MHz Tone Spacing
- Gain setting = Maximum Gain
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

Typical Performance Characteristics

Figure 3. Gain vs DSA Setting

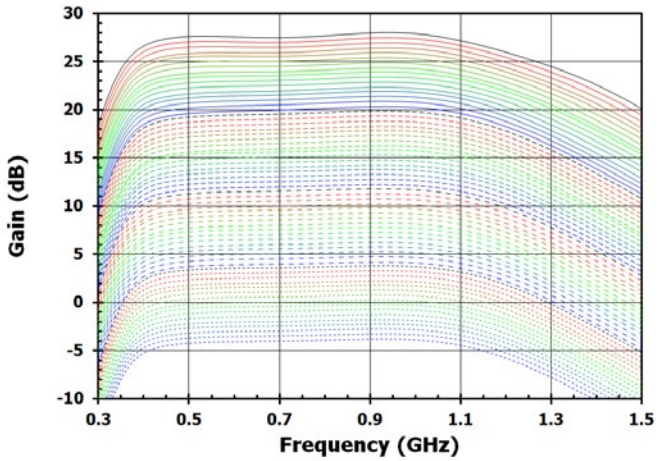


Figure 4. Gain vs Attenuation

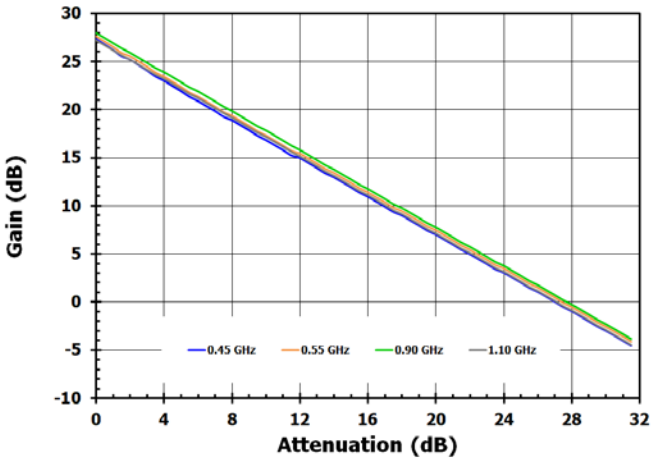


Figure 5. Gain at DSA = 0dB

Figure 6. Gain at DSA = 14dB

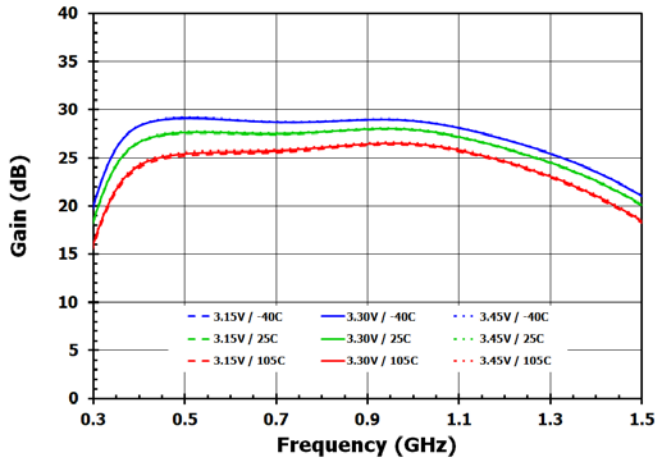


Figure 7. Gain at DSA = 31.5dB

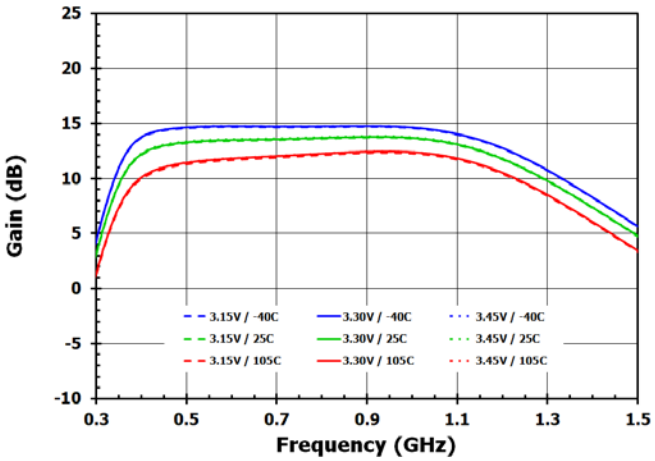
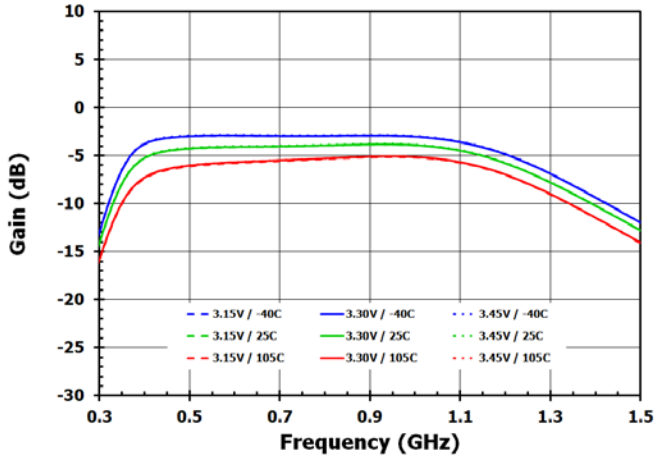


Figure 8. Gain vs Channel (DSA = 0dB)



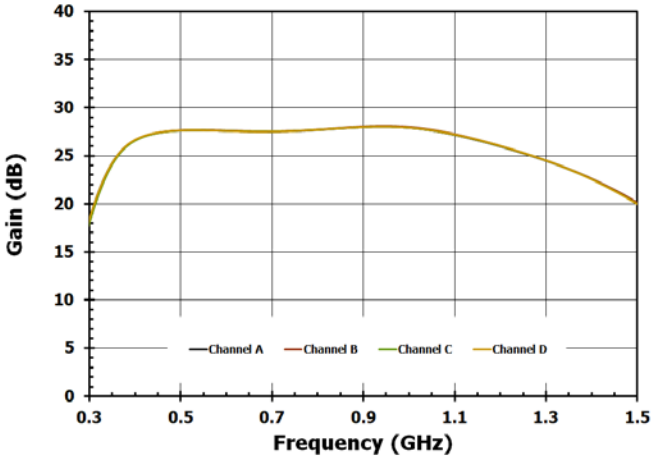


Figure 9. Reverse Isolation vs DSA Setting

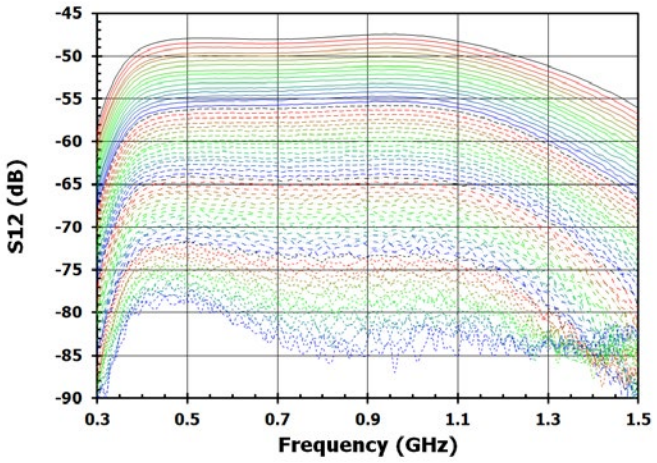


Figure 10. Reverse Isolation vs Attenuation

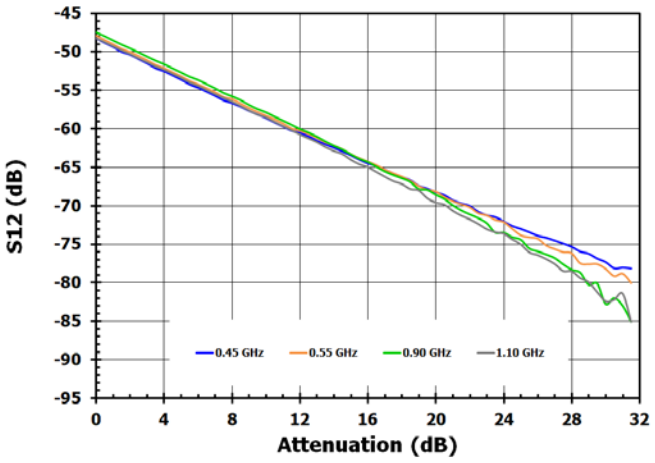


Figure 11. Reverse Isolation at DSA = 0dB

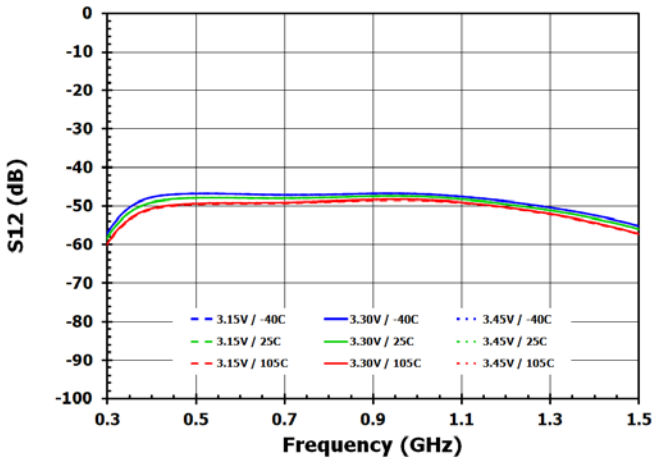


Figure 12. Reverse Isolation at DSA = 14dB

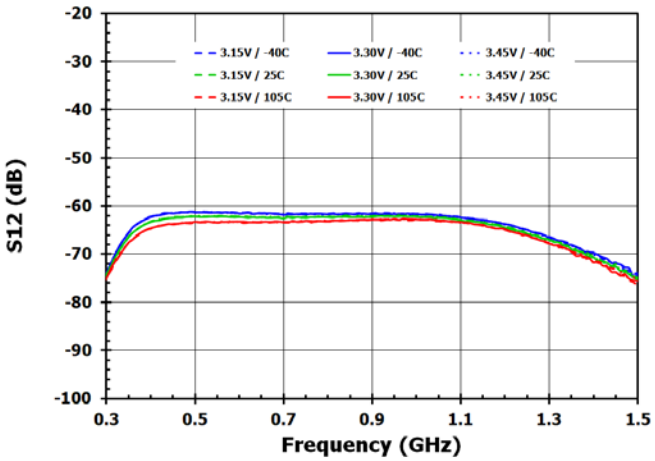


Figure 13. Reverse Isolation at DSA = 31.5dB

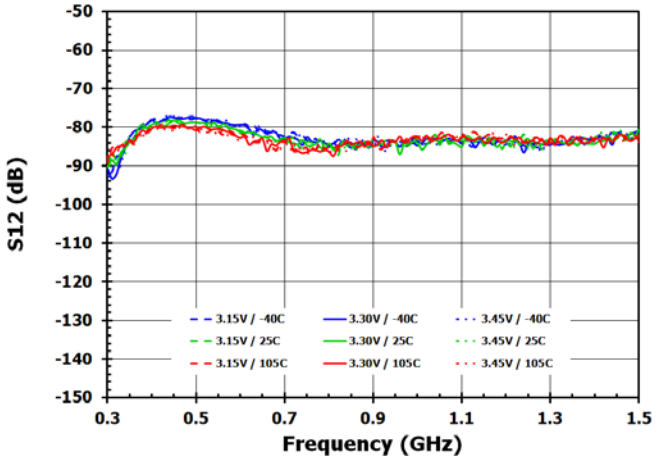


Figure 14. Reverse Isolation vs Channel (DSA = 0dB)

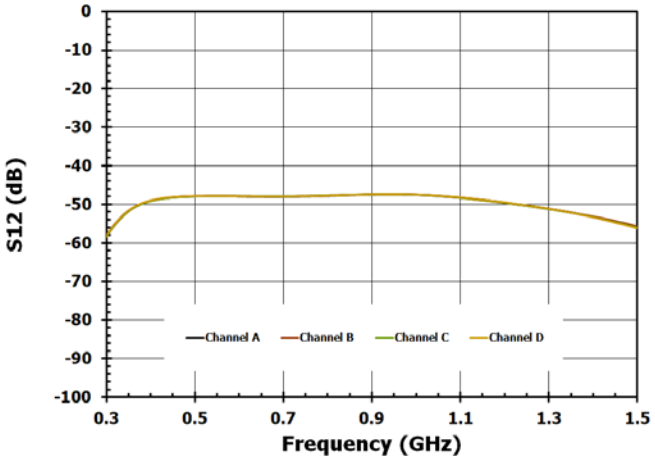


Figure 15. Input Return Loss vs DSA Setting

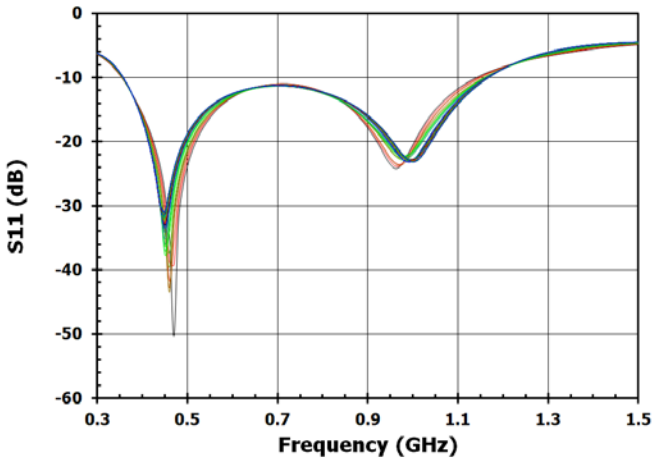


Figure 16. Input Return Loss vs Attenuation

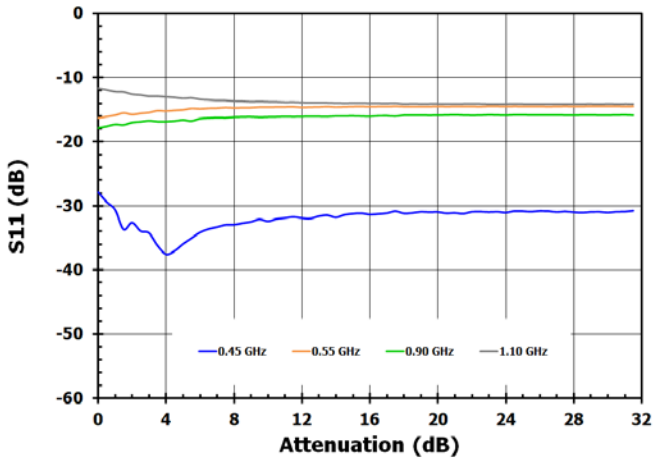


Figure 17. Input Return Loss at DSA = 0dB

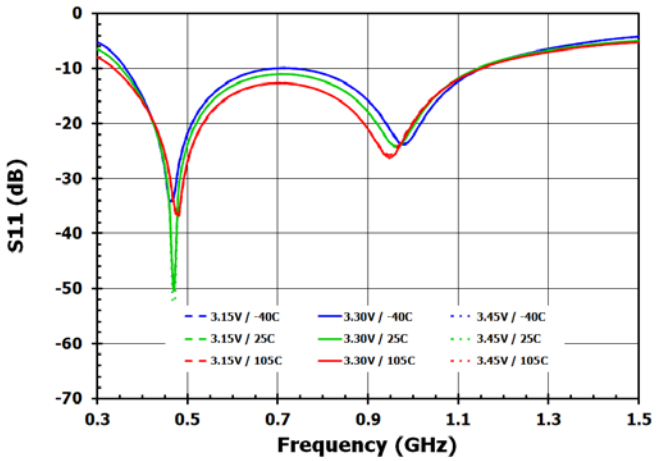


Figure 18. Input Return Loss at DSA = 14dB

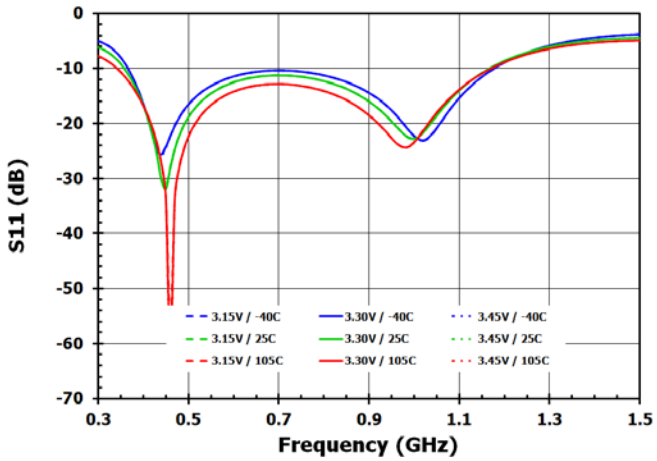


Figure 19. Input Return Loss at DSA = 31.5dB

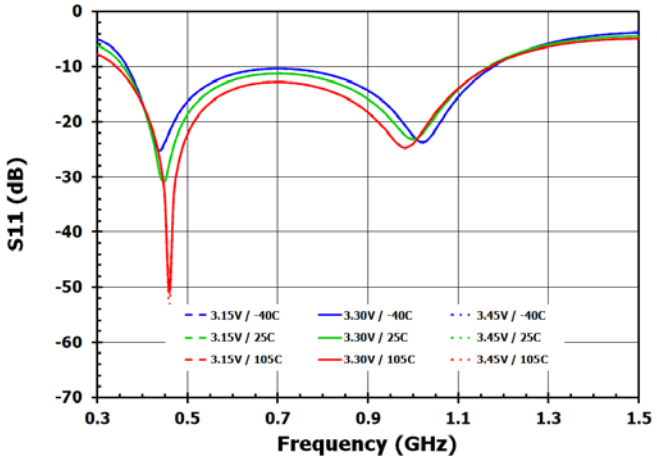


Figure 20. Input Return Loss vs Channel (DSA = 0dB)

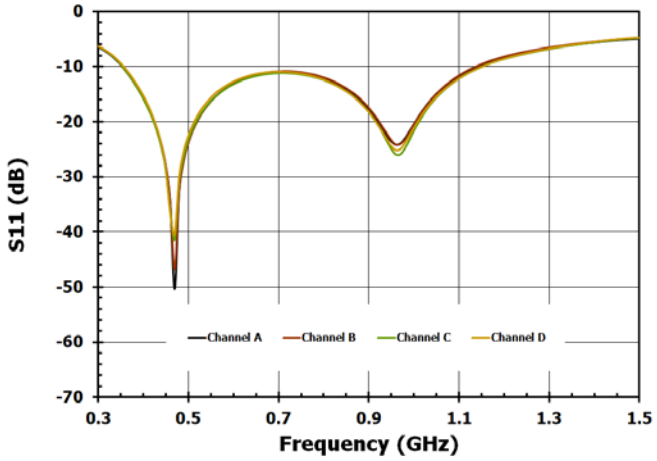


Figure 21. Output Return Loss vs DSA Setting

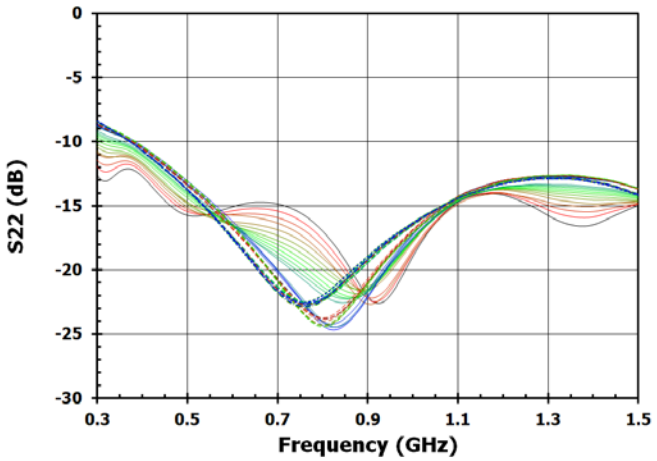


Figure 22. Output Return Loss vs Attenuation

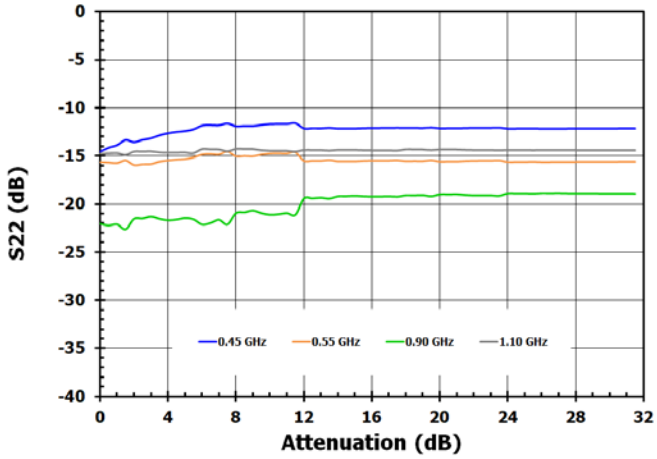


Figure 23. Output Return Loss at DSA = 0dB

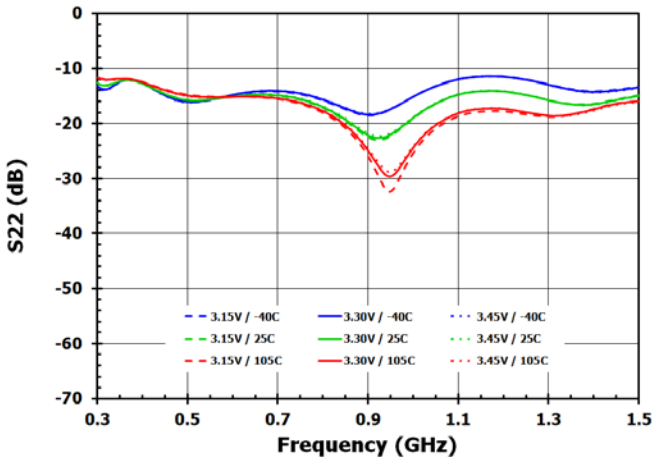


Figure 24. Output Return Loss = DSA = 14dB

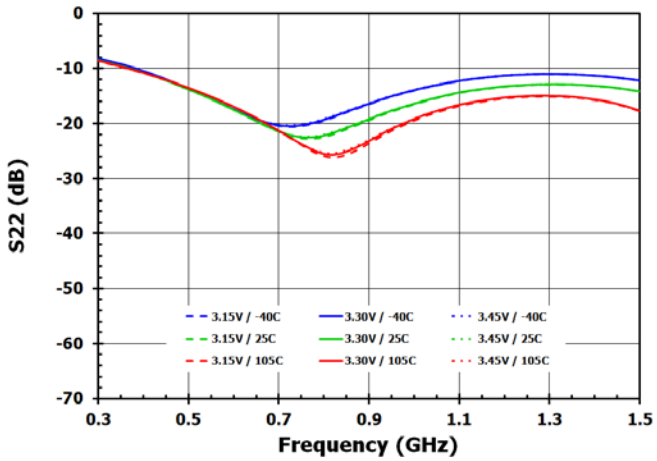


Figure 25. Output Return Loss = 31.5dB

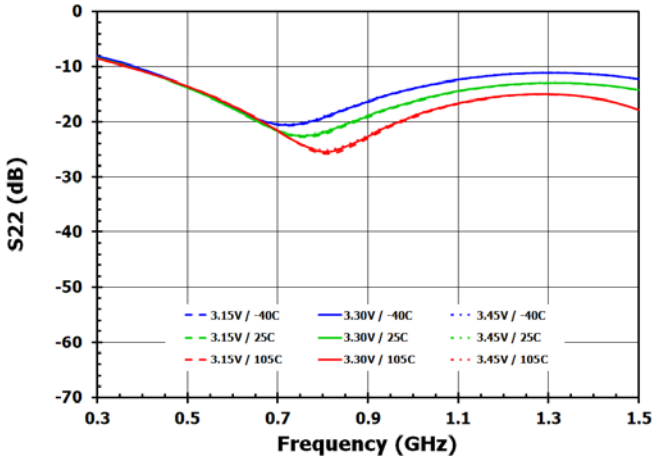


Figure 26. Output Return Loss vs Channel (DSA = 0dB)

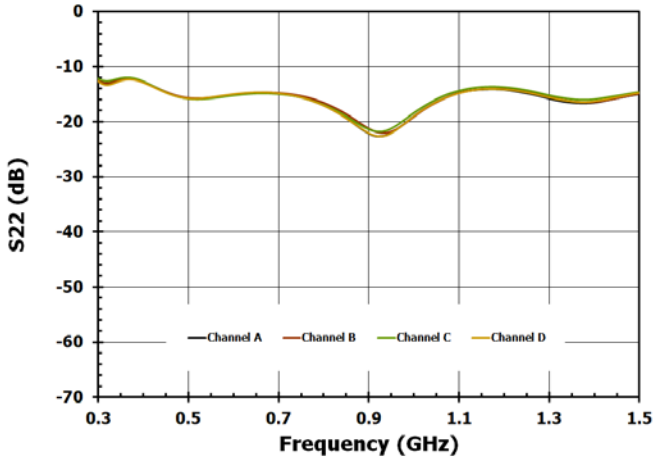


Figure 27. Out of Band Rejection (w.r.t. 450MHz, DSA = 0dB)

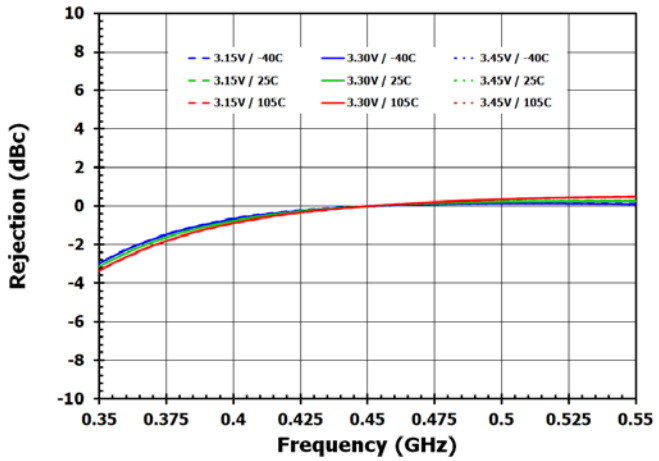


Figure 28. Out of Band Rejection vs Channel (w.r.t. 900MHz, DSA = 0dB)

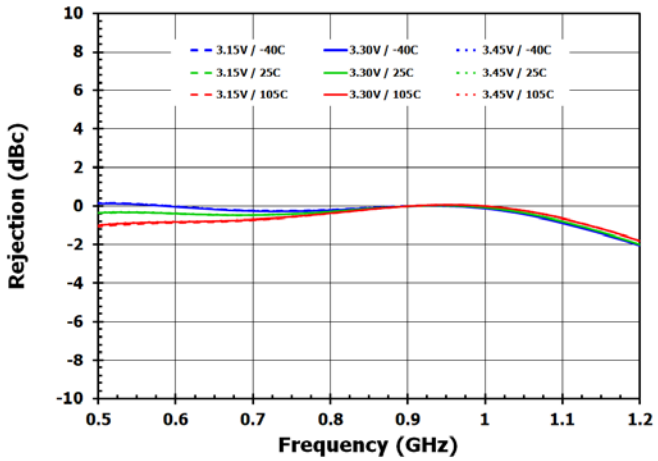


Figure 29. Out of Band Rejection (w.r.t. 900MHz, DSA = 0dB)

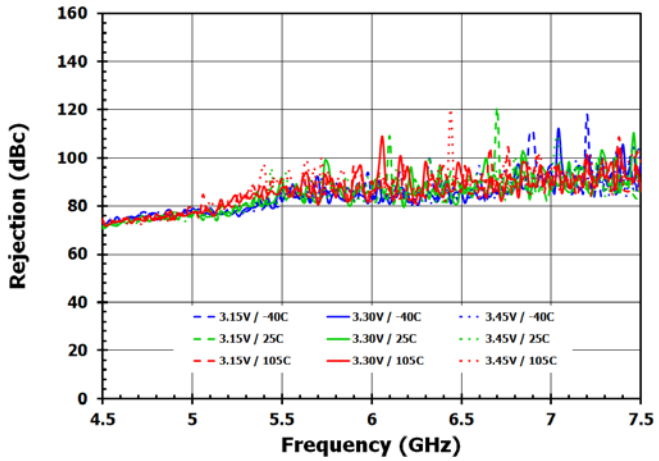


Figure 30. Out of Band Rejection vs Channel (w.r.t. 450MHz, DSA = 0dB)

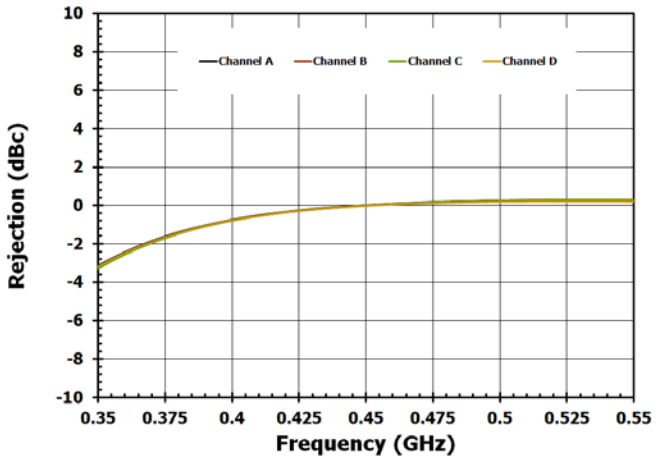


Figure 31. Out of Band Rejection (w.r.t. 900MHz, DSA = 0dB)

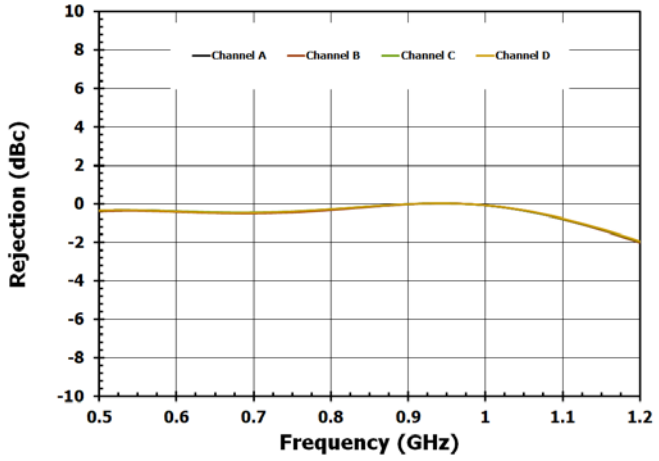


Figure 32. Out of Band Rejection vs Channel (w.r.t. 900MHz, DSA = 0dB)

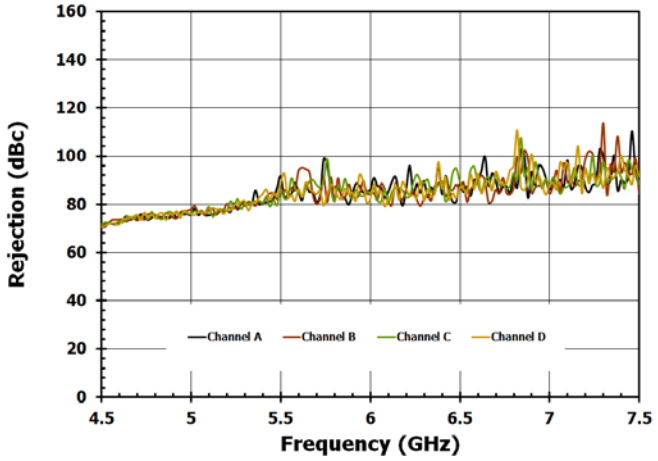


Figure 33. Absolute Error (INL)

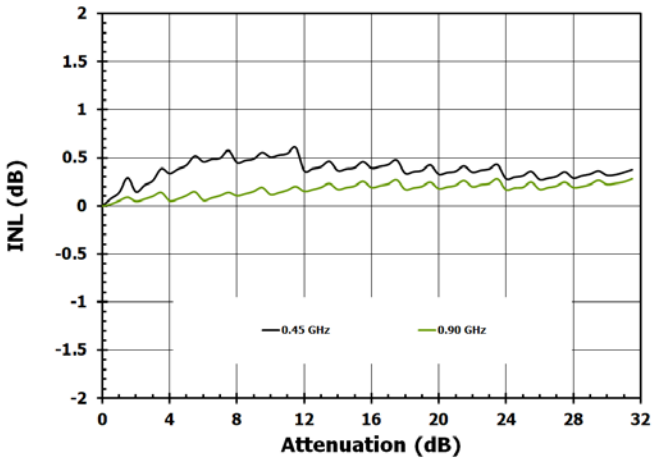


Figure 34. Absolute Error (INL) vs Channel

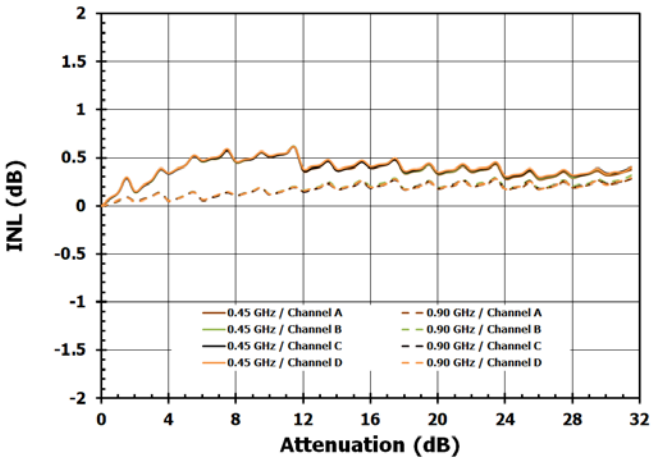


Figure 35. Step Error (DNL)

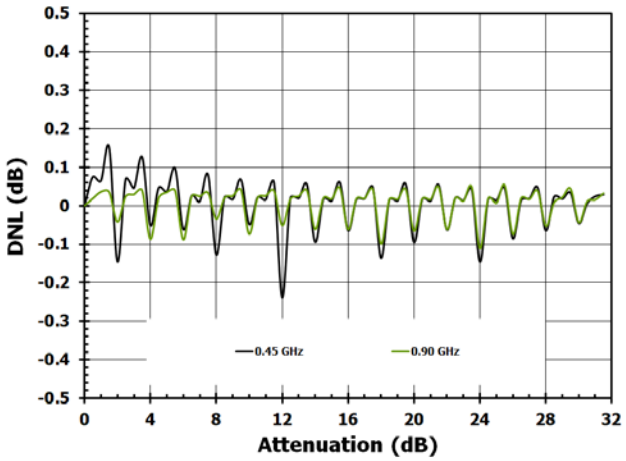


Figure 36. Step Error (DNL) vs Channel

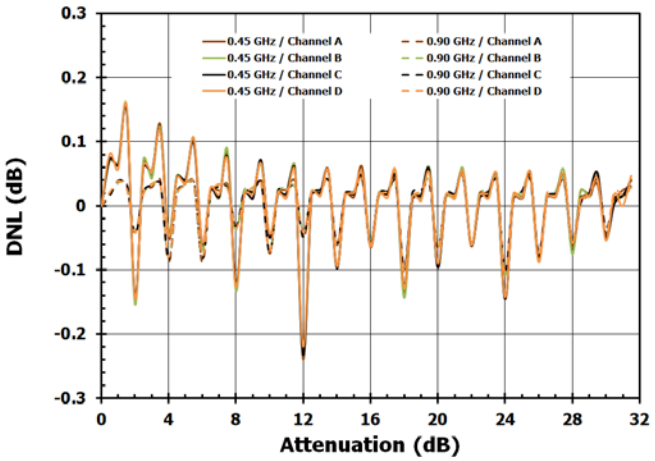


Figure 37. Common Mode Rejection

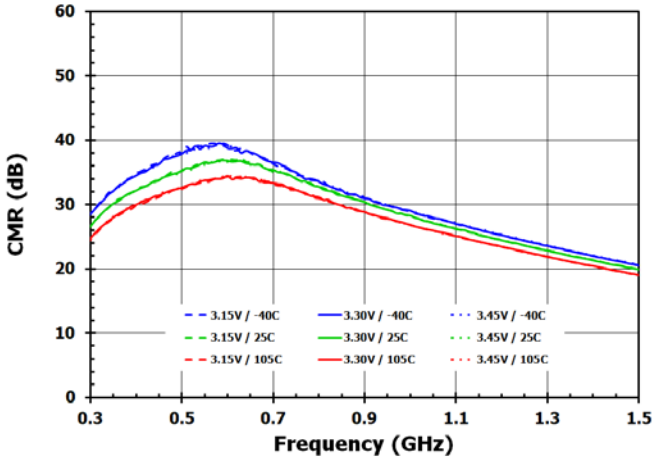


Figure 38. Common Mode Rejection vs Channel

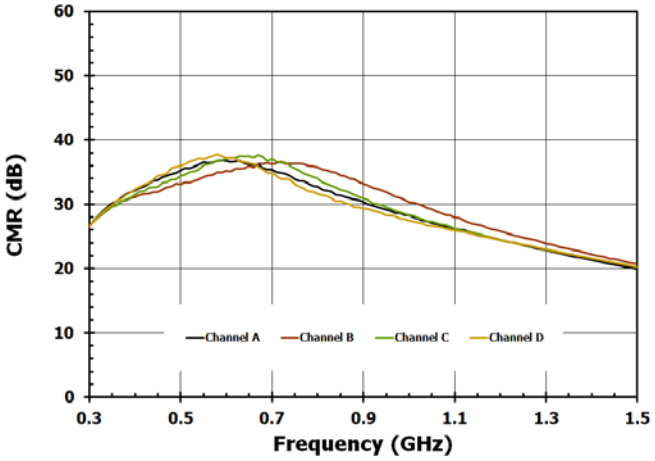


Figure 39. Amplitude Imbalance

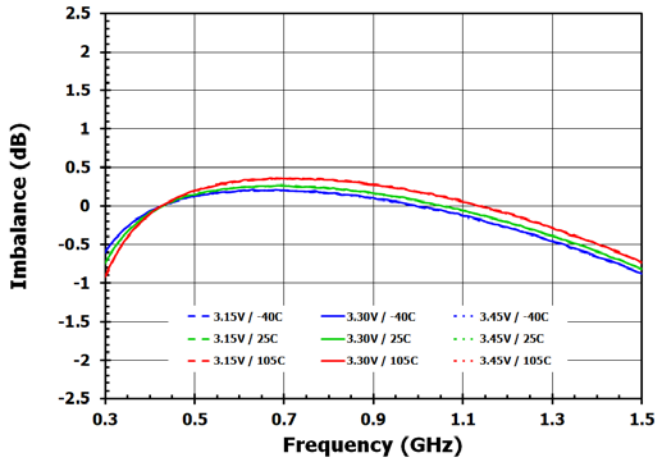


Figure 40. Amplitude Imbalance vs Channel

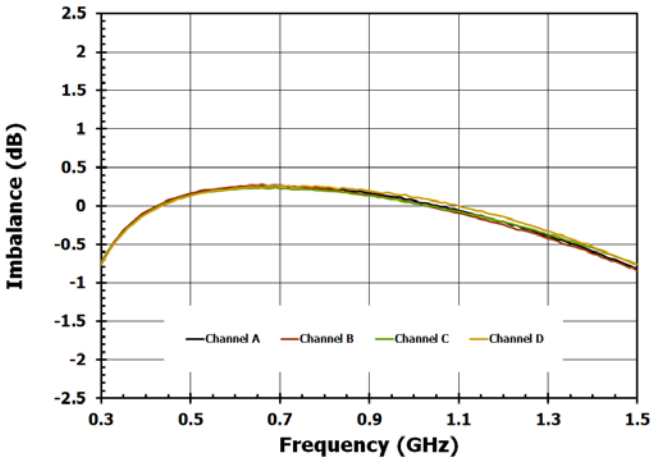


Figure 41. Phase Imbalance

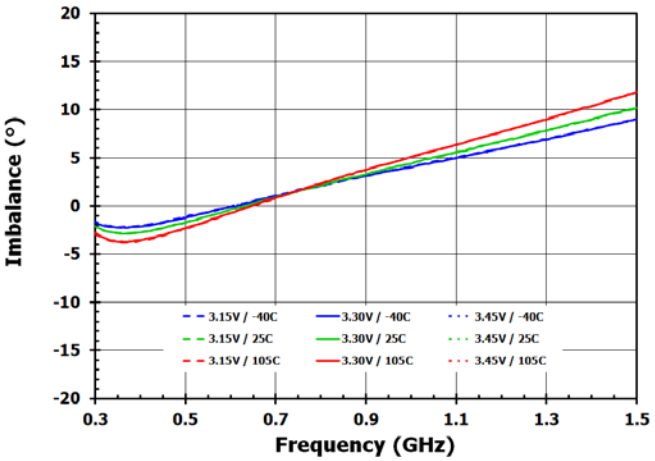


Figure 42. Phase Imbalance vs Channel

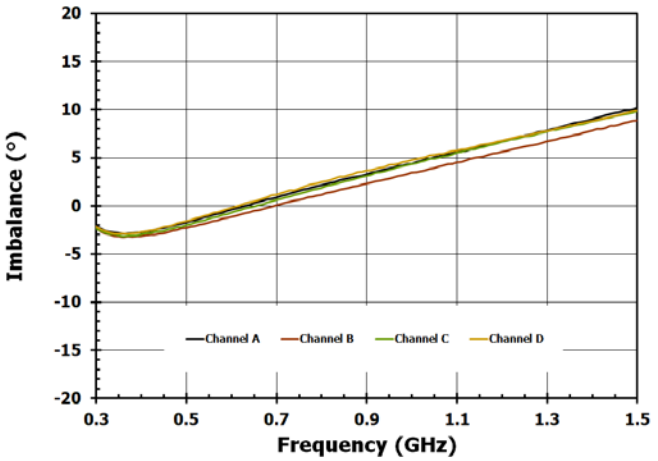


Figure 43. Phase Shift Relative to DSA = 0dB

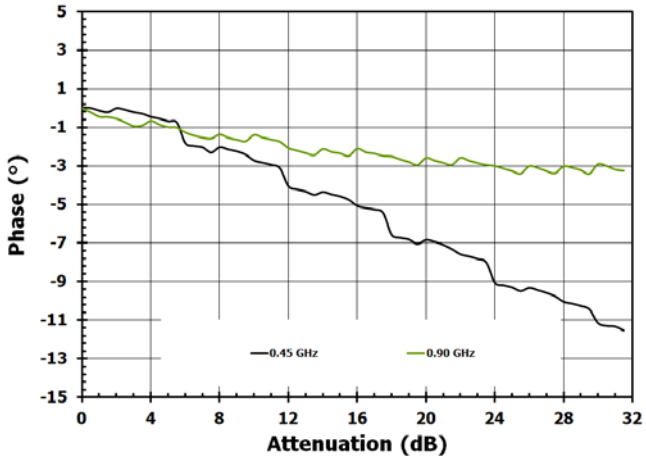


Figure 44. Phase Shift Relative to DSA = 0dB vs Channel

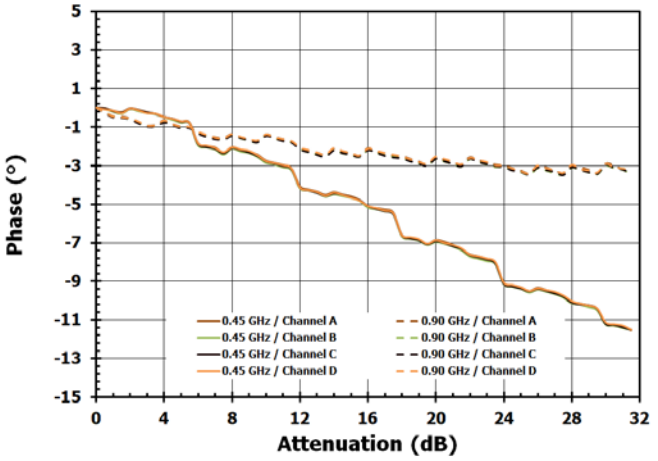


Figure 45. Group Delay at DSA = 0dB

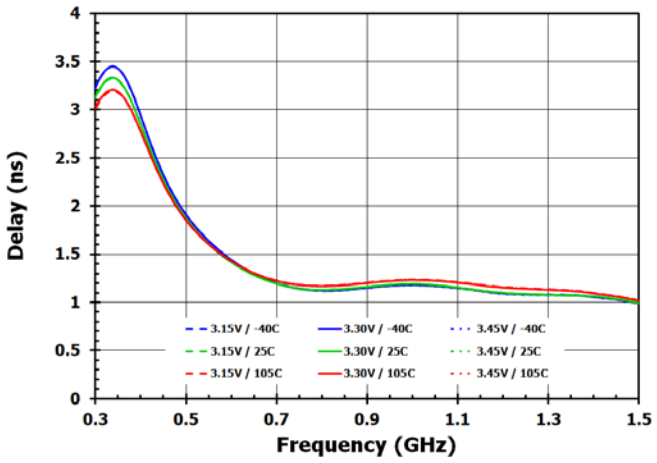


Figure 46. Group Delay vs Channel (DSA = 0dB)

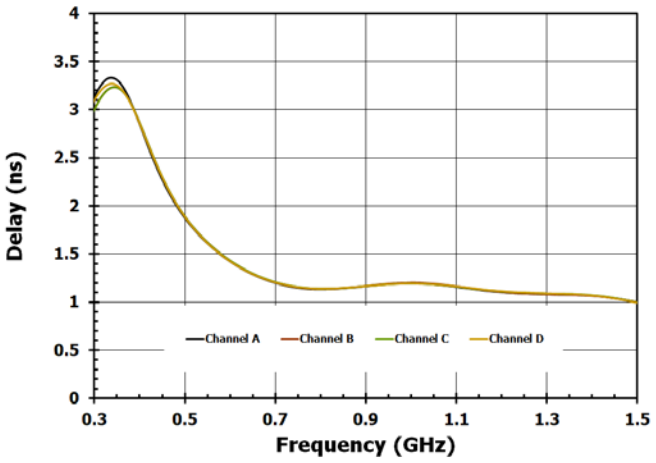


Figure 47. K Factor

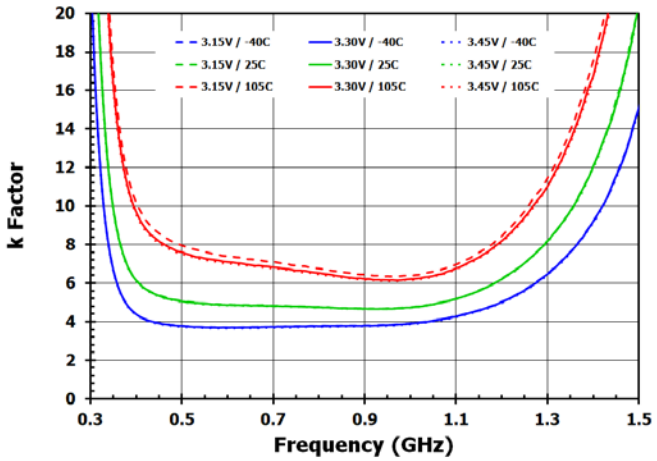


Figure 48. Inter/Intra Channel Isolation at DSA = 0dB

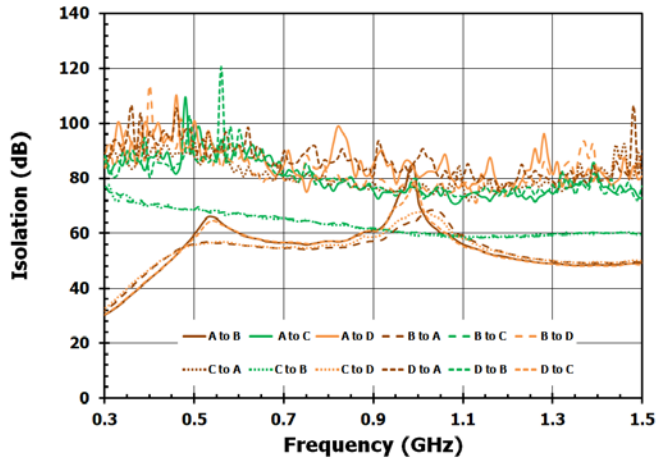


Figure 49. Supply Current

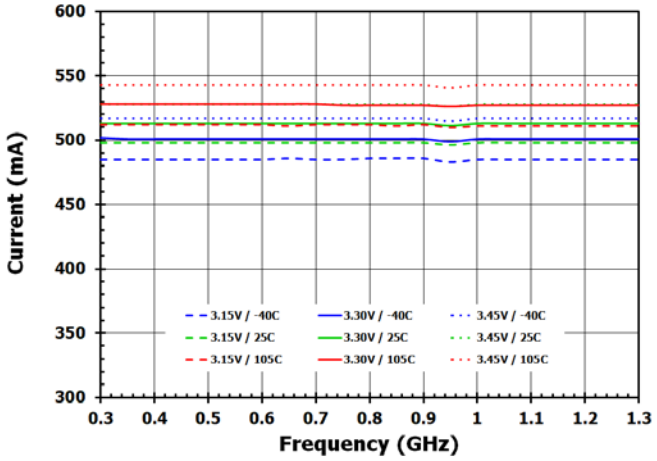


Figure 50. Noise Figure at DSA = 0dB

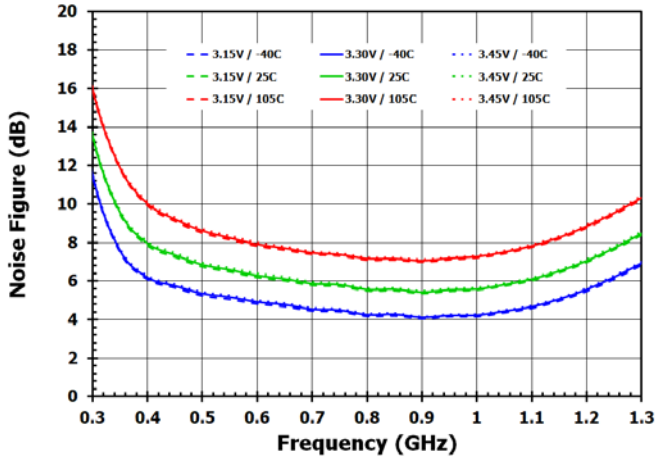


Figure 51. Noise Figure at DSA = 14dB

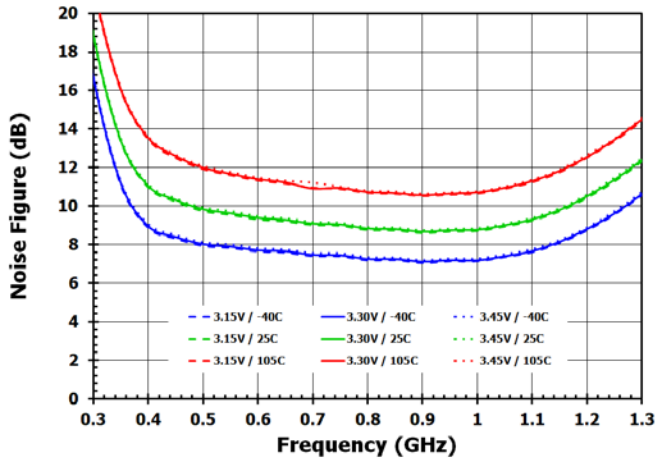


Figure 52. Noise Figure at DSA = 28dB

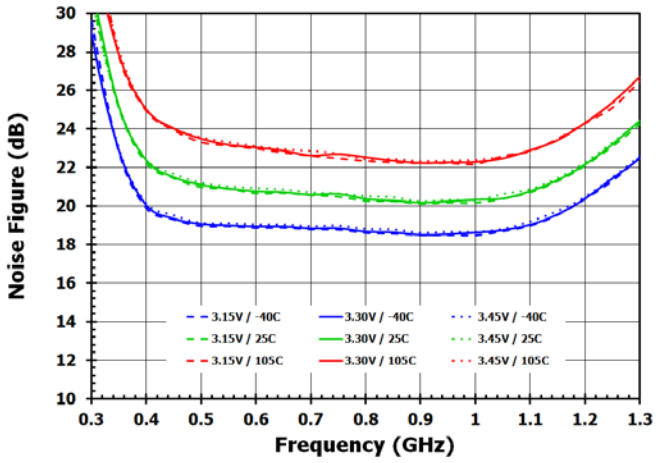


Figure 53. Noise Figure vs Channel (DSA = 0dB)

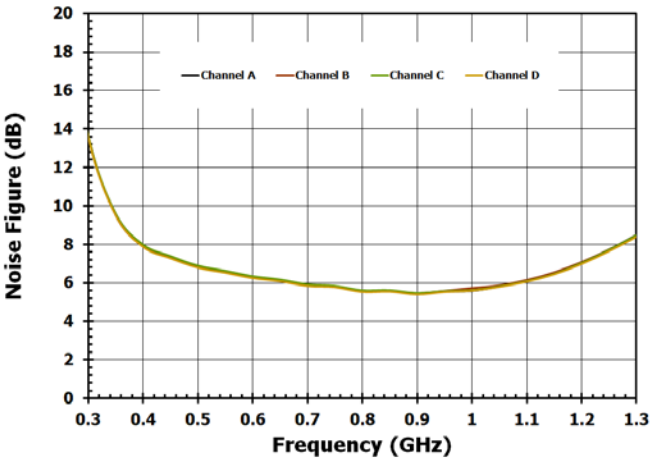


Figure 54. OIP3 at DSA = 0dB

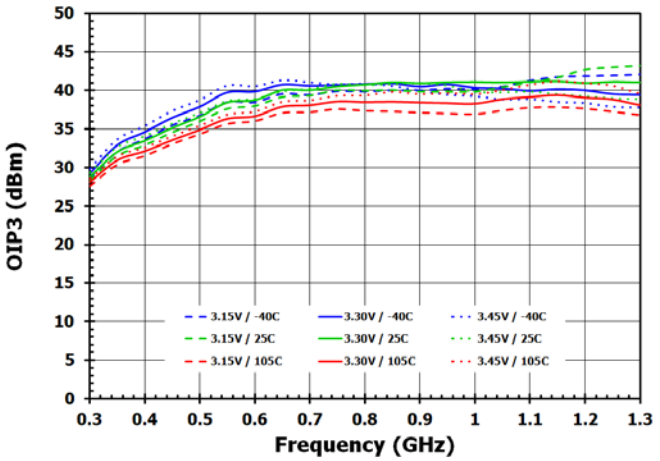


Figure 55. OIP3 at DSA = 4dB

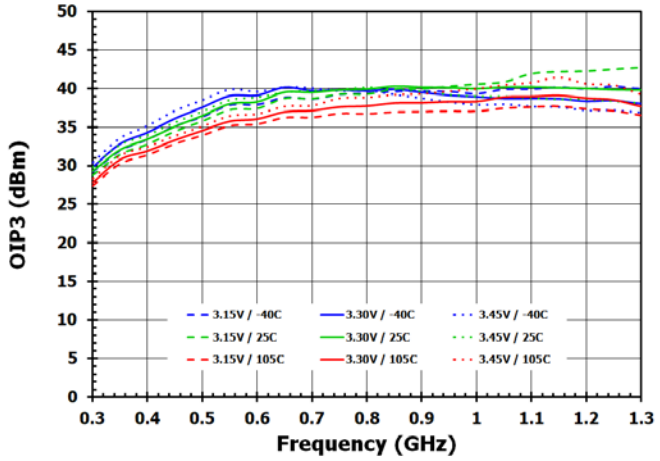


Figure 56. OIP3 at DSA = 14dB

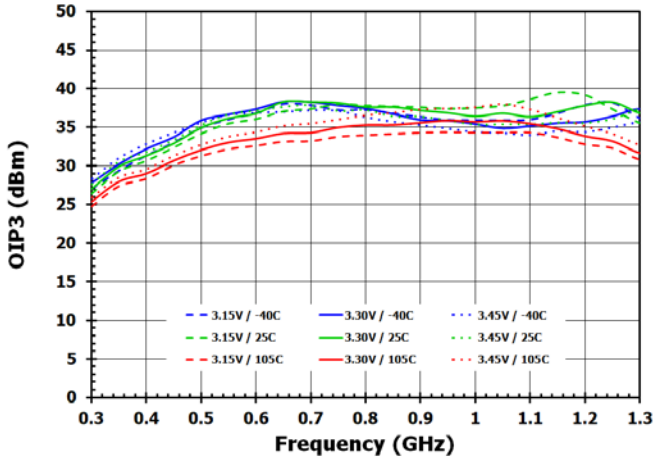


Figure 57. OIP3 at DSA = 28dB

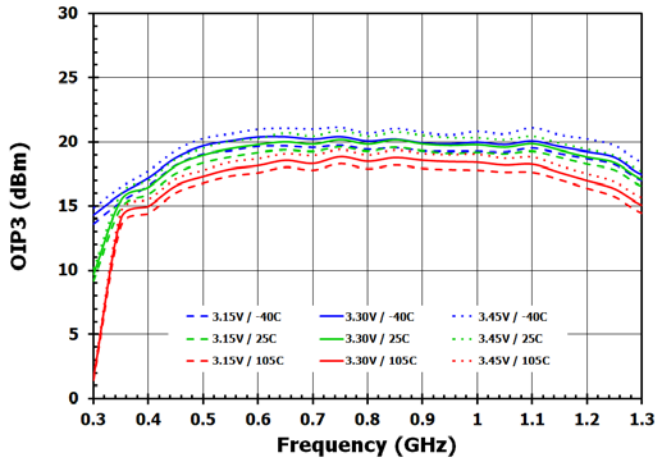


Figure 58. OIP3 vs Channel (DSA = 0dB)

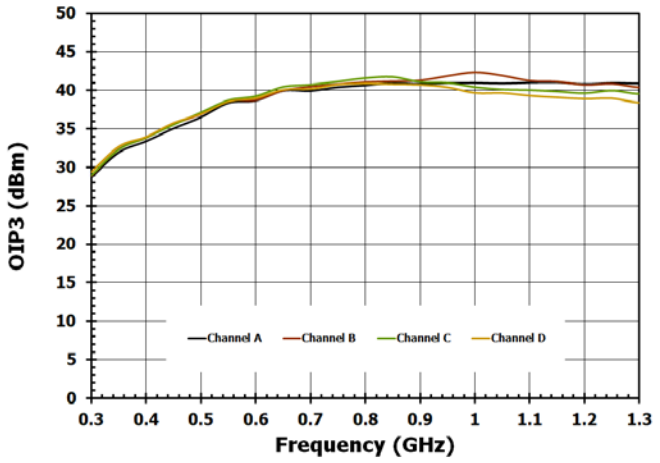


Figure 59. OP1dB at DSA = 0dB

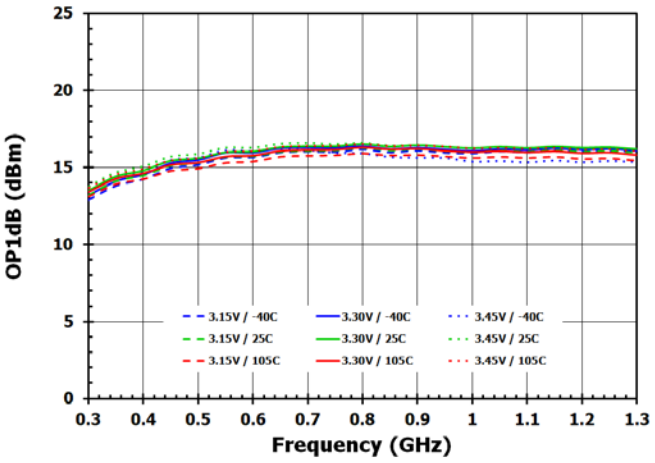


Figure 60. OP1dB at DSA = 4dB

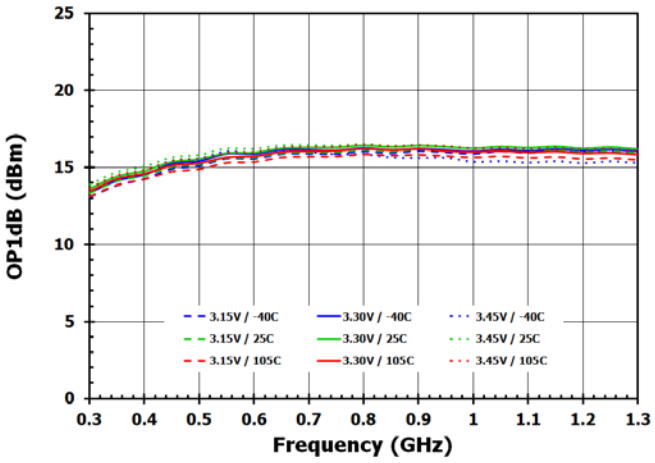


Figure 61. OP1dB at DSA = 14dB

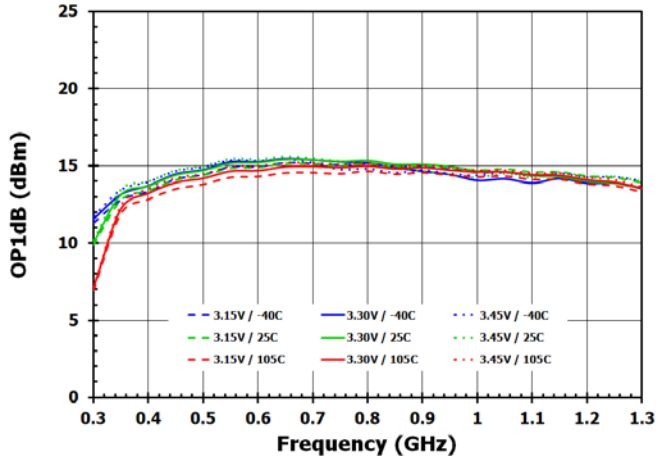


Figure 62. OP1dB at DSA = 28dB

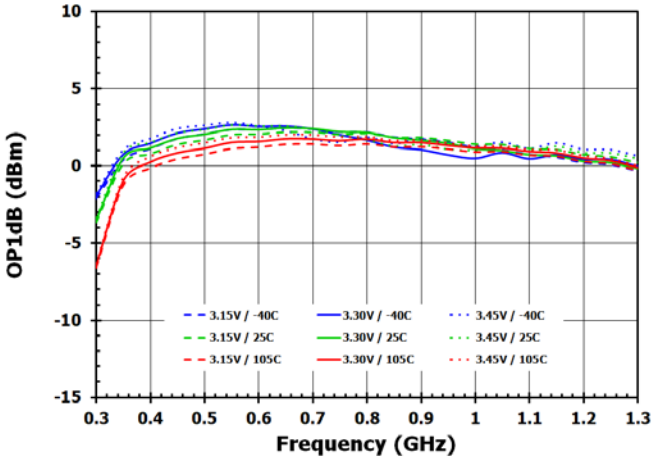
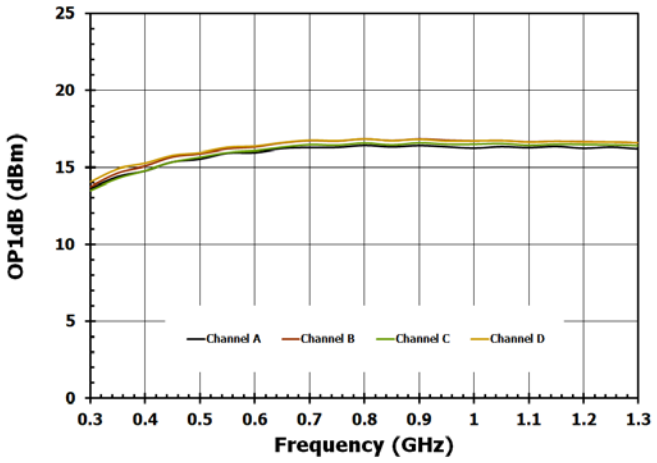


Figure 63. OP1dB vs Channel (DSA = 0dB)



Programming

The F4481 employs a variety of programming options which can be used to control the on-chip attenuators and band-select functions. The following sections provide specific details on each unique programming mode.

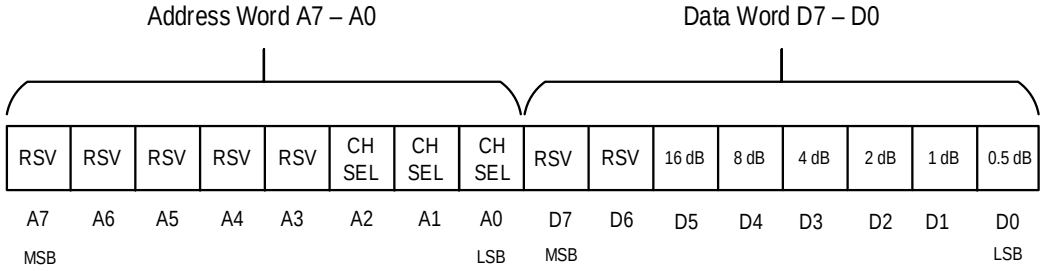
Serial Programming

The F4481 includes a SPI interface which is primarily used to program the device's on-chip attenuators.

Device Register Maps

Each channel of the VGA uses an 8-bit addressing word followed by an 8-bit data word to execute the attenuation level commands. Figure 64 shows the various bit assignments for each channel register.

Figure 64. Register Bit Map for Each Channel



The register address word (Bits A7-A0) includes five reserve bits (A7-A3) followed by three channel addressing bits (A2-A0). The channel select truth table is provided in Table 8.

Table 8. Channel Select Truth Table

Channel Select	Reserve					Address Bits		
	A7	A6	A5	A4	A3	A2	A1	A0
Channel A	X	X	X	X	X	0	0	0
Channel B	X	X	X	X	X	0	0	1
Channel C	X	X	X	X	X	0	1	0
Channel D	X	X	X	X	X	0	1	1
Channel A and B (Simultaneous Programming)	X	X	X	X	X	1	0	X
Channel C and D (Simultaneous Programming)	X	X	X	X	X	1	1	X

Note that address bit A2 is used to select either individual channel programming (logic LOW) or dual channel programming (logic HIGH). Simultaneous programming of channels A and B is achieved when setting bit A2 to a logic HIGH and A1 a logic LOW. Simultaneous programming of channels C and D occurs when bits A2 and A1 are both logic HIGHs.

Table 9 represents the truth table for the attenuator control bits. A full scale DSA setting of 000000 drives the channel DSA into its *minimum* attenuation state. Conversely, a setting of 111111 drives the channel DSA into its *maximum* attenuation state. Note that D5 is defined as the Most Significant Bit (MSB) for the attenuator control function within each respective channel.

Table 9. DVGA Attenuation Word Truth Table

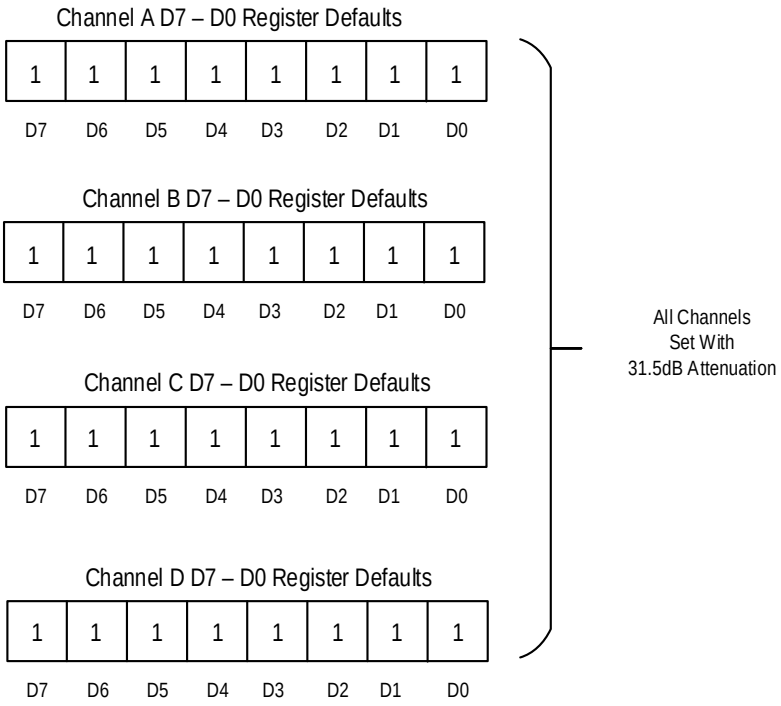
Attenuation Setting	Reserve		Control Bits					
	D7	D6	D5	D4	D3	D2	D1	D0
0.0 dB	X	X	0	0	0	0	0	0
0.5 dB	X	X	0	0	0	0	0	1
1.0 dB	X	X	0	0	0	0	1	0
2.0 dB	X	X	0	0	0	1	0	0
4.0 dB	X	X	0	0	1	0	0	0
8.0 dB	X	X	0	1	0	0	0	0
16.0 dB	X	X	1	0	0	0	0	0
31.5 dB	X	X	1	1	1	1	1	1

It should also be noted that the listing above represents an *abbreviated* version of the complete 6-bit attenuator control truth table. Any attenuator combination of 0.5dB, 1dB, 2dB, 4dB, 8dB, and 16dB can be achieved by simply assigning a logic HIGH in the respective control bit. For instance, to achieve an attenuation setting of 21.5dB within a given channel, assign a logic HIGH to bits D0, D1, D3, and D5 while assigning a logic LOW to bits D2 and D4. Doing so selects a combination of 0.5dB (D0) + 1dB (D1) + 4dB (D3) + 16dB (D5) = 21.5dB. Setting all of the control bits to logic HIGH will step in *all* of the attenuator stages.

Serial Mode Default Condition

When the device is ***first powered on,*** each channel's DSA will default to its *Maximum Attenuation* setting as shown below in Figure 65. These settings apply to a hard reset when first applying V_{CC}.

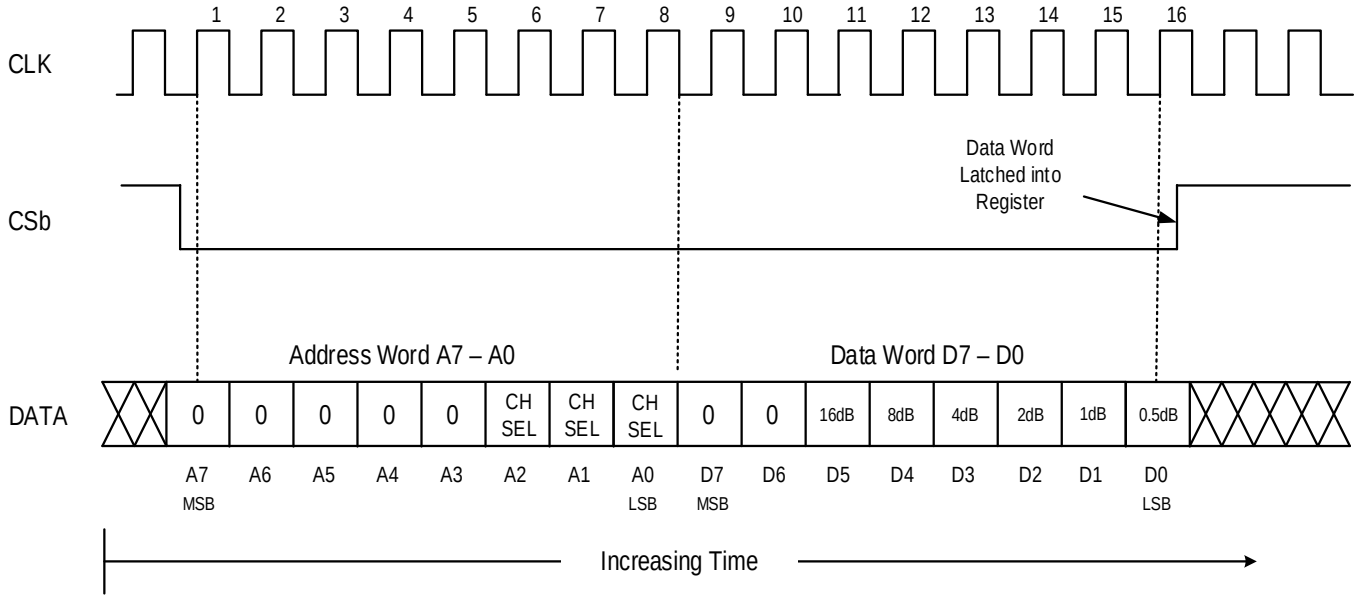
Figure 65. Serial Mode Default Condition upon Initial Power-Up



Timing Associated with Programming the Serial Registers

To program each channel, the Address Word and Data Word must be clocked in sequentially with the Most Significant Bit (MSB) first (for details, see Figure 66).

Figure 66. Timing Diagram Associated with Programming the Serial Register



SPI Timing Intervals

Figure 67 shows the relevant SPI timing intervals that are specified in Table 10.

Note – The F4481 includes a CLK inhibit feature designed to minimize sensitivity to CLK bus noise when the device is not being programmed. When CSb is high (> V_{IH}), the CLK input is disabled and serial data (DATA) is not clocked into the shift register. It is recommended that CSb be pulled high (>V_{IH}) when the device is not being programmed.

Figure 67. Serial Register Timing Diagram

(Note the Timing Spec Intervals in Blue):

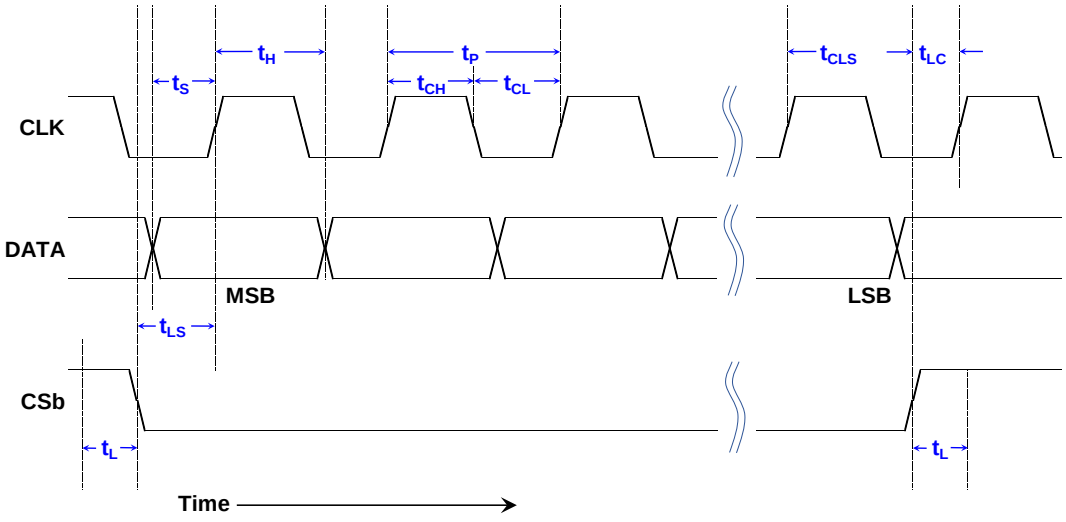


Table 10. SPI Timing Diagram Values for the Serial Mode

Parameter	Symbol	Test Condition	Minimum	Typical	Maximum	Units
CLK Frequency	f_C				50	MHz
CLK High Duration Time	t_{CH}		20			ns
CLK Low Duration Time	t_{CL}		20			ns
DATA to CLK Setup Time	t_S		10			ns
CLK Period [a]	t_P		40			ns
CLK to DATA Hold Time	t_H		10			ns
Final CLK Rising Edge to CSb Rising Edge	t_{CLS}		10			ns
CSb to CLK Setup Time	t_{LS}		10			ns
CSb Trigger Pulse Width	t_L		10			ns
CSb Trigger to CLK Setup Time [b]	t_{LC}		10			ns

[a] $(T_{CH} + T_{CL}) \geq 1/F_C$

[b] Once all desired DATA is clocked in, t_{LC} represents the time a CSb high needs to occur before any subsequent CLK signals.

Standby Mode Programming

Each channel of the F4481 can be placed into a standby mode via the dedicated Channel STBY pins (STBY_A, STBY_B, STBY_C, STBY_D); for details, see the truth table shown in Table 11. Note that when a channel is disabled, the serial register for that channel will hold the last enabled DSA state.

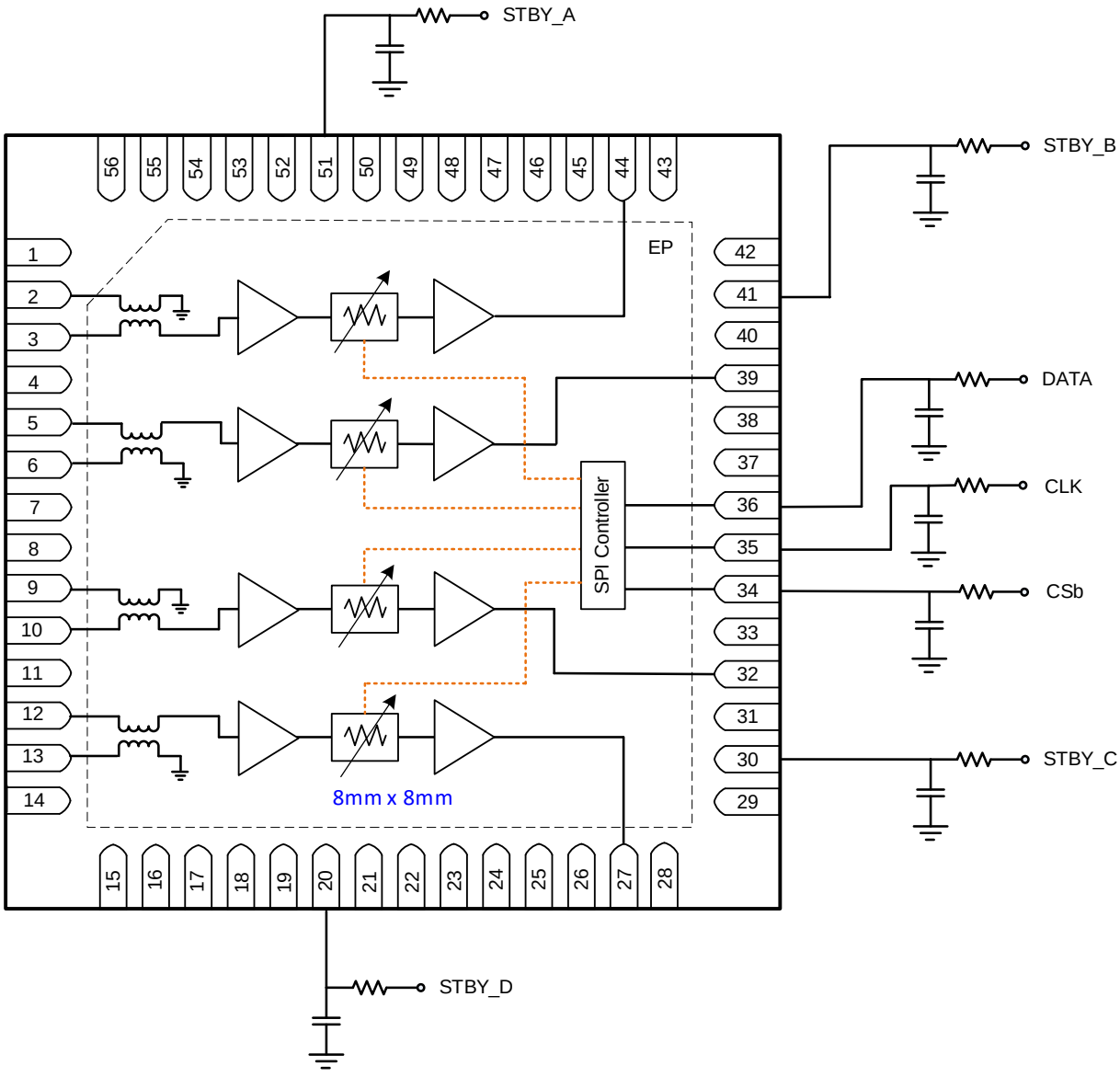
Table 11. STBY Logic Truth Table

Channel	STBY_X Pin Logic	Channel Power State
A	0	Channel A Standby (SPI still active)
	1	Channel A Power On
B	0	Channel B Standby (SPI still active)
	1	Channel B Power On
C	0	Channel C Standby (SPI still active)
	1	Channel C Power On
D	0	Channel D Standby (SPI still active)
	1	Channel D Power On

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to all control pins. Note the recommended resistor and capacitor values do not necessarily match the EV kit BOM for the case of poor control signal integrity.

Figure 68. Control Pin Interface for Signal Integrity



Evaluation Kit Images

Figure 69. Evaluation Kit Top View

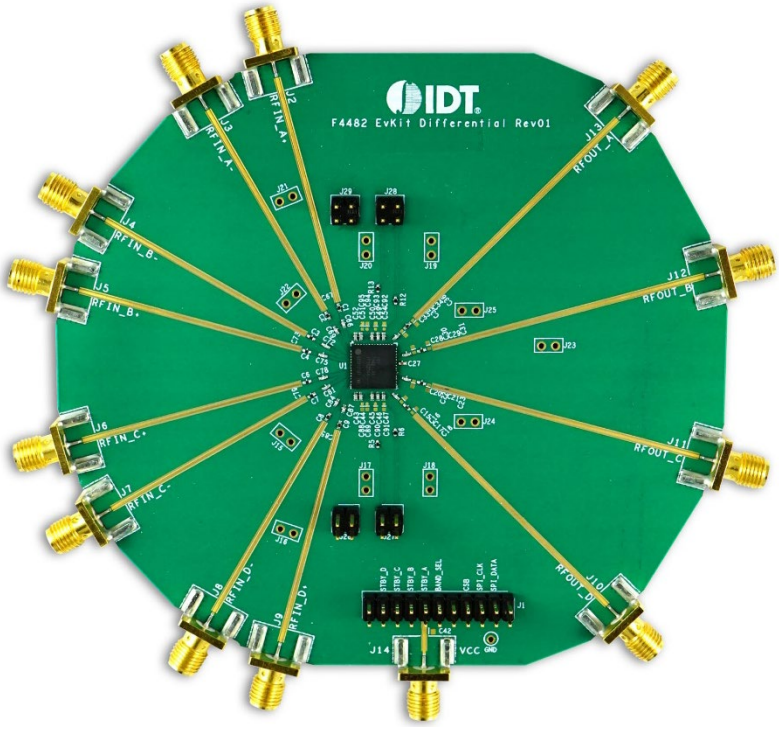
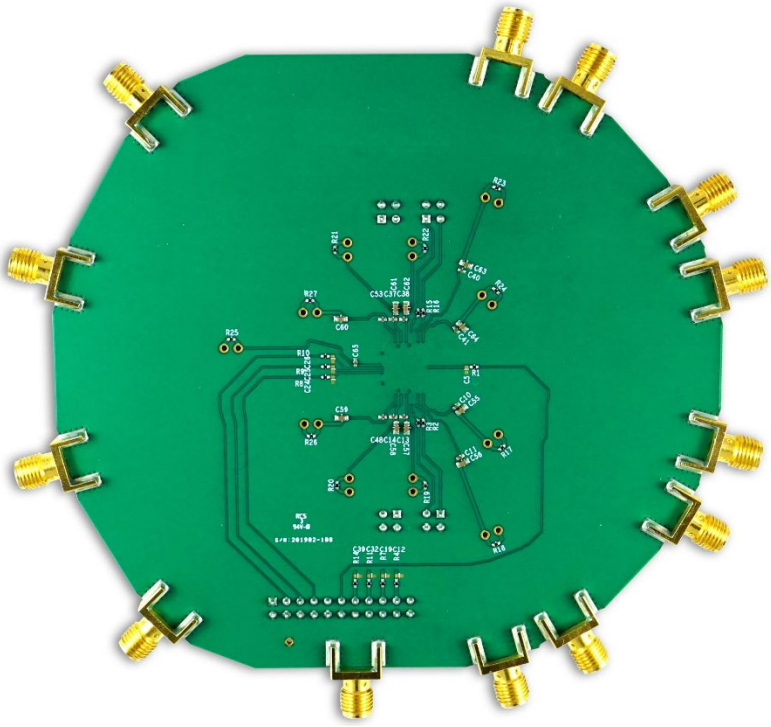


Figure 70. Evaluation Kit Bottom View



Evaluation Kit / Applications Circuit

Figure 71. Applications Circuit

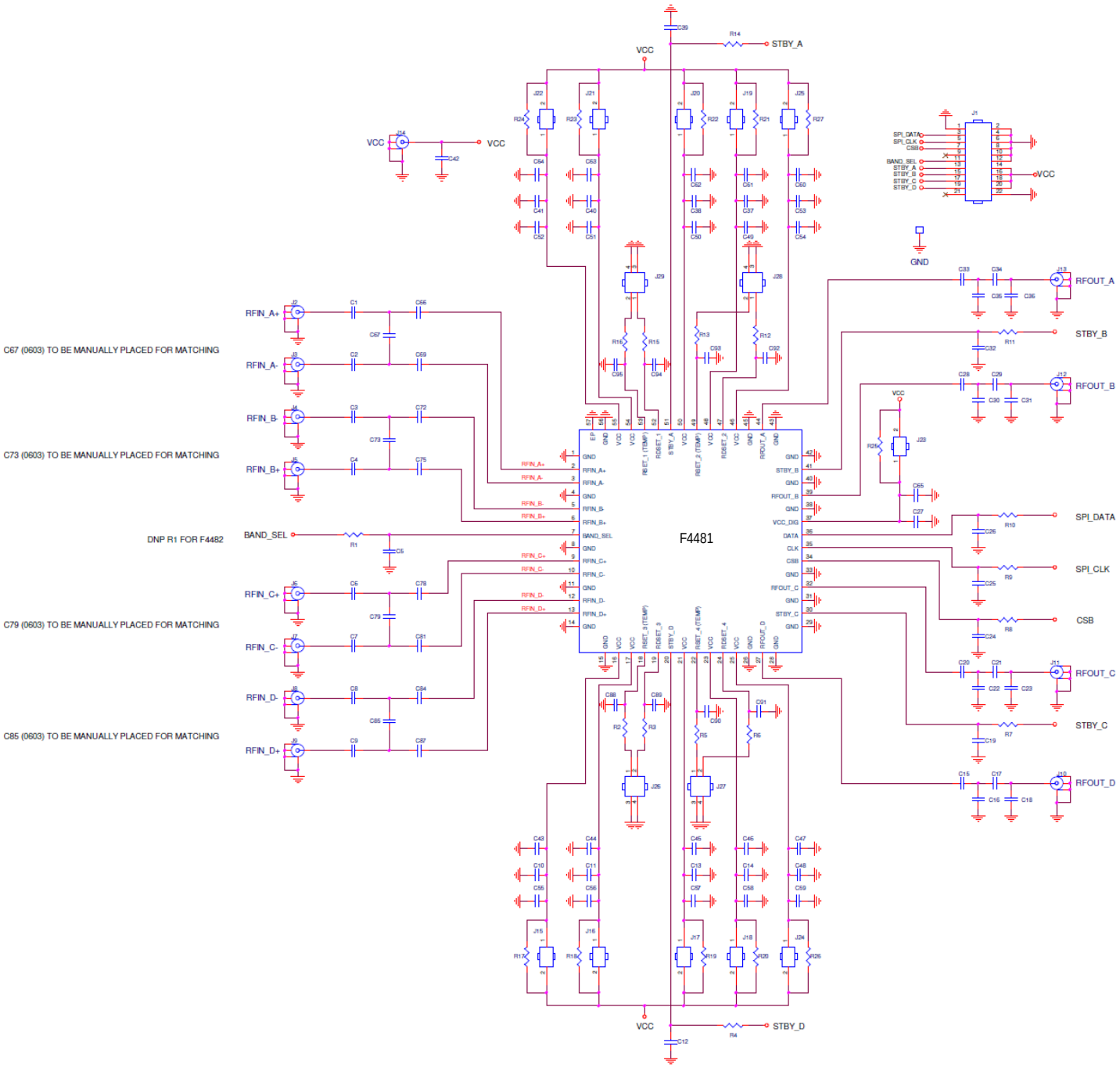


Table 12. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C10, C11, C13, C14, C27, C37, C38, C40, C41, C48, C53	11	10nF ±5%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H103J	Murata
C15, C20, C28, C33, C66, C69, C72, C75, C78, C81, C84, C87	12	100pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H101J	Murata
C43-C47, C49-C52, C54	10	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C65	1	100nF ±10%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H104K	Murata
C55-C59, C60-C64	10	10uF ±20%, 16V, X6S Ceramic Capacitor (0603)	GRM188C81C106M	Murata
R1, R4, R7-11, R14	8	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
R2, R16	2	2.0kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2001X	Panasonic
R3, R15	2	3.57kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3571X	Panasonic
R5, R13	2	2.0kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2001X	Panasonic
R6, R12	2	2.67kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2671X	Panasonic
R17-R27, C1-C4, C6-C9, C17, C21, C29, C34	23	0Ω Resistors (0402)	ERJ-2GE0R00X	Panasonic
J1	1	CONN HEADER VERT DBL 11 X 2 POS GOLD	67997-122HLF	Amphenol FCI
J2-J14	13	Edge Launch SMA (0.375 inch pitch ground, tab)	142-0701-851	Emerson Johnson
J26, J27, J28, J29	4	CONN HEADER VERT DBL 2 X 2 POS GOLD	90131-0762	Molex
U1	1	Quad Path TX DVGA 700MHz - 1100MHz	F4481	Renesas
		Printed Circuit Board	F4482 EVKIT DF REV01	Renesas
		Bill Of Material (Rev 01)		Renesas

Evaluation Kit Operation

Power Supplies

A common V_{CC} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µs. In addition, all control pins should remain at 0V (±0.3V) or floating while the supply voltage ramps or while it returns to zero.

Power Supply Setup

1. Connect pin 2 to pin 4, and pin 1 to pin 3 of J26-29. This ensures operation of the Distortion and Bias resistors.
2. Set up a power supply in the voltage range of 3.15V to 3.45V with the power supply output disabled. The voltage can be applied directly to the J14 SMA.

Power-On Procedure

Set up the voltage supplies and Evaluation Board as described in the “Power Supply Setup” and enable the V_{CC} supply.

Power-Off Procedure

1. Disable the RF input signal on all channels.
2. Disable the V_{CC} supply.

Application Information

The F4481 is optimized for use in high-performance RF applications ranging from 400MHz to 1100MHz.

Startup Condition

Upon device power-up, all channels will default to the standby mode ON. For logic levels, see Table 11.

Default Channel Power On

The default attenuation state will be 31.5dB attenuation upon powering ON each channel (i.e., standby mode OFF). For default levels, see Table 11.

Chip Select (CSb)

When CSb is set to logic high, the CLK input is disabled. When CSb is set to logic low, the CLK input is enabled and the DATA word can be programmed into the shift registers. The programmed word is then latched into the F4481 on the CSb rising edge (see Figure 67).

Standby Mode (STBY)

The F4481 has a power-down feature for power savings. The SPI bus is used to operate each channel in Standby On/Off mode (see Table 11).

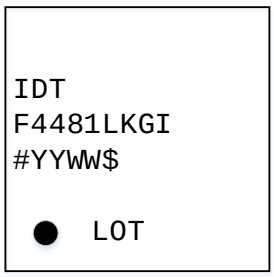
Package Outline Drawings

The package outline drawings are appended at the end of this document.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F4481LKGI	8.0 × 8.0 × 0.65 mm 56-LGA	3	Tray	-40° to +105°C
F4481LKGI8	8.0 × 8.0 × 0.65 mm 56-LGA	3	Reel	-40° to +105°C
F4481EVS	Evaluation Board			

Marking Diagram



- Lines 1 and 2 are the part number.
- Line 3 indicates the following:
  - # denotes device stepping
  - "YY" is the last two digits of the year; "WW" is the work week that the part was assembled.
  - "$" denotes the mark code
- Line 4 is the lot number.

Revision History

Revision Date	Description of Change
December 15, 2020	Removed reference to F4483.
October 15, 2020	Updated Ordering Information.
October 7, 2020	Updated Electrical Characteristics tables and Typical Performance Characteristics.
September 8, 2020	Initial release.

56-LGA, Package Outline Drawing

8.0 x 8.0 x 0.65 mm Body, 0.5mm Pitch

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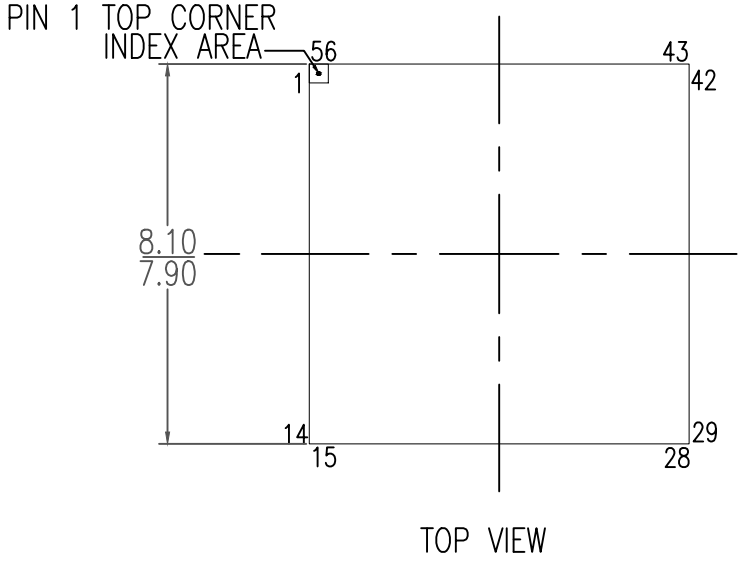
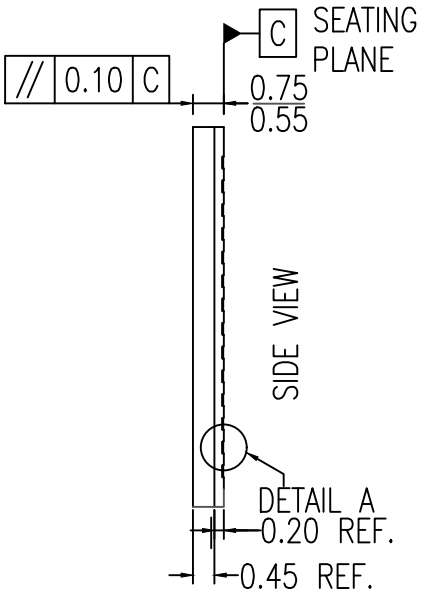
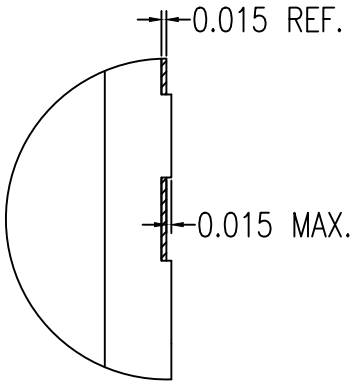
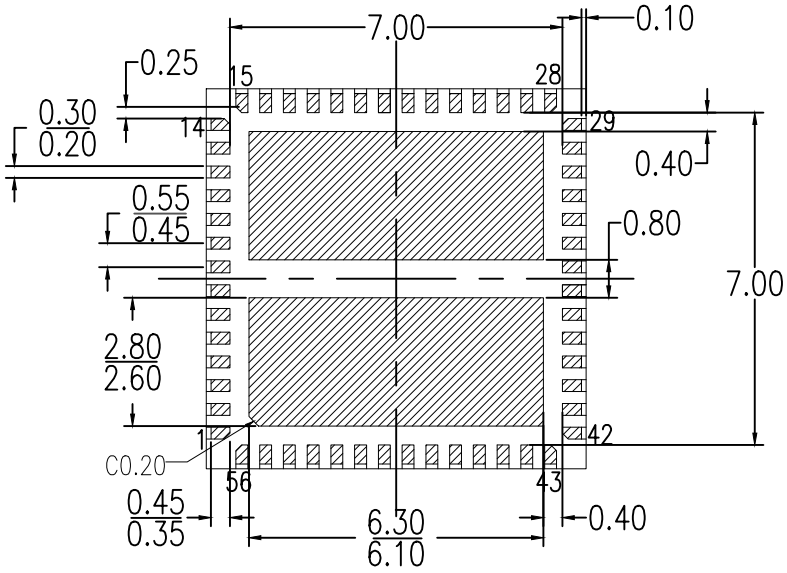


TOP VIEW





DETAIL A

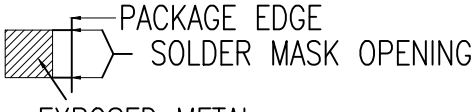


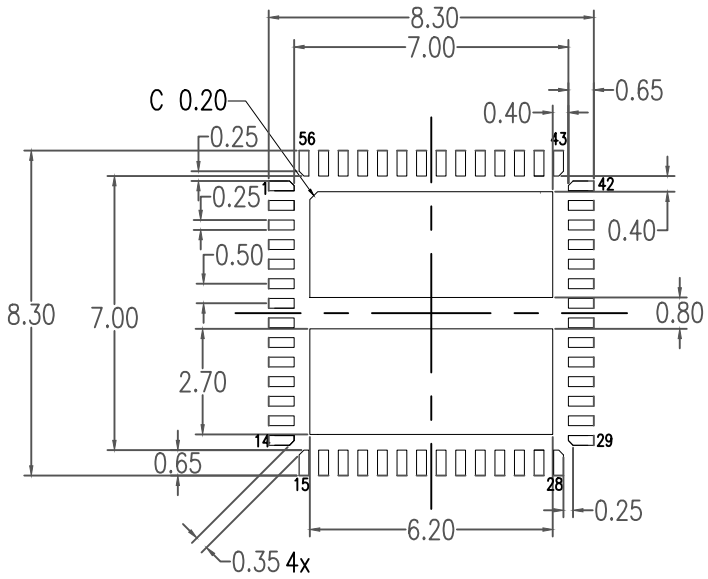
BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS ARE IN MM.

LEGEND:





RECOMMENDED LAND PATTERN DIMENSION

NOTES:
1. ALL DIMENSIONS ARE IN MM.
2. TOP DOWN VIEW. AS VIEWED ON PCB.

Package Revision History		
Date Created	Rev No.	Description
June 21, 2018	Rev 00	Initial Release

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