F6932

Dual-Channel Low Noise Amplifier 17.7GHz – 21.2GHz

Description

The F6932 is an ultra-low power consumption, dual-channel, silicon on insulator (SOI) low noise amplifier (LNA) RFIC designed for application in Ka-Band SATCOM planar phased array antennas. The exceptional combination of low power consumption, low noise, high gain, and compact size, maximizes the antenna array G/T while minimizing overall system power dissipation.

The F6932 includes two LNA channels in a compact 23-pin, 0.5mm pitch BGA package. All inputs and outputs are single-ended and 50Ω matched for ease of integration on to phased array antenna panels.

Features

- Frequency: 17.7GHz – 21.2GHz
- Gain: 22dB
- Noise Figure: 1.2dB
- Output P1dB: -2dBm
- Power Consumption: 15mW/ch
- Supply Voltage: 1.2V nominal
- Compact size for planar integration on λ/2 grid
- 2.7 × 2.7 × 0.9 mm, 23-pin BGA
- -40°C to +85°C ambient operating temperature range

Applications

- Electronically Steered Phased Array Antennas (ESAs)
- Aerospace, Maritime, and Satcom-on-the-move (SOTM)
- Ka-Band SATCOM Terminals
- Communication and Radar Systems

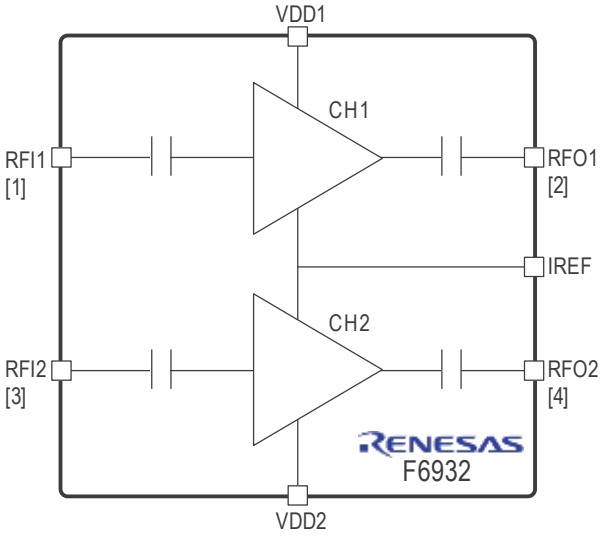

Figure 1. Block Diagram

Contents

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1. Pin Information

1.1 Pin Assignments

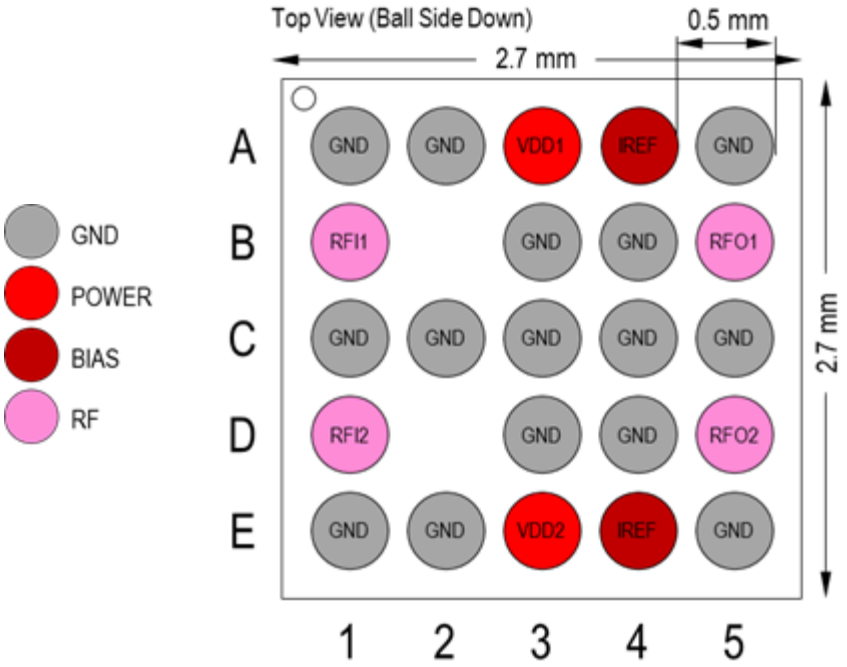


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Pin Number	Name	Type	I/O	Description
A1, A2, A5, B3, B4, C1, C2, C3, C4, C5, D3, D4, E1, E2, E5	GND	Ground	–	DC and RF ground.
A3	VDD1	Power	Input	Positive supply voltage input for channel 1. Channel 2 must also be enabled by powering VDD2 for channel 1 to be operable.
E3	VDD2	Power	Input	Positive supply voltage input for channel 2. For single channel operation of channel 2, channel 1 must be disabled by either floating or grounding VDD1.
A4, E4	IREF	Power	Input	Reference bias current input, tied to a common node shared by channels 1 and 2. Connect directly to a current source, voltage source through a resistor, or to the IBx pin of the F612x beamforming IC.
B1	RFI1	Analog	Input	Channel 1 RF input port.
D1	RFI2	Analog	Input	Channel 2 RF input port.
B5	RFO1	Analog	Output	Channel 1 RF output port.
D5	RFO2	Analog	Output	Channel 2 RF output port.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Exposure of the device to parameter values outside of the range listed below may reduce the operating lifetime and adversely and permanently alter the device characteristics. Furthermore, functional operation at or near absolute maximum ratings is not implied.

Parameter	Symbol	Conditions	Minimum	Maximum	Unit
Supply Voltage	V_{DD1} V_{DD2}	-	-0.3	1.4	V
IREF Pin Input Current	I_{REF}	-	0	70	µA
IREF Pin Voltage	V_{REF}	-	0	0.75	V
RF Input Power	P_{IN}	VSWR ≤ 2.1. 30s CW	-	0	dBm
Junction Temperature	T_J	-	-	125	°C
Lead Temperature (soldering)	T_{LEAD}	Not to exceed 30s at Max temperature per J-STD-020E	-	260	°C
Human Body Model, VHBM (Tested per JS-001-2012)	-	-	-	1000	V
Charged Device Model, VCDM (Tested per JESD22-C101)	-	-	-	150	V

2.2 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
RF Frequency Range	f_{RF}	17.7	-	21.2	GHz
Power Supply Voltage	V_{DD1} V_{DD2}	1.1	1.2	1.3	V
Reference Bias Current	I_{REF}	35	45	55	µA
Ambient Temperature	T_A	-40	-	85	°C
RF Pin Load Impedance	Z_{RF}	-	50	-	Ω

2.3 Thermal Specifications

Parameter	Symbol	Value	Unit
Theta JB. Junction to board	θ_{JB}	14	°C/W
Theta JC. Junction to case (case top)	θ_{JC}	108	°C/W
Theta JA. Junction to ambient	θ_{JA}	47	°C/W
Storage Temperature	T_{STOR}	-40 to +150	°C

2.4 Electrical Specifications

2.4.1 DC Electrical Specifications

V_{DD} = 1.2V, T_A = 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Supply Current, Per Channel	I_{DD}	I_{REF} = 45µA, T_A = 25°C	-	12.4	17.5	mA
		I_{REF} = 45µA, T_A = 85°C	-	13.1	-	mA
Supply Current, Idle-state[1]	I_{DD_IDLE}	I_{IREF} = 0µA	-	2	-	mA

1. I_{REF} pin may be grounded or left floating for idle state.

2.4.2 RF Electrical Specifications

V_{DD} = 1.2V, I_{REF} = 45µA, T_A = 25°C, Z_S = Z_L = 50Ω, f_{RF} = 17.7GHz – 21.2GHz, unless otherwise specified.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	T_A = 25°C	18	22	-	dB
		T_A = 85°C	-	21	-	dB
Gain Flatness vs. Frequency	G_{VAR_FREQ}	f_{RF} = 17.7 – 21.2 GHz	-	2.9	-	dB
		Within any 250MHz	-	0.3	-	dB
Noise Figure	NF	T_A = 25°C	-	1.2	-	dB
		T_A = 85°C	-	2.0	-	dB
Output 1dB Compression Point	OP1dB	-	-	-2	-	dBm
Output 3rd Order Intercept Point	OIP3	Pin = -35 dBm/tone, Δf = 1MHz	-	7	-	dBm
Input Return Loss	IRL	-	-	12	-	dB
Output Return Loss	ORL	-	-	13	-	dB
Reverse Isolation	ISO	-	-	45	-	dB
Channel-to-Channel Isolation	ISO_{CH-CH}	-	-	37	-	dB

3. Typical Application Circuit

Figure 3 shows two typical application circuits for biasing the F6932 supplying V_{DD1} and V_{DD2} from a single common V_{DD} supply.

The top circuit uses a voltage source V_{REF} to supply the bias reference current I_{REF} through an external resistor R_{REF}. V_{REF} should be set to achieve the recommended I_{REF} bias currents per the indicated formula. For V_{REF} = 1.2V, a value of R_{REF} = 13.7kΩ will produce the recommended typical I_{REF} bias condition.

The bottom circuit uses the programmable IDAC of the Renesas F612X beamforming IC to provide the reference current directly to the F6932.

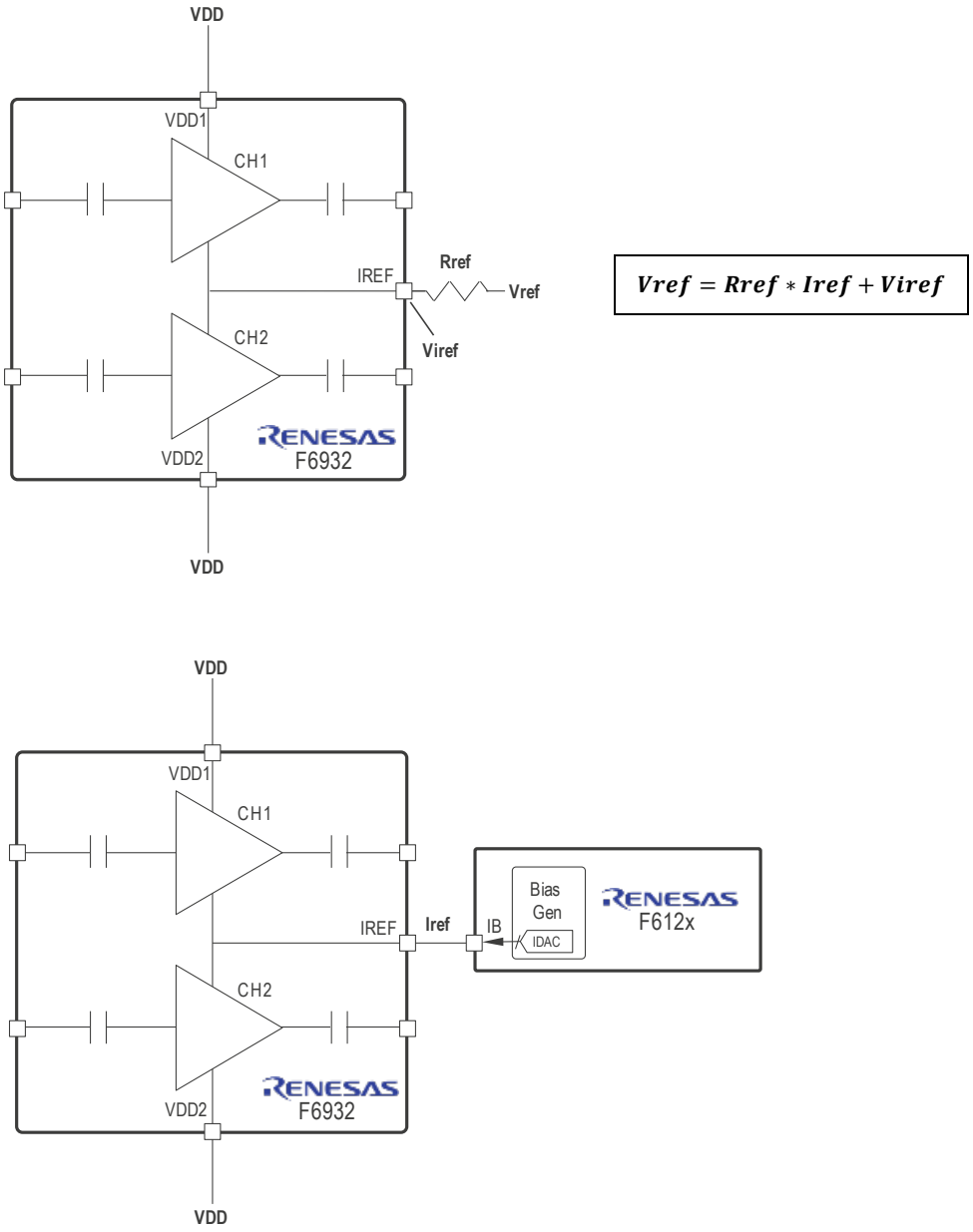


Figure 3. Typical Application Circuits

4. Typical Performance Graphs

V_{DD} = 1.2V, I_{REF} = 45µA, T_A = 25°C, Z_S = Z_L = 50Ω, f_{RF} = 19.5GHz unless otherwise stated.

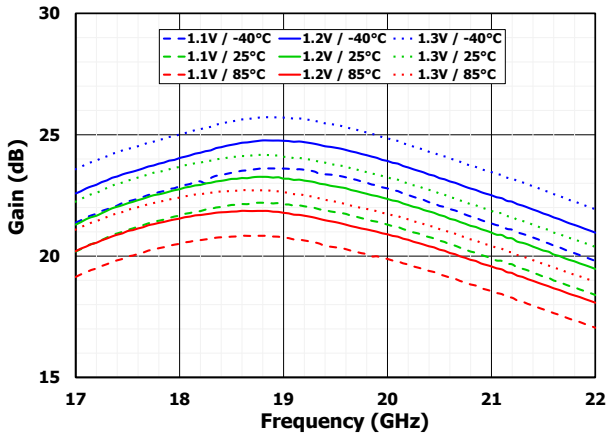


Figure 4. Gain

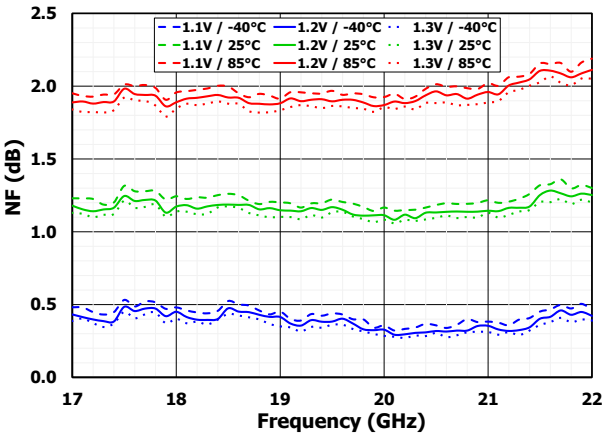


Figure 5. Noise Figure

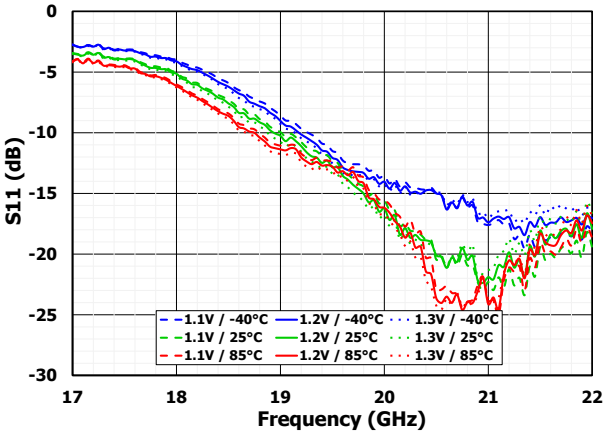


Figure 6. Input Match

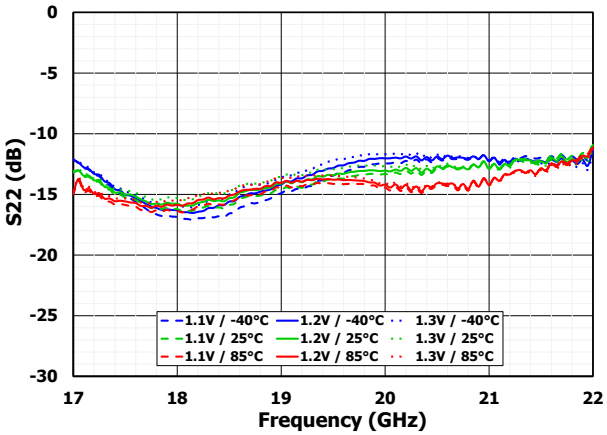


Figure 7. Output Match

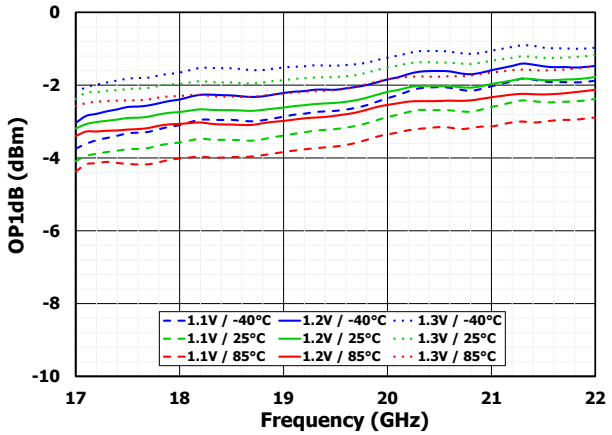


Figure 8. Output 1dB Compression

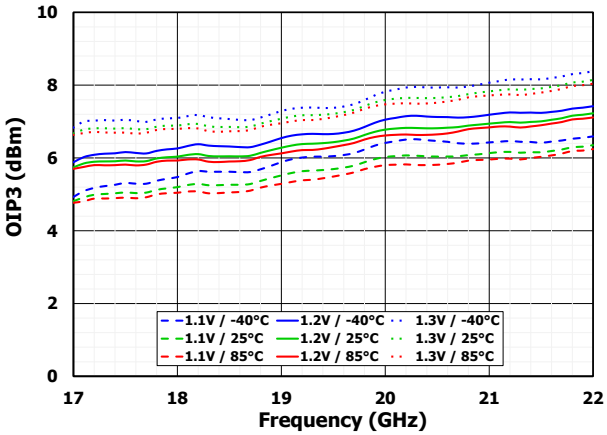


Figure 9. Output 3rd Order Intercept

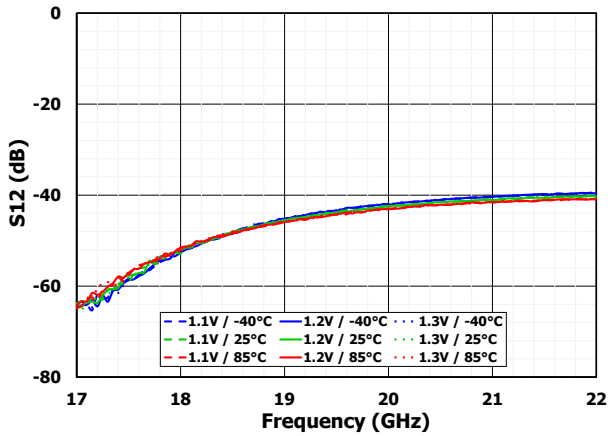


Figure 10. Reverse Isolation

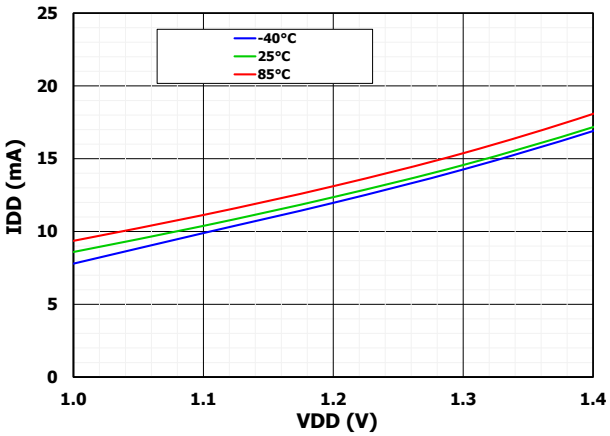


Figure 11. Supply Current, Per Channel

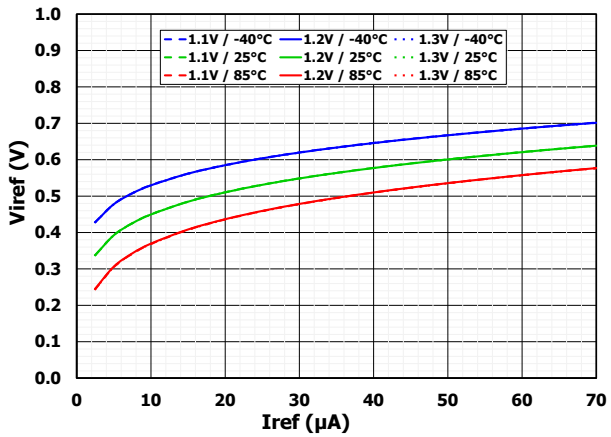


Figure 12. I_{REF} Pin Voltage vs Current

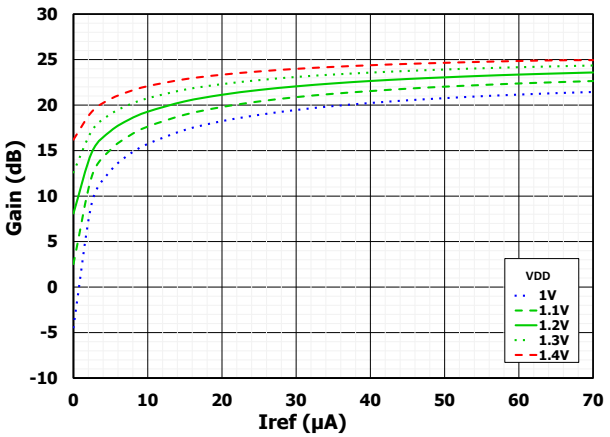


Figure 13. Gain vs Bias

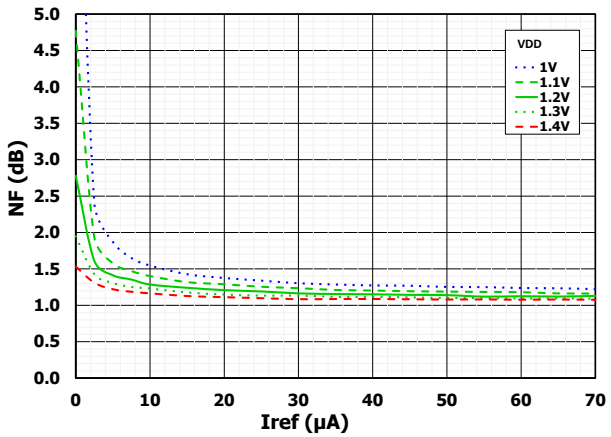


Figure 14. NF vs Bias

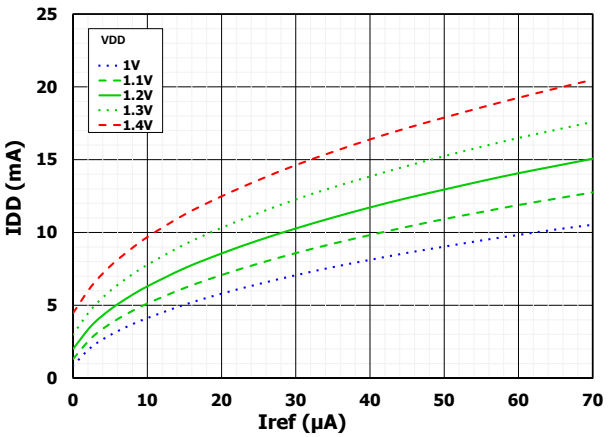


Figure 15. Supply Current vs Bias, Per Channel

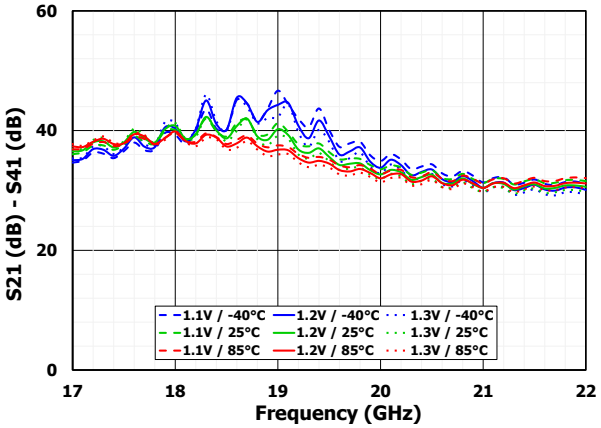


Figure 16. Channel-Channel Isolation

5. Evaluation Board

5.1 Evaluation Board Photos

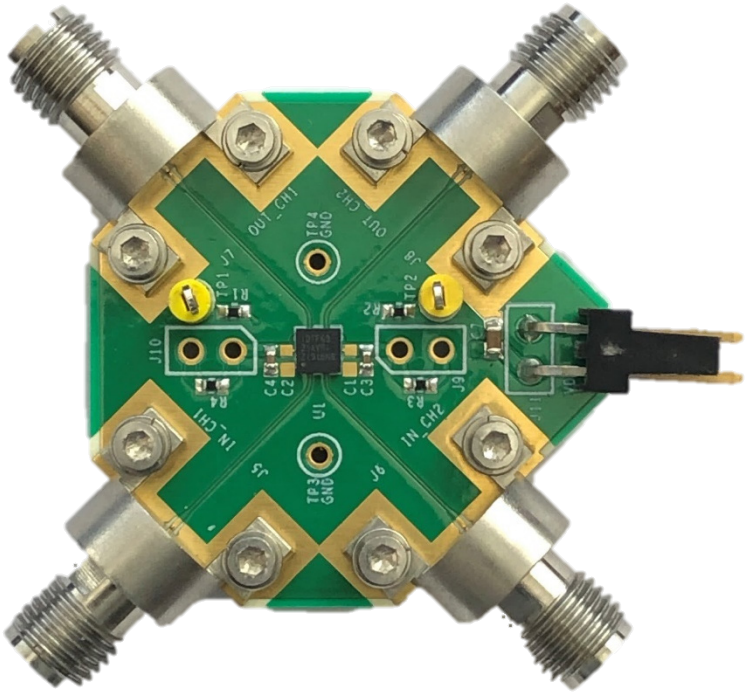


Figure 17. Evaluation Board – Top View

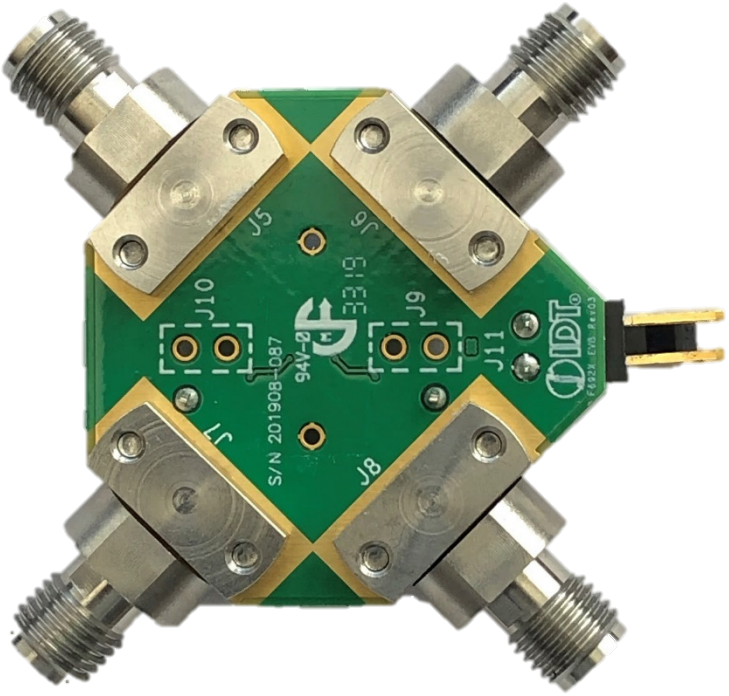


Figure 18. Evaluation Board – Bottom View

5.2 Evaluation Board Schematic

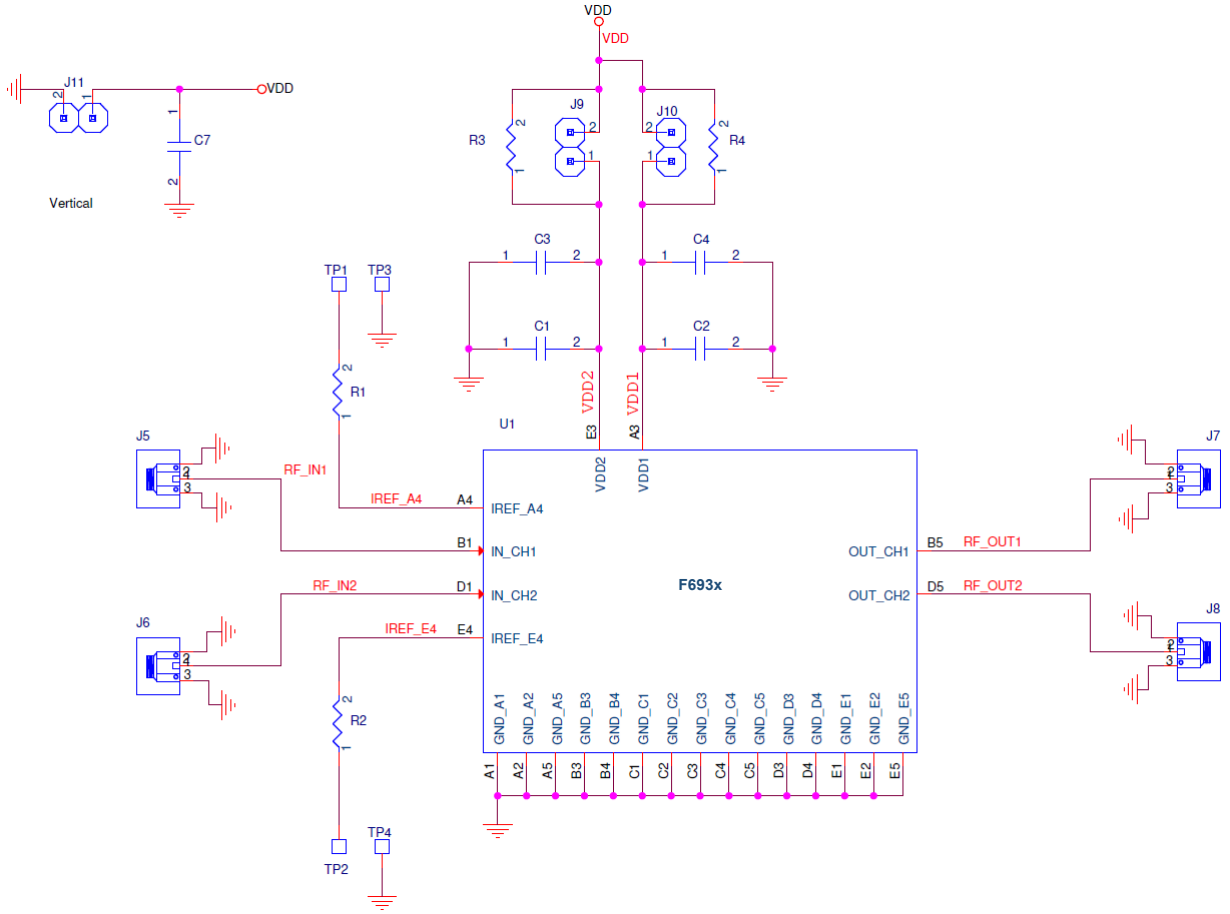


Figure 19. Evaluation Board – Schematic

Table 1. Bill of Materials (BOM)

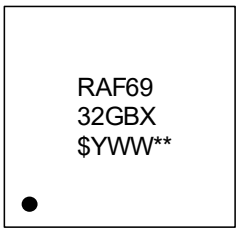
Part Reference	QTY	Description	Part Number	Manufacturer
C1, C2	2	33pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H330J	MURATA
C3, C4	2	1µF ±10%, 16V, X6S Ceramic Capacitor (0402)	GRM155C81C105K	MURATA
C7	1	10µF ±20%, 16V, X6S Ceramic Capacitor (0603)	GRM188C81C106M	MURATA
R1, R2	2	13.7kΩ ±1%, 1/16W, Resistor (0402)	RC0402FR-0713K7L	Yageo
R3, R4 [1]	2	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
J5–J8	4	Edge Launch 2.92mm 40GHz	ELF-40-002	SIGNAL MICROWAVE
J9, J10	2	DNI	DNI	DNI
J11	1	CONN HEADER R/A 2POS 2.54MM	1718571002	MOLEX
TP1, TP2, TP3, TP4	4	Test Point Yellow	5004	Keystone Electronics
U1	1	Dual-Channel Low Noise Amplifier 17.7GHZ to 21.2GHz	F6932	Renesas

1. For single channel operation of Ch2, remove R4 to disconnect VDD1 from the VDD supply pin.

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagram



- Lines 1 and 2: part number
- Line 3:
  - “$” is the mark location code
  - “Y” is the last digit of the assembly year
  - “WW” is the assembly workweek
  - “**” is the lot sequential code

8. Ordering Information

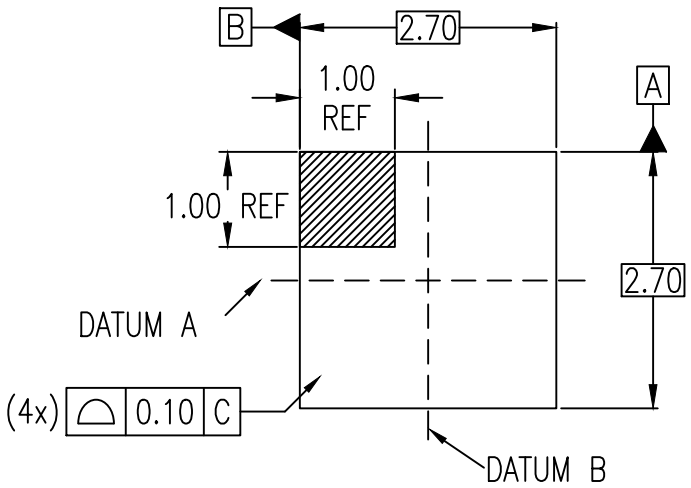
Part Number	Package Description	MSL Rating	Carrier Type	Temperature Range
RA81F6932GBX#BC0	2.7 × 2.7 × 0.9 mm 23-FCCSP	3	Tray	-40°C to +85°C
RA81F6932GBX#HC0		3	Reel	
RTKA81F6932000RU	F6932 Evaluation Board			

9. Revision History

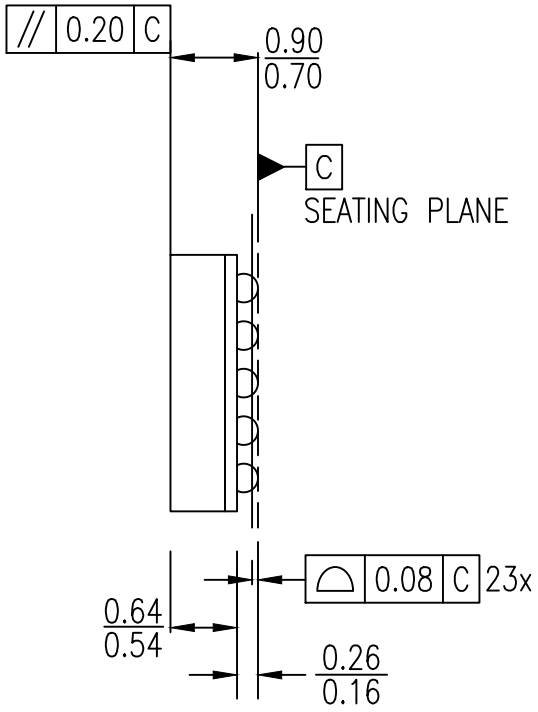
Revision	Date	Description
1.02	Nov 14, 2024	Updated Applications section on page 1.
1.01	Sep 18, 2024	Updated VDD1 and VDD2 pin descriptions in section 1.2. Added EVB BOM note about single channel operation in Table 1.
1.00	Feb 23, 2024	Initial release.

23-FCCSP, Package Outline Drawing

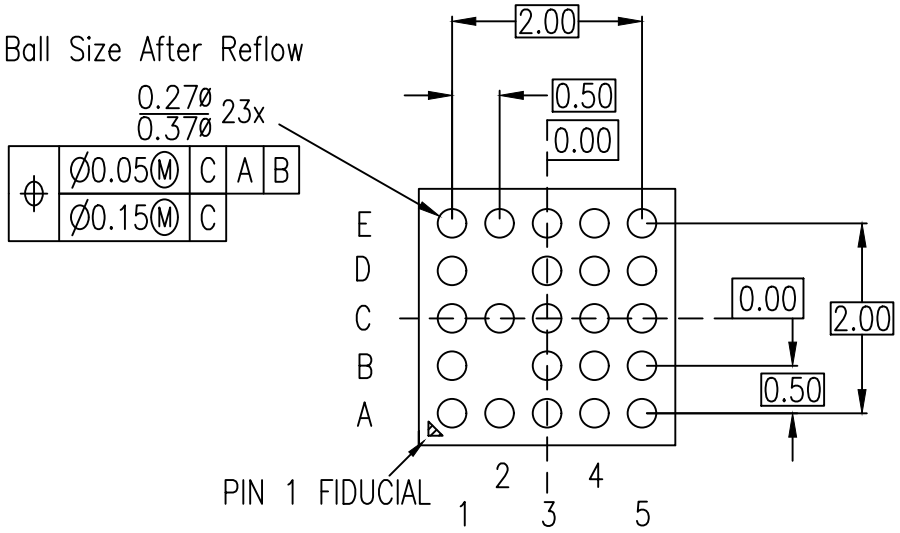
2.7 x 2.7 x 0.9 mm Body, 0.50 mm Pitch,
AVR23D1, PSC-4781-01, Rev 00, Page 1



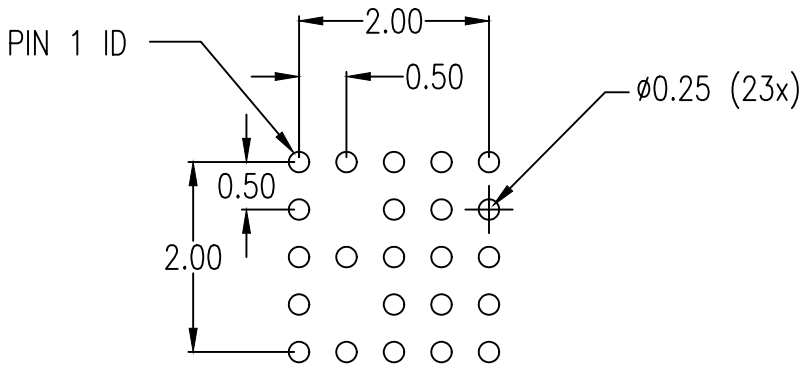
TOP VIEW



SIDE VIEW



BOTTOM VIEW
(BALL SIDE VIEW)



RECOMMENDED LAND PATTERN DIMENSION
(TOP VIEW)

NOTES:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Dec. 6, 2018	Rev 00	Initial Release

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