To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HAT2189WP

Silicon N Channel Power MOS FET
Power Switching

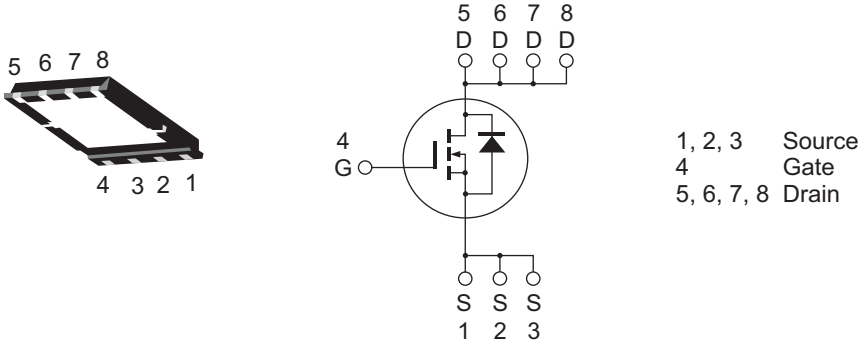
REJ03G1251-0200
Rev.2.00
Aug 28, 2009

Features

- Low on-resistance
- Low drive current
- High density mounting

Outline

RENESAS Package code: PWSN0008DA-A
(Package name: WPAK)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	8.5	A
Drain peak current	$I_{D\ (pulse)}$ Note1	17	A
Body-drain diode reverse drain current	I_{DR}	8.5	A
Body-drain diode reverse drain peak current	$I_{DR\ (pulse)}$ Note1	17	A
Avalanche current	I_{AP} Note3	8.5	A
Avalanche energy	E_{AR} Note3	4.8	mJ
Channel dissipation	Pch Note2	20	W
Channel to case thermal impedance	θch-c	6.25	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at Tc = 25°C
3. STch = 25°C, Tch ≤ 150°C

Electrical Characteristics

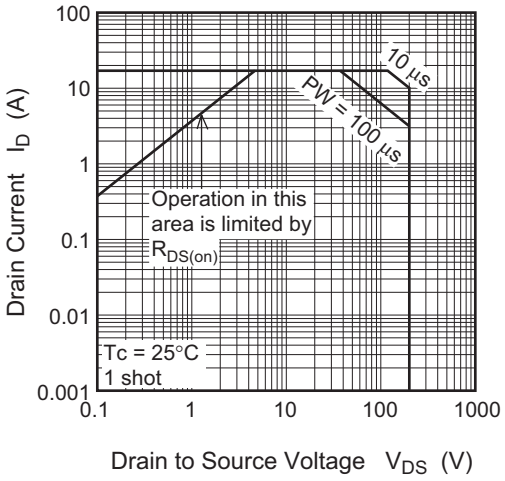
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	I_D = 10 mA, V_{GS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	V_{DS} = 200 V, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	μA	V_{GS} = ±30 V, V_{DS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward transfer admittance	$\|y_{fs}\|$	3.5	6.0	—	S	I_D = 4.3 A, V_{DS} = 10 V Note4
Static drain to source on state resistance	$R_{DS(on)}$	—	0.23	0.27	Ω	I_D = 4.3 A, V_{GS} = 10 V Note4
Input capacitance	Ciss	—	430	—	pF	V_{DS} = 25 V V_{GS} = 0 f = 1 MHz
Output capacitance	Coss	—	86	—	pF	
Reverse transfer capacitance	Crss	—	7	—	pF	
Turn-on delay time	$t_{d(on)}$	—	24	—	ns	I_D = 4.3 A V_{GS} = 10 V R_L = 23.3 Ω Rg = 10 Ω
Rise time	t_r	—	24	—	ns	
Turn-off delay time	$t_{d(off)}$	—	44	—	ns	
Fall time	t_f	—	9	—	ns	
Total gate charge	Qg	—	10	—	nC	V_{DD} = 160 V V_{GS} = 10 V I_D = 8.5 A
Gate to source charge	Qgs	—	2.7	—	nC	
Gate to drain charge	Qgd	—	3.8	—	nC	
Body-drain diode forward voltage	V_{DF}	—	0.9	1.4	V	I_F = 8.5 A, V_{GS} = 0 Note4
Body-drain diode reverse recovery time	t_{rr}	—	100	—	ns	I_F = 8.5 A, V_{GS} = 0 di_F/dt = 100 A/μs

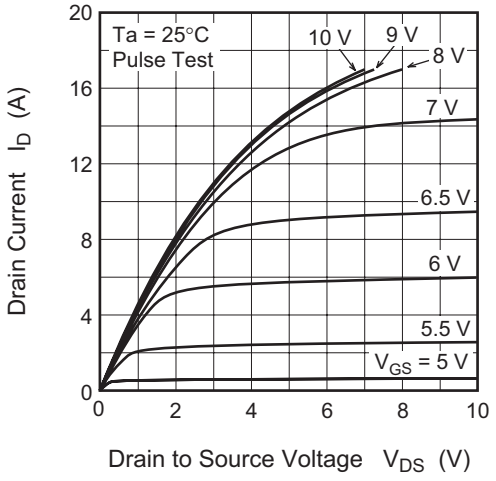
Notes: 4. Pulse test

Main Characteristics

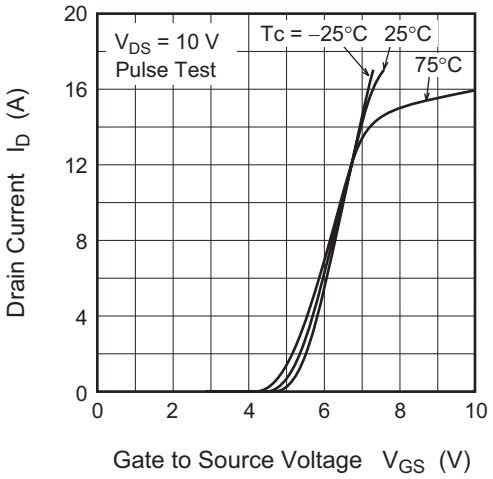
Maximum Safe Operation Area



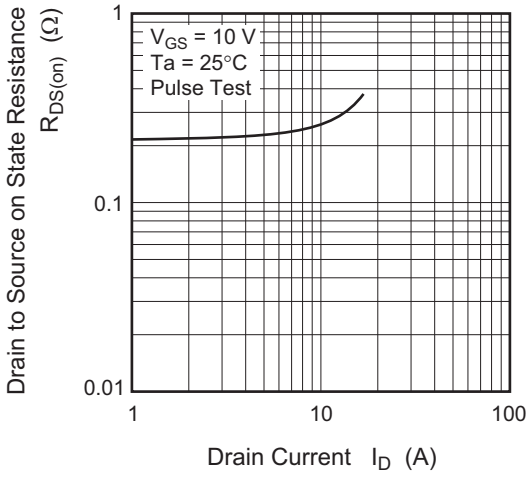
Typical Output Characteristics



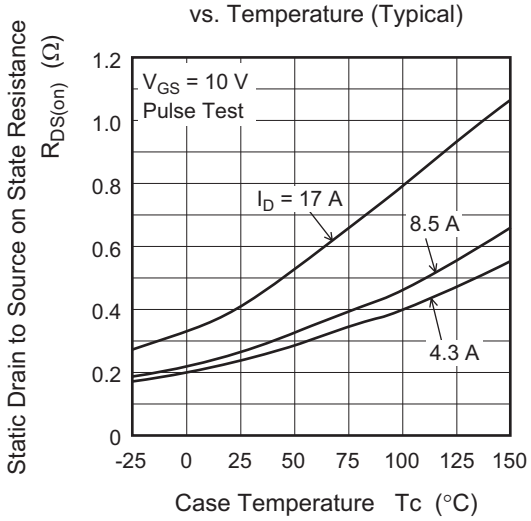
Typical Transfer Characteristics



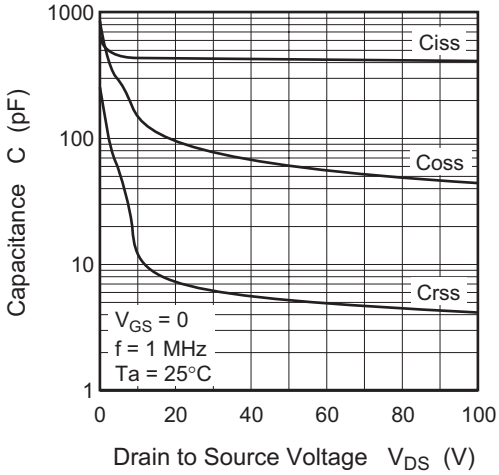
Static Drain to Source on State Resistance vs. Drain Current (Typical)



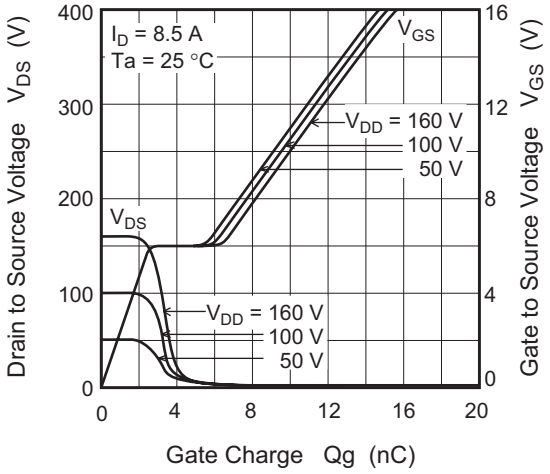
Static Drain to Source on State Resistance vs. Temperature (Typical)



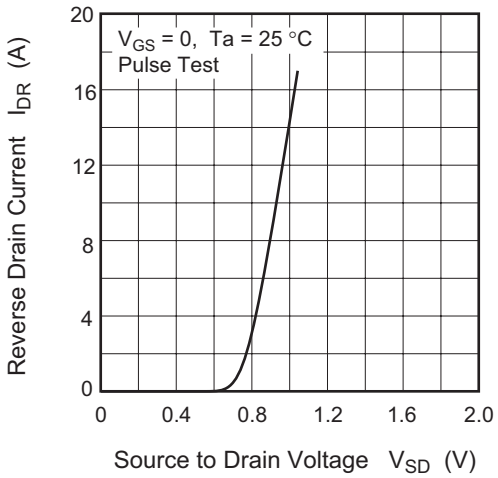
Typical Capacitance vs. Drain to Source Voltage



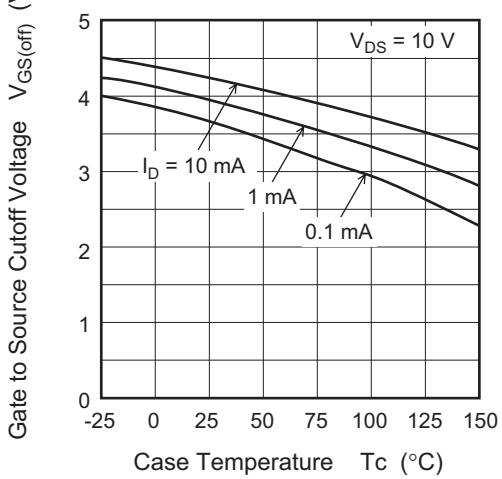
Dynamic Input Characteristics (Typical)



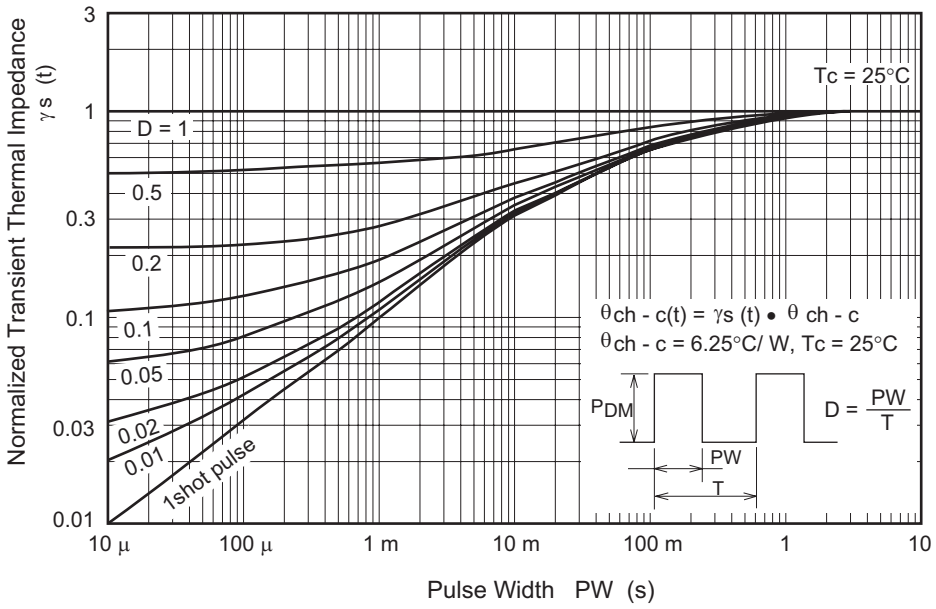
Reverse Drain Current vs. Source to Drain Voltage (Typical)



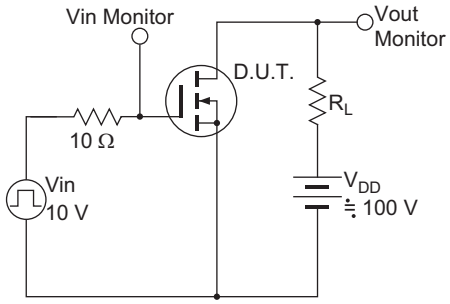
Gate to Source Cutoff Voltage vs. Case Temperature (Typical)



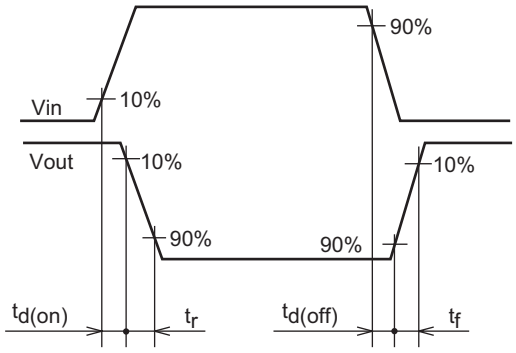
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit



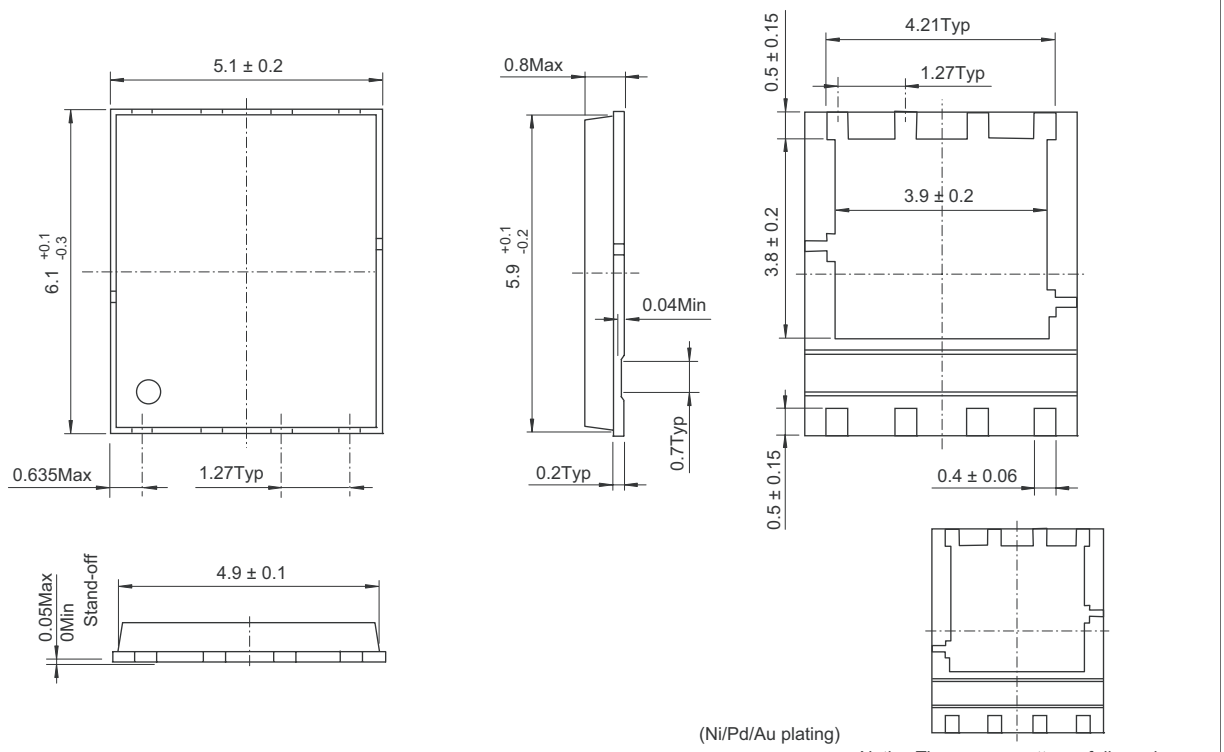
Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
WPAK	–	PWSN0008DA-A	WPAKV	0.075g

Unit: mm



Ordering Information

Part No.	Quantity	Shipping Container
HAT2189WP-EL-E	2500 pcs	Taping

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

Colophon .7.2