HS-1825ARH, HS-1825AEH

Radiation Hardened High-Speed, Dual Output PWM

FN4561
Rev 10.00
August 5, 2016

The radiation hardened HS-1825ARH, HS-1825AEH pulse width modulator is designed to be used in high frequency switched-mode power supplies and can be used in either current-mode or voltage-mode. It is well suited for single-ended boost converter applications.

Device features include a precision voltage reference, low power start-up circuit, high frequency oscillator, wide-band error amplifier and fast current-limit comparator. The use of proprietary process capabilities and unique design techniques results in fast propagation delay times and high output current over a wide range of output voltages.

Constructed with the Intersil radiation hardened Silicon Gate (RSG) Dielectric Isolation BiCMOS process, the HS-1825ARH, HS-1825AEH have been specifically designed to provide highly reliable performance when exposed to harsh radiation environments.

Features

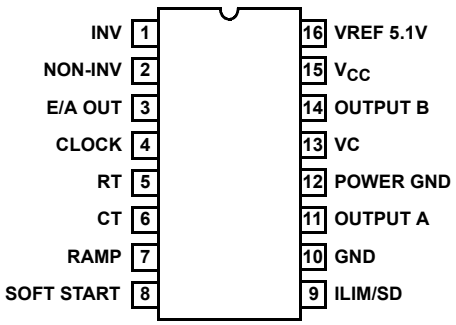
- Electrically screened to DLA SMD # 5962-99558
- QML qualified per MIL-PRF-38535 Requirements
- Radiation environment
  - Maximum total dose . . . . . 300 krad(Si)
  - Vertical architecture provides low dose rate immunity
  - DI RSG process provides latch-up immunity
- Low start-up current. . . . . 100µA (Typical)
- Fast propagation delay . . . . . 80ns (Typical)
- 12V to 30V operation
- 1A (peak) dual output drive capability
- 5.1V reference
- Undervoltage lockout
- Programmable soft-start
- Switching frequencies to 500kHz
- Latched overcurrent comparator with full cycle restart
- Programmable leading edge blanking circuit

Applications

- Current or voltage mode switching power supplies
- Motor speed and direction control

Pin Configuration

HS-1825ARH, HS-1825AEH
SBDIP (CDIP2-T16) AND FLATPACK (CDFP4-F16)
TOP VIEW



NOTE: Grounding the soft-start pin does not inhibit the outputs. The outputs may be inhibited by applying >1.26V to the ILIM/SD pin.

Ordering Information

ORDERING NUMBER (Note 2)	INTERNAL MKT. NUMBER (Note 1)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F9955801V9A	HS0-1825ARH-Q	-50 to +125	Die	
5962F9955802V9A	HS0-1825AEH-Q	-50 to +125	Die	
HS0-1825ARH/Sample	HS0-1825ARH/Sample	-50 to +125	Die	
5962F9955801VEC	HS1-1825ARH-Q	-50 to +125	16 Ld SBDIP	D16.3
5962F9955802VEC	HS1-1825AEH-Q	-50 to +125	16 Ld SBDIP	D16.3
5962F9955801QEC	HS1-1825ARH-8	-50 to +125	16 Ld SBDIP	D16.3
5962F9955801VXC	HS9-1825ARH-Q	-50 to +125	16 Ld Flatpack	K16.A
5962F9955802VXC	HS9-1825AEH-Q	-50 to +125	16 Ld Flatpack	K16.A
5962F9955801QXC	HS9-1825ARH-8	-50 to +125	16 Ld Flatpack	K16.A
HS1-1825ARH/Proto	HS1-1825ARH/Proto	-50 to +125	16 Ld SBDIP	D16.3
HS9-1825ARH/Proto	HS9-1825ARH/Proto	-50 to +125	16 Ld Flatpack	K16.A

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table must be used when ordering.

Typical Performance Curves

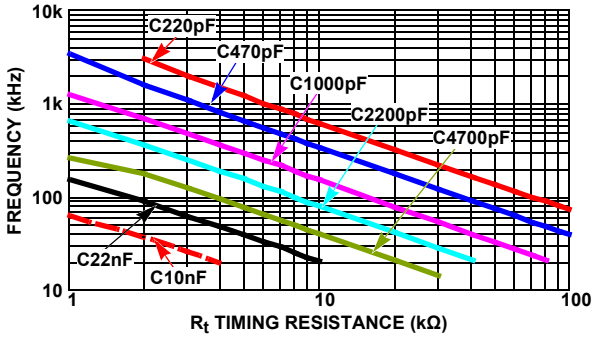


FIGURE 1. OSCILLATOR FREQUENCY vs R_t AND C_t

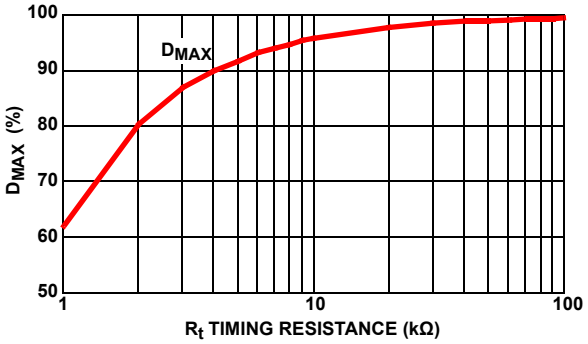


FIGURE 2. MAXIMUM DUTY CYCLE vs R_t

Die Characteristics

DIE DIMENSIONS

4860µm x 3410µm (185 mils x 140 mils)
Thickness: 483µm ±25.4µm (19 mils ±1 mil)

INTERFACE MATERIALS

Glassivation

Type: PSG (Phosphorous Silicon Glass)
Thickness: 8.0kÅ ±1.0kÅ

Top Metallization

Type: ALSiCu
Thickness: 16.0kÅ ±2kÅ

Substrate

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased (DI)

ADDITIONAL INFORMATION

Worst Case Current Density

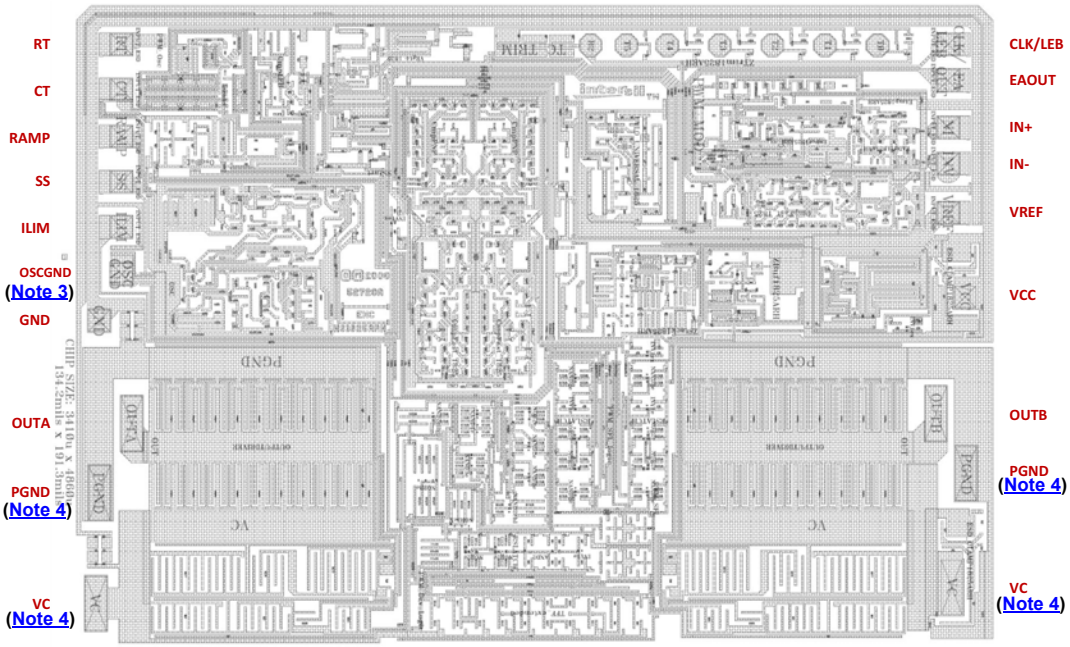
$<2.0 \times 10^5$ A/cm^2

Transistor Count

225

Metallization Mask Layout

HS-1825ARH, HS-1825AEH



NOTES:

3. This is the oscillator ground (OSCGND) bond pad and must be connected to GND.
4. PGND and VC each require two bond pad connections.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
August 5, 2016	FN4561.10	Updated the die plot in the datasheet. Changed the die dimensions from 4710µm x 3570µm to 4860µm x 3410µm. Added Revision History and About Intersil sections. Added applicable PODs.

About Intersil

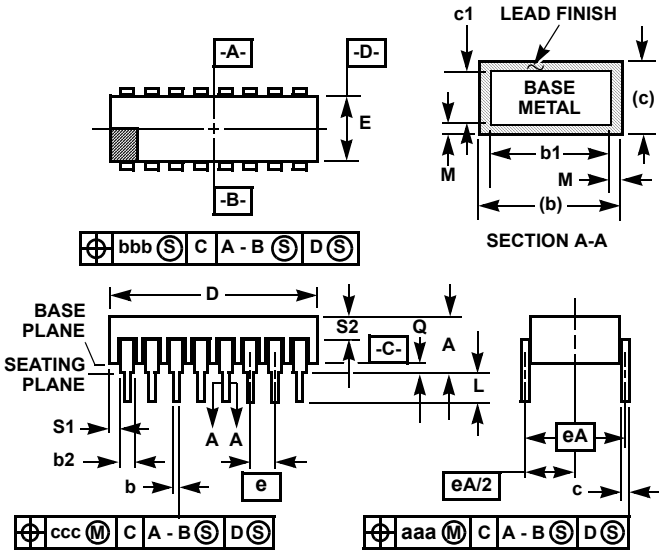
Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

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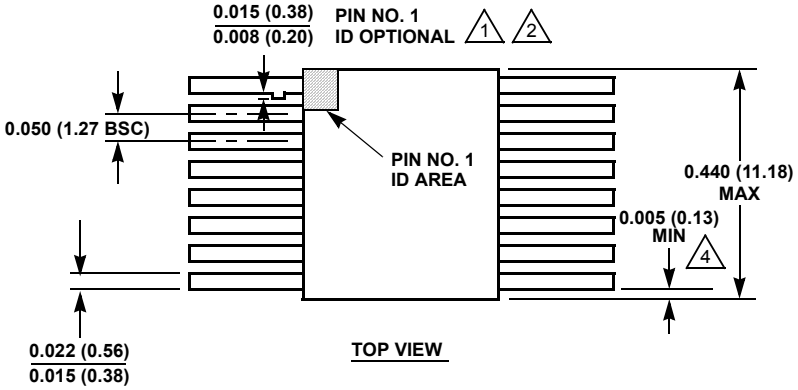
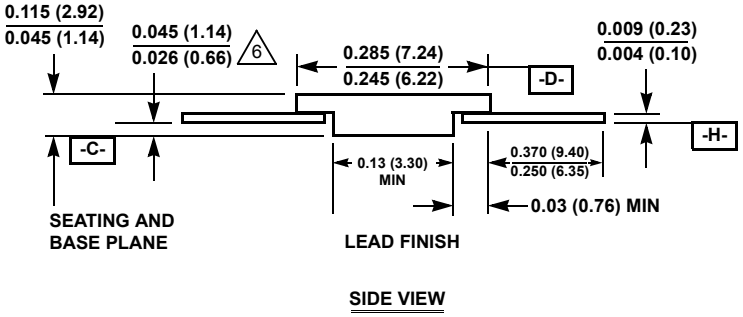
Package Outline Drawing

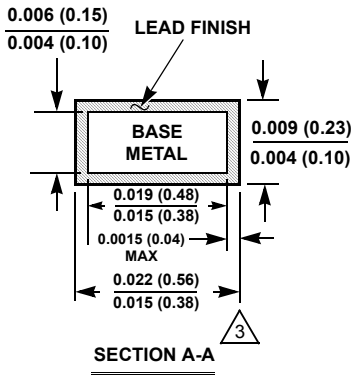
K16.A

16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 2, 1/10







NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.