HSP50415

Wideband Programmable Modulator (WPM)

FN4559
Rev 6.00
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The HSP50415 Wideband Programmable Modulator (WPM) is a quadrature amplitude modulator/upconverter designed for wideband digital modulation. The WPM combines shaping and interpolation filters, a complex modulator, timing and carrier NCOs and dual DACs into a single package.

The HSP50415 supports vector modulation, accepting up to 16-bit In phase (I) and Quadrature (Q) samples to generate virtually any quadrature AM or PM modulation format. A constellation mapper and 24 Symbol span interpolation shaping filter is provided for the input baseband signals. Gain adjustment is provided after the shaping FIR filter. A timing error generator in the input section allows the on-chip timing NCO to track the input timing.

The WPM includes a Numerically Controlled Oscillator (NCO) driven interpolation filter, which allows the input and output sample rate to have a non-integer or variable relationship. This re-sampling feature simplifies use of sample rates that do not have harmonic or integer frequency relationships to the input data rate and decouples the carrier from the DATACLK.

A complex quadrature modulator modulates the baseband data on a programmable carrier center frequency. The WPM offers digital output spurious Free Dynamic Range (SFDR) that exceeds 70dB at the maximum output sample rate of 100MSPS, for input sample rates as high as 25MSPS. X/SIN(X) rolloff compensation filtering is provided. Real 14-bit digital output data is available prior to the 12-bit DACs providing 20mA full scale output current.

Features

- Output Sample Rates . . . . . to 100MSPS
- Input Data Rates . . . . . Up to 25MSPS (I/Q)
- 32-Bit Programmable Carrier NCO
- X/SIN(X) Rolloff Compensation
- Programmable I and Q Shaping FIR Filters:
  - Up to 24 Symbol Span
- Fixed or NCO Controlled Interpolation:
  - Interpolation Range . . . . . 4 to >128k
  - Digital PLL to Lock to Input Symbol Clock
- Digital Signal Processing Capable of >70dB SFDR
- Dual 12-bit D/A Processing Capable of >50dB SFDR
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Wide-Band Digital Modulation
- Base Station Modulators
- HSP50415EVAL1 Evaluation Board Available

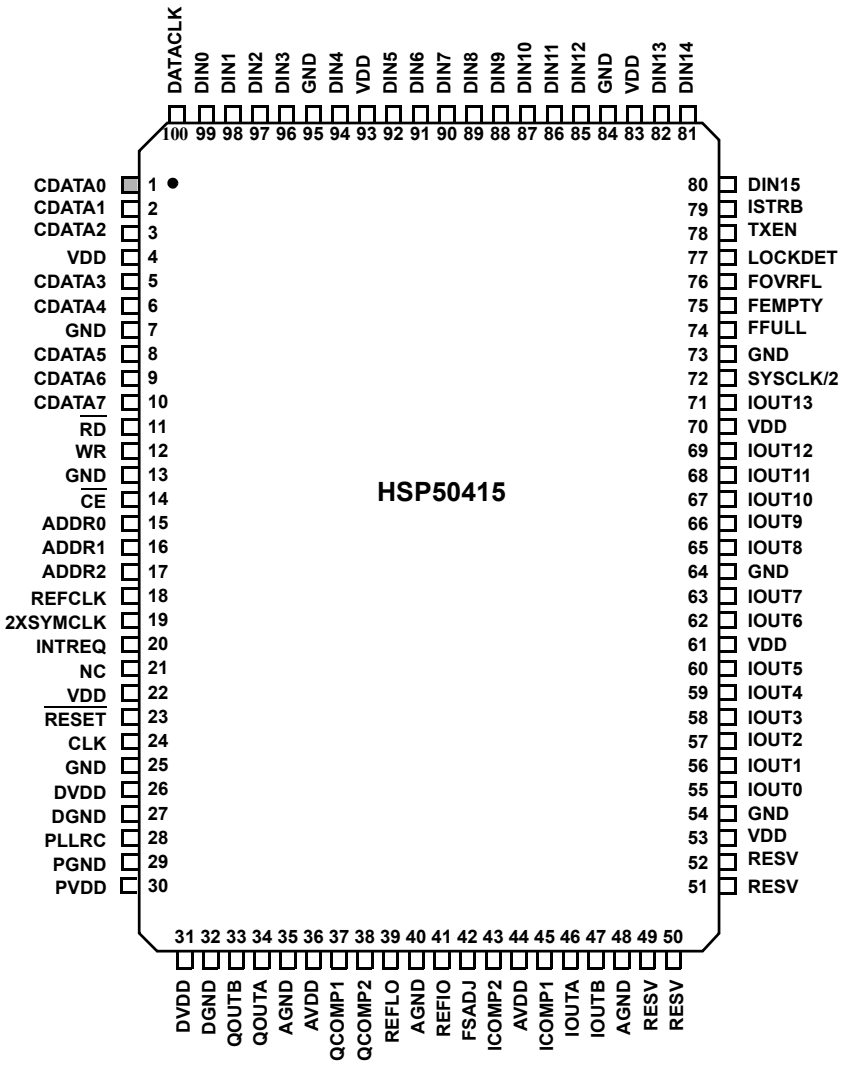
Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG #
HSP50415VI	HSP50415VI	-40 to +85	100 Ld MQFP	Q100.14x20
HSP50415VIZ (Note)	HSP50415VIZ	-40 to +85	100 Ld MQFP (Pb-free)	Q100.14x20
HSP50415EVAL1	Evaluation Board			

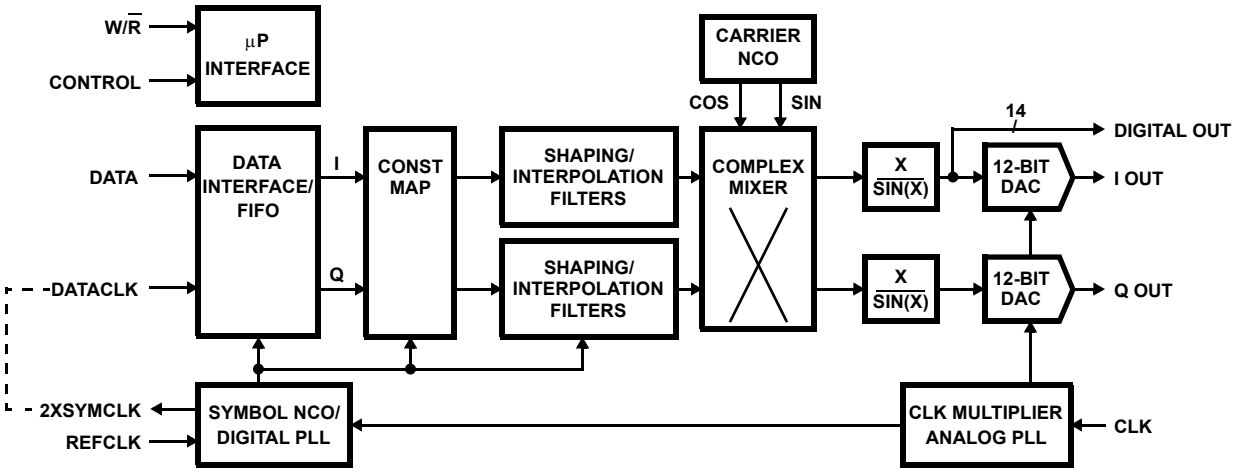
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

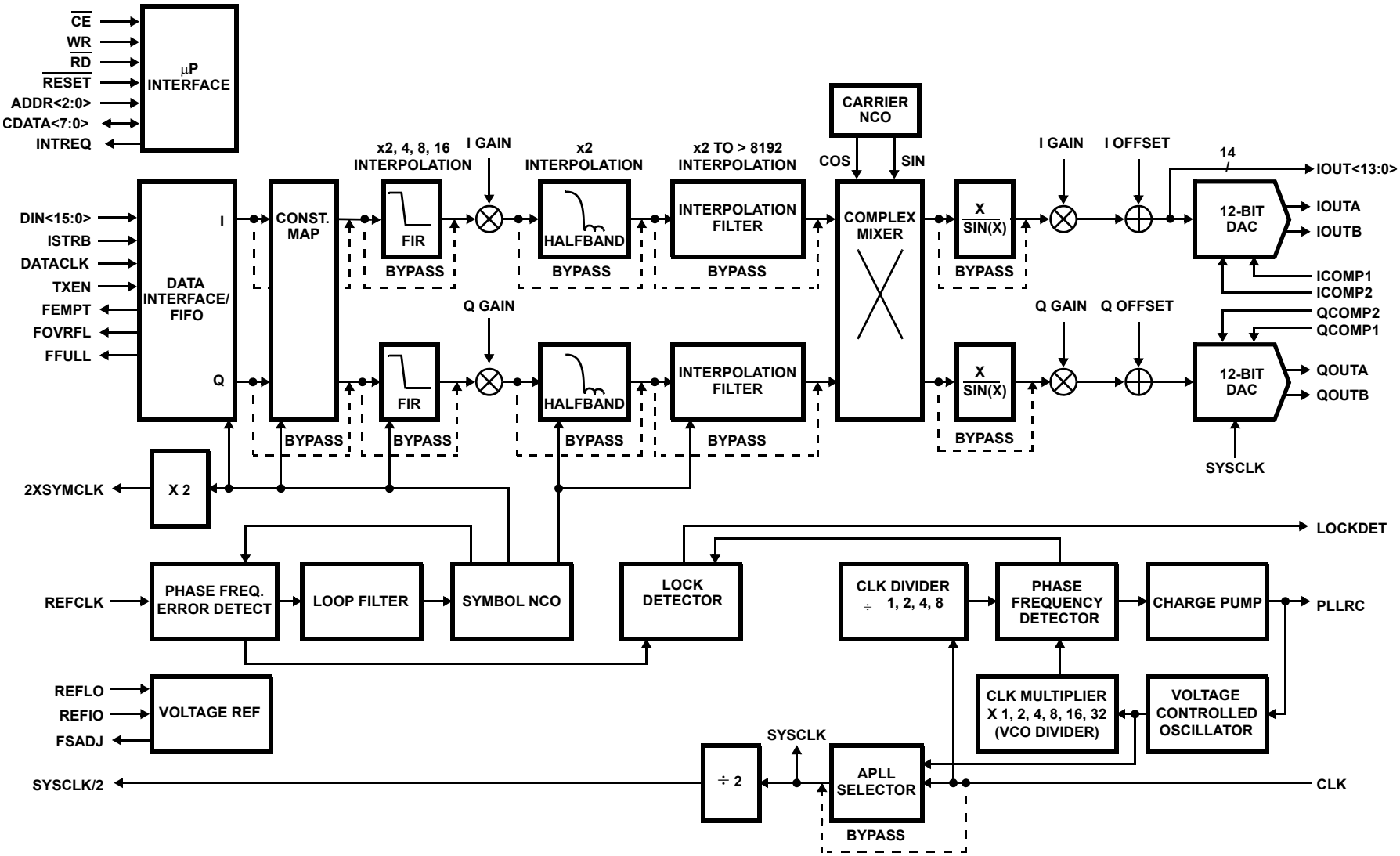
HSP50415
(100 LD MQFP)
TOP VIEW



Block Diagram



Functional Block Diagram



Pin Descriptions

NAME	TYPE	DESCRIPTION
VDD	-	Digital power.
GND	-	Digital ground.
DVDD	-	DAC digital power.
DGND	-	DAC digital ground.
AVDD	-	DAC analog power.
AGND	-	DAC analog ground.
PVDD	-	PLL analog power.
PGND	-	PLL analog ground.
PLLRC	I	PLL loop filter provides for the addition of less expensive RC components in place of a crystal oscillator. The recommended values for this pin are detailed in the ‘System CLK Generation’ section.
CLK	I	System and DAC clock input when APLL not in use, otherwise it is the reference to the APLL.
SYSCLK/2	O	Sample Clock Divided by Two. All digital output data and status pins are output from this clock. The polarity of SYSCLK/2 may be programmed via Register 2 bit-3.
2XSYMCLK	O	Tri-statable Symbol NCO Clock Output Multiplied by Two. The polarity of 2XSYMCLK may be programmed via register 2 bit-15.
REFCLK	I	External digital PLL reference clock input.
DIN<15:0>	I	Data Bus. The DIN<15:0> bus loads the input data.
DATACLK	I	Asynchronous data clock for DIN<15:0>.
TXEN	I	DIN<15:0> may be optionally gated with the TXEN pin (burst mode) or input free-running as defined by register 2 bits 18-17. The polarity of TXEN may be programmed via register 2 bit-5.
ISTRB	I	Data samples are input as I then Q serially with the ISTRB pin active with the I sample. The polarity of ISTRB may be programmed via Register 2 bit-4.
CDATA<7:0>	I/O	µP Bidirectional Data Bus. The CDATA<7:0> data bus is used for loading the configuration data and sample vectors for modulation. CDATA7 is the MSB.
RD	I	µP Read control input.
WR	I	µP Write strobe input.
CE	I	Chip enable input.
ADDR<2:0>	I	µP Address Bus. The ADDR<2:0> bus is used for addressing the proper registers for loading the configuration data and sample vectors for modulation. ADDR2 is the MSB.
INTREQ	O	Tri-statable Active High Interrupt Request Output. The INTREQ output is enabled via register 2 bit-8. Register 9 bits 6-0 enable individual events for INTREQ.
RESET		While the $\overline{\text{RESET}}$ input is asserted (driven low), all processing halts and the WPM is reset. A software reset is also available via register 10_H.
IOUT<13:0>	O	Tri-statable In-Phase Output Samples. IOUT<13:0> outputs are enabled via register 2 bit-7.
QOUT<13:0>	O	Tri-statable Quadrature Output Samples. QOUT<13:0> outputs are enabled via register 2 bit-6. The QOUT<13:0> outputs are not available on the MQFP package.
FEMPT, FOVRFL, FFULL	O	Tri-statable Status Flags for FIFO Level Monitoring. These outputs are enabled via register 2 bits 13-11. FIFO status thresholds and control are configured via register 2 bits 23-16.
LOCKDET	O	Tri-statable Status Flag of the Digital PLL. This may be used to generate an interrupt request via INTREQ. The LOCKDET output is enabled via register 2 bit-10.
IOUTA, QOUTA	O	Current Outputs of the Device. Full scale output current is achieved when all input bits are set to binary 1.
IOUTB, QOUTB	O	Complementary Current Outputs of the Device. Full scale output current is achieved on the complementary outputs when all input bits are set to binary 0.

Pin Descriptions (Continued)

NAME	TYPE	DESCRIPTION
ICOMP1, QCOMP1	I	Compensation Pin for use in Reducing Bandwidth/Noise. Each pin should be individually decoupled to AVDD with a 0.1µF capacitor. To minimize crosstalk, the part was designed so that these pins must be connected externally, ideally directly under the device packaging. The voltage on these pins is used to drive the gates of the PMOS devices that make up the current cells. Only the ICOMP1 pin is driven and therefore QCOMP1 needs to be connected to ICOMP1, but de-coupled separately to minimize crosstalk.
ICOMP2, QCOMP2	I	Compensation Pin for Internal Bias Generation. Each pin should be individually decoupled to AGND with a 0.1µF capacitor. The voltage generated at these pins represents the voltage used to supply 2.0V nominal power to the switch drivers. This arrangement helps to minimize clock feedthrough to the current cell transistors for reduced glitch energy and improved spectral performance.
REFLO	I	Reference Low Select. When the internal reference is enabled, this pin serves as the precision ground reference point for the internal voltage reference circuitry and therefore needs to have a good connection to analog ground to enable internal 1.2V reference. To disable the internal reference circuitry this pin should be connected to AVDD.
REFIO	I	Reference voltage input if internal reference is disabled. Reference voltage output if internal reference is enabled. Use 0.1µF cap to ground when internal reference is enabled.
FSADJ	I	Full Scale Current Adjust. Use a resistor to ground to adjust full scale output current. Full Scale Output Current = 32 x V_{FSADJ}/R_{SET}. Where V_{FSADJ} is the voltage at this pin. V_{FSADJ} tracks the voltage on the REFIO pin; which is typically 1.2V if the internal reference is used.
RESV	-	Reserved. These pins must be floating (not connected) for proper operation.
NC	-	No Connection. Pins may be connected to GND, AGND, DGND or left floating.

Functional Description

The HSP50415 is a wideband programmable modulator that accepts an input quadrature data stream at programmable symbol rates of up to 25MSPS (QPSK) and outputs a modulated quadrature data stream at the final sample rate up to 100MHz. The allowable symbol rates depend on the modulation type selected (QPSK, 16QAM, etc.). The input data format is parallel with respect to the bits, but serial with respect to the I and Q samples and may be input at a constant symbol rate or burst in at a different rate. The HSP50415 can symbol map the input data stream per a user programmable look up table thus allowing any standard to be supported. The mapped symbols are then interpolated to the final sample rate and low-pass filtered in order to limit the spectral occupancy of the signal. The first stage filter coefficients are user programmable, with subsequent filter stages having fixed coefficients. The HSP50415 then modulates the symbol data at the final sample rate onto a carrier signal that is tunable from 0.023Hz - 50MHz (for a final sample rate of 100MHz) producing a quadrature signal. The signal may then be optionally X/SIN(X) filtered to compensate for the SIN(X)/X roll-off of the DACs. To correct for system (or DAC induced) gain imbalances between the In phase and Quadrature signals there is a final gain correction stage prior to the output. The final Intermediate Frequency (IF) digital output can be converted to differential analog signals via the onboard 12-bit DACs or may be optionally brought out as 14-bit digital data. The 100-pin MQFP package provides a real digital output at 1/2 the final sample rate.

System CLK Generation

The HSP50415 receives I and Q input data serially at twice the input symbol rate. The data is converted to a parallel quadrature data stream at the symbol rate by the Front End Data Input Block. This data stream is upsampled to the final output sample rate of the device (FSout). This output sample rate (maximum rate of 100MHz) is used to clock the last stage of the digital logic and the dual 12-bit DACs and may be provided externally on the CLK pin or may be generated by an internal analog PLL (APLL). When enabled, the APLL uses the CLK pin as a reference and provides a selectable CLK multiplier of x2, x4, x8, x16 or x32 or CLK divider of /2, /4 or /8.

An external loop filter is required to be supplied at PLLRC. The recommend configuration is shown in Figure 1, with suggested component values calculated as:

User Input Terms:
APLLclkdivider=APLL CLK divider programmed input
APLLvcodivider=APLL VCO divider programmed input
Fclk=CLK frequency input
Fscale=loop bandwidth divisor input
Pm=loop phase margin input (degrees)

Component calculation formulas:
C1=(Fvcogain*Icp)/(wo*wo*sqrt(kk))
C2=kk*C1
R1=1/sqrt(Fvcogain*Icp*C1*sqrt(C2/C1))

Where:
Fvcogain=231000000/APLLvcodivider
Icp=0.000353
kk=(1+(sin(Pm*pi/180)))/(1-(sin(Pm*pi/180)))
wo=2*pi*((Fclk/APLLclkdivider)/Fscale)

A MATLAB or Excel program for calculating the component values is available. For improved APLL performance, utilization of specific calculated values is recommended over the general purpose ones shown in Figure 1.

Symbol NCO

As the data flows through the device, the sample rate increases up to the final sample rate, with the SYMBOL NCO generating all of the necessary intermediate sample rate clocks. Each stage's input and output sample rate is dependent on the interpolation rate through the stage. Figure 1 shows the various symbol clocks that are generated on the chip. The symbol rate clock (symclk) used internally is multiplied by 2 and output on pin 2XSYMCLK for use in driving the input DATACLK if a symbol rate synchronous (non-burst) mode is required.

The SYMBOL NCO is a 32-bit accumulator. The 32-bit frequency step (Phinc) is the sum of the user programmable 32-bit symbol Phinc and any error term generated by the Digital Phase Lock Loop (DPLL) while locking to an external symbol rate. The DPLL error term may be disabled by a control bit. The symbol rates supported are from 0.023Hz up to 25MHz (for FSout of 100MHz) with 32-bit frequency resolution. The formula for programming the symbol Phinc register is given as:

symbolPhinc = (symbolRate / FSout) * 2^32

The SYMBOL NCO also has a counter mode in which the symbol clocks are generated upon the counter reaching the 16-bit user programmable rollover count value. This mode is useful for cases where the frequency is an integer number of the system clock (SYSCLK/2).

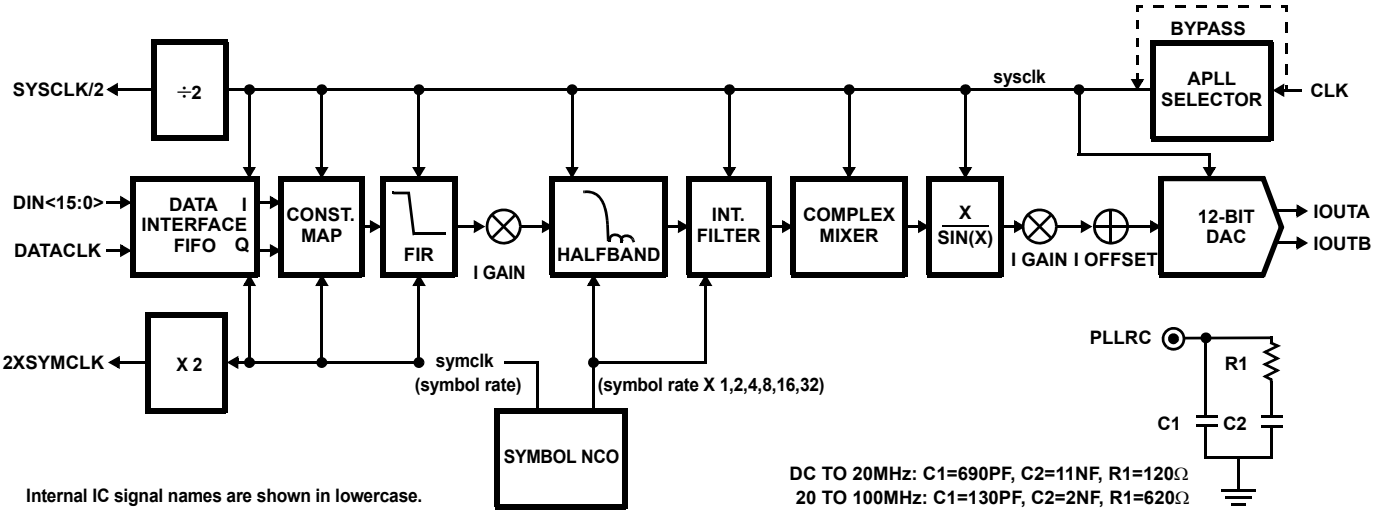


FIGURE 1. SAMPLE RATE CLK GENERATION

TABLE 1. HSP50415 FILTER CONFIGURATIONS AND RESULTING SYMBOL NCO RATES

BYPASS FIR FILTER	FIR INTERPOLATION	BYPASS HALFBAND FILTER	INTERPOLATING FILTER DATA INPUT RATE	SYMBOL NCO PHINC
0	x2 (Note)	0	Symbol Rate x 4	PhincLL x 4
0	x4	0	Symbol Rate x 8	PhincLL x 8
0	x8	0	Symbol Rate x 16	PhincLL x 16
0	x16	0	Symbol Rate x 32	PhincLL x 32
0	x2 (Note)	1	Symbol Rate x 4	PhincLL x 4
0	x4	1	Symbol Rate x 4	PhincLL x 4
0	x8	1	Symbol Rate x 8	PhincLL x 8
0	x16	1	Symbol Rate x 16	PhincLL x 16
1	Not applicable	0	Symbol Rate x 2	PhincLL x 2
1	Not applicable	1	Symbol Rate x 1	PhincLL x 1

NOTE: An optional decimate by two mode allows the device to achieve interpolation by a factor of two in the Shaping FIR.

The SYMBOL NCO 32-bit Phinc value is adjusted automatically such that the SYMBOL NCO runs at the input rate of the interpolating filter, since this is the fastest rate prior to the FSout rate. Table 1 lists possible filter configurations of the HSP50415 and the resulting interpolating filter rate. This resulting rate is affected by rate adjustments (interpolation) in the previous filter blocks.

Digital Phase Lock Loop

The HSP50415 contains a Digital Phase Lock Loop (DPLL) that performs symbol tracking to an external symbol clock (REFCLK). The DPLL consists of a programmable phase/frequency error detector followed by a loop filter and lock detector stage. The phase/frequency error detector block diagram is shown in Figure 2.

The DPLL uses two (integer) counters to give added frequency programming flexibility. The programmed symbol rates are functions of the both the REFCLK divider and the NCO divider (N = NCO divider + 1, see Figure 2), each of which can be changed separately. As an example, these two counters can be set to generate a non-integer output (NCO Symbol rate) frequency (16/3) of the input reference frequency (REFCLK). In this case NCO divider = 16, and REFCLK divider =3. If REFCLK is the desired symbol rate, then the REFCLK divider will be the same value as the NCO divider. If REFCLK is for example 2x the desired symbol rate, then the refClk divider will be 2x the NCO divider. REFCLK is divided down by the REFCLK divider. The internal symbol clk is divided down by the NCO divider. When the carry-out of the REFCLK divider is generated, the symbol NCO is sampled. The phase and frequency (dphi/dt) should be zero if the two rates are phase and frequency locked. If not, the sampled phase value is the phaseError. This value is subtracted from the previous phaseError to generate the frequency error. Both of these error terms are input to the loop filter which scales and integrates these error terms and produces a final symbol nco error term. This final error term gets added to the SYMBOL NCO to adjust the symbol rate to try to track to the divided down external REFCLK input. The loop filter error term must be enabled in the software for this error term to be added to the symbol NCO. Otherwise the Digital PLL has no effect on the symbol rate.

The minimum value the REFCLK divider and NCO divider values may be programmed to is the larger of 32/clkDivisor or 0x04, where clkDivisor is FSout/REFCLKrate. This is due to the minimum number of system clock (SYSCLK/2) cycles the loop filter requires to process the new error terms. The maximum rate of this clock is FSout/4 or 25MHz for FSout of 100MHz. The phaseError and freqError terms are input to the loop filter block which is a standard lead/lag type second order loop filter as shown in Figure 3. The loop filter requires 32 clock cycles to process a new error term.

The phaseError is weighted by the lag gain and added to the freqError weighted by the frequency gain and this sum is accumulated to give the integral response. The lag accumulator is compared to upper and lower limits and forced to the limit value if either limit is exceeded. This keeps the SYMBOL NCO frequency within the expected symbol rate uncertainty and limits the pull in range. This accumulator output is then added to the phaseError weighted by the lead gain to get a proportional response. This lead term should be zeroed during initial tracking. The gain values are user programmable with a mantissa and exponent of the following format

Gain = 01.MMMM * 2^(EEEEE-17)

where MMMM denotes the 4-bit gain value and EEEEE is the 5-bit shift value.

The phaseError and freqError signals may be monitored on the digital outputs for test or the lock detect pin may be used to monitor the symbol tracking phase error. The lock detect pin indicates whether the DPLL has phase locked to the external symbol clock. The lock detect status may also be used to generate an interrupt event. The lock detect block diagram is shown in Figure 4.

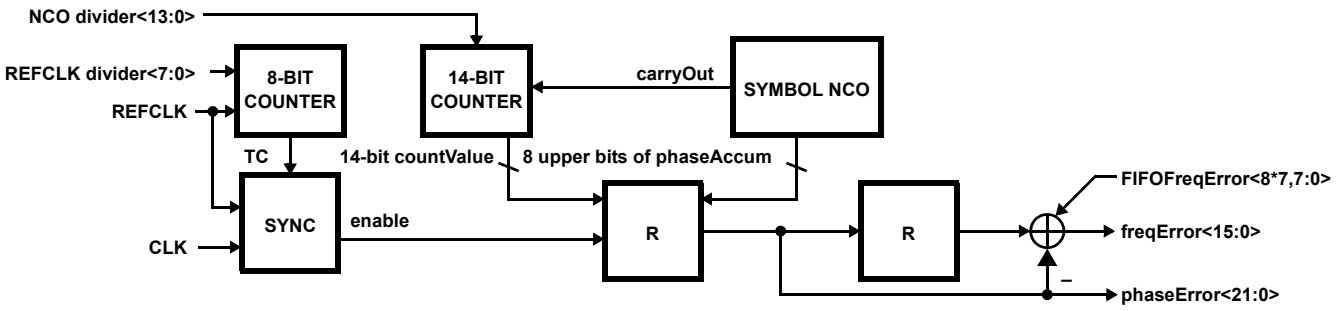


FIGURE 2. PHASE/FREQUENCY ERROR DETECTOR

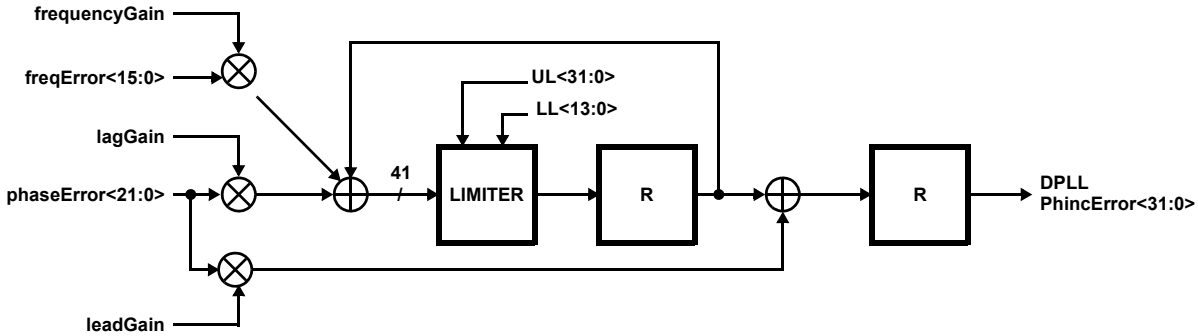


FIGURE 3. DPLL LOOP FILTER

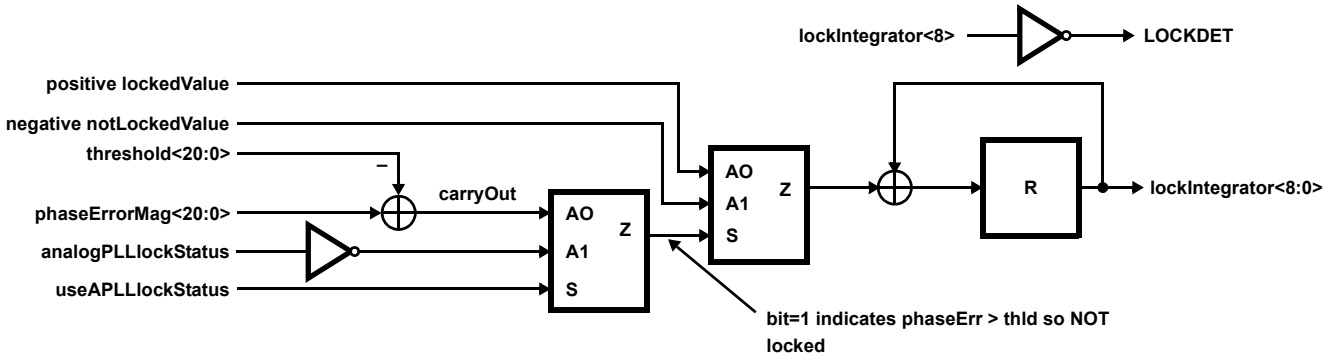


FIGURE 4. LOCK DETECTION BLOCK DIAGRAM

The Lock Detector compares the magnitude of the phaseError to a programmable 21-bit threshold value. If the carry out from this comparison is “1” then the phaseError is greater than or equal to the threshold value and a negative value is added to the lock integrator. If the carry out is “0” then the phaseError is less than the threshold and a positive value is added. As the phaseError magnitude stays below the threshold level the lock integrator will grow from a negative number to a positive one thus indicating a locked condition. The lock integrator resets to a full-scale negative value. The sign bit of the lock integrator is output as the LOCKDET status flag. The values added or subtracted to the lock integrator are user selectable as follows in Table 2.

TABLE 2. LOCK INTEGRATOR ADDENDS

LOCK FACTOR	CARRY OUT	ADDEND	BINARY VALUE
0xx	1	-0.5	111111000
1xx	1	-0.25	111111100
x00	0	+0.0625	000000001
x01	0	+0.1250	000000010
x10	0	+0.2500	000000100
x11	0	+0.5000	000001000

Front-End Data Input Block

The HSP50415 accepts input data in a parallel bit fashion with I and Q samples input serially as shown in Figure 5. The signal pins on the device that input data to the front-end are the DIN<15:0> bus, the ISTRB and TXEN control pins and the DATACLK pin.

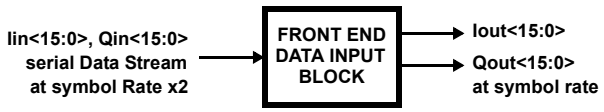


FIGURE 5. SERIAL TO PARALLEL DATA CONVERSION

All data is synchronous to the DATACLK. Further references to bit-widths will be with respect to a single channel (I and Q channels are identical). The input data may be from 1-bit up to 16-bits wide with bits positioned on the LSB's of the bus. The data samples are input as I then Q serially with the ISTRB pin active with the I sample. The maximum data rate is 50MHz at FSout of 100MHz or twice the maximum symbol rate. The data written into the chip may be gated with the TXEN pin (burst Mode) or input free-running. The ISTRB and TXEN pins have user-programmable active states thus allowing spectral inversion to be implemented by simply changing the ISTRB polarity. Figure 6 shows the input data timing (assuming the ISTRB pin is an active high).

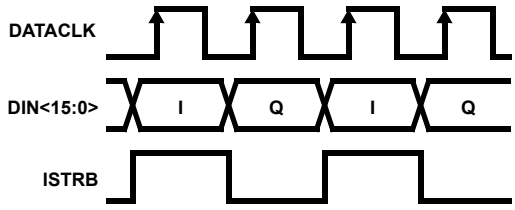


FIGURE 6. I/Q INPUT DATA TIMING

Once a valid pair of I and Q samples has been received, the data pair is written into the 256x32-bit FIFO. The data is read out of the FIFO at the symbol rate using the internally generated symbol clock which is synchronous to the clock pin. This internally generated symbol clock is available on the 2XSYMCLK pin of the chip. It has been multiplied up to twice the symbol rate to facilitate tying it to the DATACLK pin in symbol rate synchronous modes. The data is always input to the chip at twice the rate at which it is written to the FIFO since I and Q are input serially. In a symbol rate synchronous mode, the data is input to the front-end at twice the symbol rate, written to the FIFO at the symbol rate and read from the FIFO also at the symbol rate. This mode ensures that no FIFO overflow or underflow conditions will occur. Optionally, in a totally synchronous mode, the FIFO may be bypassed altogether if power conservation is critical.

Reading data out of the FIFO for transmission may be optionally gated by the TXEN pin if the user wishes to burst the data into the chip and delay transmission of the data. If the data reads are not gated, then after 2 FIFO locations have been written, data reads are initiated. Via user-programmable bits, the data may be zeroed leaving the front-end if the FIFO runs out of data or in gated-read mode, if the TXEN pin is inactive. Conversely, writing data into the FIFO may be optionally disabled upon a FIFO full condition. Control of the starting address for the gated reads is user-programmable where the address may be zeroed upon start of transmission or simply incremented from where it left off on the last transmission.

The FIFO logic contains user programmable threshold detection (high and low thresholds) as well as full/empty detection. There are 4 status flags available to the user for FIFO level monitoring: FIFOOverFlow (FOVRFL), FIFOFull (FFULL), FIFOUnderFlow, and FIFO empty (FEMPT). These status flags may be monitored via 3 output pins: the underflow and empty share one pin with a user selectable function. Any one of these flags may be used to trigger an interrupt on the INTREQ pin if the mask register for that status bit is set. A rising edge of the status signal will set the interrupt status register bit and cause an external interrupt if enabled. The only way to clear the status bit and INTREQ pin is to write a "1" to the corresponding status register bit.

Another feature of the FIFO is the adaptive symbol rate control logic. The internal symbol rate of the device is controlled by the digital PLL if enabled. Since the data is read out of the FIFO at the internal symbol rate, there may arise a need for the FIFO to adjust the symbol rate if the data is not being written in and read out at the same rate. This is achieved by either adding or subtracting a frequency error term to the digital PLL's loop filter frequency term or by forcing the loop filter lag term to its programmed limit. If a FIFO overflow occurs, then the data is being written into the FIFO faster than it is being read out, which indicates the symbol rate needs to be increased thus speeding up the reads. This scenario would cause the FIFO to try to increase the final symbol rate error term by either adding the FIFO frequency error term (user programmable) to the loop filter's frequency error term or force the loop filter lag accumulator to its programmed upper limit. If a FIFO underflow occurs, then the data is being read out of the FIFO faster than it is being written in and the FIFO would attempt to slow down the symbol rate by subtracting the frequency error term or by forcing the lag accumulator to its lower limit. This adaptive rate control is user programmable via Register 2 bits 21:20.

Constellation Mapper

The I/Q data pair from the Front End Input Block enters the constellation mapper at the internal symbol rate and is mapped via a user programmable look up table to new symbol data. The symbol mapping is only supported for I/Q bit widths of 4-bits (256-QAM) or less. The I data is concatenated with the Q data to form the 8-bit address (Iin<3:0>:Qin<3:0>) to the 256x8-bit RAM. The 8-bit data output from the RAM is the new symbol data in the form

Iout<3:0>:Qout<3:0>. See Figure 7 for a constellation mapping example. For bit widths less than 4-bits the data in the RAM may simply be zero's for the unused bit positions and the unused addresses since the HSP50415 will discard the unused bits. For example, if the user programs the number of bits to be 1 and the upper bits of the DIN<15:0> bus are tied to "0", the user need only program addresses 0, 1, 16 and 17 since the other addresses will never be selected. In this example, the only data that is used will be memory address bits 4 and 0 since these map to I<0> and Q<0> respectively. For data bit widths larger than 4 bits or if mapping is not required, the constellation mapper may be bypassed.

Shaping FIR Filters

Following the constellation mapping, the I/Q data pair is input to the programmable FIR filters for the first stage of interpolation. The interpolating FIR filters' have programmable coefficients and must be loaded via the microprocessor interface. The I and Q filter stages are identical and may be loaded simultaneously or separately thus allowing for different gains and responses through the FIR filter if desired. The loading options are programmable including readback modes and will be discussed in detail in the 'Microprocessor Interface' section. Since the hardware for the I and Q filters is identical, further discussion will pertain to a single channel.

The basic interpolation rates allowed through the FIR are x4, x8 or x16. An optional decimate by 2 mode is available that subsamples the output of the filter thus reducing the interpolation rate by a factor of 2. Each filter multiplication is implemented as a series of shifts and adds thus constraining the maximum input symbol rate as follows:

symbolRateMax is the smaller of:

(CLK * 2 * 2^twoBitMode) / (#bits * interpolationRate)

and CLK/4

where CLK is the final sample rate clock (100MHz max), #bits is the data bit width of a single channel and twoBitMode is a special processing mode where 2-bits at a time are computed. The gain through the filter is:

A = (sum of coefficients) / interpolation rate

The FIR filter contains saturation logic in the event that the final output peaks over 1.0. Table 3 outlines the filter characteristics for the various interpolation rates.

TABLE 3. FIR FILTER CHARACTERISTICS

2-BITMODE	INTERP. RATE	SYMBOL SPAN	# FILTER TAPS
0	x4	24	96
0	x8	20	160
0	x16	16	256
1	x4	12	48
1	x8	10	80
1	x16	8	128

The programmable coefficients are stored in RAM as bit-sliced sums of products.

The data exits the interpolating FIR filters as a parallel I<15:0> and Q<15:0> data stream at the interpolated sample rate. These filters may be totally bypassed if higher input symbol rates are required. When bypassed, the RAMs may be loaded with all zeros for power conservation.

Post FIR Gain Control

Following the FIR filter pair is a gain stage where I and Q are scaled equally. The programmable gain consists of a 6-bit mantissa and a 4-bit exponent stage. The equation for the gain is as follows:

dataOut<15:0> =
(dataIn<15:0> * 1.MMMMMM) * 2 ^ (EEEE - 11)

where MMMMMM denotes the 6-bit gain value and EEEE is the 4-bit shift value.

For a gain of 1.0 through this stage, program the mantissa to 0x00 and the exponent to 0xB. This stage is implemented with a signed 16-bit by unsigned 7-bit multiplier with the

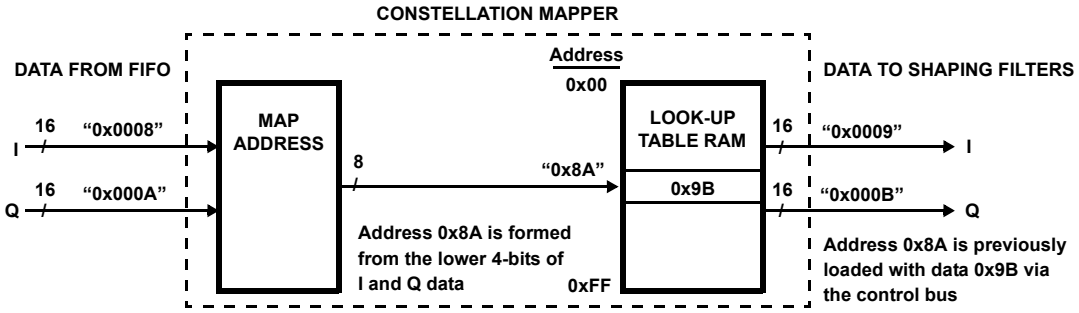


FIGURE 7. CONSTELLATION MAPPING

resulting 23-bit output rounded at bit position 5 (multOut<5>) to 17-bits. The extra bit is carried to check for overflow at the output of the shifter. The output of the multiplier (multOut<22:6>) is then shifted to the appropriate position per the exponent bits with a shift value of 0xB positioning the data at the top of the shifter. The final shifted output is then checked for saturation and limited to 16-bits before being output.

Fixed Coefficient 19-TAP Interpolating Halfband

Following the post-FIR gain stage is a pair of fixed coefficient 19-tap interpolate by 2 halfband filters. The halfband filter may be totally bypassed if not required. If bypassed, the data to the filter is zeroed which reduces power consumption. The halfband filter coefficients are:

1, 0, -17, 0, 87, 0, -299, 0, 1252, 2048, 1252, 0, -299, 0, 87, 0, -17, 0, 1

The interpolate by 2 is accomplished via zero-stuffing and low-pass filtering. The output of this filter is rounded to 16-bits. The output is checked for saturation and limited if necessary. The data exits the halfband filters as a parallel I<15:0> and Q<15:0> data stream at the interpolated sample rate. Figure 8 shows the frequency response of the Half-Band filter.

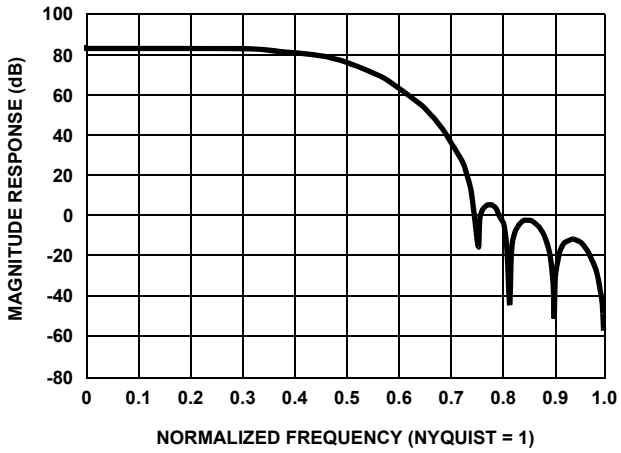


FIGURE 8. HALF-BAND FREQUENCY RESPONSE

Interpolating Filter

Following the halfband stage, the data enters the last stage of interpolating filters. Again, the I and Q filters are identical so the subsequent discussion will refer to a single channel. The data is input to the interpolating filter at this stage's input sample rate which is dependent on the previous stage's interpolation rate. At this stage the input sample rate clock is generated by the SYMBOL NCO. For every output sample generated, there is a 12-bit phase value that is also generated in the SYMBOL NCO (the top 12-bits of the phase accumulator). The Interpolator uses this phase value to compute output samples at the output sample rate (FSOUT) which is the final output sample rate of the chip. The nulls in the interpolation filter frequency response align with the interpolation images of the shaping filter. Input to this stage should be no greater than -2dB fullscale to prevent overflow. The impulse response of the Interpolation filter is shown in Figures 9 through 11 for an interpolate by 16 filter (the interpolation ratio, L, is equal to 16). This block may be bypassed if desired. Figures 12 through 17 depict the response for varying interpolation ratios.

Typical Performance Curves

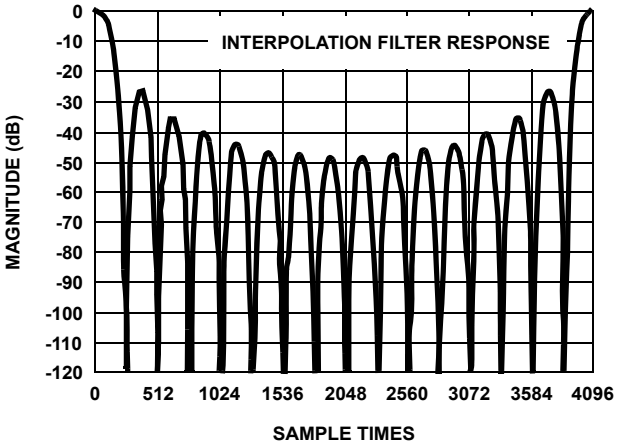


FIGURE 9. RESPONSE FOR L = 16; FOUT = 4096

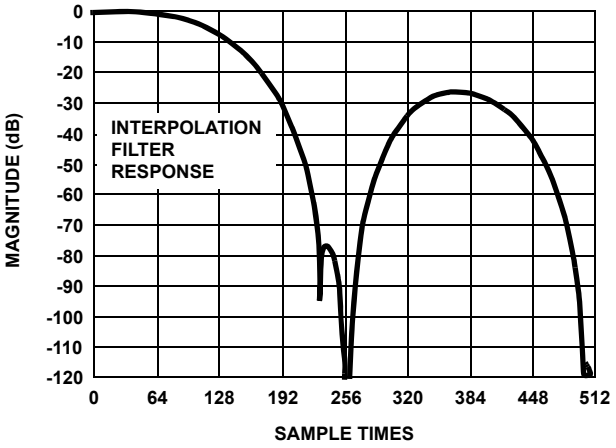


FIGURE 10. RESPONSE FOR L = 16, FOUT = 4096

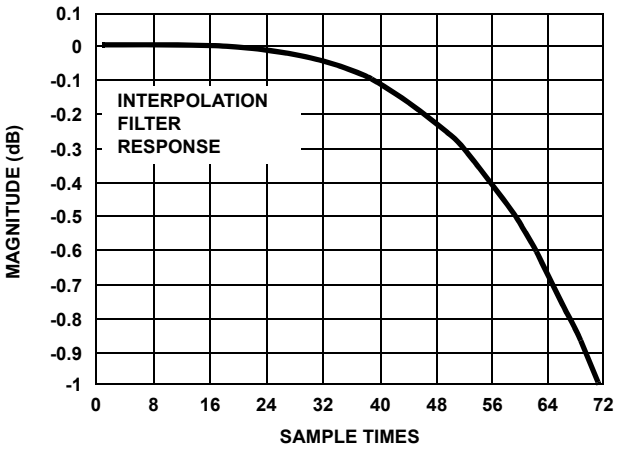


FIGURE 11. RESPONSE FOR L = 16; FOUT = 4096

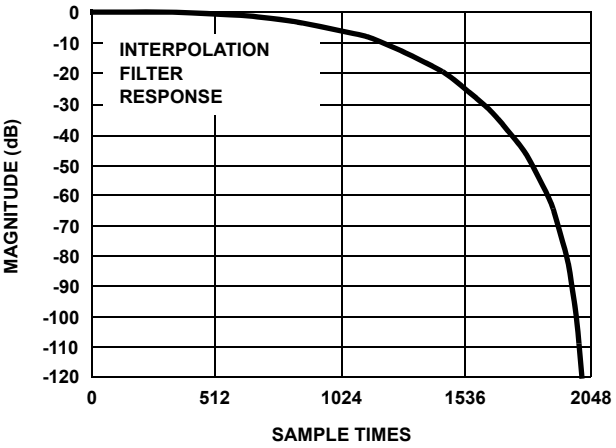


FIGURE 12. RESPONSE FOR L = 2; FOUT = 4096

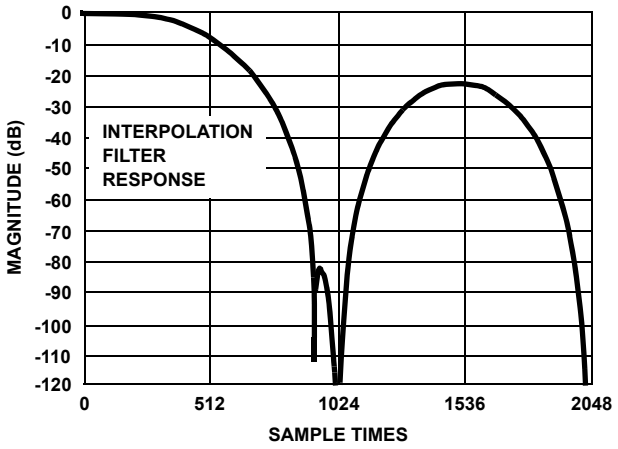


FIGURE 13. RESPONSE FOR L = 4; FOUT = 4096

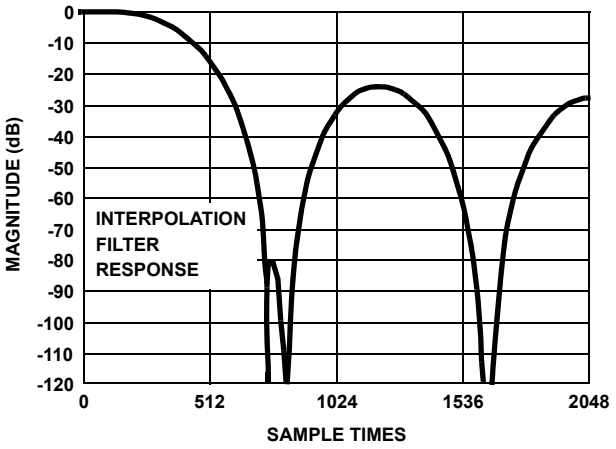


FIGURE 14. RESPONSE FOR L = 5; FOUT = 4096

Typical Performance Curves (Continued)

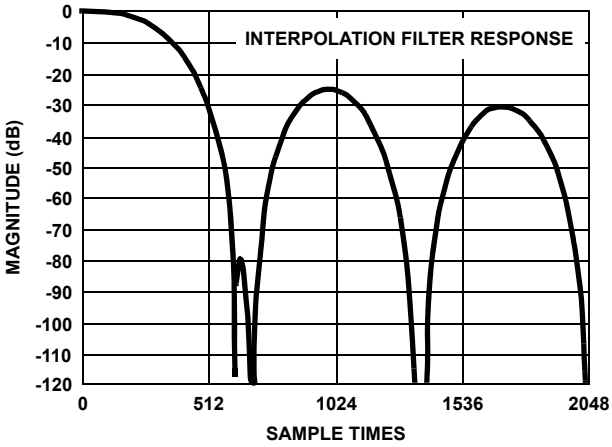


FIGURE 15. RESPONSE FOR L = 6; FOUT = 4096

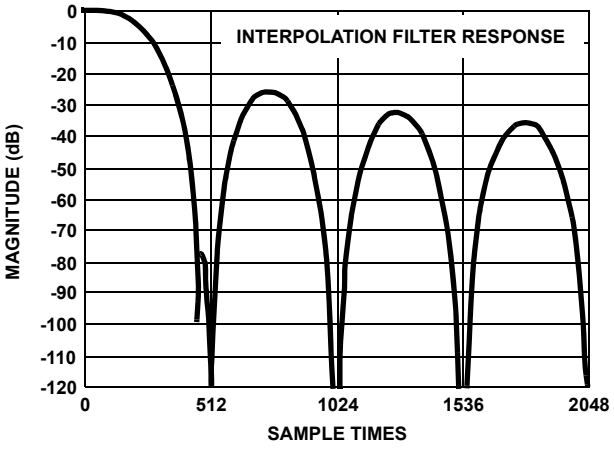


FIGURE 16. RESPONSE FOR L = 8; FOUT = 4096

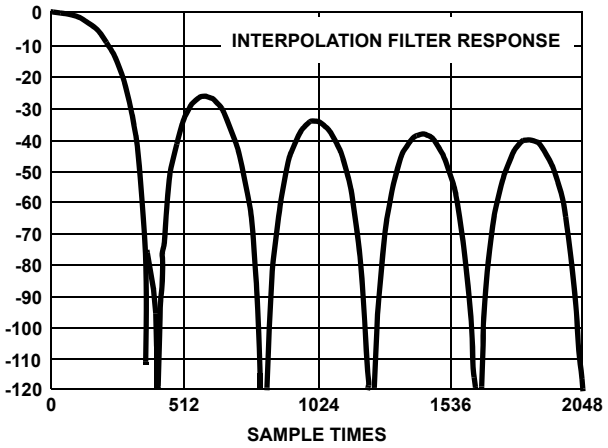


FIGURE 17. RESPONSE FOR L = 10; FOUT = 4096

Carrier NCO and Complex Mixer

Following the interpolating filter is the complex mixer stage where the quadrature data is modulated onto a carrier signal via a complex multiply operation resulting in a quadrature output sample. The carrier NCO has a 32-bit programmable frequency increment value which is programmed as follows:

carrierPhinc = (carrierFrequency / FSout) * 2^32

The frequency may be positive or negative with a range from -50 to +50MHz (for FSout of 100MHz). The phase adder and accumulator are also 32-bits wide.

X/SIN(X) Compensation Filters

Following the complex mixer stage is a pair of fixed coefficient 11-tap X/SIN(X) compensation filters. The X/SIN(X) filter performs peaking to compensate for the SIN(X)/X rolloff that occurs at the output of the DACs. These filters may be totally bypassed if not required. The X/SIN(X) filter coefficients are:

-1, 2, -4, 10, -34, 384, -34, 10, -4, 2, -1

The output is rounded to 16-bits. The output of the filter is not checked for saturation since the maximum sum of products is 486/512 (0.949) and overflow will never occur. The data exits the X/SIN(X) filters as a parallel I<15:0> and Q<15:0> data streams at the final sample rate. Figure 18 plots of the inverse sinc function, sinc function, and the effect of compensation.

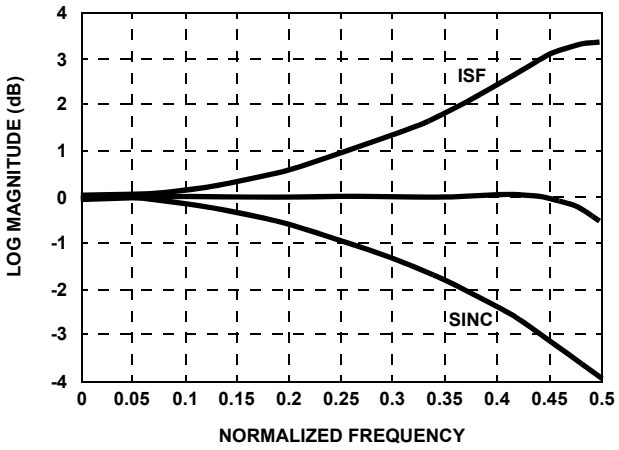


FIGURE 18. X/SIN(X) FILTER RESPONSE

I/Q Gain Imbalance Correction Stage

Following the X/SIN(X) filter pair is a gain stage where I and Q are scaled independently. The programmable gain consists of a 10-bit scale factor and a 10-bit DC offset. The equation for the gain is as follows:

dataOut<15:0> = (dataIn<15:0> * (1.0 +/- 0.00SSSSSSSSSS)) +/- 0.00DDDDDDDDDD

Where SSSSSSSSSS denotes the 10-bit scale factor and DDDDDDDDDD is the 10-bit DC offset value. The scale factor may be optionally added or subtracted from 1.0 and the DC offset may optionally be added or subtracted to the result of the scale operation.

For a gain of 1.0 through this stage, program the scale factor to 0x000 and the DC offset to 0x000 for both the I and Q values. The output is rounded to either 14-bits or 12-bits. The rounding options are programmable as shown in Table 4.

TABLE 4. IQ GAIN CORRECTION STAGE ROUNDING OPTIONS

RNDBITS<1:0>	ROUND SELECTION
00	No rounding performed, data is truncated
01	Round to 14-bits
10	Round to 12-bits
11	Round in both positions

If saturation does occur, the output is symmetrically limited.

Digital to Analog (D/A) Converters

The HSP50415 outputs using dual 12-bit, 150MSPS, high speed, low power, D/A converters. The converter provides 20mA of full scale output current and includes edge-triggered CMOS input data latches. Low glitch energy and excellent frequency domain performance is achieved by the DACs segmented current source architecture.

Voltage Reference

The internal voltage reference of the device has a nominal value of + 1.2V with a $\pm$10ppm/^{o}C drift coefficient over the full temperature range of the converter. It is recommended that a 0.1μF capacitor be placed as close as possible to the REFIO pin, connected to the analog ground. The REFLO pin selects the reference. The internal reference can be selected if REFLO is tied low (ground). If an external reference is desired, then REFLO should be tied high (the analog supply voltage) and the external reference driven into REFIO. The full scale output current of the converter is a function of the voltage reference used and the value of R_{SET}. I_{OUT} should be within the 2mA to 20mA range, though operation below 2mA is possible, with performance degradation.

V_{FSADJ} and V_{REFIO} will be equivalent except for a small offset voltage. If the internal reference is used, V_{FSADJ} will equal approximately 1.2V on the FSADJ. If an external reference is used, V_{FSADJ} will equal the external reference. The calculation for I_{OUT}(Full Scale) is:

I_{OUT}(Full Scale) = (V_{FSADJ}/R_{SET}) X 32.

If the full scale output current is set to 20mA by using the internal voltage reference (1.2V) and a 1.91kΩ R_{SET} resistor, then the input coding to output current is shown in Table 5.

TABLE 5. INPUT CODING vs OUTPUT CURRENT

INPUT CODE <D11-D0>	I/QOUTA (mA)	I/QOUTB (mA)
11 11111 11111	20	0
10 00000 00000	10	10
00 00000 00000	0	20

Outputs

The 5 MSBs for each DAC on the HSP50415 drive a thermometer decoder**,** which is a digital decoder that has a 5-bit binary coded input word with 2^5-1 (or 31) output bits, where the number of output bits that are active correlate directly to the input binary word. The HSP50415 uses a thermometer decoder to significantly minimize the output glitch energy for each DAC. I/QOUTA and I/QOUTB are complementary current outputs. The sum of the two currents is always equal to the full scale output current minus one LSB. If single ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be either grounded or equally terminated. The voltage developed at the output must not violate the output voltage compliance range of -0.3V to 1.25V. R_{LOAD} (the impedance loading each current output) should be chosen so that the desired output voltage is produced in conjunction with the output full scale current. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage equation is:

$V_{OUT} = I_{OUT}$ X R_{LOAD}.

These outputs can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. The SFDR measurements in this data sheet were performed with a 1:1 transformer on the output of the DAC (see Figure 19). With the center tap grounded, the output swing of I/QOUTA and I/QOUTB will be biased at zero volts. The loading as shown in Figure 19 will result in a 500mV signal at the output of the transformer if the full scale output current of the DAC is set to 20mA. $V_{OUT} = 2 \times I_{OUT} \times R_{EQ}$, where R_{EQ} is ~12.5Ω.

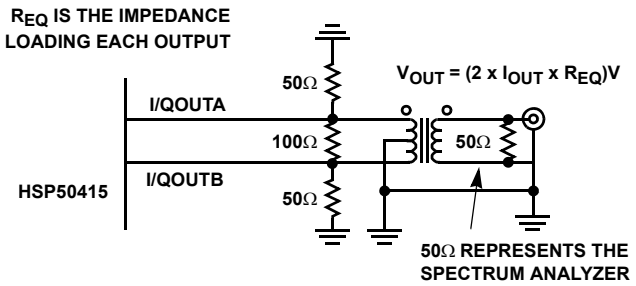


FIGURE 19. DAC OUTPUTS

Allowing the center tap to float will result in identical transformer output, however the output pins of the DAC will have positive DC offset. Since the DACs output voltage compliance range is -0.3V to +1.25V, the center tap may need to be left floating or DC offset in order to increase the amount of signal swing available. The 50Ω load on the output of the transformer represents the spectrum analyzer's input impedance.

Definition of DAC Specifications

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Full Scale Gain Drift, is measured by setting the data inputs to be all logic high (all 1s) and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (full scale range) per ^{o}C.

Full Scale Gain Error, is the error from an ideal ratio of 32 between the output current and the full scale adjust current (through R_{SET}).

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Internal Reference Voltage Drift, is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm per ^{o}C.

Offset Drift, is measured by setting the data inputs to all logic low (all 0s) and measuring the output voltage through a known resistance as the temperature is varied from T_{MIN} to T_{MAX}. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either T_{MIN} or T_{MAX}. The units are ppm of FSR (full scale range) per degree ^{o}C.

Offset Error, is measured by setting the data inputs to all logic low (all 0s) and measuring the output voltage through a known resistance. Offset error is defined as the maximum *deviation* of the output current from a value of 0mA.

Output Settling Time, is the time required for the output voltage to settle to within a specified error band measured from the beginning of the output transition. The measurement is done by switching quarter scale. Termination impedance was 25Ω due to the parallel resistance of the 50Ω loading on the output and the oscilloscope's 50Ω input. This also aids the ability to resolve the specified error band without overdriving the oscilloscope.

Output Voltage Compliance Range, is the voltage limit imposed on the output. The output impedance should be chosen such that the voltage developed does not violate the compliance range.

Reference Input Multiplying Bandwidth, is defined as the 3dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs set to all 1s. The frequency is increased until the amplitude of the output waveform is 0.707 (-3dB) of its original value.

Microprocessor Interface

The HSP50415 is highly configurable with 16 writable/readable control registers and four addresses reserved for generating internal control signals. The microprocessor interface (uPI) is a parallel bus type with the following device pins being used for I/O: CDATA<7:0>, ADDR<2:0>, $\overline{CE}$ and $\overline{RD}$. These device pins are synchronous to the WR pin which is actually the clock for the uPI logic. Data is written to control words by writing to a sequence of address locations with the data present on the CDATA<7:0> bus. The uPI contains a 32-bit master register which is first loaded with the control word data one byte at a time, then downloaded to a slave register that is synchronous to the digital core clock (SYSCLK/2). The sequence of writes necessary to program control word 12, for example, with the value 0xAABBCCDD would be as shown in Table 6 and Figure 20.

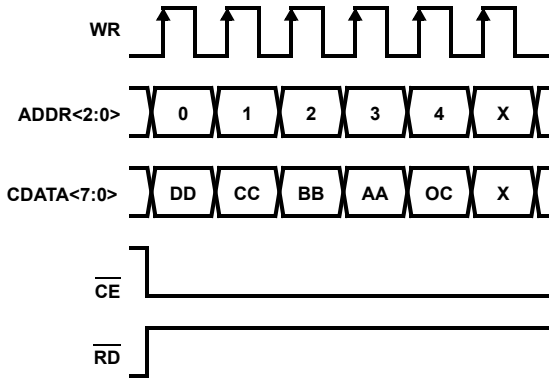


FIGURE 20. CONTROL REGISTER LOADING SEQUENCE

There should be at least 4 digital core clock cycles between writing to address 4 and reloading the MasterReg as the data from the MasterReg is being downloaded to slave registers synchronous to the core clock cycles and synchronization circuitry is required. The frequency of the WR pin may not exceed CLK/4 (25MHz max for CLK of 100MHz). To readback the value in control word 12, the following sequence of writes/reads shown in Table 7 should occur. Note that the $\overline{RD}$ pin is the Three-State control for the CDATA<7:0> bus with a logic 1 on the $\overline{RD}$ pin disabling the output drivers configuring the pins as inputs and a logic 0 on the $\overline{RD}$ pin enabling the output drivers making the pins outputs. The $\overline{CE}$ pin must be active for any read or write to the device to be processed. The ADDR<2:0>, CDATA<7:0> and $\overline{CE}$ pins when writing to the device ($\overline{RD}$=1) are synchronous to the WR pin, but when reading ($\overline{RD}$=0), the ADDR<2:0> and $\overline{CE}$ pins are not synchronous to the WR pin, and are actually mux controls to determine which byte of the read data is output on the CDATA<7:0> bus.:

TABLE 6. SEQUENCE OF WRITES TO LOAD CNTLWORD12

ADDR<2:0>	CDATA<7:0>	CE	RD	WR	INTERNAL OPERATION
0	0xDD	0	1	1	write to MasterReg<7:0>
1	0xCC	0	1	1	write to MasterReg<15:8>
2	0xBB	0	1	1	write to MasterReg<23:16>
3	0xAA	0	1	1	write to MasterReg<31:24>
4	0x0C	0	1	1	MasterReg<31:0> -> cntlWord12<31:0>

TABLE 7. READBACK OF CNTLWORD12

ADDR<2:0>	CDATA<7:0>	CE	RD	WR	INTERNAL OPERATION
5	0x0C	0	1	1	write to addrReg<4:0>
0	0xDD	0	0	x	read CntlWord12<7:0>
1	0xCC	0	0	x	read CntlWord12<15:8>
2	0xBB	0	0	x	read CntlWord12<23:16>
3	0xAA	0	0	x	read CntlWord12<31:24>

Writing and reading back the internal RAMs require a different sequence of writes and reads. Each RAM on the device is accessible through the uPI, with the FIFO only having readback capability. The user selects which memory to access and the access type (read or write) as well as the address mode by programming the memory configuration bits in ControlWord 0 as shown in Table 8.

TABLE 8. CONTROL WORD 0 - MEMORY CONTROL BITS

BIT #	VALUE	DEFINITION
7	x	Not Used
6	0	Disable Memory Address Auto Increment Mode - User must provide address
	1	Auto-Increment Memory Address Mode Active
5	0	Memory R/W select: Write to Selected Memory
	1	Memory R/W select: Read from Selected Memory
4:2	000	No Memory Access Active
	001	I channel 64x72-bit coefficient RAM selected
	010	Q channel 64x72-bit coefficient RAM selected
	011	I and Q channel 64x72-bit coefficient RAMs selected for simultaneous access
	100	256x8-bit constellation map RAM selected
	101	256x32-bit FIFO RAM selected
	110	Not Used
	111	Not Used
1:0	00	Memory Word Select Bits <1:0>, load with 00 prior to starting load sequence

Once these bits are programmed, the user loads up the masterReg<31:0> using the same sequence as shown in Table 8 followed by a write to internal address 0x0F to download the masterReg<31:0> data to the internal memory word buffer. If auto-increment address mode is selected then the user does not need to provide the memory address for the data; the address is generated sequentially internal to the device. If the 64x72-bit RAMs are selected for the access, then 72-bits of data must be loaded to the internal memory buffer per memory address. This is accomplished

by performing three (3) 24-bit master to slave loads. Table 9 demonstrates the sequence of writes necessary to load memory location 0 of the I and Q channel coefficient RAMs simultaneously.

If auto-increment address mode had been enabled, then the write to MasterReg<31:24> with the destination memory address would not have been required, as writing to Control Word 0 would reset the internal auto-increment address to 0. Writing a 0x0F to address 4 generates an internal memUpdate signal that loads the memory buffer from MasterReg<23:0>. Which section of the memory buffer gets the data is dependent on the memory word select counter shown in column 7 of Table 9. A memUpdate strobe increments the word select counter as well as updating the memBuffer. When the word select counter is equal to 2 and a memUpdate strobe occurs, memBuf<71:0> data is written to memAddr<7:0> of the I/Q coefficient RAMs and the mem word select counter is cleared ready for the next sequence of writes to the memory buffer. Writing to the constellation map RAM is much simpler as Table 10 demonstrates.

TABLE 9. EXAMPLE SEQUENCE OF WRITES TO LOAD I/Q COEFFICIENT RAM

ADDR<2:0>	CDATA<7:0>	CE	RD	WR	INTERNAL OPERATION	MEM WORD SELECT<1:0>
0	0x0C	0	1	1	write to MasterReg<7:0>	xx
4	0x00	0	1	1	MasterReg<7:0> -> cntlWord0<7:0>	00
0	memData[0][7:0]	0	1	1	write to MasterReg<7:0>	00
1	memData[0][15:8]	0	1	1	write to MasterReg<15:8>	00
2	memData[0][23:16]	0	1	1	write to MasterReg<23:16>	00
4	0x0F	0	1	1	MasterReg<23:0> -> memBuf<23:0>	00
0	memData[0][31:24]	0	1	1	write to MasterReg<7:0>	01
1	memData[0][39:32]	0	1	1	write to MasterReg<15:8>	01
2	memData[0][47:40]	0	1	1	write to MasterReg<23:16>	01
4	0x0F	0	1	1	MasterReg<23:0> -> memBuf<47:24>	01
0	memData[0][55:48]	0	1	1	write to MasterReg<7:0>	10
1	memData[0][63:56]	0	1	1	write to MasterReg<15:8>	10
2	memData[0][71:64]	0	1	1	write to MasterReg<23:16>	10
3	0x00 (memAddr)	0	1	1	write to MasterReg<31:24>	10
4	0x0F	0	1	1	MasterReg<23:0> -> memBuf<71:48>	10
					MasterReg<31:24> -> memAddr<7:0>	10

TABLE 10. EXAMPLE SEQUENCE OF WRITES TO LOAD CONSTELLATION MAP RAM

ADDR<2:0>	CDATA<7:0>	CE	RD	WR	INTERNAL OPERATION	MEM WORD SELECT<1:0>
0	0x10	0	1	1	write to MasterReg<7:0>	xx
4	0x00	0	1	1	MasterReg<7:0> -> cntlWord0<7:0>	00
2	memData[0][7:0]	0	1	1	write to MasterReg<23:16>	00
3	0x00 (memAddr)	0	1	1	write to MasterReg<31:24>	00
4	0x0F	0	1	1	MasterReg<23:16> -> memBuf<71:64>	00
					MasterReg<31:24> -> memAddr<7:0>	00

When writing to the constellation map RAM, when the word select counter is equal to 0 and a memUpdate strobe occurs, memBuf<71:64> data is written to memAddr<7:0> of the constellation map RAM.

When reading back the memories, The sequence is similar to reading back the Control Words, except the uPI addresses written to are different. When reading back the I/Q channel coefficient memories, 9 bytes (72-bits) of data are read per memory address, the constellation map RAM contains 1 byte of data per address, while the FIFO RAM contains 4 bytes of data per address. An internal byte counter takes care of which byte is being read out with a write to address 6 with the memory address to be read back will reset the byte counter to 0. A write to address 7 will increment the byte counter so the WR clock must be pulsed during the memory reads in order to increment the byte counter. Table 11 defines the sequence of writes/reads necessary to read back the I channel coefficient memory data at memory address 0x12.

The constellation map RAM and the FIFO RAM are read back in a similar manner with fewer writes to address 7 since fewer bytes per address are read back.

A synopsis of the uPI address space functions is shown in Table 12, with Tables 13 through 32 providing detailed descriptions.

TABLE 11. EXAMPLE SEQUENCE OF WRITES TO READ I COEFFICIENT RAM

ADDR<2:0>	CDATA<7:0>	CE	RD	WR	INTERNAL OPERATION	MEM BYTE COUNT<3:0>
0	0x24	0	1	1	write to MasterReg<7:0>	xx
4	0x00	0	1	1	MasterReg<7:0> -> cntlWord0<7:0>	xx
6	0x12 (memAddr)	0	1	1	write to memReadAddr<7:0>	0
6	0x12 (memAddr)	0	1	1	write to memReadAddr<7:0>	0
7	memData[18][7:0]	0	0	1	read memData[18] byte 0	0
7	memData[18][15:8]	0	0	1	read memData[18] byte 1	1
7	memData[18][23:16]	0	0	1	read memData[18] byte 2	2
7	memData[18][31:24]	0	0	1	read memData[18] byte 3	3
7	memData[18][39:32]	0	0	1	read memData[18] byte 4	4
7	memData[18][47:40]	0	0	1	read memData[18] byte 5	5
7	memData[18][55:48]	0	0	1	read memData[18] byte 6	6
7	memData[18][63:56]	0	0	1	read memData[18] byte 7	7
7	memData[18][71:64]	0	0	1	read memData[18] byte 8	8

TABLE 12. MICROPROCESSOR INTERFACE ADDRESS SPACE DEFINITIONS

ADDR <2:0>	WR/RD	INTERNAL OPERATION
0	wr	Write to MasterReg<7:0> (CDATA<7:0> -> MasterReg<7:0>)
1	wr	Write to MasterReg<15:8> (CDATA<7:0> -> MasterReg<15:8>)
2	wr	Write to MasterReg<23:16> (CDATA<7:0> -> MasterReg<23:16>)
3	wr	Write to MasterReg<31:24> (CDATA<7:0> -> MasterReg<31:24>)
4	wr	Download MasterReg<31:0> -> Control Word x (x=CDATA<4:0>)
5	wr	Write address of Control Word to be read back (CDATA<4:0> -> addrReg<4:0>)
6	wr	Write address of Accessed Memory to be read back (CDATA<7:0> -> memAddr<7:0>)
7	wr	Increment Memory Address Read Back Byte Counter (byteCount<3:0>)
0	rd	Read ControlWordx<7:0> (x=addrReg<4:0>)
1	rd	Read ControlWordx<15:8> (x=addrReg<4:0>)
2	rd	Read ControlWordx<23:16> (x=addrReg<4:0>)
3	rd	Read ControlWordx<31:24> (x=addrReg<4:0>)
4	rd	Read byte # of MemWord<x> (x=memAddr<7:0>, byte # =byteCount<3:0>)
5	rd	Read byte # of MemWord<x> (x=memAddr<7:0>, byte # =byteCount<3:0>)
6	rd	Read byte # of MemWord<x> (x=memAddr<7:0>, byte # =byteCount<3:0>)
7	rd	Read byte # of MemWord<x> (x=memAddr<7:0>, byte # =byteCount<3:0>)

TABLE 13. HSP50415 REGISTER SUMMARY

ADDRESS	BIT WIDTH	REGISTER NAME	RESET VALUE
00_H	8	Memory Write/Read Controls	0x00
01_H	32	Device Configuration Controls	0x0000602B
02_H	32	FIFO And I/O Control	0x00000000
03_H	32	FIFO Upper Threshold and I Channel Gain	0xFF000002
04_H	32	FIFO Lower Threshold and Q Channel Gain	0x00000002
05_H	32	Gain and Phase Error Control	0x02FFFFFF
06_H	32	Digital Loop Filter Control	0x50000000
07_H	32	Lock Detect and Analog PLL Control	0x00400000
08_H	8	Interrupt Status	0x00
09_H	8	Interrupt Enable	0x00
$0A_H$	32	Carrier Frequency	0x00000000
$0B_H$	32	Symbol Frequency	0x00000000
$0C_H$	32	Digital Loop Filter Upper Limit	0x7FFFFFFF
$0D_H$	32	Digital Loop Filter Lower Limit	0x80000000
$0E_H$		FIFO Reset Strobe	0
$0F_H$		Memory Word Load Strobe	0
10_H		Soft Reset Signal	0
11_H	19	Coefficient Ram Preload Data	0x00000
12_H		FIFO Write Strobe	0

TABLE 14. MEMORY WRITE/READ CONTROL

ADDRESS = 00_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
7	Reserved	0
6	Auto Increment Memory Address	0
5	Memory R/W (Used in conjunction with bits 4:2) 0 = Write 1 = Read	0
4:2	Memory Access Select. 000_B = No Access (note: must set no access for normal running of part) 001_B = IfirMem Access 010_B = QfirMem Access 011_B = I+QfirMem Access 100_B = Constellation Map Memory Access 101_B = FIFO Access	000_B
1:0	Memory Word Select	00

TABLE 15. DEVICE CONFIGURATION CONTROL

ADDRESS = 01_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31:16	Symbol NCO Counter MaxCount<15:0>	0000_H
15	Symbol NCO Counter Mode Enable	0_B
14	Fast DAC delay	1_B
13	Bypass Final Interpolation Filter	1_B

TABLE 15. DEVICE CONFIGURATION CONTROL (Continued)

ADDRESS = 01_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
12	2-bit Filter Mode. Input data at 2x rate with ½ # taps used.	0_B
11:10	Shaping Filter Interpolation 00_B = 4x 01_B = 8x 10_B = 16x 11_B = reserved	00_B
9:6	Data Bit Width NumBits/2^{B12}-1 If Bit 12 = 0, 0000_B = 1 bit 0001_B = 2 bits… 1110_B = 15 bits 1111_B = 16 bits If Bit 12 = 1, 0000_B = 2 bits 0001_B = 4 bits… 1110_B = 30 bits 1111_B = 32 bits	0000_B
5	X/Sin(X) Filter Bypass. 0 = Enable 1 = Bypass	1
4	Half Band Filter Enable 0 = Bypass 1 = Enable	0
3	Shaping Filter Bypass 0 = Enable 1 = Bypass	1
2	Decimate by 2 at output of Shaping Filter 0 = Disable 1 = Enable	0
1	Constellation Map Bypass 0 = Enable 1 = Bypass	1
0	FIFO Bypass 0 = Enable 1 = Bypass	1

TABLE 16. FIFO AND I/O CONTROL

ADDRESS = 02_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31:24	FIFO Frequency Term 4 Loop Filter <7:0>.	00_H
23	FIFO Full Stop Writing	0
22	FIFO Empty, Force 0 data	0
21:20	FIFO Threshold Mode 00_B = Disable Threshold Logic and FIFOUnderFlow / FIFOOverFlow flags 01_B = Enable Thresholds, Disable Symbol Rate Modifications 10_B = Enable Thresholds and Modify Frequency Error Term 11_B = Enable Thresholds and Force lag accumulator to Limit	00_B
19	FIFO TXEN Zero Data. (Function: If FIFO Reads are gated with TXEN Pin then force data out of FIFO block to 0x0000 if TXEN is inactive.)	0
18	FIFO TXEN Enable Gated Write 0 = TXEN Pin gates writing to FIFO 1 = FIFO writes not gated by TXEN	0

TABLE 16. FIFO AND I/O CONTROL (Continued)

ADDRESS = 02_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
17	FIFO TXEN Gated Read 0 = FIFO reads not gated by TXEN (reads begin after 2 FIFO locations written) 1 = TXEN Pin gates read from FIFO	0
16	FIFO Underflow/Empty Pin Function 0 = Output FIFO underflow status on Pin FEMPT 1 = Output FIFO empty status on Pin FEMPT	0
15	2XSYMCLK polarity	0
14	2XSYMCLK Three-State enable 0 = off 1 = enable output	0
13	FFULL, FIFO Full Output Enable	0
12	FOVRFL, FIFO Overflow Output Enable	0
11	FEMPT, FIFO Under/Empty Output Enable	0
10	LOCKDET Output Enable	0
9	SYSCLK/2 Output Enable	0
8	INTREQ Pin Output Enable	0
7	IOUT<13:0> Output Enable	0
6	QOUT<13:0> Output Enable	0
5	TXEN Polarity 0 = Active High 1 = Active Low	0
4	ISTRB Polarity. 0 = Active High (DIN<15:0> contains Isample when ISTRB is high) 1 = Active Low (DIN<15:0> contains Isample when ISTRB is low)	0
3	SYSCLK/2 polarity. 0 = IOUT<13:0>/QOUT<15:0> data out on falling edge 1 = IOUT<13:0>/QOUT<15:0> data out on rising edge	0
2	FIFO Gated Read No Address Reset	0
1	IDAC Power Enable	0
0	QDAC Power Enable	0

TABLE 17. I CHANNEL CALIBRATION

ADDRESS = 03_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31:24	FIFO Threshold Upper Limit<7:0>	FF_H
23:14	I Scale Factor<9:0>	000_H
13:4	I DC Offset <9:0>	000_H
3	I Negate Scale Factor	0
2	I Subtract DC Offset	0
1:0	I Programmable Round 00_B = No Rounding 01_B = Round to 14-bits at output 10_B = Round to 12-bits at output 11_B = Round in both positions	10_B

TABLE 18. Q CHANNEL CALIBRATION

ADDRESS = 04_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31:24	FIFO Threshold Lower Limit<7:0>	FF_H
23:14	Q Scale Factor<9:0>	000_H
13:4	Q DC Offset <9:0>	000_H
3	Q Negate Scale Factor	0
2	Q Subtract DC Offset	0
1:0	Q Programmable Round 00_B = No Rounding 01_B = Round to 14-bits at output 10_B = Round to 12-bits at output 11_B = Round in both positions	10_B

TABLE 19. GAIN AND PHASE ERROR CONTROL

ADDRESS = 05_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31:26	Post Shaping Filter Gain 01.XXXXXX	000000_B
25:22	Post Shaping Filter Shift<3:0>	1011_B
21:8	N Count <13:0> for Phase Error Detector	$3FFF_H$
7:0	M Count <7:0> for Phase Error Detector. (Minimum value = 4)	FF_H

TABLE 20. DIGITAL LOOP FILTER CONTROL

ADDRESS = 06_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31	Reserved	0
30	Invert Phase Error	1
29	Invert Frequency Error	0
28	Disable Offset Frequency	1
27:16	Loop Filter Gains: Bits 27:24 = lag[3:0] Bits 23:20 = frq[3:0] Bits 19:16 = lead[3:0]	000_H
15:1	Loop Filter Shifts: Bits 15:11 = lag[4:0] Bits 10:6 = frq[4:0] Bits 5:1 = lead[4:0]	0000_H
0	Zero Loop Filter Accumulator	0

TABLE 21. LOCK DETECT CONTROL

ADDRESS = 07_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31	Use Analog PLL lock status bit for Lock Detection	0
30:28	Analog PLL VCO divider 000_B = 1x 001_B = 2x 010_B = 4x 011_B = 8x 100_B = 16x 101_B = 32x	000_B
27:26	Analog PLL CLK divider 00_B = /1 01_B = /2 10_B = /4 11_B = /8	00_B
25	Enable Analog PLL	0
24	Use Analog PLLCLK for CLK	0
23:3	Phase Error Threshold[20:0]	08000_H
2:1	Less than Threshold Increment 00_B = + 0.0625 01_B = + 0.125 10_B = + 0.25 11_B = + 0.50	00_B
0	Greater than Threshold Decrement 0 = -0.50 1 = -0.25	0

TABLE 22. INTERRUPT STATUS

ADDRESS = 08_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
7	Not Used	0
6	FIFO Full	0
5	FIFO Empty	0
4	FIFO Overflow	0
3	FIFO Underflow	0
2	Digital PLL Lock Detect	0
1	Analog PLL Lock Detect	0
0	Reset Done	0

TABLE 23. INTERRUPT ENABLE

ADDRESS = 09_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
7	Not Used	0
6	FIFO Full	0
5	FIFO Empty	0
4	FIFO Overflow	0
3	FIFO Underflow	0
2	Digital PLL Lock Detect	0
1	Analog PLL Lock Detect	0
0	Reset Done	0

TABLE 24. CARRIER FREQUENCY

ADDRESS = $0A_H$		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31:0	Carrier NCO Frequency Step	00000000_H

TABLE 25. SYMBOL FREQUENCY

ADDRESS = $0B_H$		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31:0	Symbol NCO Frequency Step	00000000_H

TABLE 26. DIGITAL LOOP FILTER UPPER LIMIT

ADDRESS = $0C_H$		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31:0	Digital Loop Filter Upper Limit	$7FFFFFFF_H$

TABLE 27. DIGITAL LOOP FILTER LOWER LIMIT

ADDRESS = $0D_H$		
BIT NO.	**DESCRIPTION**	**RESET STATE**
31:0	Digital Loop Filter Lower Limit	00000000_H

TABLE 28. FIFO RESET STROBE

ADDRESS = $0E_H$		
BIT NO.	**DESCRIPTION**	**RESET STATE**
NA	Writing to control word 0x0E generates an internal FIFOReset strobe that resets the FIFO address pointers and flags.	0

TABLE 29. MEMORY BUFFER UPDATE STROBE

ADDRESS = $0F_{Hf}$		
BIT NO.	**DESCRIPTION**	**RESET STATE**
NA	Writing to control word 0x0F generates an internal memBuf update strobe that downloads the appropriate MasterReg byte to the memory Buffer.	0

TABLE 30. SOFT RESET SIGNAL

ADDRESS = 10_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
NA	Writing to uPI address space 4 with CDATA<7:0> = 0x10 forces the internal soft Reset signal active. The soft Reset stays active until different CDATA<7:0> other than 0x10 is written to address space 4.	0

TABLE 31. SHAPING FIR ROUNDING AND BALANCE

ADDRESS = 11_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
19	I/Q FIR preLoad<18:0> filter seed value.	0

TABLE 32. FIFO DATA WRITE STROBE

ADDRESS = 12_H		
BIT NO.	**DESCRIPTION**	**RESET STATE**
NA	Strobe used to enable writes to FIFO - data from DIN<15:0.>, ISTRB interface.	0

Power Consumption

The HSP50415 power consumption is as shown in Figure 21.

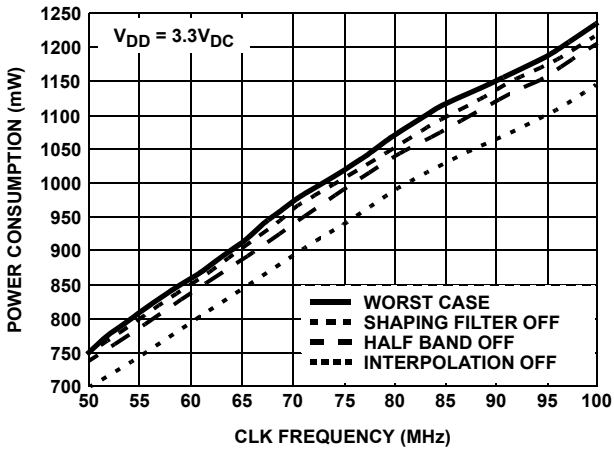


FIGURE 21. POWER CONSUMPTION vs CLK FREQUENCY

Evaluation Kit

The HSP50415EVAL1 is an evaluation kit for the HSP50415 wideband programmable modulator. The kit consists of an evaluation Circuit Card Assembly complete with the HSP50415 device and additional circuitry to provide for control via a computer parallel port. Windows based demonstration software is provided for full user programmability and control of all HSP50415 operational modes. Documentation includes a user's manual, full evaluation board schematics and PCB layout materials.

Absolute Maximum Ratings

Supply Voltage (VDD to GND) 6V
All Signal Pins . . . . . (GND – 0.5V) to (V_{DD} + 0.5V)
ESD Classification . . . . . .Class 2

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
MQFP Package	28

Maximum Junction Temperature . . . . . .+150°C
Maximum Storage Temperature Range . . . . . .-65°C to +150°C
Vapor Phase Soldering, 1 Minute
MQFP Package . . . . . .+220°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Electrical Specifications

VDD = +3.3V ±5%, T_A = -40°C to +85°C, Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS					
Power Supply Voltage, AVDD, DVDD		3.15	3.3	3.45	V
Supply Current (I_{VDD})	IOUTFS = 20mA	-	420	500	mA
Power Dissipation	IOUTFS = 20mA	-	-	1.75	W
Supply Current (I_{VDD}) Sleep Mode	DAC in sleep mode CLK stopped	-	4	6	mA
Power Supply Rejection	Single Supply	-0.2	-	+0.2	%FSR/V
DC CHARACTERISTICS: DIGITAL I/O					
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Current, I_{IL}	V_{IN} = 0.0V	-10	-	10	µA
Input Logic High Current, I_{IH}	V_{IN} = DVDD	-10	-	10	µA
Output Tristate Low Current, I_{XL}		-10	-	10	µA
Output Tristate High Current, I_{XH}		-10	-	10	µA
Input Capacitance, C_{IN}	(Note 1)	-	6	-	pF
Output Logic Low Voltage, V_{OL}	I_{OL} = 2mA	-	-	0.4	V
Output Logic High Voltage, V_{OH}	I_{OH} = -2mA	2.6	-	-	V
Output Capacitance, C_{OUT}	(Note 1)	-	6	-	pF
AC CHARACTERISTICS: DIGITAL CONTROL AND PROCESSOR INTERFACE					
CLK Frequency, f_{CLK}		-	-	100	MHz
CLK High, t_{CH}	(Note 1)	4	-	-	ns
CLK Low, t_{CL}	(Note 1)	4	-	-	ns
$\overline{\text{RESET}}$ Setup Time, t_{RTS}	To CLK, (Note 1)	3	-	-	ns
$\overline{\text{RESET}}$ Hold Time, t_{RTH}	From CLK, (Note 1)	1	-	-	ns
$\overline{\text{RESET}}$ Pulsewidth, t_{RPW}	CLK Cycles, (Note 1)	10	-	-	Cycles
WR Frequency		-	-	CLK/4	MHz
Setup Time, t_S	CDATA<7:0>, ADDR<2:0> and $\overline{\text{CE}}$ to WR, (Note 1)	15	-	-	ns
Hold Time, t_H	CDATA<7:0>, ADDR<2:0> and $\overline{\text{CE}}$ from WR, (Note 1)	0	-	-	ns
CDATA<7:0> Output Delay, t_{DA}	CDATA<7:0> from ADDR<2:0>, (Note 1)	-	-	20	ns
CDATA<7:0> Output Delay, t_{DW}	CDATA<7:0> from WR, (Note 1)	-	-	20	ns
AC CHARACTERISTICS: DIGITAL I/Q DATA INPUT					
DATACLK Frequency, F_{DCLK}		-	-	CLK / 2	MHz
DATACLK High, T_{DCH}		5	-	-	ns

Electrical Specifications VDD = +3.3V ±5%, T_A = -40°C to +85°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
DATACLK Low, t_{DCL}		5	-	-	ns
Setup Time, t_{DS}	DIN<15:0>, TXEN, ISTRB to DATACLK, (Note 1)	8	-	-	ns
Hold Time, t_{DH}	DIN<15:0>, TXEN, ISTRB from DATACLK, (Note 1)	0	-	-	ns
AC CHARACTERISTICS: DIGITAL STATUS / DATA					
REFCLK Frequency, f_{RCK}		-	-	CLK / 4	MHz
REFCLK High, t_{RCH}		5	-	-	ns
REFCLK Low, t_{RCL}		5	-	-	ns
Digital Status and Output Data Delay, t_{DO}	From SYSCLK/2 Includes IOUT<13:0>, FIFO status pins, LOCKDET and $\overline{\text{INTREQ}}$., (Note 1)	-	-	5	ns
ANALOG OUTPUT PERFORMANCE:					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	“Best Fit” Straight Line (Note 4)	-	±1	-	LSB
Differential Linearity Error, DNL	(Note 4)	-	±0.5	-	LSB
Offset Error, I_{OS}	(Note 4)	-0.025		+0.025	% FSR
Offset Drift Coefficient	(Note 4)	-	0.1	-	ppm FSR/^{O}C
Full Scale Gain Error, FSE	With External Reference (Notes 3, 4)	-10	±2	+10	% FSR
	With Internal Reference (Notes 3, 4)	-10	±1	+10	% FSR
Full Scale Gain Drift	With External Reference (Note 4)	-	±50	-	ppm FSR/^{O}C
	With Internal Reference (Note 4)	-	±100	-	ppm FSR/^{O}C
Full Scale Output Current, I_{FS}		2	-	20	mA
Output Capacitance	(Note 1)	-	30	-	pF
Output Voltage Compliance Range	(Note 1, 4)	-1.0	-	1.25	V
Gain Matching Between Channels		-8	-	+8	% FSR
Offset Matching Between Channels		-	±0.05	-	% FSR
Phase Matching Between Channels	(Note 1)	-	±0.5	-	Degrees
VOLTAGE REFERENCE:					
Internal Reference Voltage, V_{REF}		-	1.23	-	V
Internal Reference Voltage Drift	(Note 1)	-	±40	-	ppm/^{O}C
Internal Reference Output Current Sink/Source Capability	(Note 1)	-	±0.1	-	µA
Reference Input Impedance	(Note 1)	-	1	-	MΩ
Reference Input Multiplying Bandwidth	(Notes 1, 4)	-	1.4	-	MHz

NOTES:

1. Parameter guaranteed by design or characterization and not production tested.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 625µA). Ideally the ratio should be 32.
4. See ‘Definition of DAC Specifications’ section.

Waveforms

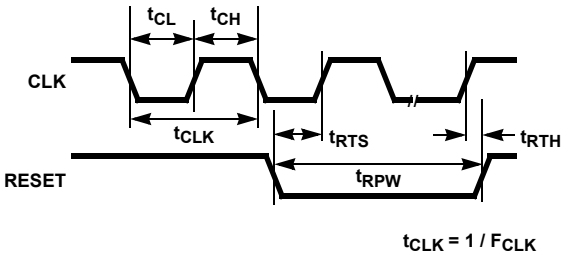


FIGURE 22. CLK AND RELATIVE RESET TIMING

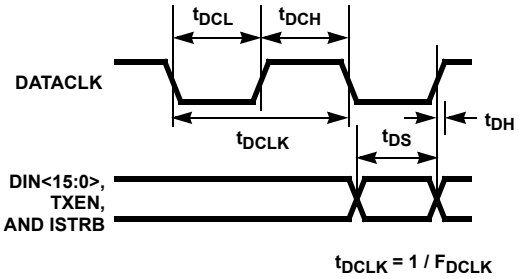


FIGURE 23. TIMING RELATIVE TO DATACLK

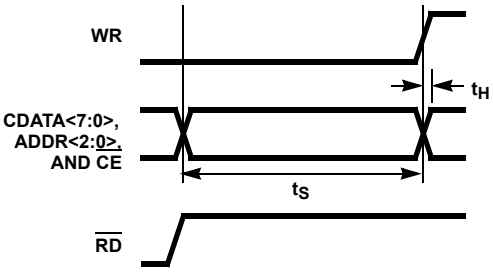


FIGURE 24. TIMING RELATIVE TO WR, LOADING SEQUENCE

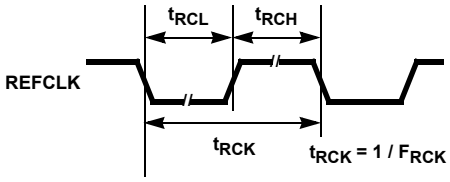


FIGURE 25. REFCLK TIMING

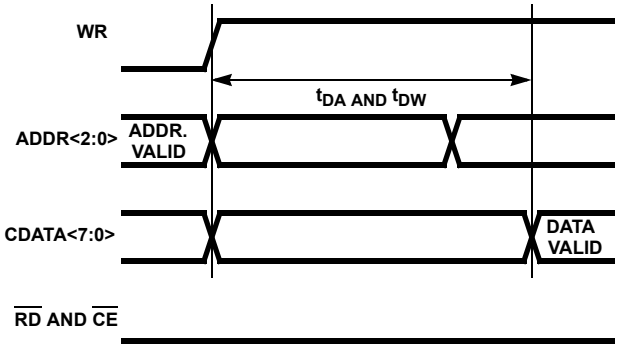


FIGURE 26. TIMING RELATIVE TO WR, READING SEQUENCE

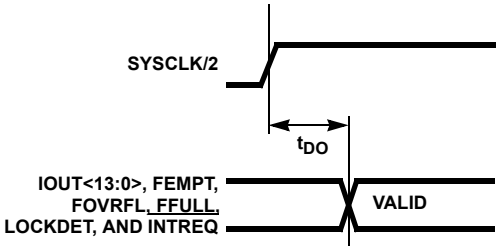
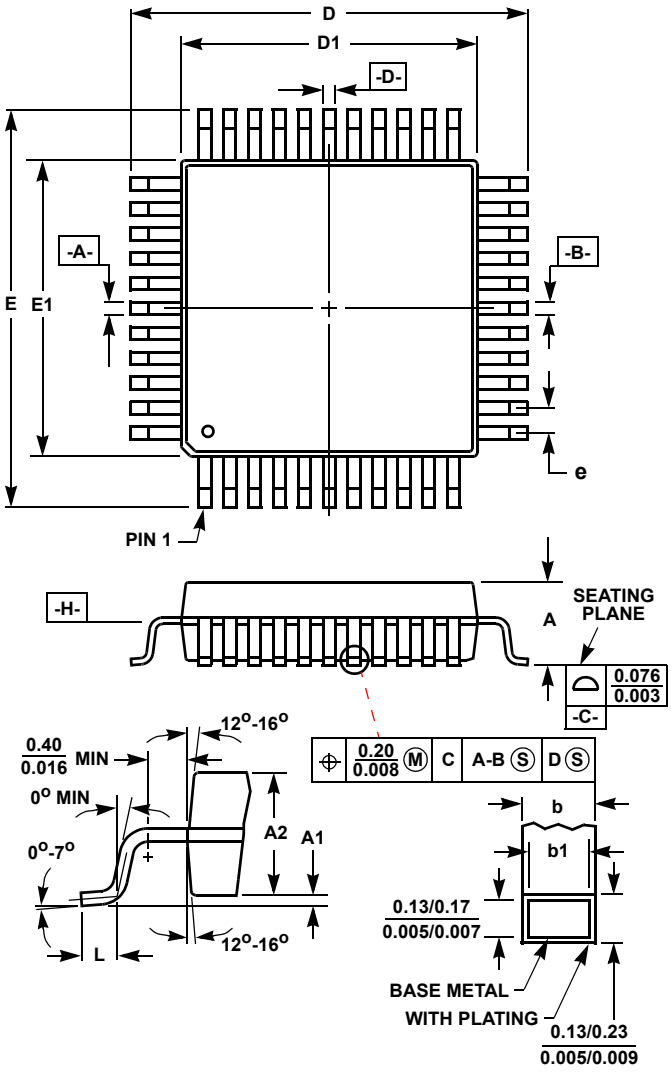


FIGURE 27. SYSCLK/2 RELATIVE TIMING

Metric Plastic Quad Flatpack Packages (MQFP)



Q100.14x20 (JEDEC MS-022GC-1 ISSUE B)
100 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.134	-	3.40	-
A1	0.010	-	0.25	-	-
A2	0.101	0.113	2.57	2.87	-
b	0.009	0.015	0.22	0.38	6
b1	0.009	0.013	0.22	0.33	-
D	0.908	0.918	23.08	23.32	3
D1	0.782	0.792	19.88	20.12	4, 5
E	0.673	0.681	17.10	17.30	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.029	0.040	0.73	1.03	-
N	100		100		7
e	0.026 BSC		0.65 BSC		-
ND	30		30		-
NE	20		20		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.