3.0V Standard Cell for TSMC 40nm LP

Overview

The Renesas 3.0V Standard Cell is useful library for low leak macro of TSMC 40nm LP process. It's suitable for low-speed and low leak macro development.

Key Features

- 3.0VTr-cell is Low Leak very smaller than Core-Cells (0.16pA @2NAND)
- Gate Delay: 180ps@2NAND@Slow Condition
- Technology is TSMC 40nm LP.
- Electrical characteristic

Parameter	Min	Typ	Max	Unit
Operating Voltage(VCC)	1.55	3.0	3.6	V
Junction Temperature	-40	25	125	℃

- Cell Lineup

Type	Sub-Type	Cell	Drive					
			X1	X2	X3	X4	X6	X8
Combinational	Simple Logic	BUF	✓	✓	✓	✓	✓	✓
		INV	✓	✓	✓	✓	✓	✓
		2-AND	✓	✓	✓	✓		
		2-OR	✓					
		2-NAND	✓	✓	✓	✓		
		2-NOR	✓					
		TIE-LOW	✓					
		TIE-HIGH	✓					
	Complex Logic	2to1 MUX	✓	✓	✓	✓		
Storage	Flip-Flop	Scan D-F/F (with Resetbar)	✓					
		Scan D-F/F (with Resetbar Data Enable)	✓					
	Latch	D-Latch(with ResetBar)	✓					

**This IP is contract design IP. Please contact for detail.*