ISL22317

Precision Single Digitally Controlled Potentiometer (XDCP™) Low Noise, Low Power, I²C™ Bus, 128 Taps

FN6912
Rev 1.00
April 15, 2010

The digitally controlled potentiometer is implemented with a combination of resistor elements and CMOS switches. The position of the wiper is controlled by the user through the I²C bus interface. The potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR control the position of the wiper. At power up, the device recalls the contents of the DCP's IVR to the WR.

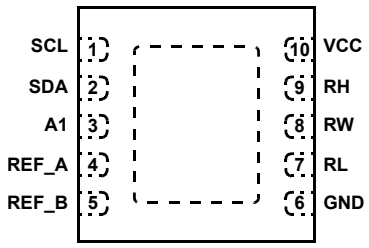
The highly precise ISL22317 features a low end-to-end temperature coefficient of TC_Ref ±10ppm/°C and precise resistance selection. It maintains less than ±1% typical variance from the ideal resistance at each wiper position providing 99% accuracy of selected resistance value. This highly accurate DCP eliminates the need for complex algorithms to guarantee precision. The ISL22317 allows the user to dial in an accurate resistance and the EEPROM memory stores the set value for life, or until changed by the user.

An external 0.5% or better reference resistor must be attached to the ISL22317. The ISL22317 will mirror both the precise resistance and temperature coefficient of the external resistor.

The DCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Pinout

ISL22317
(10 LD TDFN)
TOP VIEW



Features

- Precision Digitally Controlled Potentiometer
  - 99% Typical Accuracy Of Resistance Over Operational Conditions
  - Zero-Compensated Wiper Resistance
- Integrated Digitally Controlled Potentiometer
  - 128-Tap Positions
  - I²C Serial Interface
  - Pin Selectable Slave Address
  - 10kΩ, 50kΩ and 100kΩTotal Resistance
  - Monotonic Over-Temperature
  - Non-Volatile EEPROM Storage of Wiper Position
  - 0 to VCC Terminal Voltage
- Single 2.7V to 5.5V Supply
- High Reliability
  - 50 Years Retention @ ≤ +55°C
  - 15 Years Retention @ +125°C
  - 1,000,000 Cycles Endurance
- 3mmx3mm Thin DFN Package – 0.75mm Max Thickness, 0.65mm Pitch
- Pb-Free (RoHS Compliant)

Applications

- Setting Precise Current Values for DC Margining and Backlight Control
- Replaces Complex Compensation Circuitry That Stores Values in Look-up Tables Needed for Precise Resistor Setting
- Setting Precise Resistance Values for Test and Measurement Circuits
- Adjust Specific Resistances in Analog Circuits
- Precise Calibration and Fine Tune-Up

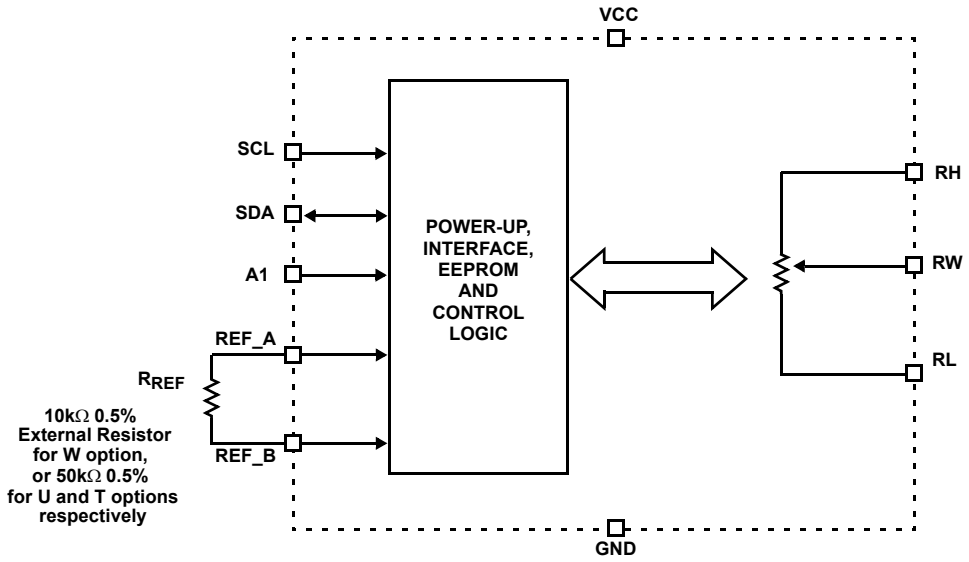
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	RESISTANCE OPTION (kΩ)	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL22317TFRTZ	317T	100	-40 to +125	10 Ld TDFN	L10.3x3B
ISL22317UFRTZ	317U	50	-40 to +125	10 Ld TDFN	L10.3x3B
ISL22317WFRTZ	317W	10	-40 to +125	10 Ld TDFN	L10.3x3B

NOTES:

1. Add “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL22317. For more information on MSL please see techbrief TB363.

Block Diagram



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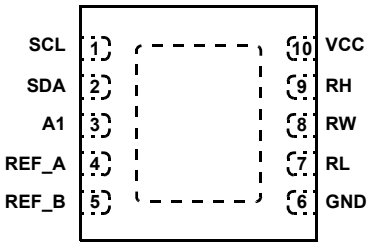


Pin Descriptions

TDFN PIN #	SYMBOL	DESCRIPTION
1	SCL	Open drain I^2C interface clock input
2	SDA	Open drain Serial data I/O for the I^2C interface
3	A1	Device address input for the I^2C interface
4	REF_A	Terminal A for an external reference resistor
5	REF_B	Terminal B for an external reference resistor
6	GND	Device ground pin
7	RL	“Low” terminal of DCP
8	RW	“Wiper” terminal of DCP
9	RH	“High” terminal of DCP
10	VCC	Power supply pin
	EPAD*	Exposed Die Pad internally connected to GND

*PCB thermal land for QFN/TDFN EPAD should be connected to GND plane or left floating. For more information refer to http://www.intersil.com/data/tb/TB389.pdf

Absolute Maximum Ratings

Voltage at any Digital Interface Pin with respect to GND . . . . . -0.3V to V_{CC} + 0.3V
V_{CC} . . . . . -0.3V to +6.0V
Voltage at any DCP Pin with respect to GND . . . . . 0V to V_{CC}
I_W (10s) . . . . . ±6mA
Latchup (Note 6) . . . . . Class II, Level B at +125°C
ESD
Human Body Model 5kV
Machine Model 500V

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Lead TDFN	44	3

Storage Temperature . . . . . -65°C to +150°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature Range (Extended Industrial) . . . . . -40°C to +125°C
V_{CC} . . . . . 2.7V to 5.5V
V_{RH}-V_{RL} . . . . . 1V to V_{CC} - 0.3V
V_{RW}-V_{RL} . . . . . 0.3V to V_{CC} - 0.3V
Power Rating 15mW
Wiper Current . . . . . ±3.0mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
6. Jedec Class II pulse conditions and failure criterion used. Level B exceptions is using a minimum negative pulse of -0.8V on the A1 pin.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 22)	TYP (Note 7)	MAX (Note 22)	UNIT
R_{TOTAL}	RH to RL Resistance	W option		10		kΩ
		U option		50		kΩ
		T option		100		kΩ
	RH to RL Resistance Tolerance	U and T options	-3	±1	+3	%
		W option	-4	±1	+4	%
	End-to-End Temperature Coefficient	All options, match external reference TCr		TCref ±10		ppm/°C
V_{RH}	DCP High Terminal Voltage	V_{RH} to GND	V_{RL} + 1		V_{CC} - 0.3	V
V_{RL}	DCP Low Terminal Voltage	V_{RL} to GND	0		V_{CC} - 1V	V
R_W	Wiper Resistance	Precision On, RH - floating, V_{RL} = 0V, force I_W current to wiper, $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$		0		Ω
		Precision Off, RH - floating, V_{RL} = 0V, force I_W current to wiper, $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$		70		Ω
R_{REF}	External Reference Resistor	for W option, 0.5%		10		kΩ
		for U option, 0.5%		50		kΩ
		for T option, 0.5%		50		kΩ
I_{LkgDCP}	Leakage on DCP Pins	Voltage at pin from GND to V_{CC}		0.1	0.5	µA
VOLTAGE DIVIDER MODE (0V @ RL; V_{CC} -0.3V @ RH; measured at RW, unloaded)						
INL (Note 12)	Integral Non-linearity	W, U or T option V_{RL} + 0.3V < V_{RW} < V_{CC} - 0.3V	-0.5	±0.1	0.5	LSB (Note 8)
DNL (Note 11)	Differential Non-linearity	W, U or T option V_{RL} + 0.3V < V_{RW} < V_{CC} - 0.3V	-0.5	±0.1	0.5	LSB (Note 8)

Analog Specifications

Over recommended operating conditions unless otherwise stated. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 22)	TYP (Note 7)	MAX (Note 22)	UNIT
ZSerror (Note 9)	Zero-scale Error	W, U or T option $V_{RL} < V_{RW} < V_{RL} + 0.3V$		0.5	2	LSB (Note 8)
FSerror (Note 10)	Full-scale Error	W, U or T option $V_{CC} - 0.3V < V_{RW} < V_{CC}$	-2	-0.5		LSB (Note 8)
TC_V (Notes 13, 19)	Ratiometric Temperature Coefficient	Match to external Rref, DCP register set between 15 hex and 7F hex		TCref ±10		ppm/°C
f_{cutoff} (Note 19)	-3dB Cut Off Frequency	Wiper at midpoint (40hex) W option (10k)		1		kHz
		Wiper at midpoint (40hex) U option (50k)		1		kHz
		Wiper at midpoint (40hex) T option (100k)		1		kHz
RESISTOR MODE (Measurements between RW and RL with RH not connected)						
RINL (Note 17)	Integral Non-linearity	W, U or T option Current forced to the wiper $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$ (Note 20)	-3	±1	3	MI (Note 14)
RDNL (Note 16)	Differential Non-linearity	W, U or T option Current forced to the wiper $I_W = (V_{CC} - V_{RL})/R_{TOTAL}$ (Note 20)	-3	±1	3	MI (Note 14)
Roffset (Note 15)	Offset	W, U or T option, wiper is out of recommended operation conditions	0	1	2	MI (Note 14)
TC_R (Notes 18, 19)	Resistance Temperature Coefficient	Match to external Rref, DCP register set between 15 hex and 7F hex, all options		TCref ±10		ppm/°C

Operating Specifications

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 22)	TYP (Note 7)	MAX (Note 22)	UNIT
I_{CC1}	V_{CC} Supply Current (volatile write/read)	V_{CC} = +5.5V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)		0.6	1.2	mA
		V_{CC} = +2.7V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states), 10k		0.35	0.9	mA
I_{CC2}	V_{CC} Supply Current (non-volatile write/read)	V_{CC} = +5.5V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)		1.75	2.5	mA
		V_{CC} = +2.7V, f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)		1.0	1.8	mA
I_{SB}	V_{CC} Current (Standby)	V_{CC} = +5.5V @ +125°C, I^2C interface in standby state		0.5	1.0	mA
		V_{CC} = +2.7V @ +125°C, I^2C interface in standby state, 10k		0.3	0.75	mA
I_{SD}	V_{CC} Current (Shutdown)	V_{CC} = +5.5V @ +125°C, I^2C interface in standby state		0.5	1.5	µA
I_{LkgDig}	Leakage Current, at Pins REF_A, REF_B, A1, SDA, and SCL	Voltage at pin from GND to V_{CC}	-0.25		0.25	µA
t_{DCP} (Note 19)	DCP Wiper Response Time	SCL falling edge of last bit of DCP data byte to wiper new position		150		µs
$t_{ShdnRec}$ (Note 19)	DCP Recall Time from Shutdown Mode	SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection		150		µs
Vpor	Power-on Recall Voltage	Minimum V_{CC} at which memory recall occurs			2.6	V
VCC Ramp	V_{CC} Ramp Rate		0.2		50	V/ms

Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 22)	TYP (Note 7)	MAX (Note 22)	UNIT
t_D	Power-up Delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			1	ms
EEPROM SPECIFICATION						
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature T ≤ +55°C	50			Years
		Temperature T ≤ +125°C	15			Years
t_{WC} (Note 21)	Non-volatile Write Cycle Time			12	20	ms
SERIAL INTERFACE SPECS						
V_{IL}	A1, A0, SDA, and SCL Input Buffer LOW Voltage				$0.3*V_{CC}$	V
V_{IH}	A1, A0, SDA, and SCL Input Buffer HIGH Voltage		$0.7*V_{CC}$			V
Hysteresis (Note 19)	SDA and SCL Input Buffer Hysteresis		$0.05*V_{CC}$			V
V_{OL} (Note 19)	SDA Output Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin (Note 19)	A1, A0, SDA, and SCL Pin Capacitance				10	pF
f_{SCL}	SCL Frequency				400	kHz
t_{sp}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window			900	ns
t_{BUF}	Time the Bus must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	1300			ns
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0			ns

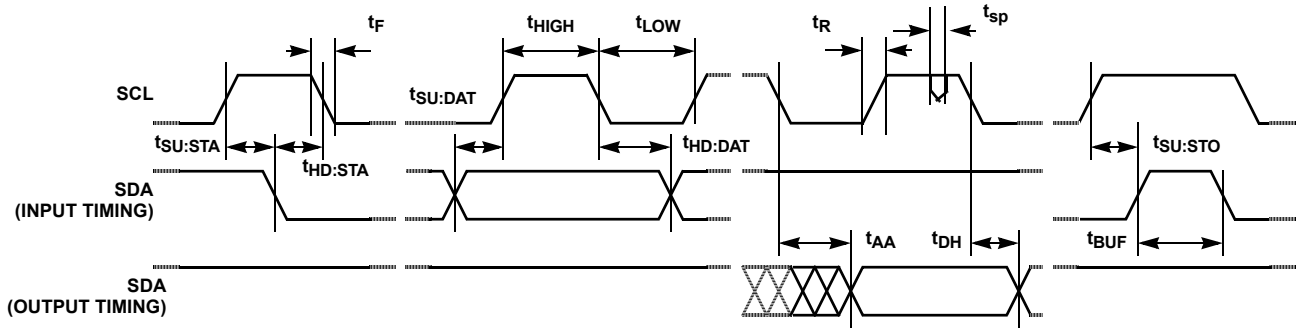
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 22)	TYP (Note 7)	MAX (Note 22)	UNIT
t_R (Note 19)	SDA and SCL Rise Time	From 30% to 70% of V_{CC}	20 + 0.1*Cb		250	ns
t_F (Note 19)	SDA and SCL Fall Time	From 70% to 30% of V_{CC}	20 + 0.1*Cb		250	ns
Cb (Note 19)	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 19)	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ ~ 2.5kΩ For Cb = 40pF, max is about 15kΩ ~ 20kΩ	1			kΩ
$t_{SU:A}$	A1 Setup Time	Before START condition	600			ns
$t_{HD:A}$	A1 Hold Time	After STOP condition	600			ns

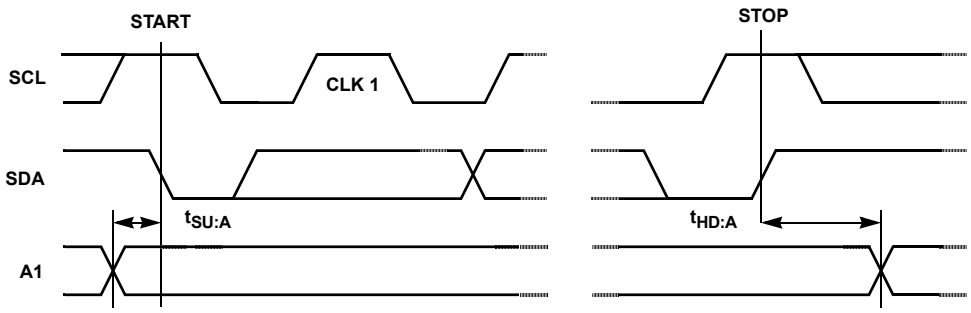
NOTES:

7. Typical values are for T_A = +25°C and 3.3V supply voltage.
8. LSB: $[V(R_W)_{127} – V(R_W)_0]/127$. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
9. $ZS_{ERROR} = V(RW)_0/LSB$.
10. $FS_{error} = [V(RW)_{127} – V_{CC}]/LSB$.
11. $DNL = [V(RW)_i – V(RW)_{i-1}]/LSB-1$, for i = 1 to 127, where i is the DCP register setting.
12. $INL = [V(RW)_i – i • LSB – V(RW)_0]/LSB$ for i = 1 to 127
13. $TC_V = \frac{Max(V(RW)_i) – Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{+165°C}$ for i = 15 to 127 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
14. $MI = |RW_{127} – RW_0|/127$. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
15. $R_{OFFSET} = RW_0/MI$, when measuring between RW and RL.
16. $R_{DNL} = (RW_i – RW_{i-1})/MI$ -1, for i = 1 to 127.
17. $R_{INL} = [RW_i – (MI • i) – RW_0]/MI$, for i = 1 to 127.
18. $TC_R = \frac{[Max(Ri) – Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{+165°C}$ for i = 15 to 127, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
19. Limits should be considered typical and are not production tested.
20. In rheostat mode, if a current is injected into the RW terminal, the magnitude of the current should be such that the developed potential difference between RW and RL terminals is at least 300mV, even at the minimum wiper setting. This ensures that the recommended operating condition of $V(RW) \geq V(RL) + 0.3V$ is satisfied and the part operates in its most accurate resistance. Minimum and Maximum wiper setting can be calculated as follow, MIN code = (0.3V*127)/(Iw*Rtotal), Max code = $[(V_{CC} - 0.3V)*127]/(I_W*R_{TOTAL})$.
21. t_{WC} is the time from a valid STOP condition at the end of a Write sequence of I^2C serial interface, to the end of the self-timed internal non-volatile write cycle.
22. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SDA vs SCL Timing



A1 Pin Timing



Typical Performance Curves

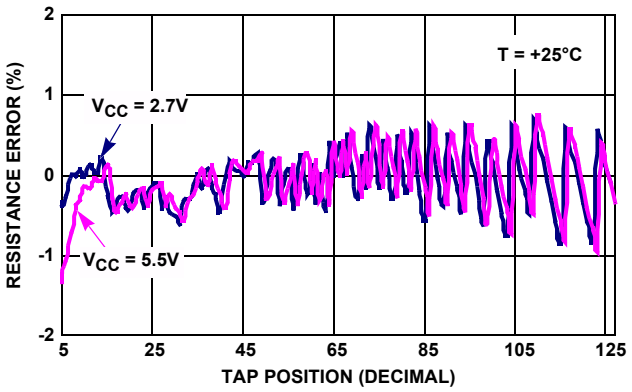


FIGURE 1. RESISTANCE ERROR vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 100kΩ (T)

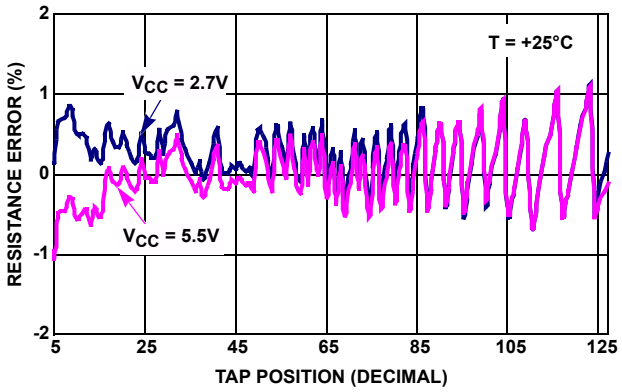


FIGURE 2. RESISTANCE ERROR vs TAP POSITION [I(RW) = V_{CC}/R_{TOTAL}] FOR 10kΩ (W)

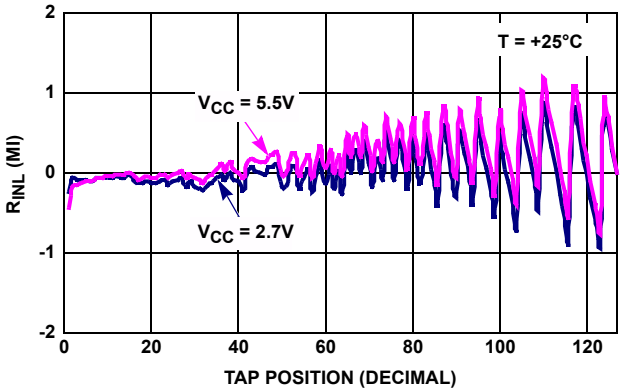


FIGURE 3. INL vs TAP POSITION IN RHEOSTAT MODE FOR 100kΩ (T)

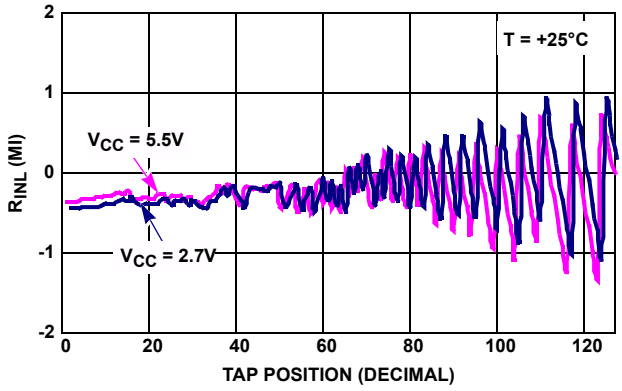


FIGURE 4. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

Typical Performance Curves (Continued)

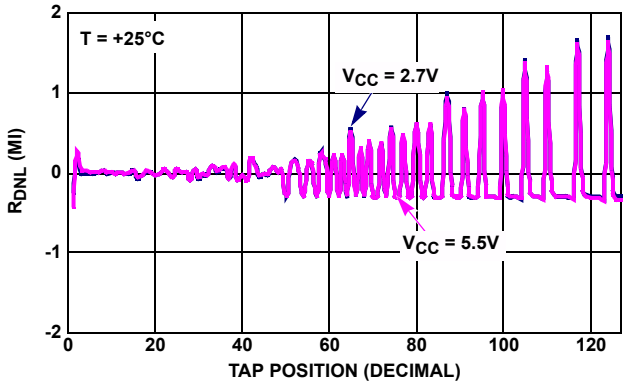


FIGURE 5. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 100kΩ (T)

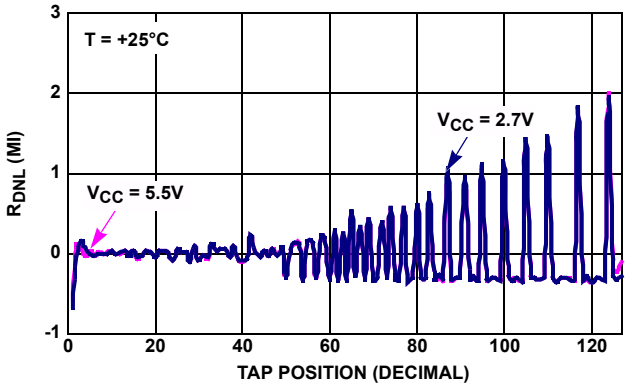


FIGURE 6. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

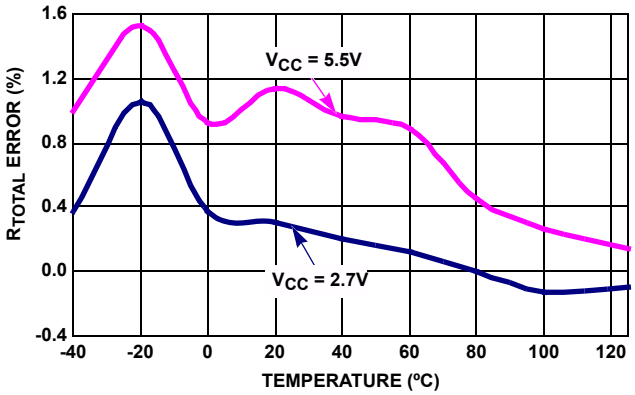


FIGURE 7. R_{TOTAL} ERROR vs TEMPERATURE FOR 100kΩ (T)

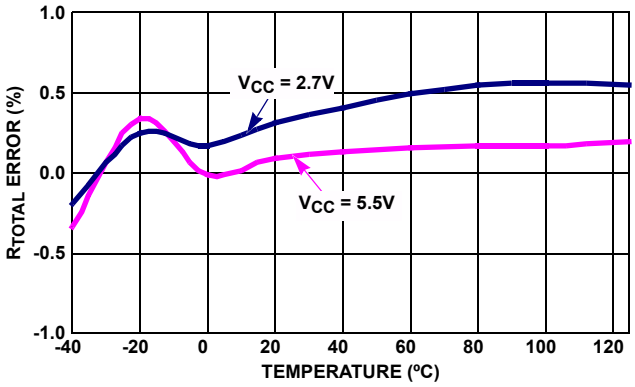


FIGURE 8. R_{TOTAL} ERROR vs TEMPERATURE FOR 10kΩ (W)

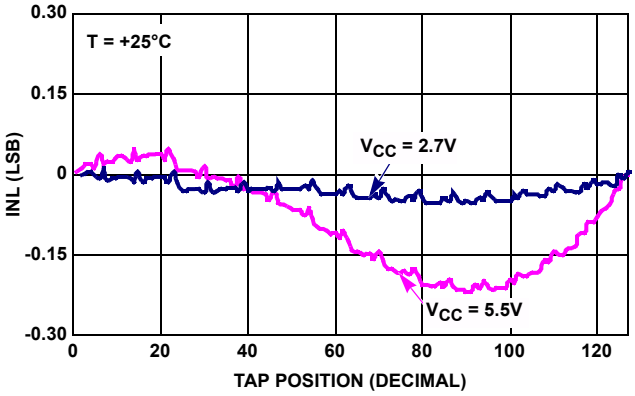


FIGURE 9. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 100kΩ (T)

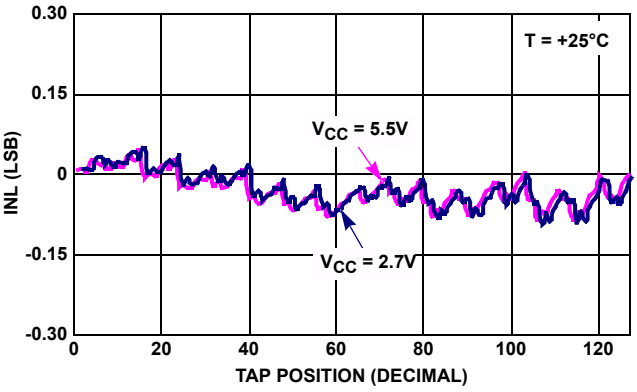


FIGURE 10. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

Typical Performance Curves (Continued)

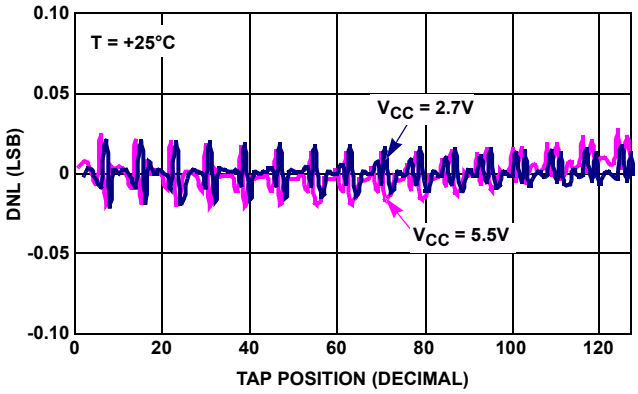


FIGURE 11. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 100kΩ (T)

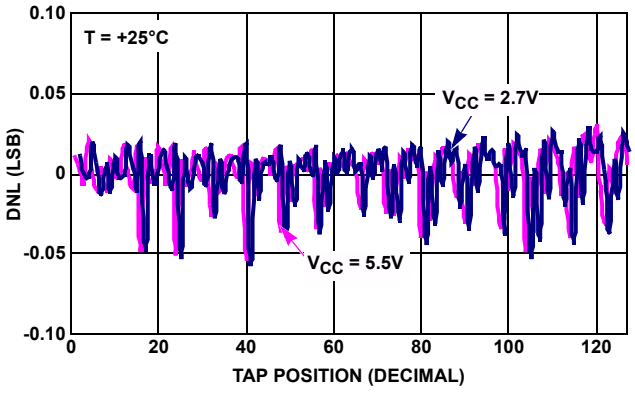


FIGURE 12. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

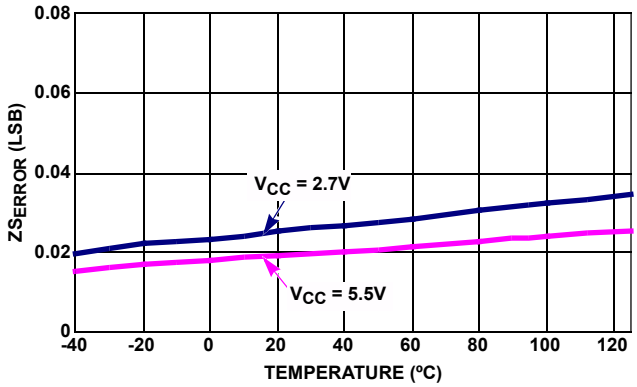


FIGURE 13. ZS_{ERROR} vs TEMPERATURE FOR 100kΩ (T)

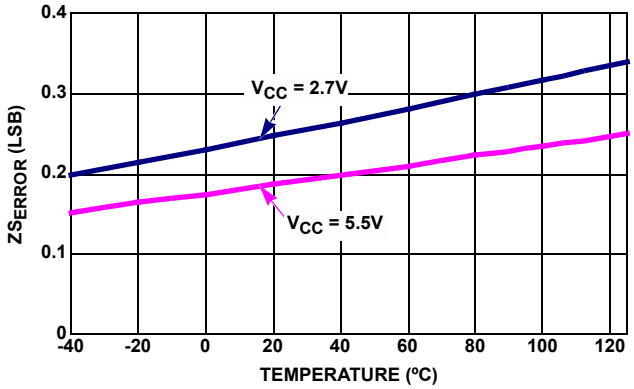


FIGURE 14. ZS_{ERROR} vs TEMPERATURE FOR 10kΩ (W)

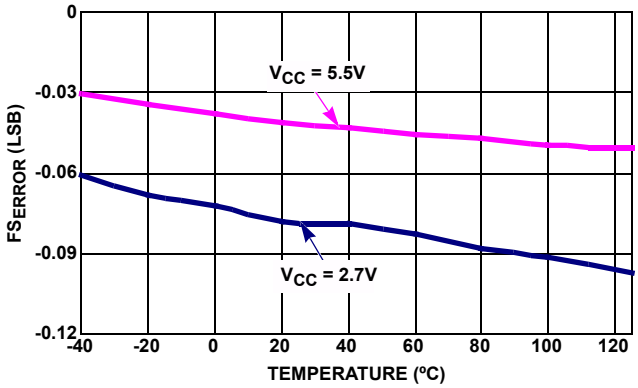


FIGURE 15. FS_{ERROR} vs TEMPERATURE FOR 100kΩ (T)

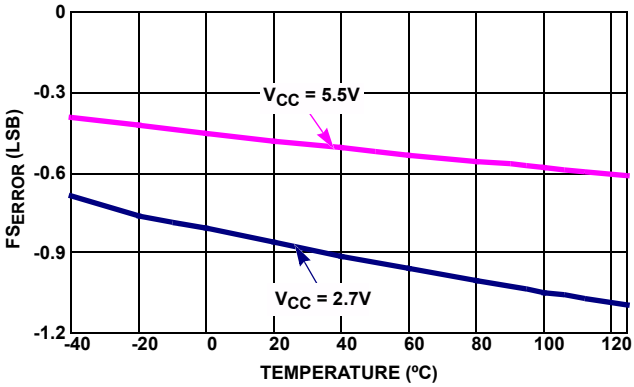


FIGURE 16. FS_{ERROR} vs TEMPERATURE FOR 10kΩ (W)

Typical Performance Curves (Continued)

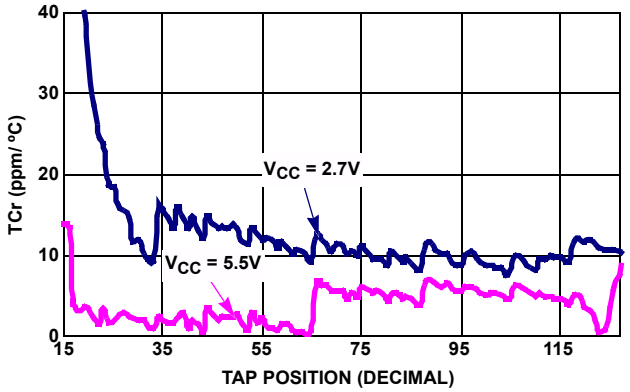


FIGURE 17. TC FOR RHEOSTAT MODE (10k/50k/100k) IN ppm [R_{REF} 2ppm/°C]

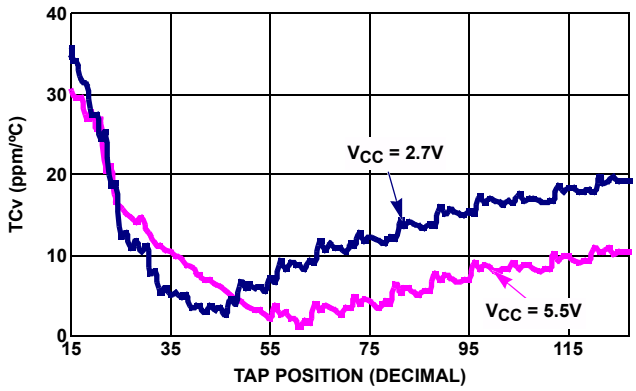


FIGURE 18. TC FOR VOLTAGE DIVIDER MODE (10k/50k/100k) IN ppm [R_{REF} 10ppm/°C]

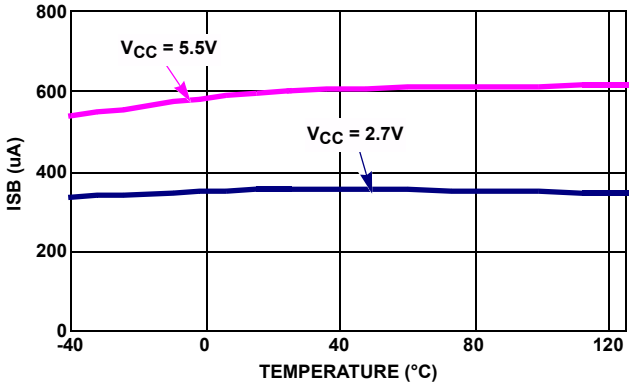


FIGURE 19. STANDBY I_{CC} vs TEMPERATURE

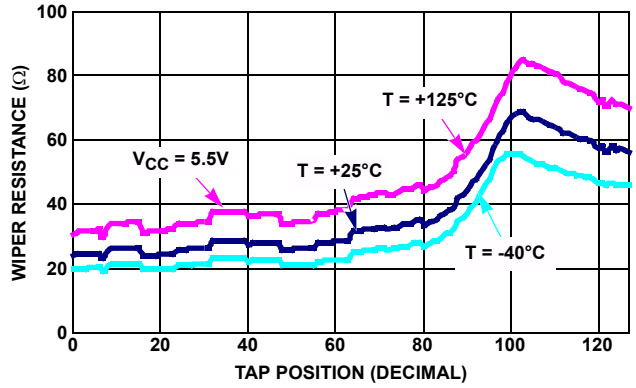


FIGURE 20. WIPER RESISTANCE vs TAP POSITION WHEN PRECISION IS OFF

Pin Description

Potentiometers Pins

RH AND RL

The high (RH) and low (RL) terminals of the ISL22317 are equivalent to the fixed terminals of a mechanical potentiometer. RH and RL are referenced to the relative position of the wiper and the voltage potential on the terminals. With WR set to 127 decimal, the wiper will be closest to RH. With the WR set to 0, the wiper is closest to RL. The voltage potential on the RH terminal must be higher than voltage potential on RL terminal.

RW

RW is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR register.

REF_A, REF_B

REF_A and REF_B are pins to connect an external resistor. If application is required to connect RL terminal to GND, then the REF_B pin should also be connected to GND.

Warning! Do not connect REF_A to GND under any circumstances. That may damage the ISL22317.

Bus Interface Pins

SERIAL DATA INPUT/OUTPUT (SDA)

The SDA is a bidirectional serial data input/output pin for I^2C interface. It receives device address, operation code, wiper address and data from an I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor, since it is an open drain input/output.

SERIAL CLOCK (SCL)

This input is the serial clock of the I^2C serial interface.

DEVICE ADDRESS (A1)

The address input is used to set the A1 bit of the 7-bit I^2C interface slave address, see Table 4. A match in the slave address serial data stream must match with the Address input pins in order to initiate communication with the ISL22317. A

maximum of two ISL22317 devices may occupy the I^2C serial bus with addresses 50h and 54h.

Principles of Operation

The ISL22317 is an integrated circuit incorporating one DCP with its associated registers, non-volatile memory and an I^2C serial interface providing direct communication between a host and the potentiometer and memory. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor, is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVR will be maintained in the non-volatile memory. When power is restored, the contents of the IVR is recalled and loaded into the WR to set the wiper to the initial value.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by a 7-bit volatile Wiper Register (WR). When the WR of a DCP contains all zeroes (WR<6:0>: 00h), its wiper terminal (RW) is closest to its “Low” terminal (RL). When the WR register of a DCP contains all ones (WR<6:0>: 7Fh), its wiper terminal (RW) is closest to its “High” terminal (RH). As the value of the WR increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH.

While the ISL22317 is being powered up, the WR is reset to 40h (64 decimal), which locates RW roughly at the center between RL and RH. After the power supply voltage becomes large enough for reliable non-volatile memory reading, the WR will be reload with the value stored in a non-volatile Initial Value Register (IVR).

The WR and IVR can be read or written to directly using the I^2C serial interface as described in the following sections.

Memory Description

The ISL22317 contains one non-volatile 8-bit Initial Value Register (IVR), one 8-bit non-volatile Mode Select Register (MSR), and two volatile 8-bit registers: Wiper Register (WR) and Access Control Register (ACR). Memory map of ISL22317 is in Table 1. The non-volatile register (IVR) at address 0, contains initial wiper position and the volatile register (WR) contains current wiper position.

TABLE 1. MEMORY MAP

ADDRESS (hex)	NON-VOLATILE	VOLATILE
2	NA	ACR
1	Mode Select Register	NA
0	IVR	WR

The non-volatile IVR and volatile WR registers are accessible with the same address 0.

The ISL22317 is pre-programed with 40h in the IVR.

The Access Control Register (ACR) at address 2 contains information and control bits described below in Table 2.

The VOL bit (ACR<7>) determines whether the access is to wiper registers WR or initial value registers IVR.

TABLE 2. ACCESS CONTROL REGISTER (ACR)

VOL	SHDN	WIP	0	0	0	0	0
(MSB)							(LSB)

If VOL bit is 0, the non-volatile IVR register is accessible. If VOL bit is 1, only the volatile WR is accessible. Note, value is written to IVR register also is written to the WR. The default value of this bit is 0.

The SHDN bit (ACR<6>) disables or enables Shutdown mode. When this bit is 0, DCP is in Shutdown mode. Default value of SHDN bit is 1.

The WIP bit (ACR<5>) is read only bit. It indicates that non-volatile write operation is in progress. It is impossible to write to the WR or ACR while WIP bit is 1.

The Mode Select Bit in Mode Select Register (MSR<7>) at address 1 allows selection of Rheostat or Voltage Divider Mode, see Table 3.

TABLE 3. MODE SELECT REGISTER (MSR)

Mode Select	Precision Off	x	x	x	x	x	x
(MSB)							(LSB)

When this bit is 0, DCP is in two-terminal Rheostat Mode. In Rheostat Mode, the RH pin should be left unconnected and DCP can be used as variable resistor between RW and RL pins.

When this bit is 1, DCP is in three-terminal Voltage Divider Mode. In Voltage Divider Mode, signal is applied between RH and RL terminals. Total resistance between RH and RL terminals is precisely matched to external reference resistor. Refer to reference resistor value in “Analog Specifications” Table on page 3.

Default value of Mode Select Bit is 0.

The Precision Off bit (MSR<6>) allows the user to turn off the matching mechanism and use the device as a regular, non-

precision DCP by setting this bit to 1. Default value of the Precision Off bit is 0, i.e. matching to external resistor is ON.

Note, if the external resistor between REF_A/REF_B is not populated, the DCP will work as a normal DCP without giving 99% precision and with ~40% higher value of the resistance. It is highly recommended to use the bit option (MSR<6>) to turn OFF the precision mode first and then removing the external resistor.

All other bits MSR<5:0> are reserved and cannot be written. Any value read from these bits should be ignored.

I²C Serial Interface

The ISL22317 supports an I²C bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22317 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 21). On power-up of the ISL22317, the SDA pin is in the input mode.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22317 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 21). A START condition is ignored during the power-up of the device.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 21). A STOP condition at the end of a read operation, or at the end of a write operation, places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 22).

The ISL22317 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22317 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 01010 as the five MSBs, and the following bit matching the logic value present at pin A1. The LSB is the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation (See Table 4).

TABLE 4. IDENTIFICATION BYTE FORMAT

					Logic value at pin A1		
0	1	0	1	0	A1	0	R/$\overline{\text{W}}$
(MSB)							(LSB)

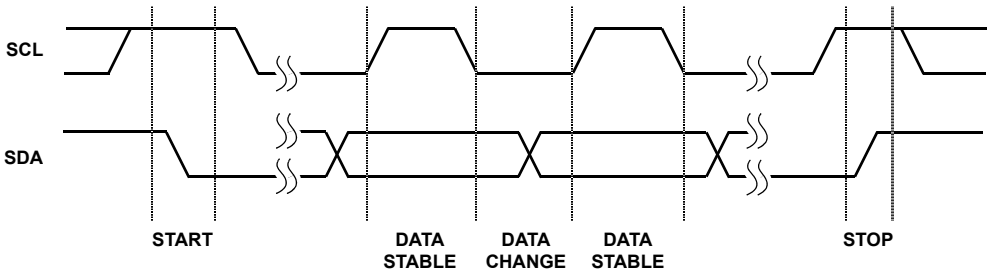


FIGURE 21. VALID DATA CHANGES, START, AND STOP CONDITIONS

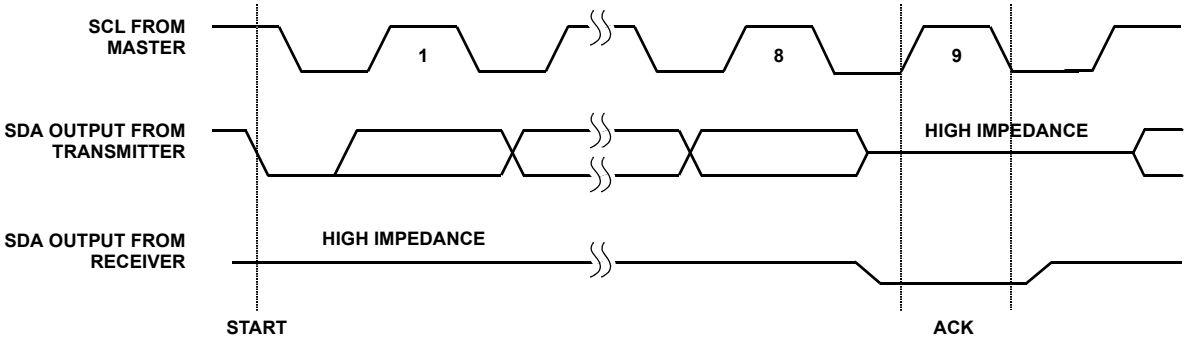


FIGURE 22. ACKNOWLEDGE RESPONSE FROM RECEIVER

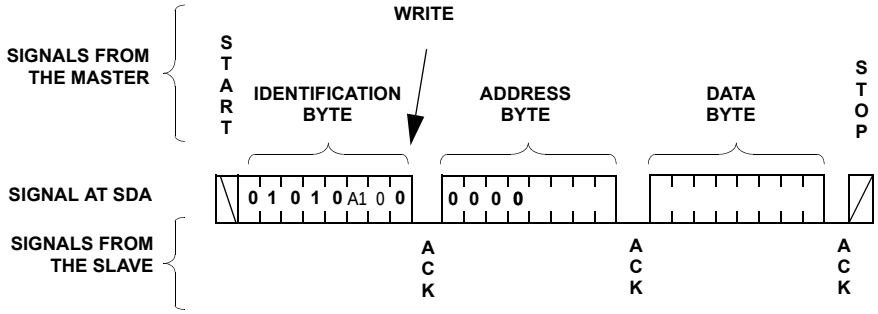


FIGURE 23. BYTE WRITE SEQUENCE

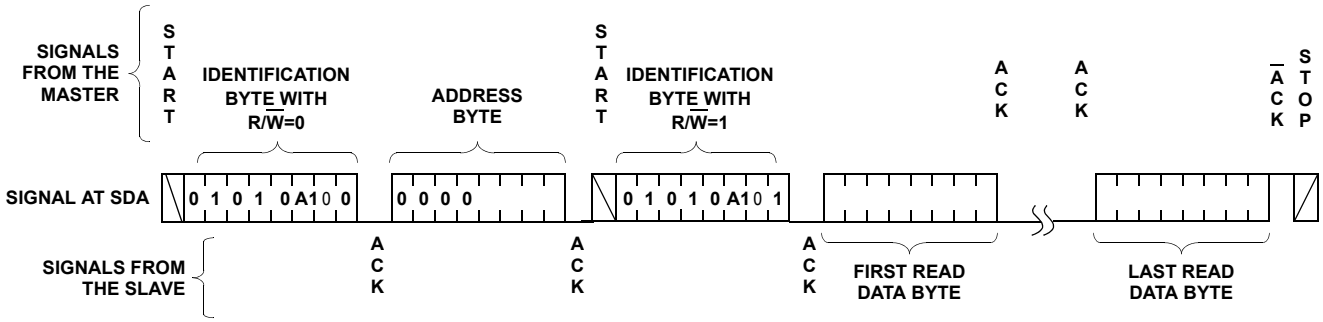


FIGURE 24. READ SEQUENCE

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22317 responds with an ACK. At this time, the device enters its standby state (see Figure 23). The non-volatile write cycle starts after a STOP condition is determined and requires up to 20ms delay for the next non-volatile write.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 24). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL22317 responds with an ACK. Then the ISL22317 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a $\overline{ACK}$ and STOP condition) following the last bit of the last Data Byte (see Figure 24).

In order to read back the non-volatile IVR, it is recommended that the application reads the ACR first to verify the WIP bit is 0. If the WIP bit (ACR[5]) is not 0, the host should repeat its reading sequence again.

Rheostat Mode Configuration

When DCP is used as a two-terminal variable resistor, the RH terminal should be left unconnected and MSR<7> is 0. Resistance between RW and RL terminal can be calculated by Equation 1:

$$Ri = \frac{Rtotal}{127} \times i \quad \text{(EQ. 1)}$$

Where *i* is a decimal code from 0 to 127. Note, that resistance accuracy will decrease at the lowest and the highest taps, where voltage drops < 0.3V. In other words, a minimum and maximum decimal code at which the DCP resistance not exceed 3% precision is as shown in Equations 2 and 3:

$$i(min) = \frac{0.3 \times 127}{Iwiper \times Rtotal} \quad \text{(EQ. 2)}$$

$$i(max) = \frac{(Vcc - 0.3) \times 127}{Iwiper \times Rtotal} \quad \text{(EQ. 3)}$$

Where *Iwiper* is a current going through the wiper terminal.

Voltage Divider Mode Configuration

In Voltage Divider Mode, voltage or signal is applied between RH and RL terminals and MSR<7> is 1. A potential at RH terminal must be higher than at RL terminal at any time. Total resistance between RH and RL terminal is fixed and matched to external reference resistor. Voltage on the wiper terminal RW can be calculated by Equation 4:

$$Vrw(i) = \frac{Vrh - Vrl}{127} \times i \quad \text{(EQ. 4)}$$

Where *i* is a decimal code from 0 to 127. Note, that the wiper voltage accuracy will decrease at the lowest and the highest taps, where it is less than 0.3V from ground or from V_{CC} respectively.

Applications Information

In order to get better accuracy in applications where RL pin is connected to GND, it is highly recommended that REF_B pin is also connected to GND.

The coupling capacitors of 1µF and 0.1µF should be placed close to VCC pin.

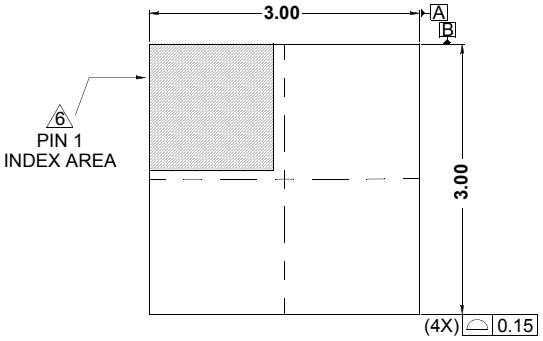
Revision History

DATE	REVISION	CHANGE
4/6/10	FN6912.1	Page 10 description of Pin A1 references Table 3 changed to Table 4. Page 5, tHD:DAT parameter test condition,"From SCL rising edge ..." changed to "From SCL falling edge ..." Added MSL note to ordering information. Replaced POD to recent version with following changes: 1. Removed mention of "b" from Note 4 since "b" does not exist on the drawing. 2. Added Note 6 callout to lead width on "Bottom View". 3. Corrected the word "indentifier" in Note 6 to read "identifier".
5/26/09	FN6912.0	Initial Release of Datasheet. Issued FN6912 making it a Rev 0.

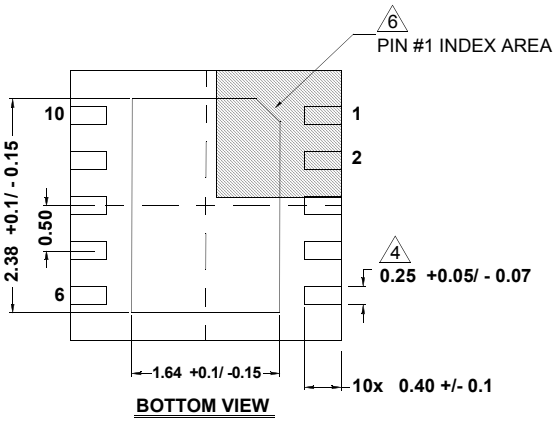
Package Outline Drawing

L10.3x3B

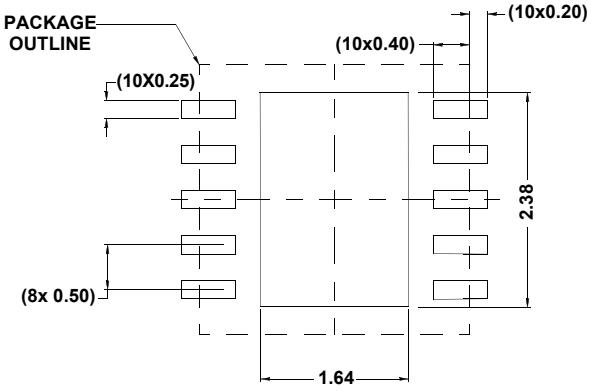
10 LEAD THIN DUAL FLAT PACKAGE (TDFN) WITH E-PAD
Rev 2, 03/10



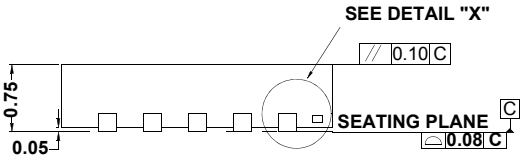
TOP VIEW



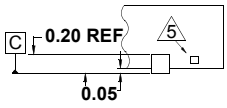
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.