ISL22326

Dual Digitally Controlled Potentiometers (XDCP™) Low Noise, Low Power, I²C Bus, 128 Taps

The ISL22326 integrates two digitally controlled potentiometers (XDCP) and non-volatile memory on a monolithic CMOS integrated circuit.

The digitally controlled potentiometers are implemented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the I²C bus interface. Each potentiometer has an associated volatile Wiper Register (WR) and a non-volatile Initial Value Register (IVR) that can be directly written to and read by the user. The contents of the WR controls the position of the wiper. At power-up the device recalls the contents of the two DCP's IVR to the corresponding WRs.

The DCPs can be used as three-terminal potentiometers or as two-terminal variable resistors in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- Two potentiometers in one package
- 128 resistor taps
- I²C serial interface
  - Three address pins, up to eight devices/bus
- Non-volatile storage of wiper position
- Wiper resistance: 70Ω typical at V_{CC} = 3.3V
- Shutdown mode
- Shutdown current 5µA max
- Power supply: 2.7V to 5.5V
- 50kΩ or 10kΩ total resistance
- High reliability
  - Endurance: 1,000,000 data changes per bit per register
  - Register data retention: 50 years at T ≤ +55°C
- 14 Ld TSSOP or 16 Ld QFN package
- Pb-free (RoHS compliant)

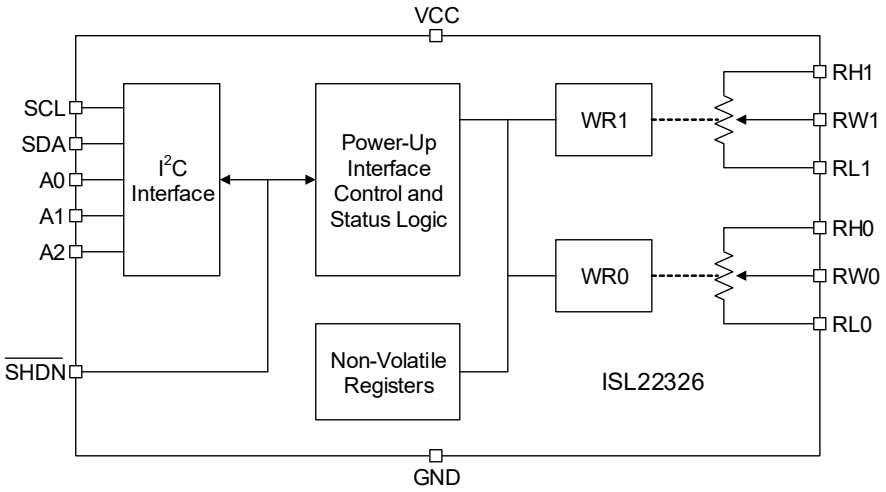


Figure 1. Block Diagram

Contents

1. Pin Information

1.1 Pin Assignments

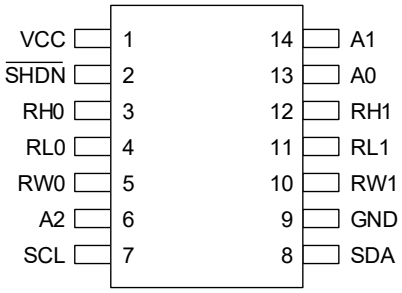


Figure 2. (14 LD TSSOP) - Top View

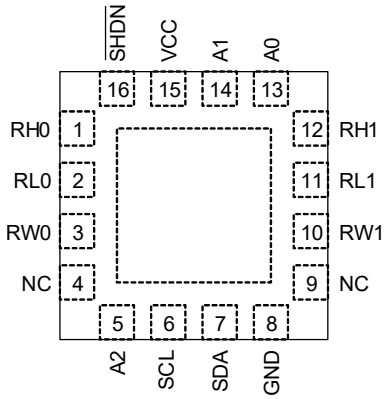


Figure 3. (16 LD QFN) - Top View

1.2 Pin Descriptions

TSSOP Pin Number	QFN Pin Number	Pin Name	Description
1	15	VCC	Power supply pin
2	16	$\overline{SHDN}$	Shutdown active low input
3	1	RH0	High terminal of DCP0
4	2	RL0	Low terminal of DCP0
5	3	RW0	Wiper terminal of DCP0
6	5	A2	Device address input for the I^2C interface
7	6	SCL	Open drain I^2C interface clock input
8	7	SDA	Open drain Serial data I/O for the I^2C interface
9	8	GND	Device ground pin
10	10	RW1	Wiper terminal of DCP1
11	11	RL1	Low terminal of DCP1
12	12	RH1	High terminal of DCP1
13	13	A0	Device address input for the I^2C interface
14	14	A1	Device address input for the I^2C interface
-	4, 9	NC	No connection
-	EPAD[1]	-	Exposed Die Pad internally connected to GND

1. PCB thermal land for QFN EPAD should be connected to GND plane or left floating. For more information refer to TB389.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Voltage at any Digital Interface Pin with Respect to GND	-0.3	VCC +0.3	V
VCC	-0.3	6	V
Voltage at any DCP Pin with Respect to GND	-0.3	VCC	V
I_W (10s)	-6	6	mA
Maximum Junction Temperature	-	150	°C
Maximum Storage Temperature Range	-65	150	°C
Human Body Model (Tested per JESD22-A114E)	-	2.5	kV
Machine Model (Tested per JESD22-A115A)	-	350	V
Latch-Up (Tested per JESD78A; Class 2, Level B at 125°C)[1]	-	100	mA

1. Jedec Class II pulse conditions and failure criterion used. Level B exceptions are: using a max positive pulse of 6.5V on the $\overline{SHDN}$ pin, and using a max negative pulse of -0.8V for all pins.

2.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range (Extended Industrial)	-40	125	°C
VCC	2.7V	5.5	V
Power Rating	-	15	mW
Wiper Current	-3	3	mA

2.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	14 Lead TSSOP	θ_{JA}[1]	Junction to ambient	100	°C/W
		θ_{JC}	Junction to case	N/A	
	16 Lead QFN	θ_{JA}[1]	Junction to ambient	40	°C/W
		θ_{JC}[2]	Junction to case	3	

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

2.4 Analog Specifications

Over recommended operating conditions, unless otherwise stated.

Parameter	Symbol	Test Conditions	Min[1]	Typ[2]	Max[1]	Unit
R_H to R_L Resistance	R_{TOTAL}	W option	-	10	-	kΩ
		U option	-	50	-	kΩ
R_H to R_L Resistance Tolerance		W and U option	-20	-	+20	%
End-to-End Temperature Coefficient[3]		W option	-	±50	-	ppm/°C
		U option	-	±80	-	ppm/°C
Wiper Resistance	R_W	V_{CC} = 3.3V, wiper current = V_{CC}/R_{TOTAL}	-	70	200	Ω
V_{RH} and V_{RL} Terminal Voltages	V_{RH}, V_{RL}	V_{RH} and V_{RL} to GND	0	-	V_{CC}	V
Potentiometer Capacitance[4]	$C_H/C_L/C_W$	-	-	10/10/25	-	pF
Leakage on DCP Pins	I_{LkgDCP}	Voltage at pin from GND to V_{CC}	-	0.1	1	µA
Voltage Divider Mode (0V at R_Li; V_{CC} at R_Hi; measured at R_Wi, unloaded; i = 0 or 1)						
Integral Non-linearity	INL[5]	Monotonic over all tap positions, W and U option	-1	-	1	LSB[6]
Differential Non-linearity	DNL[7]	Monotonic over all tap positions, W and U option	-0.5	-	0.5	LSB[6]
Zero-scale Error	ZSerror[8]	W option	0	1	5	LSB[6]
		U option	0	0.5	2	
Full-scale Error	FSerror[9]	W option	-5	-1	0	LSB[6]
		U option	-2	-1	0	
DCP to DCP Matching	V_{MATCH}[10]	Any two DCPs at same tap position, same voltage at all RH terminals, and same voltage at all RL terminals	-2	-	2	LSB[6]
Ratiometric Temperature Coefficient	TC_V[11]	DCP register set to 40 hex	-	±4	-	ppm/°C
Resistor Mode (Measurements between R_Wi and R_Li with R_Hi not connected, or between R_Wi and R_Hi with R_Li not connected. i = 0 or 1)						
Integral Non-linearity	RINL[12]	DCP register set between 10h and 7Fh; monotonic over all tap positions	-1	-	1	MI[13]
Differential Non-linearity	RDNL[14]	DCP register set between 10h and 7Fh; monotonic over all tap positions, W option	-1	-	1	MI[13]
		DCP register set between 10h and 7Fh; monotonic over all tap positions, U option	-0.5	-	0.5	MI[13]
Offset	Roffset[15]	W option	0	1	5	MI[13]
		U option	0	0.5	2	MI[13]
DCP to DCP Matching	R_{MATCH}[16]	Any two DCPs at the same tap position with the same terminal voltages	-2	-	2	MI[13]

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Typical values are for T_A = +25°C and 3.3V supply voltage.
3. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 112, T = -40°C to +125°C. Max( ) is the maximum value of the resistance and Min( ) is the minimum value of the resistance over the temperature range.

4. Limits should be considered typical and are not production tested.
5. INL = $[V(RW)_i – i • LSB – V(RW)_0]/LSB$ for i = 1 to 127.
6. LSB: $[V(R_W)_{127} – V(R_W)_0]/127$. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
7. DNL = $[V(RW)_i – V(RW)_{i-1}]/LSB-1$, for i = 1 to 127. i is the DCP register setting.
8. ZS error = $V(RW)_0/LSB$.
9. FS error = $[V(RW)_{127} – V_{CC}]/LSB$.
10. $V_{MATCH} = [V(RWx)_i – V(RWy)_i]/LSB$, for i = 1 to 127, x = 0 to 1 and y = 0 to 1.
11. $TC_V = \frac{Max(V(RW)_i) - Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{+165°C}$ for i = 16 to 112 decimal, T = -40°C to +125°C. Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range
12. $RINL = [RW_i – (MI • i) – RW_0]/MI$, for i = 16 to 127.
13. $MI = |RW_{127} – RW_0|/127$. MI is a minimum increment. RW_{127} and RW_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
14. $RDNL = (RW_i – RW_{i-1})/MI -1$, for i = 16 to 127.
15. $Roffset = RW_0/MI$, when measuring between RW and RL.
    $Roffset = RW_{127}/MI$, when measuring between RW and RH.
16. $R_{MATCH} = (RW_{i,x} – RW_{i,y})/MI$, for i = 1 to 127, x = 0 to 1 and y = 0 to 1.

2.5 Operating Specifications

Over the recommended operating conditions, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min[1])	Typ[2]	Max[1]	Unit
V_{CC} Supply Current (Volatile Write/Read)	I_{CC1}	f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)	-	-	0.5	mA
V_{CC} Supply Current (Non-volatile Write/Read)	I_{CC2}	f_{SCL} = 400kHz; SDA = Open; (for I^2C, active, read and write states)	-	-	3	mA
V_{CC} Current (Standby)	I_{SB}	V_{CC} = +5.5V at +85°C, I^2C interface in standby state	-	-	5	µA
		V_{CC} = +5.5V at +125°C, I^2C interface in standby state	-	-	7	µA
		V_{CC} = +3.6V at +85°C, I^2C interface in standby state	-	-	3	µA
		V_{CC} = +3.6V at +125°C, I^2C interface in standby state	-	-	5	µA
V_{CC} Current (Shutdown)	I_{SD}	V_{CC} = +5.5V at +85°C, I^2C interface in standby state	-	-	3	µA
		V_{CC} = +5.5V at +125°C, I^2C interface in standby state	-	-	5	µA
		V_{CC} = +3.6V at +85°C, I^2C interface in standby state	-	-	2	µA
		V_{CC} = +3.6V at +125°C, I^2C interface in standby state	-	-	4	µA
Leakage Current, at Pins A0, A1, A2, $\overline{SHDN}$, SDA and SCL	I_{LkgDig}	Voltage at pin from GND to V_{CC}	-1	-	1	µA
DCP Wiper Response Time[3]	t_{WRT}	SCL falling edge of last bit of DCP data byte to wiper new position	-	1.5	-	µs

Over the recommended operating conditions, unless otherwise specified. (Cont.)

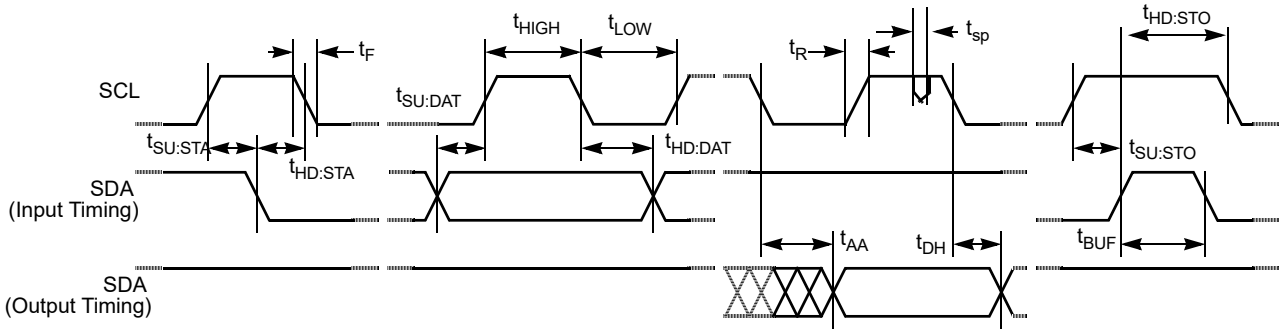
Parameter	Symbol	Test Conditions	Min[1])	Typ[2]	Max[1]	Unit
DCP Recall Time from Shutdown Mode[3]	$t_{ShdnRec}$	From rising edge of $\overline{SHDN}$ signal to wiper stored position and RH connection	-	1.5	-	µs
		SCL falling edge of last bit of ACR data byte to wiper stored position and RH connection	-	1.5	-	µs
Power-On Recall Voltage	Vpor	Minimum V_{CC} at which memory recall occurs	2.0	-	2.6	V
V_{CC} Ramp Rate	VccRamp	-	0.2	-	-	V/ms
Power-Up Delay	t_D	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state	-	-	3	ms
EEPROM Specification						
EEPROM Endurance	-	-	1,000,000	-	-	Cycles
EEPROM Retention	-	Temperature T ≤ +55°C	50	-	-	Years
Non-volatile Write Cycle Time	t_{WC}[4]	-	-	12	20	ms
Serial Interface Specifications						
A2, A1, A0, $\overline{SHDN}$, SDA, and SCL Input Buffer LOW Voltage	V_{IL}	-	-0.3	-	$0.3*V_{CC}$	V
A2, A1, A0, $\overline{SHDN}$, SDA, and SCL Input Buffer HIGH Voltage	V_{IH}	-	$0.7*V_{CC}$	-	V_{CC} + 0.3	V
SDA and SCL Input Buffer Hysteresis	Hysteresis	-	$0.05*V_{CC}$	-	-	V
SDA Output Buffer LOW Voltage, Sinking 4mA	V_{OL}	-	0	-	0.4	V
A2, A1, A0, $\overline{SHDN}$, SDA, and SCL Pin Capacitance[3]	Cpin	-	-	10	-	pF
SCL Frequency	f_{SCL}	-	-	-	400	kHz
Pulse Width Suppression Time at SDA and SCL Inputs	t_{sp}	Any pulse narrower than the max spec is suppressed	-	-	50	ns
SCL falling edge to SDA output data valid	t_{AA}	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window	-	-	900	ns
Time the Bus Must be Free Before the Start of a New Transmission	t_{BUF}	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300	-	-	ns
Clock LOW Time	t_{LOW}	Measured at the 30% of V_{CC} crossing	1300	-	-	ns
Clock HIGH Time	t_{HIGH}	Measured at the 70% of V_{CC} crossing	600	-	-	ns
START Condition Setup Time	$t_{SU:STA}$	SCL rising edge to SDA falling edge; both crossing 70% of V_{CC}	600	-	-	ns
START Condition Hold Time	$t_{HD:STA}$	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600	-	-	ns

Over the recommended operating conditions, unless otherwise specified. (Cont.)

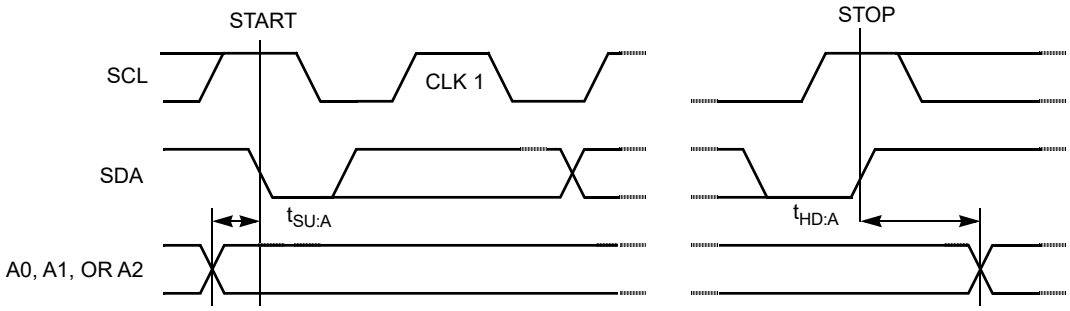
Parameter	Symbol	Test Conditions	Min[1])	Typ[2]	Max[1]	Unit
Input Data Setup Time	$t_{SU:DAT}$	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100	-	-	ns
Input Data Hold Time	$t_{HD:DAT}$	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0	-	-	ns
STOP Condition Setup Time	$t_{SU:STO}$	From SCL rising edge crossing 70% of V_{CC} to SDA rising edge crossing 30% of V_{CC}	600	-	-	ns
STOP Condition Hold Time for Read, or Volatile Only Write	$t_{HD:STO}$	From SDA rising edge to SCL falling edge; both crossing 70% of V_{CC}	1300	-	-	ns
Output Data Hold Time	t_{DH}	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0	-	-	ns
SDA and SCL Rise Time	t_R	From 30% to 70% of V_{CC}	20 + 0.1*Cb	-	250	ns
SDA and SCL Fall Time	t_F	From 70% to 30% of V_{CC}	20 + 0.1*Cb	-	250	ns
Capacitive Loading of SDA or SCL	Cb	Total on-chip and off-chip	10	-	400	pF
SDA and SCL Bus Pull-up Resistor Off-chip	Rpu	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2kΩ~2.5kΩ For Cb = 40pF, max is about 15kΩ~20kΩ	1	-	-	kΩ
A2, A1 and A0 Setup Time	$t_{SU:A}$	Before START condition	600	-	-	ns
A2, A1 and A0 Hold Time	$t_{HD:A}$	After STOP condition	600	-	-	ns

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Typical values are for T_A = +25°C and 3.3V supply voltage.
3. Limits should be considered typical and are not production tested.
4. t_{WC} is the time from a valid STOP condition at the end of a Write sequence of I^2C serial interface, to the end of the self-timed internal non-volatile write cycle.

2.6 SDA vs SCL Timing



2.7 A0, A1, and A2 Pin Timing



3. Typical Performance Curves

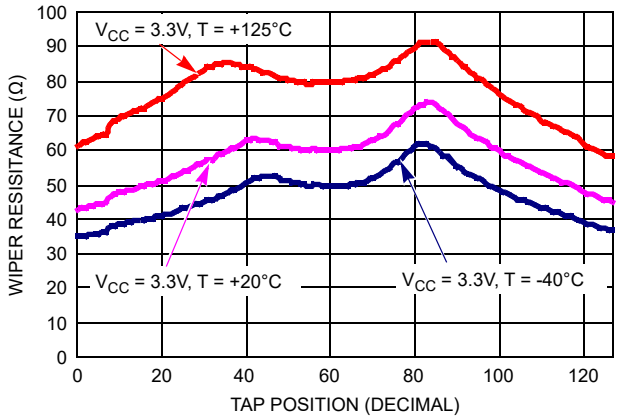


Figure 4. Wiper Resistance vs Tap Position [I(RW) = V_{CC}/R_{TOTAL}] for 10kΩ (W)

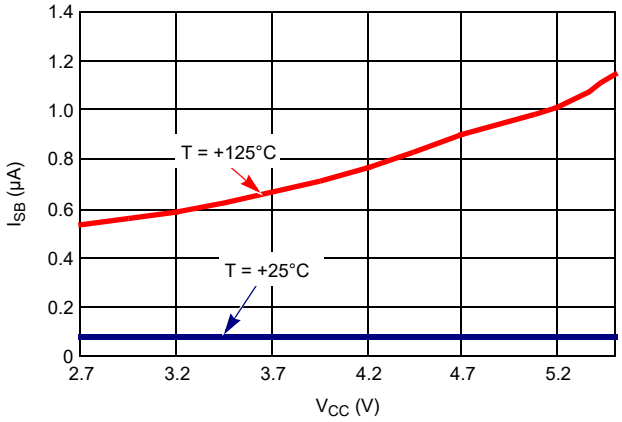


Figure 5. Standby I_{CC} vs V_{CC}

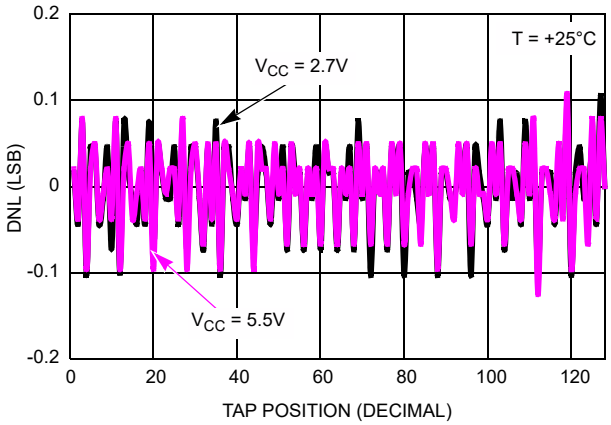


Figure 6. DNL vs Tap Position in Voltage Divider Mode for 10kΩ (W)

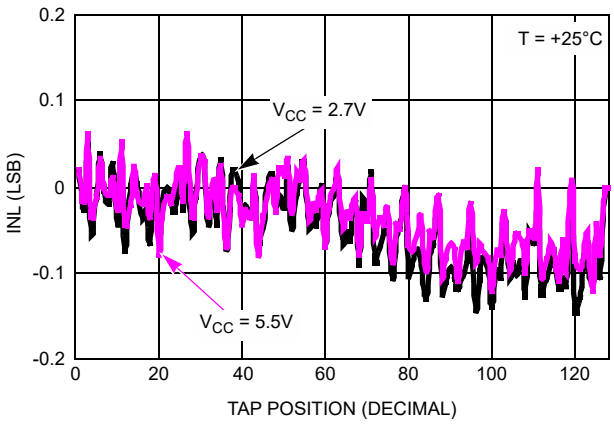


Figure 7. INL vs Tap Position in Voltage Divider Mode for 10kΩ (W)

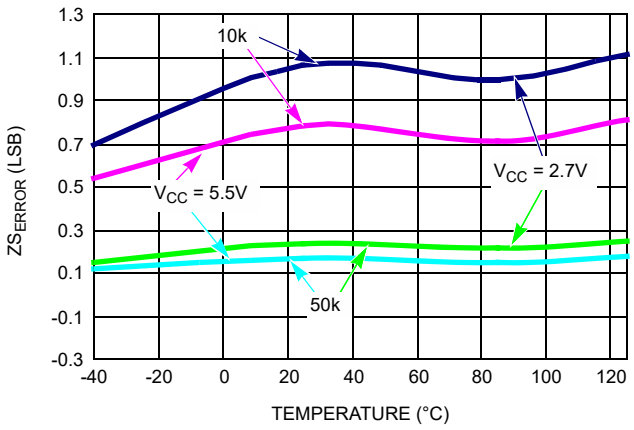


Figure 8. ZS_{ERROR} vs Temperature

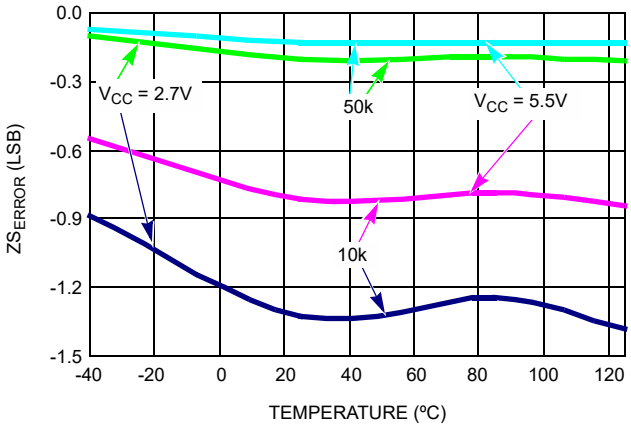


Figure 9. FS_{ERROR} vs Temperature

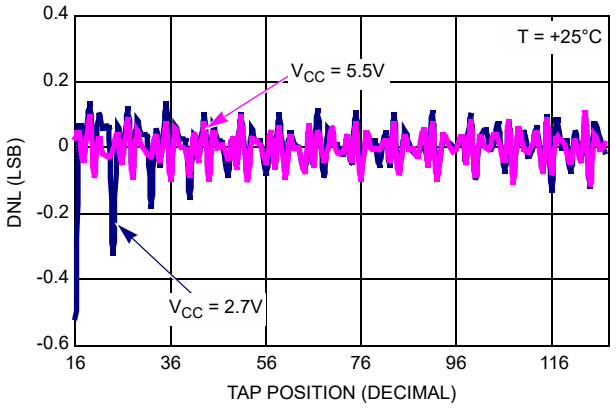


Figure 10. DNL vs Tap Position in Rheostat Mode for 10kΩ (W)

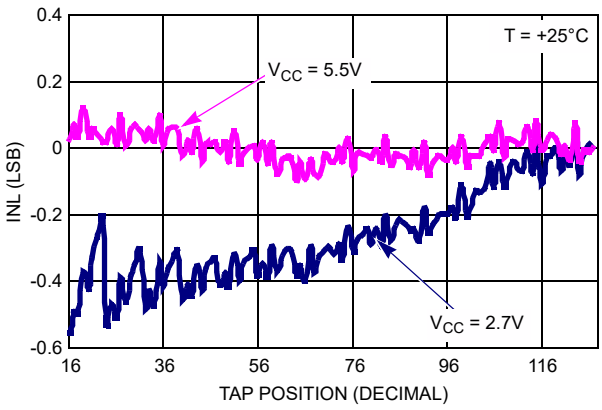


Figure 11. INL vs Tap Position in Rheostat Mode for 10kΩ (W)

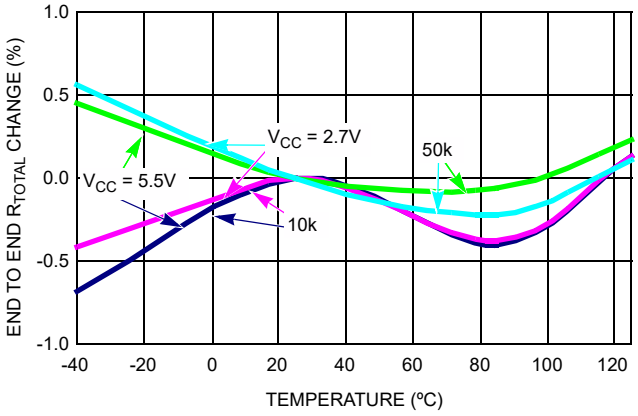


Figure 12. End-to-End R_{TOTAL} % Change vs Temperature

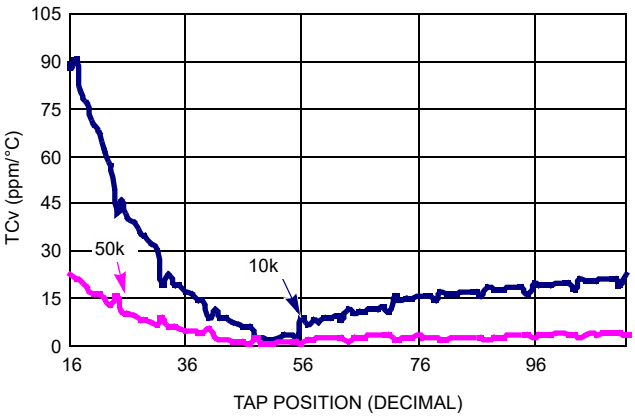


Figure 13. TC for Voltage Divider Mode in ppm

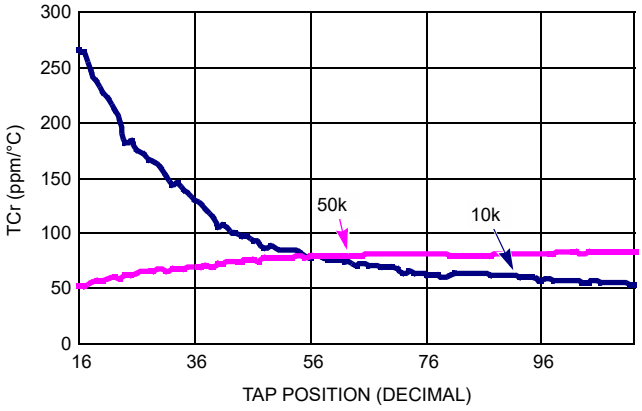


Figure 14. TC for Rheostat Mode in ppm

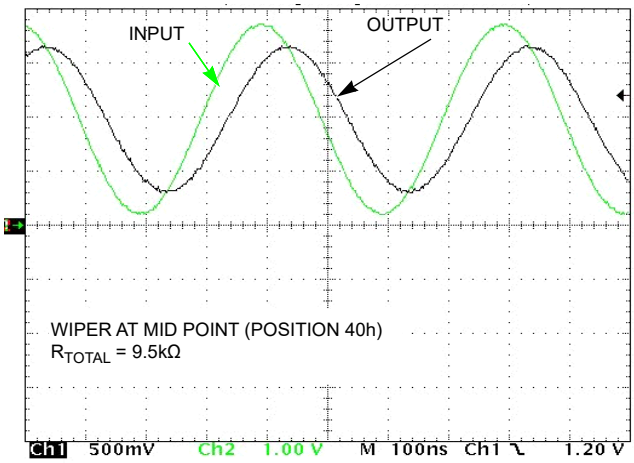


Figure 15. Frequency Response (2.6MHz)

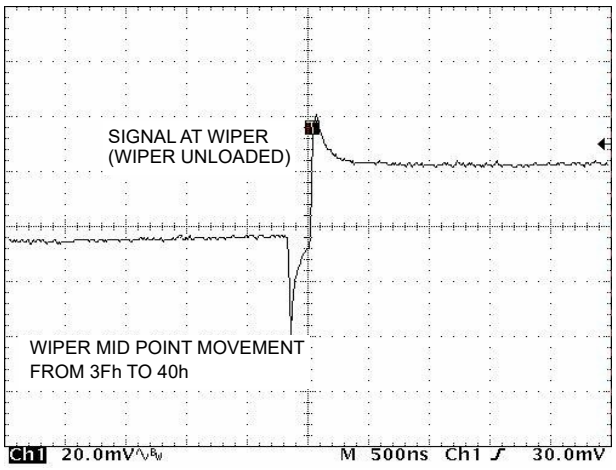


Figure 16. MIDSCALE GLITCH, CODE 3Fh TO 40h

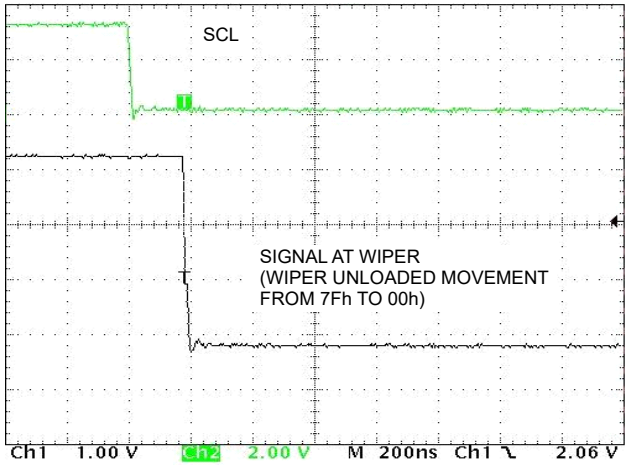


Figure 17. LARGE SIGNAL SETTLING TIME

4. Pin Descriptions

4.1 Potentiometers Pins

4.1.1 RHi and RLi (i = 0, 1)

The high (RHi) and low (RLi) terminals of the ISL22326 are equivalent to the fixed terminals of a mechanical potentiometer. RHi and RLi are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WRi set to 127 decimal, the wiper is closest to RHi, and with the WRi set to 0, the wiper is closest to RLi.

4.1.2 RWi (i = 0,1)

RWi is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WRi register.

4.1.3 SHDN

The $\overline{\text{SHDN}}$ pin forces the resistor to end-to-end open circuit condition on RHi and shorts RWi to RLi. When $\overline{\text{SHDN}}$ is returned to logic high, the previous latch settings put RWi at the same resistance setting prior to shutdown. This pin is logically ANDed with SHDN bit in ACR register. I^2C interface is still available in shutdown mode and all registers are accessible. This pin must remain HIGH for normal operation.

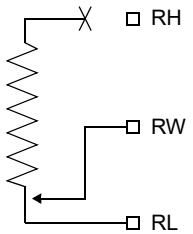


Figure 18. DCP Connection in Shutdown Mode

4.2 Bus Interface Pins

4.2.1 Serial Data Input/Output (SDA)

The SDA is a bidirectional serial data input/output pin for I^2C interface. It receives device address, operation code, wiper address and data from an I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock.

SDA requires an external pull-up resistor because it is an open-drain input/output.

4.2.2 Serial Clock (SCL)

This is the serial clock input of the I^2C serial interface. SCL requires an external pull-up resistor because it is an open-drain input.

4.2.3 Device Address (A2 - A0)

The address inputs are used to set the least significant 3 bits of the 7-bit I^2C interface slave address. A match in the slave address serial data stream must match with the Address input pins to initiate communication with the ISL22326. A maximum of eight ISL22326 devices may occupy the I^2C serial bus.

5. Principles of Operation

The ISL22326 is an integrated circuit incorporating two DCPs with their associated registers, non-volatile memory and an I^2C serial interface providing direct communication between a host and the potentiometers and memory. The resistor arrays are comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The electronic switches on the device operate in a make-before-break mode when the wiper changes tap positions.

When the device is powered down, the last value stored in IVRi is maintained in the non-volatile memory. When power is restored, the contents of the IVRi are recalled and loaded into the corresponding WRi to set the wipers to the initial value.

5.1 DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL pins). The RW pin of each DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by volatile Wiper Register (WR). Each DCP has its own WR. When the WR of a DCP contains all zeroes (WR[6:0] = 00h), its wiper terminal (RW) is closest to its Low terminal (RL). When the WR register of a DCP contains all ones (WR[6:0] = 7Fh), its wiper terminal (RW) is closest to its High terminal (RH). As the value of the WR increases from all zeroes (0) to all ones (127 decimal), the wiper moves monotonically from the position closest to RL to the closest to RH. At the same time, the resistance between RW and RL increases monotonically, while the resistance between RH and RW decreases monotonically.

While the ISL22326 is being powered up, all WRs are reset to 40h (64 decimal), which locates RW roughly at the center between RL and RH. After the power supply voltage becomes large enough for reliable non-volatile memory reading, all WRs are reloaded with the value stored in corresponding non-volatile Initial Value Registers (IVRs).

The WRs can be read or written to directly using the I^2C serial interface as described in the following sections. The I^2C interface Address Byte has to be set to 00h or 01h to access the WR of DCP0 or DCP1 respectively.

5.2 Memory Description

The ISL22326 contains seven non-volatile and three volatile 8-bit registers. Memory map of ISL22326 is on Table 1. The two non-volatile registers (IVRi) at address 0 and 1, contain initial wiper value and volatile registers (WRi) contain current wiper position. In addition, five non-volatile General Purpose registers from address 2 to address 6 are available.

Table 1. Memory Map

Address	Non-Volatile	Volatile
8	—	ACR
7	Reserved	
6	General Purpose	Not Available
5	General Purpose	Not Available
4	General Purpose	Not Available
3	General Purpose	Not Available
2	General Purpose	Not Available
1	IVR1	WR1
0	IVR0	WR0

The non-volatile IVRi and volatile WRi registers are accessible with the same address.

The Access Control Register (ACR) contains information and control bits described in Table 2. The VOL bit at access control register (ACR[7]) determines whether the access is to wiper registers WRi or initial value registers IVRi.

Table 2. Access Control Register (ACR)

VOL	SHDN	WIP	0	0	0	0	0

If VOL bit is 0, the non-volatile IVRi registers are accessible. If VOL bit is 1, only the volatile WRi are accessible. *Note*: The value written to the IVRi register is also written to the corresponding WRi. The default value of this bit is 0.

The SHDN bit (ACR[6]) disables or enables Shutdown mode. This bit is logically ANDed with $\overline{\text{SHDN}}$ pin. When this bit is 0, DCP is in Shutdown mode. Default value of SHDN bit is 1.

The WIP bit (ACR[5]) is read only bit. It indicates that non-volatile write operation is in progress. It is impossible to write to the IVRi, WRi, or ACR while WIP bit is 1.

5.3 Shutdown Mode

The device can be put in Shutdown mode either by pulling the $\overline{\text{SHDN}}$ pin to GND or setting the SHDN bit in the ACR register to 0. The truth table for Shutdown mode is in Table 3.

Table 3. Truth Table for Shutdown Mode

$\overline{\text{SHDN}}$ pin	SHDN Bit	Mode
High	1	Normal operation
Low	1	Shutdown
High	0	Shutdown
Low	0	Shutdown

5.4 I²C Serial Interface

The ISL22326 supports an I²C bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL22326 operates as a slave device in all applications.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

5.5 Protocol Conventions

Data states on the SDA line must change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 19). On power-up of the ISL22326, the SDA pin is in the input mode.

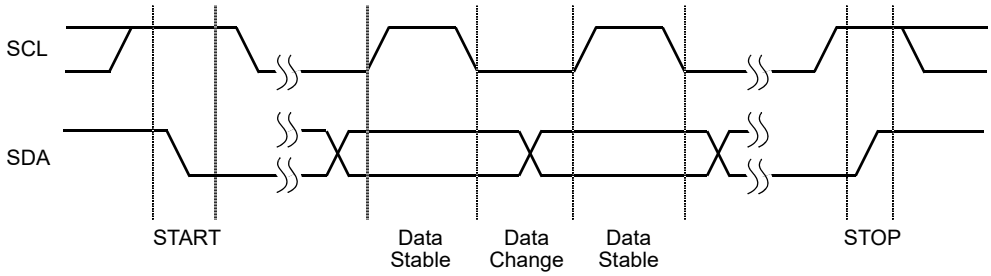


Figure 19. Valid Data Changes, START and STOP Conditions

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL22326 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 19). A START condition is ignored during the power-up of the device.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 19). A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (see Figure 20).

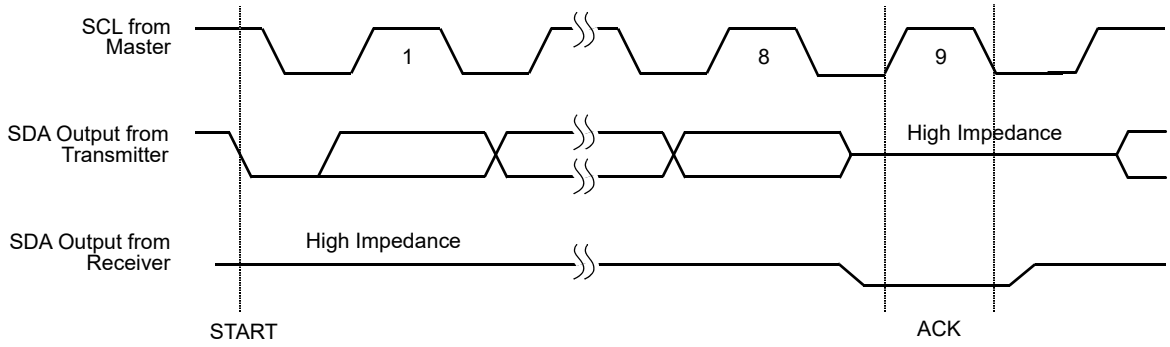


Figure 20. Acknowledge Response from Receiver

The ISL22326 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL22326 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 1010 as the four MSBs, and the following three bits matching the logic values present at pins A2, A1, and A0. The LSB is the Read/Write bit. Its value is 1 for a Read operation, and 0 for a Write operation (see Table 4).

Table 4. Identification Byte Format

				Logic values at pins A2, A1, and A0 respectively			
1	0	1	0	A2	A1	A0	R/$\overline{W}$
(MSB)							(LSB)

5.6 Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL22326 responds with an ACK. At this time, the device enters its standby state (see Figure 21). The device can receive more than one byte of data by auto incrementing the address after each received byte. Note after reaching the address 08h, the internal pointer “rolls over” to address 00h.

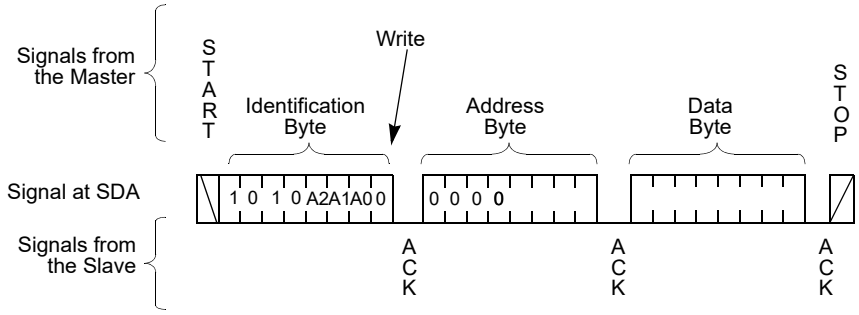


Figure 21. Byte Write Sequence

The non-volatile write cycle starts after STOP condition is determined and it requires up to 20ms delay for the next non-volatile write. Thus, non-volatile registers must be written individually.

5.7 Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (see Figure 22). The master initiates the operation issuing the following sequence: a START, the Identification byte with the R/$\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the R/$\overline{W}$ bit set to “1”. After each of the three bytes, the ISL22326 responds with an ACK. Then the ISL22326 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a $\overline{ACK}$ and a STOP condition) following the last bit of the last Data Byte (see Figure 22).

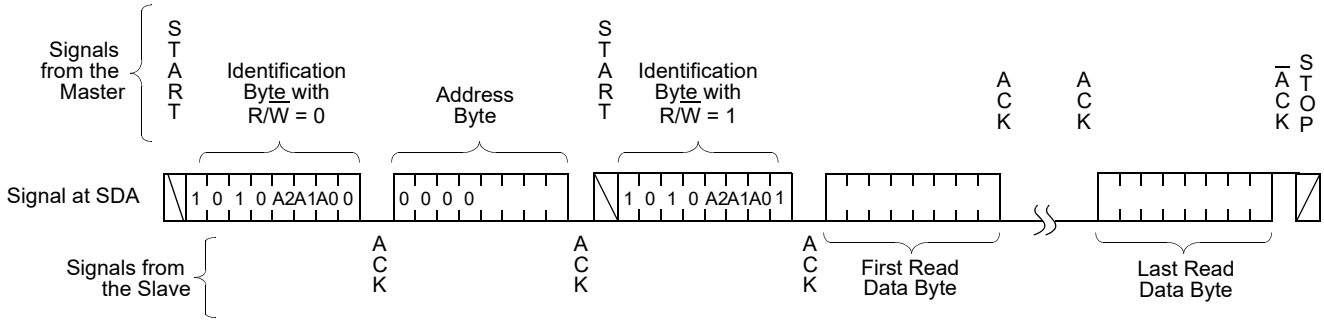


Figure 22. Read Sequence

The Data Bytes are from the registers indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 08h, the pointer rolls over to 00h, and the device continues to output data for each ACK received.

To read back the non-volatile IVR, Renesas recommends that the application reads the ACR first to verify the WIP bit is 0. If the WIP bit (ACR[5]) is not 0, the host should repeat its reading sequence again.

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Ordering Information

Part Number[1][2]	Part Marking	Resistance Option (kΩ)	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type [4]	Temp. Range
ISL22326UFV14Z **(No longer available, recommended replacement: ISL22326WFR16Z-TK)**	22326 UFVZ	50	14 Ld TSSOP	M14.173	Tube	-40 to +125°C
ISL22326UFR16Z **(No longer available, recommended replacement: ISL22326WFR16Z-TK)**	223 26UFZ	50	16 Ld 4x4 QFN	L16.4x4A	Tray	
ISL22326WFV14Z	22326 WFVZ	10	14 Ld TSSOP	M14.173	Tube	
ISL22326WFV14Z-TK					Reel, 1k	
ISL22326WFR16Z	223 26WFZ	10	16 Ld 4x4 QFN	L16.4x4A	Tray	
ISL22326WFR16Z-TK					Reel, 1k	

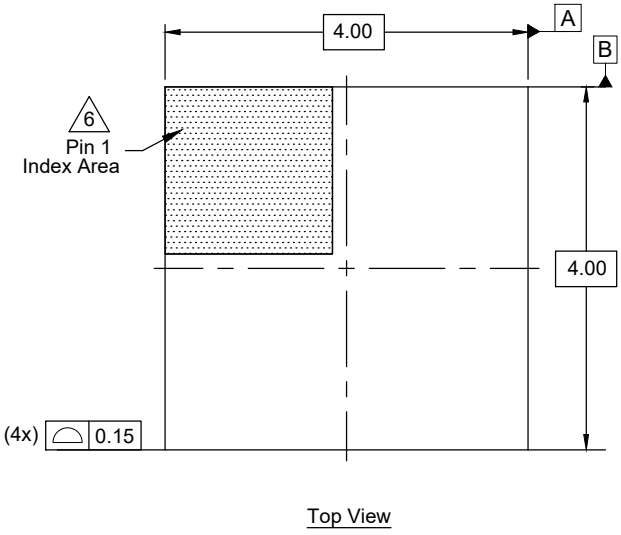
1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL22326 product page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

8. Revision History

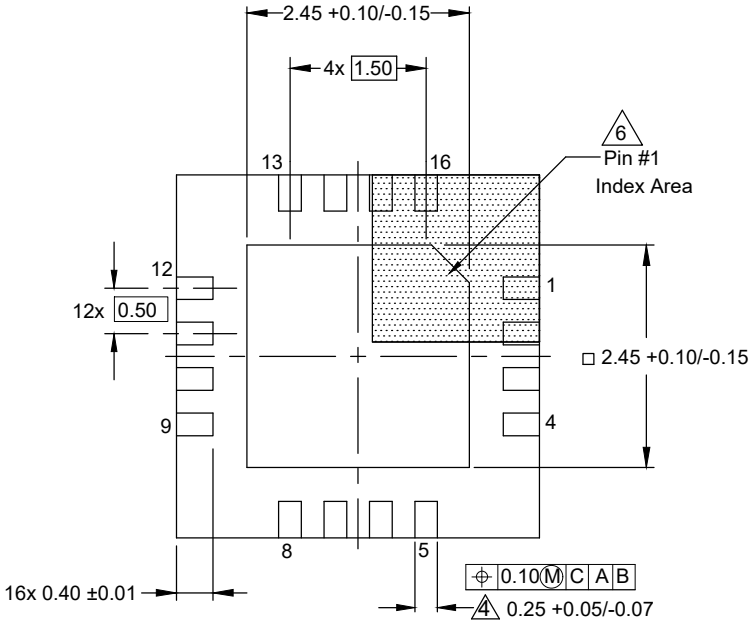
Revision	Date	Description
4.00	Sep 16, 2024	Applied latest template. Updated Ordering table. Updated L16.4x4A POD to the latest version. Removed About Intersil section.
3.00	Sept 9, 2015	Updated Ordering Information table on page 2. Added Revision History and About Intersil sections. Updated Package Outline Drawing L16.4x4A to the latest revision. -Revision 2 to Revision 3 changes - Updated to new POD format by removing table listing dimensions and moving dimensions onto drawing. Added Typical Recommended Land Pattern. Removed package option. Updated Package Outline Drawing M14.173 to the latest revision. -Revision 2 to Revision 3 changes - Updated drawing to remove table and added land pattern.

Package Outline Drawing

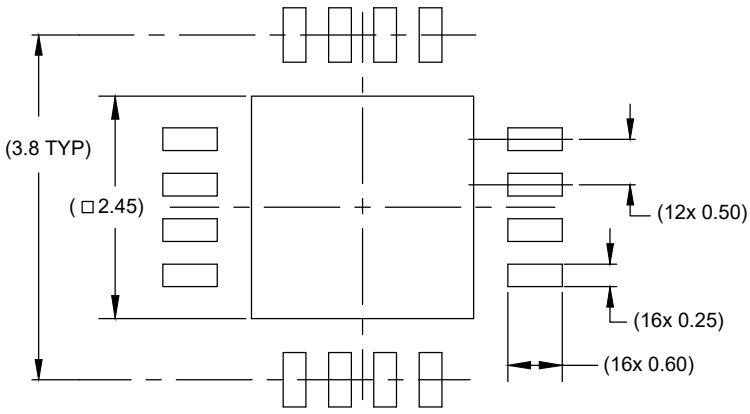
16 Lead Quad Flat No-Lead Plastic Package
L16.4X4A, Revision : 06, Date Created: August 26, 2024



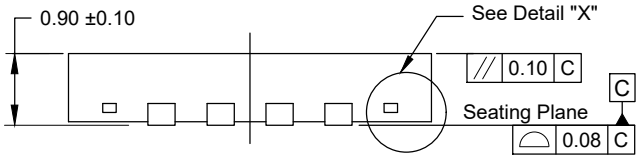
Top View



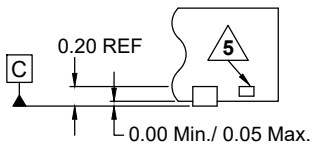
Bottom View



Typical Recommended Land Pattern



Side View



Detail "X"

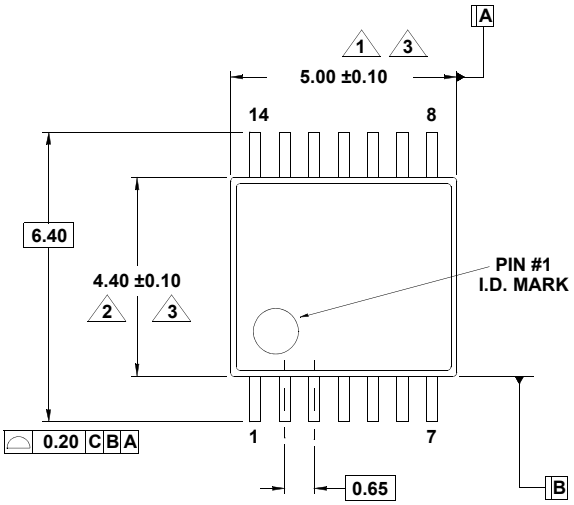
Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASMEY14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

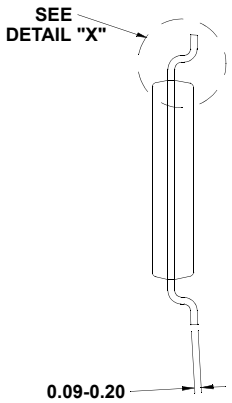
Package Outline Drawing

M14.173

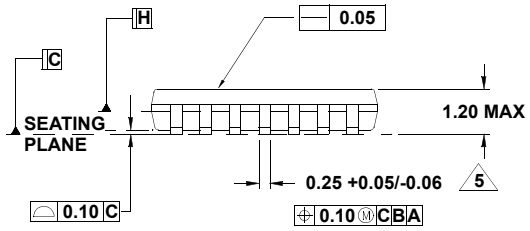
14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)
Rev 3, 10/09



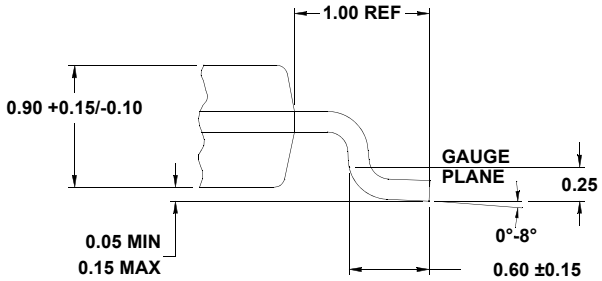
TOP VIEW



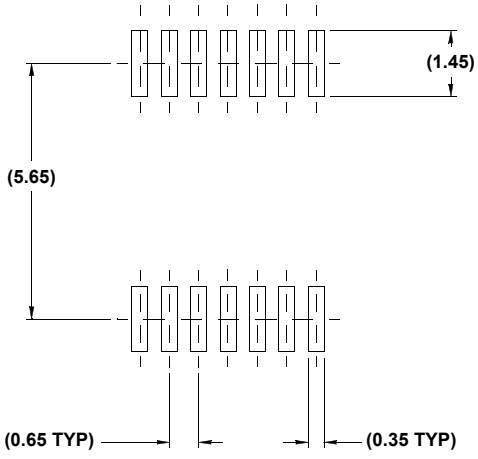
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.

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