

ISL26712, ISL26710, ISL26708

12-Bit, 10-Bit and 8-Bit, 1MSPS SAR ADCs

FN7999

Rev 3.00

September 5, 2012

The ISL26712, ISL26710, ISL26708 are 12-bit, 10-bit and 8-bit, 1MSPS sampling SAR-type ADCs featuring excellent linearity over supply and temperature variations. The robust, fully-differential input offers high impedance to minimize errors due to leakage currents, and the specified measurement accuracy is maintained with input signals up to the supply rails.

The reference accepts inputs from 0.1V to 2.2V for 3V operation and 0.1V to 3.5V for 5V operation, providing design flexibility in a wide variety of applications. The ISL26712/10/08 also features up to 8kV Human Body Model ESD survivability.

The serial digital interface is SPI compatible and is easily interfaced to popular FPGAs and microcontrollers. Power dissipation is 8.5mW at a sampling rate of 1MSPS, and just 5µW between conversions utilizing Auto Power-Down mode (with a 5V supply), making the ISL26712/10/08 excellent solutions for remote industrial sensors and battery-powered instruments.

The ISL26712/10/08 are available in an 8 Ld TDFN or an SOT-23 package, and are specified for operation over the Industrial temperature range (-40°C to +85°C).

Features

- Differential Input
- Simple SPI-compatible Serial Digital Interface
- Guaranteed No Missing Codes
- 1MHz Sampling Rate
- 3V or 5V Operation
- Low Operating Current
 - 1.25mA at 1MSPS with 3V Supplies
 - 1.70mA at 1MSPS with 5V Supplies
- Power-down Current between Conversions: 1µA
- Excellent Differential Non-Linearity
- Low THD: -83dB (typ)
- Pb-Free (RoHS Compliant)
- Available in TDFN Package (3x3mm)
- Available in SOT-23 Package

Applications

- Remote Data Acquisition
- Battery Operated Systems
- Industrial Process Control
- Energy Measurement
- Data Acquisition Systems
- Pressure Sensors
- Flow Controllers

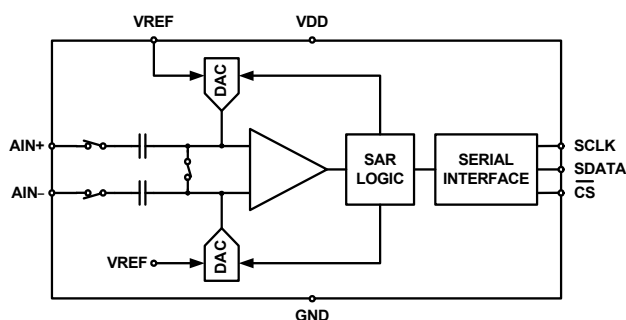


FIGURE 1. BLOCK DIAGRAM

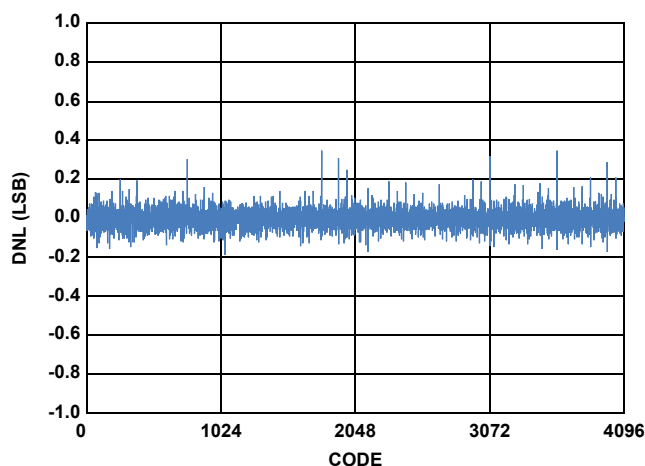
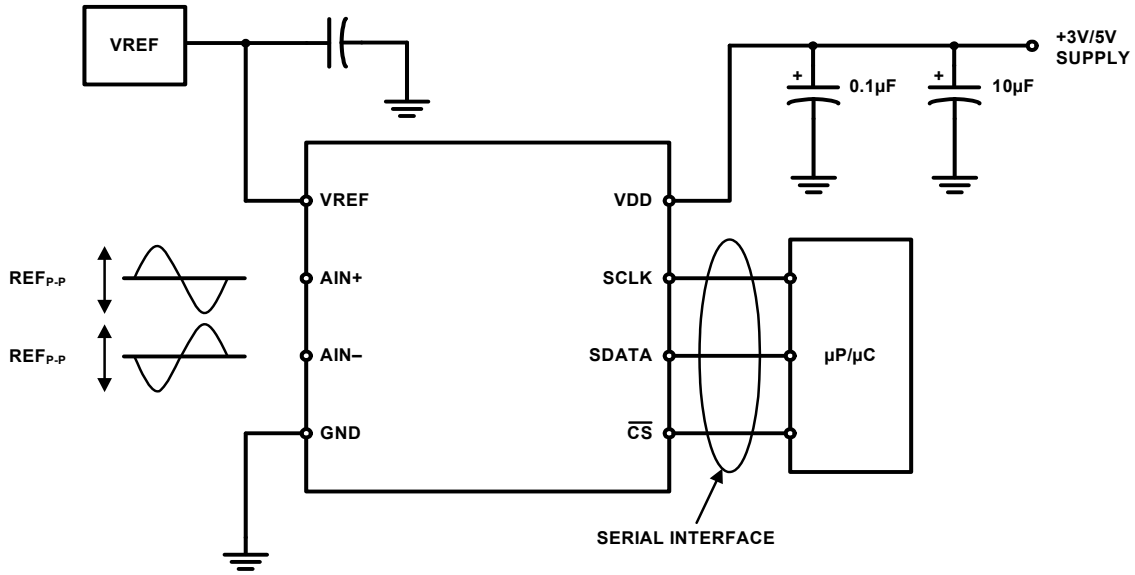


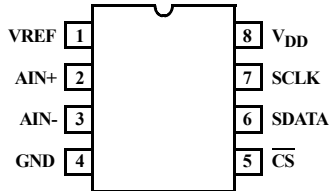
FIGURE 2. ISL26712 DIFFERENTIAL LINEARITY ERROR vs CODE

Typical Connection Diagram

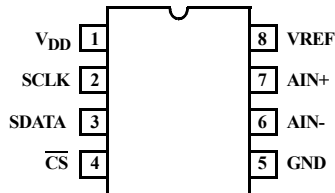


Pin Configurations

ISL26712/10/08
(8 LD TDFN)
TOP VIEW



ISL26712/10/08
(8 LD SOT-23)
TOP VIEW



Pin Description

ISL26712/10/08			DESCRIPTION
PIN NAME	PIN NUMBER (TDFN)	PIN NUMBER (SOT-23)	
VDD	8	1	Supply voltage, +2.7V to 5.25V.
SCLK	7	2	Serial clock input. Controls digital I/O timing and clocks the conversion.
SDATA	6	3	Digital conversion output.
CS	5	4	Chip select input. Generally controls the start of a conversion though not always the sampling signal.
GND	4	5	Ground
AIN-	3	6	Negative analog input.
AIN+	2	7	Positive analog input.
VREF	1	8	Reference voltage.

Pin-Compatible Family

PART NUMBER	RESOLUTION (Bits)
ISL26712	12
ISL26710	10
ISL26708	8

Ordering Information

PART NUMBER (Note 4)	PART MARKING	VDD RANGE (V)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL26712IRTZ (Note 3)	6712	2.7 to 5.25	-40 to +85	8 Ld TDFN	L8.3x3I
ISL26712IRTZ-T (Notes 1, 3)	6712	2.7 to 5.25	-40 to +85	8 Ld TDFN	L8.3x3I
ISL26712IRTZ-T7A (Notes 1, 3)	6712	2.7 to 5.25	-40 to +85	8 Ld TDFN	L8.3x3I
ISL26710IRTZ (Note 3)	6710	2.7 to 5.25	-40 to +85	8 Ld TDFN	L8.3x3I
ISL26710IRTZ-T (Notes 1, 3)	6710	2.7 to 5.25	-40 to +85	8 Ld TDFN	L8.3x3I
ISL26710IRTZ-T7A (Notes 1, 3)	6710	2.7 to 5.25	-40 to +85	8 Ld TDFN	L8.3x3I
ISL26708IRTZ (Note 3)	6708	2.7 to 5.25	-40 to +85	8 Ld TDFN	L8.3x3I
ISL26708IRTZ-T (Notes 1, 3)	6708	2.7 to 5.25	-40 to +85	8 Ld TDFN	L8.3x3I
ISL26712IHZ-T (Notes 1, 2)	6712 (Note 5)	2.7 to 5.25	-40 to +85	8 Ld SOT-23	P8.064
ISL26712IHZ-T7A (Notes 1, 2)	6712 (Note 5)	2.7 to 5.25	-40 to +85	8 Ld SOT-23	P8.064
ISL26710IHZ-T (Notes 1, 2)	6710 (Note 5)	2.7 to 5.25	-40 to +85	8 Ld SOT-23	P8.064
ISL26710IHZ-T7A (Notes 1, 2)	6710 (Note 5)	2.7 to 5.25	-40 to +85	8 Ld SOT-23	P8.064
ISL26708IHZ-T (Notes 1, 2)	6708 (Note 5)	2.7 to 5.25	-40 to +85	8 Ld SOT-23	P8.064
ISL26708IHZ-T7A (Notes 1, 2)	6708 (Note 5)	2.7 to 5.25	-40 to +85	8 Ld SOT-23	P8.064

NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for [ISL26712](#), [ISL26710](#), [ISL26708](#). For more information on MSL please see techbrief [TB363](#).
5. The part marking is located on the bottom of the part.

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Absolute Maximum Ratings

Any Pin to GND	-0.3V to +6.0V
Analog Input to GND	-0.3V to $V_{DD} + 0.3V$
Digital I/O to GND	-0.3V to $V_{DD} + 0.3V$
Digital Input Voltage to GND	-0.3V to $V_{DD} + 0.3V$
Maximum Current In to Any Pin	10mA
ESD Rating	
Human Body Model (Tested per JESD22-A114F)	8kV
Machine Model (Tested per JESD22-A115B)	400V
Charged Device Model (Tested per JESD22-C101E)	
TDFN Package	2.0kV
SOT-23 Package	1.5kV
Latch Up (Tested per JESD78C; Class 2, Level A)	100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^{\circ}C/W$)	θ_{JC} ($^{\circ}C/W$)
8 Ld TDFN Package (Notes 6, 8)	41	6
8 Ld SOT-23 Package (Notes 7, 9)	135	99
Operating Temperature	-40 $^{\circ}C$ to +85 $^{\circ}C$	
Storage Temperature	-65 $^{\circ}C$ to +150 $^{\circ}C$	
Junction Temperature	+150 $^{\circ}C$	
Pb-Free Reflow Profile	see link below	
	http://www.intersil.com/pbfree/Pb-FreeReflow.asp	

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief [TB379](#).
- θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.
- For θ_{JC} , the "case temp" location is taken at the package top center.

Electrical Specifications $V_{DD} = +3.0V$ to $+3.6V$, $F_{SCLK} = 18MHz$, $F_S = 1MSPS$, $V_{REF} = 2.0V$; $V_{DD} = +4.75V$ to $+5.25V$, $F_{SCLK} = 18MHz$, $F_S = 1MSPS$, $V_{REF} = 2.5V$; $V_{CM} = V_{REF}$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$. **Boldface limits apply over the operating temperature range, -40 $^{\circ}C$ to +85 $^{\circ}C$.**

SYMBOL	PARAMETER	TEST CONDITIONS	ISL26712			ISL26710			ISL26708			UNITS
			MIN (Note 10)	TYP	MAX (Note 10)	MIN (Note 10)	TYP	MAX (Note 10)	MIN (Note 10)	TYP	MAX (Note 10)	
DYNAMIC PERFORMANCE												
SINAD	Signal-to (Noise + Distortion) Ratio	$F_{IN} = 100kHz$ $V_{DD} = +4.75V$ to $+5.25V$	70.0	71.4		61.0	61.6		49.0	49.8		dB
		$F_{IN} = 100kHz$ $V_{DD} = +3.0V$ to $+3.6V$	68.5	70.5		60.7	61.5		49.0	49.8		dB
THD	Total Harmonic Distortion	$F_{IN} = 100kHz$ $V_{DD} = +4.75V$ to $+5.25V$		-84	-76		-82	-74		-75	-60	dB
		$F_{IN} = 100kHz$ $V_{DD} = +3.0V$ to $+3.6V$		-84	-74		-82	-72		-73	-60	dB
SFDR	Spurious Free Dynamic Range	$F_{IN} = 100kHz$ $V_{DD} = +4.75V$ to $+5.25V$		-87	-76		-82	-76		-68	-60	dB
		$F_{IN} = 100kHz$ $V_{DD} = +3.0V$ to $+3.6V$		-85	-74		-82	-74		-68	-60	dB
IMD	Intermodulation Distortion	2nd and 3rd order, $F_{IN} = 90kHz, 110kHz$		-89			-83			-81		dB
tpd	Aperture Delay			1			1			1		ns
Δtpd	Aperture Jitter			15			15			15		ps
$\beta 3dB$	Full Power Bandwidth	@ -3dB		15			15			15		MHz
DC ACCURACY												
N	Resolution		12			10			8			Bits
INL	Integral Nonlinearity		-1	± 0.4	1	-0.5	± 0.1	0.5	-0.2	± 0.03	0.2	LSB
DNL	Differential Nonlinearity	Guaranteed no missing codes	-0.95	± 0.3	0.95	-0.5	± 0.1	0.5	-0.2	± 0.03	0.2	LSB
OFFSET	Zero-Code Error	Zero Volt Differential Input	-6	± 0.2	6	-2.5	± 0.2	2.5	-1.25	± 0.03	1.25	LSB

Electrical Specifications $V_{DD} = +3.0V$ to $+3.6V$, $F_{SCLK} = 18MHz$, $F_S = 1MSPS$, $V_{REF} = 2.0V$; $V_{DD} = +4.75V$ to $+5.25V$, $F_{SCLK} = 18MHz$, $F_S = 1MSPS$, $V_{REF} = 2.5V$; $V_{CM} = V_{REF}$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+85^\circ C$.** (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	ISL26712			ISL26710			ISL26708			UNITS
			MIN (Note 10)	TYP	MAX (Note 10)	MIN (Note 10)	TYP	MAX (Note 10)	MIN (Note 10)	TYP	MAX (Note 10)	
GAIN	Positive Gain Error	$\pm V_{REF}$ input range	-2	± 0.1	2	-1	± 0.1	1	-0.75	± 0.04	0.75	LSB
	Negative Gain Error		-2	± 0.1	2	-1	± 0.1	1	-0.75	± 0.04	0.75	LSB
ANALOG INPUT (Note 11)												
AIN	Full-Scale Input Span	$2 \times V_{REF}$	$(AIN+) - (AIN-)$			$(AIN+) - (AIN-)$			$(AIN+) - (AIN-)$			V
AIN+, AIN-	Absolute Input Voltage Range		$V_{CM} \pm V_{REF}/2$			$V_{CM} \pm V_{REF}/2$			$V_{CM} \pm V_{REF}/2$			V
	AIN+	$V_{CM} = V_{REF}$	$V_{CM} \pm V_{REF}/2$			$V_{CM} \pm V_{REF}/2$			$V_{CM} \pm V_{REF}/2$			V
AIN-	$V_{CM} \pm V_{REF}/2$			$V_{CM} \pm V_{REF}/2$			$V_{CM} \pm V_{REF}/2$			V		
I _{LEAK}	Input DC Leakage Current		-1		1	-1		1	-1		1	μA
C _{VIN}	Input Capacitance	Track/Hold mode		13/5			13/5			13/5		pF
REFERENCE INPUT												
V _{REF}	V _{REF} Input Voltage Range	$V_{DD} = 3V$ (1% tolerance for specified performance)		2.0			2.0			2.0		V
		$V_{DD} = 5V$ (1% tolerance for specified performance)		2.5			2.5			2.5		V
I _{LEAK}	DC Leakage Current		-1		1	-1		1	-1		1	μA
C _{REF}	V _{REF} Input Capacitance	Track/Hold mode		21/18.5			21/18.5			21/18.5		pF
LOGIC INPUTS												
V _{IH}	Input High Voltage		2.4			2.4			2.4			V
V _{IL}	Input Low Voltage			0.8			0.8			0.8		V
I _{LEAK}	Input Leakage Current		-1		1	-1		1	-1		1	μA
C _{IN}	Input Capacitance			10			10			10		pF
LOGIC OUTPUTS												
V _{OH}	Output High Voltage	I _{SOURCE} = 200 μA	V_{DD} - 0.3			V_{DD} - 0.3			V_{DD} - 0.3			V
V _{OL}	Output Low Voltage	I _{SINK} = 200 μA		0.4			0.4			0.4		V
I _{OZ}	Floating-State Output Current		-1		1	-1		1	-1		1	μA
C _{OUT}	Floating-State Output Capacitance			10			10			10		pF
	Output Coding		Two's Complement									
CONVERSION RATE												
t _{CONV}	Conversion Time	F _{SCLK} = 18MHz			888			888			888	ns
t _{ACQ}	Acquisition Time	F _{SCLK} = 18MHz			200			200			200	ns
F _{max}	Throughput Rate				1000			1000			1000	kSPS
POWER REQUIREMENTS												
V _{DD}	Positive Supply Voltage Range		2.7		3.6	2.7		3.6	2.7		3.6	V
			4.75		5.25	4.75		5.25	4.75		5.25	V

Electrical Specifications $V_{DD} = +3.0V$ to $+3.6V$, $f_{SCLK} = 18MHz$, $f_S = 1MSPS$, $V_{REF} = 2.0V$; $V_{DD} = +4.75V$ to $+5.25V$, $f_{SCLK} = 18MHz$, $f_S = 1MSPS$, $V_{REF} = 2.5V$; $V_{CM} = V_{REF}$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+85^\circ C$.** (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	ISL26712			ISL26710			ISL26708			UNITS
			MIN (Note 10)	TYP	MAX (Note 10)	MIN (Note 10)	TYP	MAX (Note 10)	MIN (Note 10)	TYP	MAX (Note 10)	
I_{DD}	Positive Supply Input Current											
	Static				1			1			1	μA
	Dynamic	3V			1250			1250			1250	μA
		5V			1700			1700			1700	μA
	Power Dissipation											
	Static Mode	$V_{DD} = 3V$			3			3			3	μW
		$V_{DD} = 5V$			5			5			5	μW
	Dynamic	$V_{DD} = 3V, f_{smp1} = 1MSPS$			3.75			3.75			3.75	mW
		$V_{DD} = 5V, f_{smp1} = 1MSPS$			8.50			8.50			8.50	mW

NOTES:

10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
 11. The absolute voltage applied to each analog input must be between GND and V_{DD} to guarantee datasheet performance.

Timing Specifications $V_{DD} = 3.0V$ to $3.6V$, $f_{SCLK} = 18MHz$, $f_S = 1MSPS$, $V_{REF} = 2.0V$; $V_{DD} = 4.75V$ to $5.25V$, $f_{SCLK} = 18MHz$, $f_S = 1MSPS$, $V_{REF} = 2.5V$; $V_{CM} = V_{REF}$, unless otherwise noted. **Boldface limits apply over the operating temperature range, $-40^\circ C$ to $+85^\circ C$.**

SYMBOL	PARAMETER (Note 12)	TEST CONDITIONS	MIN (Note 10)	TYP	MAX (Note 10)	UNITS
fSCLK	Clock Frequency		0.01		18	MHz
tSCLK	Clock Period		55			ns
tACQ	Acquisition Time (Note 13)					ns
tCONV	Conversion Time				888	ns
tCSW	\overline{CS} Pulse Width		10			ns
tCSS	\overline{CS} Falling Edge to SCLK Falling Edge Setup Time		10			ns
tCDV	\overline{CS} Falling Edge to SDATA Valid				20	ns
tCLKDV	SCLK Falling Edge to SDATA Valid				40	ns
tSDH	SCLK Falling Edge to SDATA Hold		10			ns
tSW	SCLK Pulse Width			$0.4 \times t_{SCLK}$	$0.6 \times t_{SCLK}$	ns
tDISABLE	CSB Rising Edge to SDATA Disable Time (Note 14)	Extrapolated back to true bus relinquish	10		35	ns
tQUIET	Quiet Time Before Sample		60			ns

NOTES:

12. Limits established by characterization and are not production tested.
 13. See "ACQUISITION TIME" on page 17.
 14. During characterization, tDISABLE is measured from the release point with a 10pF load (see Figure 4).

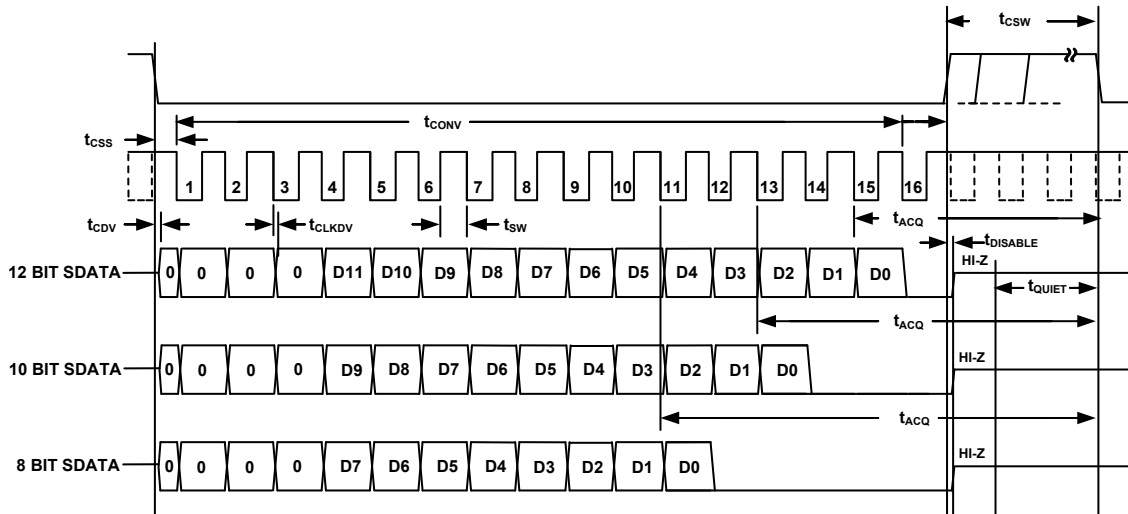


FIGURE 3. SERIAL INTERFACE TIMING DIAGRAM

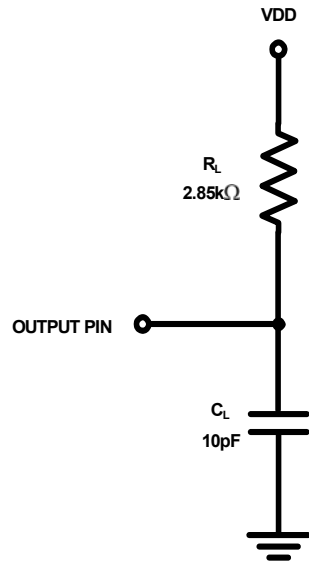


FIGURE 4. EQUIVALENT LOAD CIRCUIT

Typical Performance Characteristics

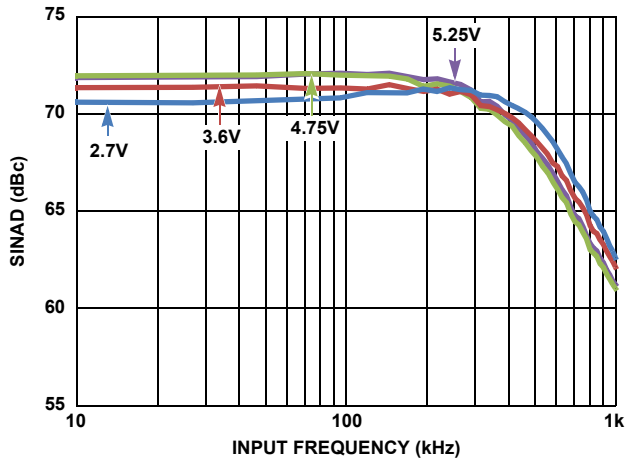


FIGURE 5. ISL26712 SINAD vs ANALOG INPUT FREQUENCY FOR VARIOUS SUPPLY VOLTAGES

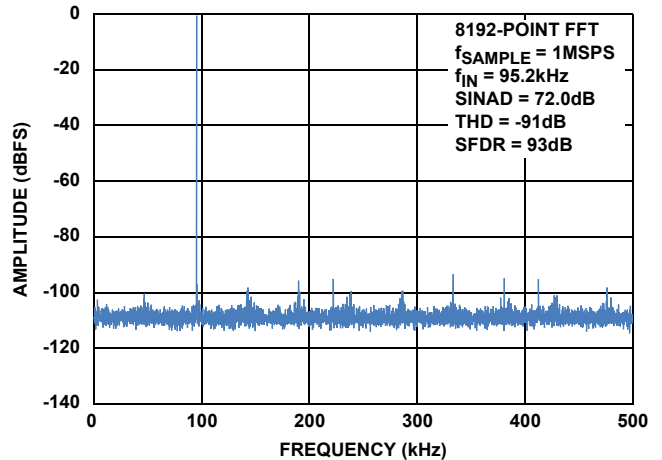


FIGURE 6. ISL26712 DYNAMIC PERFORMANCE WITH VDD = 5V

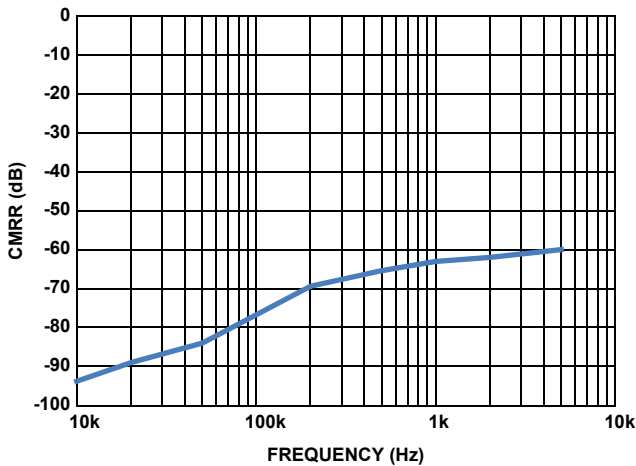


FIGURE 7. CMRR vs FREQUENCY FOR VDD = 5V

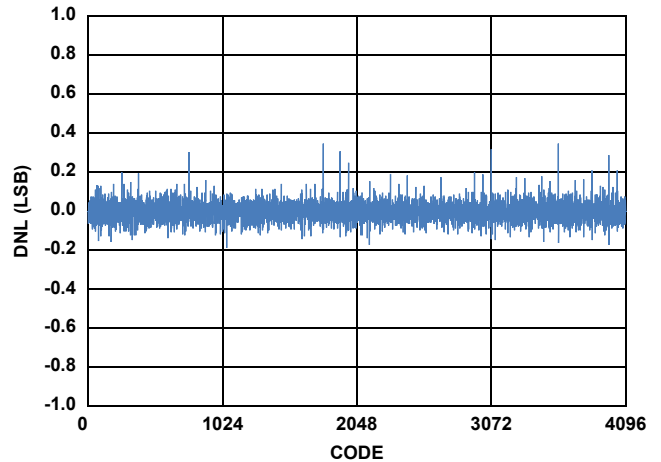


FIGURE 8. TYPICAL DNL FOR THE ISL26712 FOR VDD = 5V

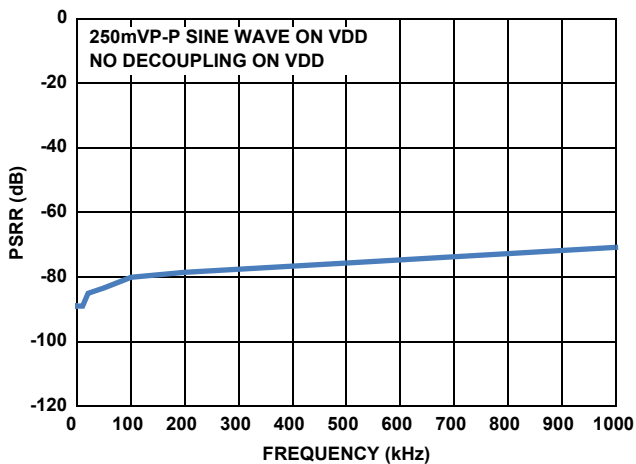


FIGURE 9. PSRR vs SUPPLY RIPPLE FREQUENCY WITHOUT SUPPLY DECOUPLING

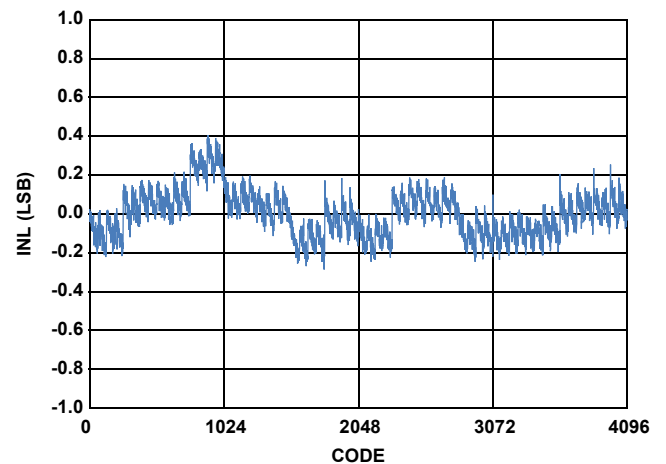


FIGURE 10. TYPICAL INL FOR THE ISL26712 FOR VDD = 5V

Typical Performance Characteristics (Continued)

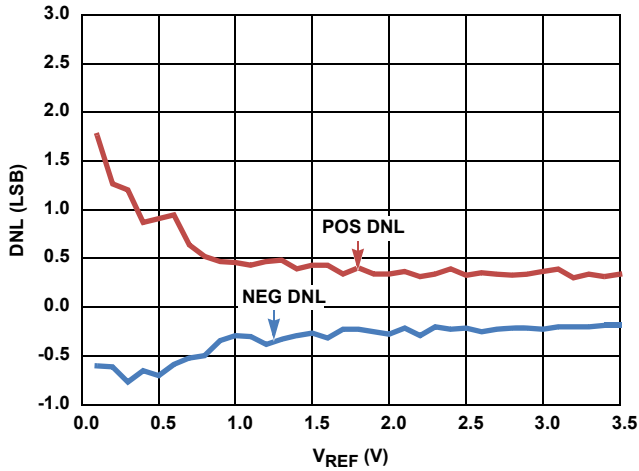


FIGURE 11. CHANGE IN DNL vs VREF FOR THE ISL26712 FOR VDD = 5V

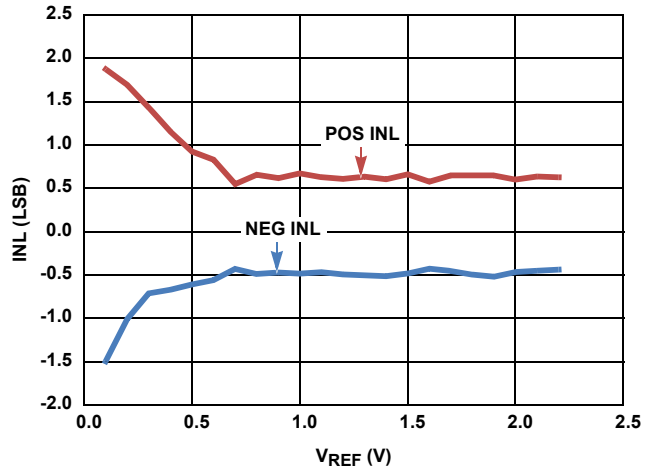


FIGURE 12. CHANGE IN INL vs VREF FOR THE ISL26712 FOR VDD = 3V

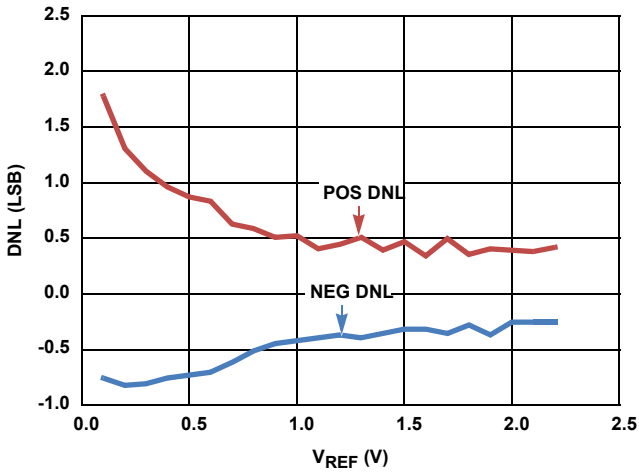


FIGURE 13. CHANGE IN DNL vs VREF FOR THE ISL26712 FOR VDD = 3V

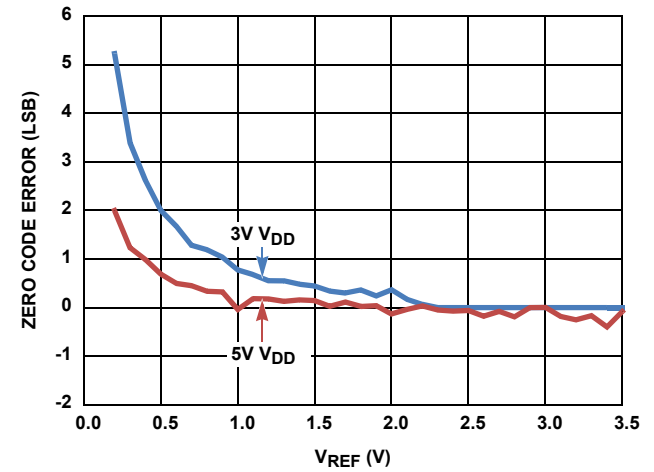


FIGURE 14. CHANGE IN OFFSET ERROR vs REFERENCE VOLTAGE FOR VDD = 5V AND 3V FOR THE ISL26712

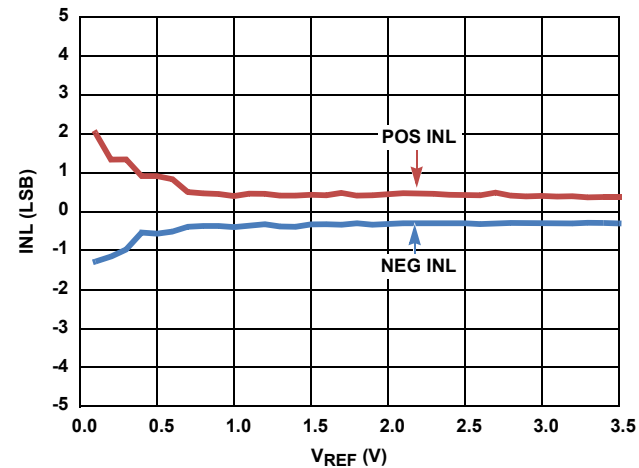


FIGURE 15. CHANGE IN INL vs VREF FOR THE ISL26712 FOR VDD = 5V

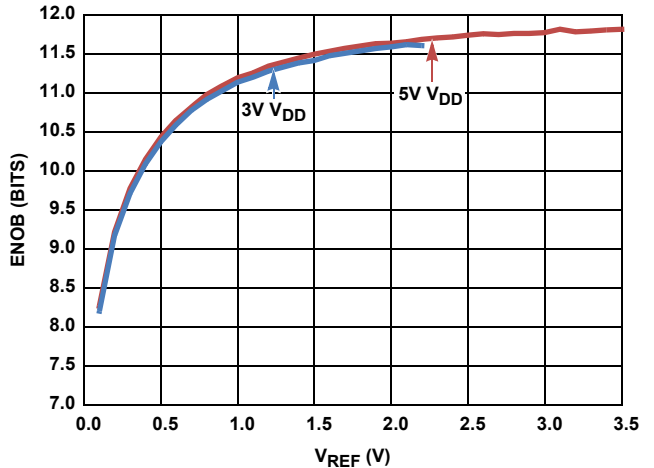


FIGURE 16. CHANGE IN ENOB vs REFERENCE VOLTAGE FOR VDD = 5V AND 3V FOR THE ISL26712

Typical Performance Characteristics (Continued)

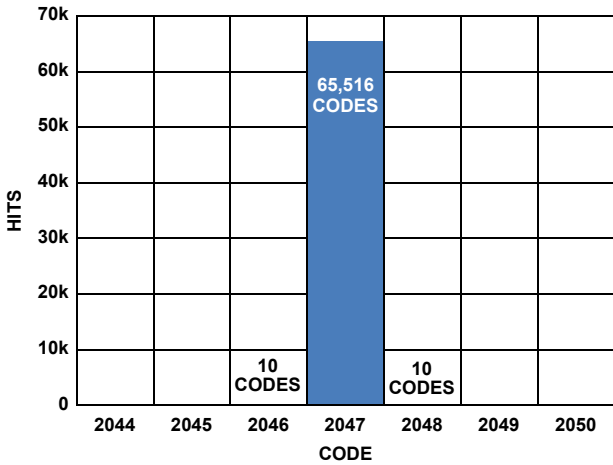


FIGURE 17. HISTOGRAM OF 10,000 CONVERSIONS OF A DC INPUT FOR THE ISL26712 WITH VDD = 5V

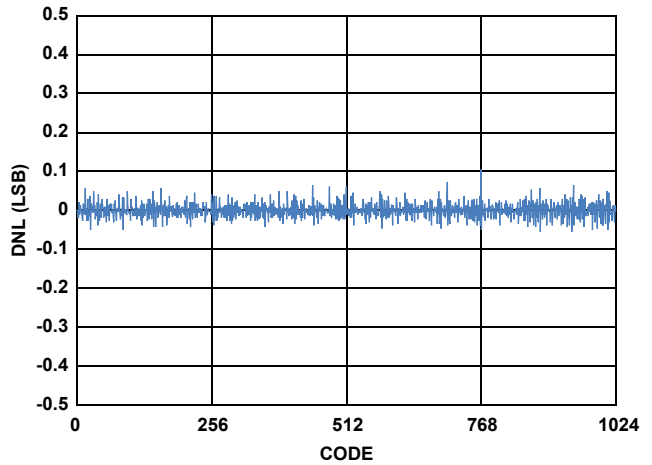


FIGURE 18. TYPICAL DNL FOR THE ISL26710 FOR VDD = 5V

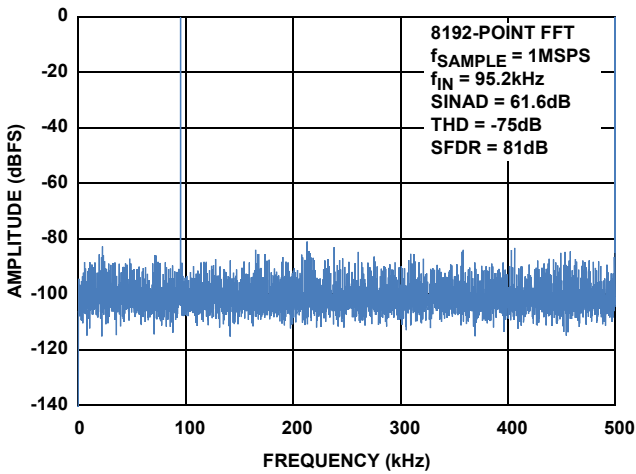


FIGURE 19. ISL26710 DYNAMIC PERFORMANCE WITH VDD = 5V

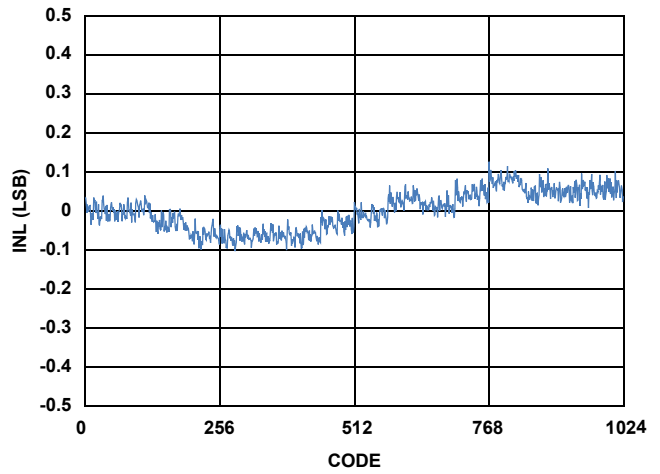


FIGURE 20. TYPICAL INL FOR THE ISL26710 FOR VDD = 5V

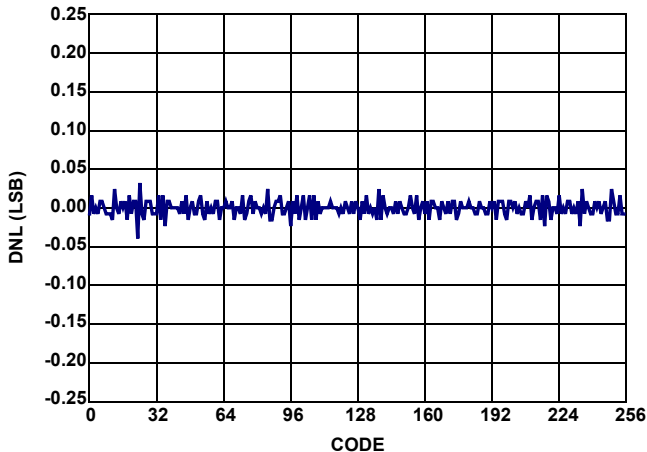


FIGURE 21. TYPICAL DNL FOR THE ISL26708 FOR VDD = 5V

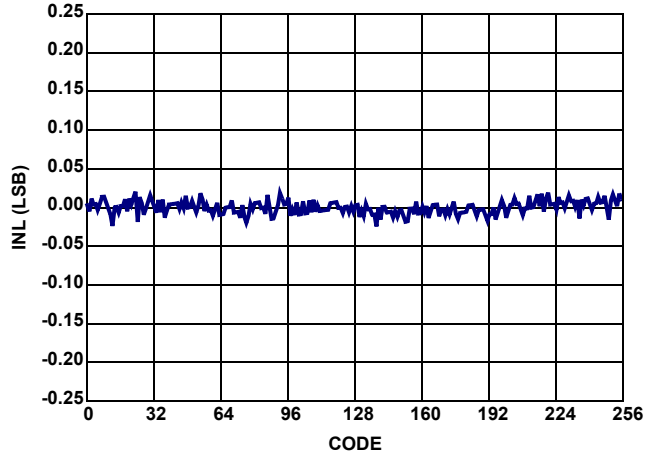


FIGURE 22. TYPICAL INL FOR THE ISL26708 FOR VDD = 5V

Typical Performance Characteristics (Continued)

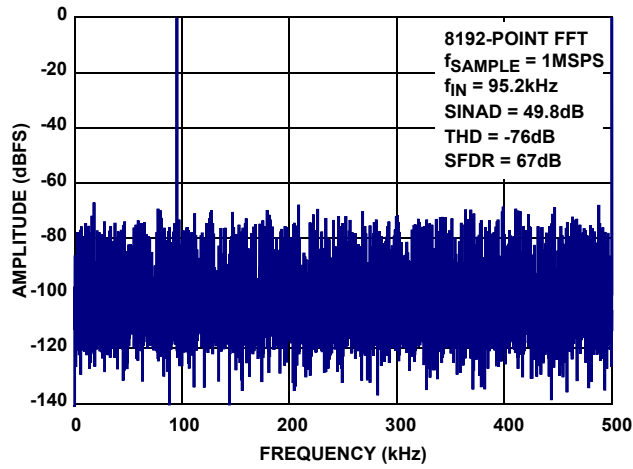


FIGURE 23. ISL26708 DYNAMIC PERFORMANCE WITH VDD = 5V

Functional Description

The ISL26712/10/08 are based on a successive approximation register (SAR) architecture utilizing capacitive charge redistribution digital-to-analog converters (DACs). Figure 24 shows a simplified representation of the converter. During the acquisition phase (ACQ), the differential input is stored on the sampling capacitors (CS). The comparator is in a balanced state since the switch across its inputs is closed. The signal is fully acquired after t_{ACQ} has elapsed and the switches then transition to the conversion phase (CONV) so the stored voltage may be converted to digital format. The comparator will become unbalanced when the differential switch opens and the input switches transition (assuming that the stored voltage is not exactly at mid-scale). The comparator output reflects whether the stored voltage is above or below mid-scale, which sets the value of the MSB. The SAR logic then forces the capacitive DACs to adjust up or down by one quarter of full-scale by switching in binarily weighted capacitors. Again, the comparator output reflects whether the stored voltage is above or below the new value, setting the value of the next lowest bit. This process repeats until all 12 bits have been resolved.

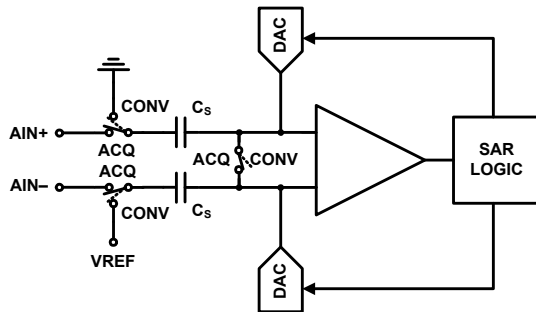


FIGURE 24. SAR ADC ARCHITECTURAL BLOCK DIAGRAM

An external clock must be applied to the SCLK pin to generate a conversion result. The allowable frequency range for SCLK is 10kHz to 18MHz (556SPS to 1MSPS). Serial output data is transmitted on the falling edge of SCLK. The receiving device (FPGA, DSP or Microcontroller) may latch the data on the rising edge of SCLK to maximize set-up and hold times.

A stable, low-noise reference voltage must be applied to the VREF pin to set the full-scale input range and common-mode voltage. See “Voltage Reference Input” on page 14 for more details.

ADC Transfer Function

The output coding for the ISL26712/10/08 is two's complement. The first code transition occurs at successive LSB values (i.e., 1 LSB, 2 LSB, and so on). The LSB size of the ISL26712 is $2 \cdot V_{REF} / 4096$, while the LSB size of the ISL26710 is $2 \cdot V_{REF} / 1024$ and the ISL26708 is $2 \cdot V_{REF} / 512$. The ideal transfer characteristic of the ISL26712/10/08 is shown in Figure 25.

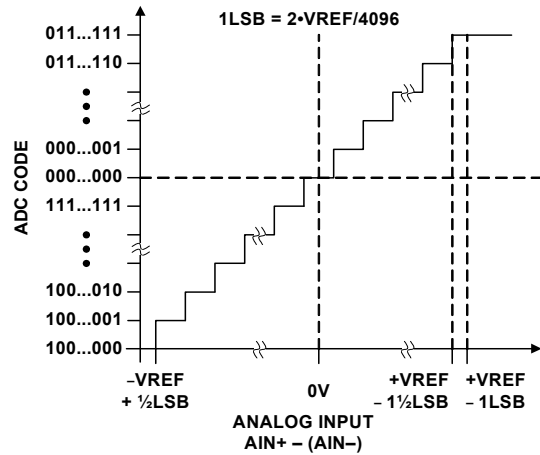


FIGURE 25. IDEAL TRANSFER CHARACTERISTICS

Analogue Input

The ISL26712/10/08 feature a fully differential input with a nominal full-scale range equal to twice the applied VREF voltage. Each input swings V_{REF} V_{p-p}, 180° out-of-phase from one another for a total differential input of $2 \cdot V_{REF}$ (refer to Figure 26).

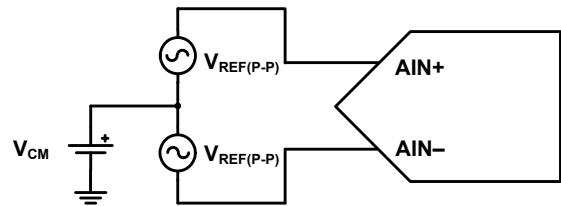


FIGURE 26. DIFFERENTIAL INPUT SIGNALING

Differential signaling offers several benefits over a single-ended input, such as:

- Doubling of the full-scale input range (and therefore the dynamic range)
- Improved even order harmonic distortion
- Better noise immunity due to common mode rejection

Figure 27 shows the relationship between the reference voltage and the full-scale input range for two different values of VREF. Note that there is a trade-off between VREF and the allowable common mode input voltage (VCM). The full-scale input range is proportional to VREF; therefore the VCM range must be limited for larger values of VREF in order to keep the absolute maximum and minimum voltages on the AIN+ and AIN- pins within specification. Figures 28 and 29 illustrate this relationship for 5V and 3V operation, respectively. The dashed lines show the theoretical VCM range based solely on keeping the AIN+ and AIN- pins within the supply rails. Additional restrictions are imposed due to the required headroom of the input circuitry, resulting in practical limits shown by the shaded area.

Voltage Reference Input

An external low-noise reference voltage must be applied to the VREF pin to set the full-scale input range of the converter. The reference input accepts voltages ranging from 0.1V to 2.2V for 3V operation and 0.1V to 3.5V for 5V operation. The device is specified with a reference voltage of 2.5V for 5V operation and 2.0V for 3V operation.

Figures 30 and 31 illustrate possible voltage reference options for the ISL267440/ISL26750A or ISL267817. Figure 30 uses the precision ISL21090 voltage reference which exhibits exceptionally low drift and low noise. The ISL21090 must use a power supply greater than 4.7V. The VREF input pin of the ISL267XX devices uses very low current, so the decoupling capacitor can be small (0.1µF).

Figure 31 illustrates the ISL21010 voltage reference being used with these ADCs. The ISL21010 series voltage references have higher noise and drift than the ISL26090 devices, but they consume very low operating current and are excellent for battery-powered applications.

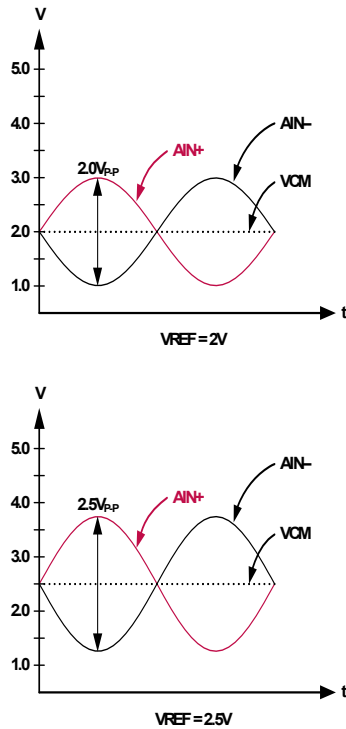


FIGURE 27. RELATIONSHIP BETWEEN VREF AND FULL-SCALE RANGE

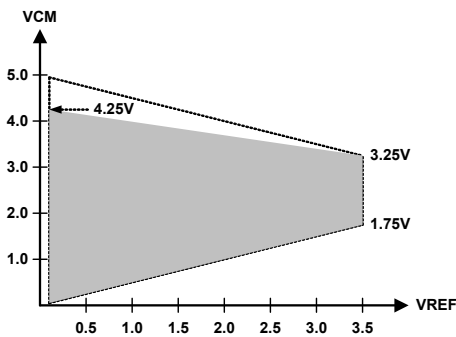


FIGURE 28. RELATIONSHIP BETWEEN VREF AND VCM FOR VDD = 5V

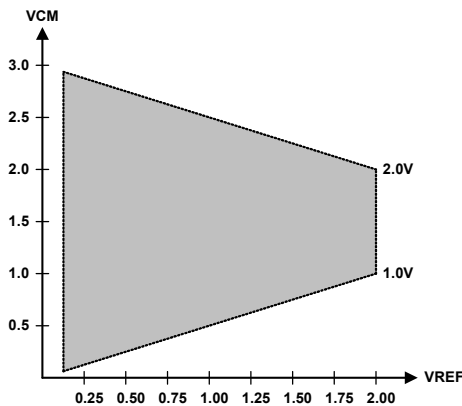


FIGURE 29. RELATIONSHIP BETWEEN VREF AND VCM FOR VDD = 3V

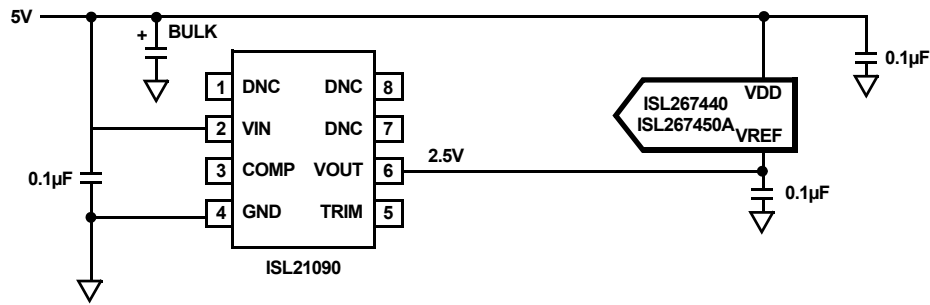


FIGURE 30. PRECISION VOLTAGE REFERENCE FOR +5V SUPPLY

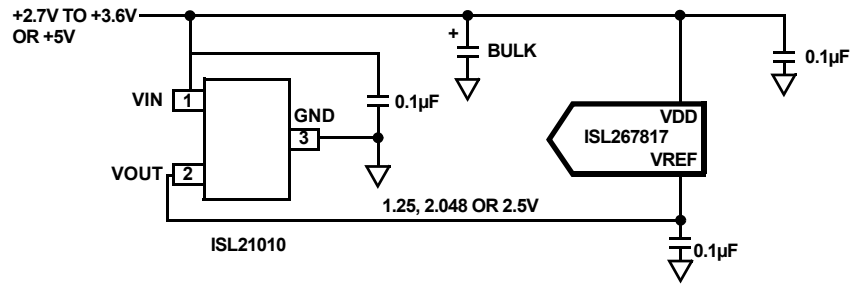


FIGURE 31. VOLTAGE REFERENCE FOR +2.7V TO +3.6V, OR FOR +5V SUPPLY

Converter Operation

The ISL26712, ISL26710 and ISL26708 are designed to minimize power consumption by only powering up the SAR comparator during conversion time. When the converter is in track mode (its sample capacitors are tracking the input signal) the SAR comparator is powered down. The state of the converter is dictated by the logic state of \overline{CS} . When \overline{CS} is high the SAR comparator is powered down while the sampling capacitor array is tracking the input. When \overline{CS} transitions low, the capacitor array immediately captures the analog signal that is being tracked. After \overline{CS} is taken low, the SCLK pin is toggled 16 times. For the first 3 clocks, the comparator is powered up and auto-zeroed, then the SAR decision process is begun. This process uses 12 SCLK cycles for the 12-bit ISL26712. Each SAR decision is presented to the SDATA output on the next clock cycle after the SAR decision is performed. The SAR process (12 bits) is completed on SCLK cycle 15. At this point in time, the SAR comparator is powered down and the capacitor array is placed back into Track mode. The last SAR comparator decision is output from SDATA on the 16th SCLK cycle. When the last data bit is output from SDATA the output switches to a logic 0 until \overline{CS} is taken high, at which time, the SDATA output enters a High-Z state.

The ISL26710 and ISL26708 will take fewer clock cycles for their SAR decisions and will output fewer data bits. The extra bits following the output of the LSB will be logic zeroes.

Figures 32, 33, and 34 illustrate the system timing for the 12-, 10- and 8-bit converters respectively.

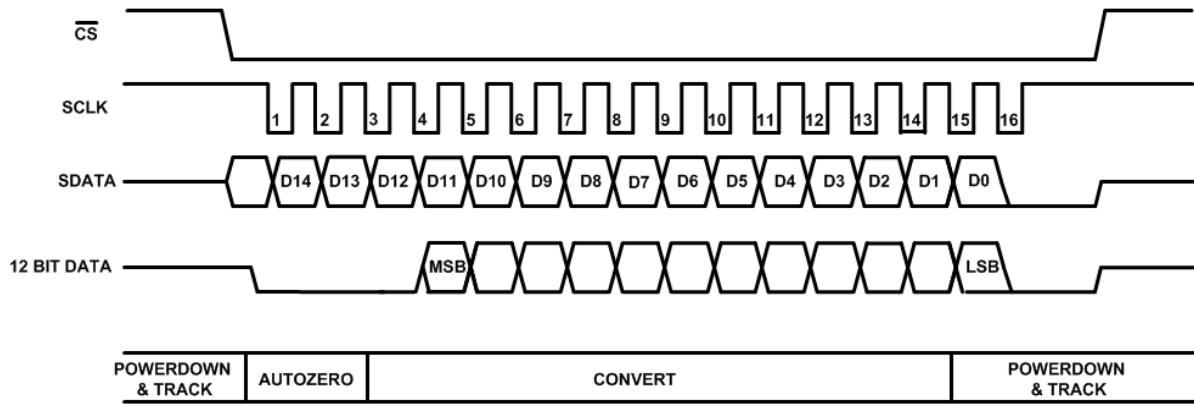


FIGURE 32. ISL26712 SYSTEM TIMING

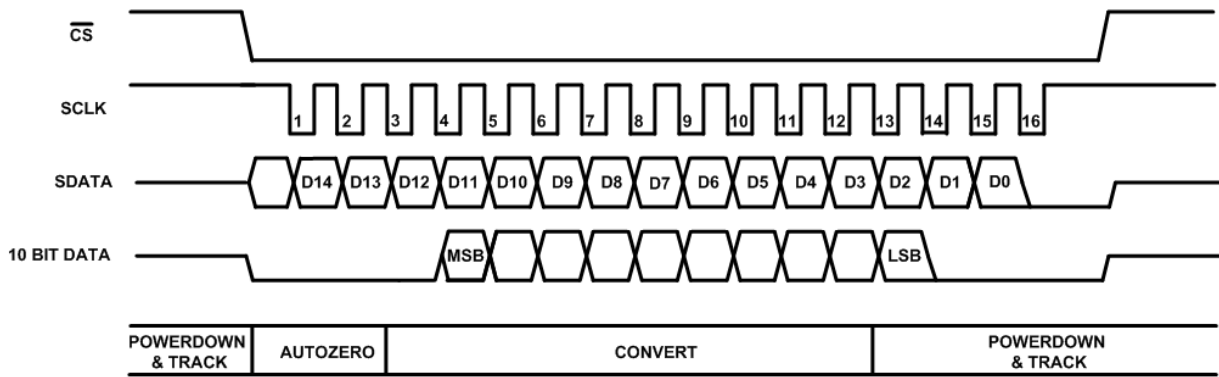


FIGURE 33. ISL26710 SYSTEM TIMING

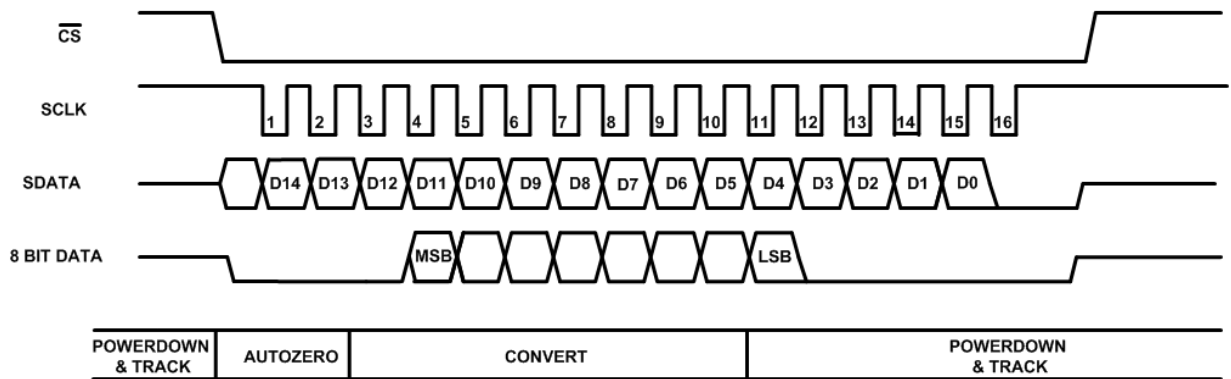


FIGURE 34. ISL26708 SYSTEM TIMING

SHORT CYCLING

In cases where a lower resolution conversion is acceptable, \overline{CS} can be pulled high before all SCLK falling edges have elapsed. This is referred to as short cycling, and it can be used to further optimize power consumption. In this mode a lower resolution result will be output, but the ADC will enter static mode sooner and exhibit a lower average power consumption than if the complete conversion cycle were carried out. The minimum acquisition time (t_{ACQ}) requirement of 200ns must be met for the next conversion to be valid.

POWER-ON RESET

When power is first applied, the ISL26712/10/08 performs a power-on reset that requires approximately 2.5ms to execute. After this is complete, a single dummy conversion must be executed (by taking \overline{CS} low) in order to initialize the switched capacitor track and hold. The dummy conversion cycle will take 1 μ s with an 18MHz SCLK. Once the dummy cycle is complete, the ADC mode will be determined by the state of \overline{CS} . Regular conversions can be started immediately after this dummy cycle is completed and time has been allowed for proper acquisition.

ACQUISITION TIME

To achieve the maximum sample rate (1 MSps) in the ISL26712 device, the maximum acquisition time is 200ns. For slower conversion rates, or for conversions performed using a slower SCLK value than 18MHz, the minimum acquisition time is 200ns. This same minimum applies to the ISL26710 and ISL26708. This minimum acquisition time applies to all the devices if short cycling is utilized.

POWER vs THROUGHPUT RATE

The ISL26712/10/08 provide reduced power consumption at lower conversion rates by automatically switching into a low-power mode after completing a conversion. The average power consumption of the ADC decreases at lower throughput rates. Figure 35 shows the typical power consumption over a wide range of throughput rates.

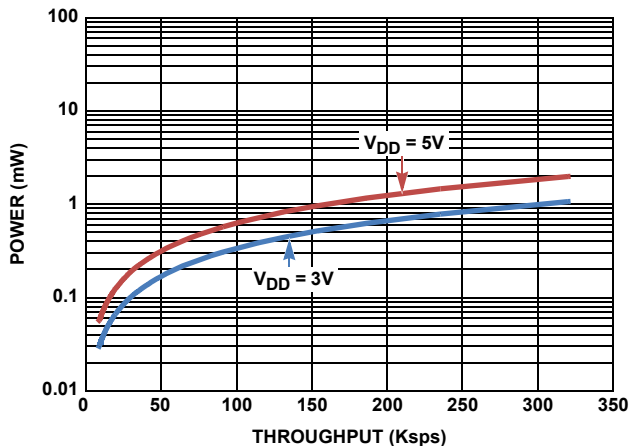


FIGURE 35. POWER CONSUMPTION vs THROUGHPUT RATE

Serial Digital Interface

Conversion data is accessed with an SPI-compatible serial interface. The interface consists of the serial clock (SCLK), serial data output (SDATA), and chip select (\overline{CS}).

The serial interface is designed around using 16 SCLK cycles to perform an autozero on the SAR comparator and additional SCLK cycles for SAR comparator decisions (12 SCLKs in the 12-bit device, 10 SCLKs in the 10-bit device, and 8 SCLKs in the 8-bit device). If short cycling is not used, all converter throughput cycles take 16 SCLKs. The SDATA output goes low after the last conversion decision has been presented to the SDATA output, as shown in Figures 32, 33, and 34.

Data Format

Output data is encoded in two's complement format as shown in Table 1. The voltage levels in the table are idealized and don't account for any gain/offset errors or noise.

TABLE 1. OUTPUT CODES - DIFFERENTIAL

Input Voltage	Two's Complement (12-bit)
>(VFS-1.5 LSB)	7FF
VFS-1.5 LSB	7FF ... 7FE
-0.5 LSB	000 ... FFF
-VFS +0.5 LSB	801 ... 800

NOTE: VFS in the table above equals the voltage between AIN+ and AIN-. Differential full scale is equal to 2* VREF.

Terminology

Signal-to-(Noise + Distortion) Ratio (SINAD)

This is the measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_s/2$), excluding DC. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

Equation 1:

$$\text{Signal-to-(Noise + Distortion)} = (6.02 N + 1.76) \text{dB} \quad (\text{EQ. 1})$$

Thus, for a 12-bit converter this is 74dB, and for a 10-bit this is 62dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the ISL26712/10/08, it is defined as Equation 2:

$$\text{THD(dB)} = 20 \log \sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}{V_1^2}} \quad (\text{EQ. 2})$$

where V_1 is the rms amplitude of the fundamental and $V_2, V_3, V_4, V_5,$ and V_6 are the rms amplitudes of the second to the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_s/2$ and excluding DC) to the rms value of the

fundamental. Also referred to as Spurious Free Dynamic Range (SFDR). Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_a and f_b , any active device with nonlinearities will create distortion products at sum and difference frequencies of $m f_a \pm n f_b$ where m and $n = 0, 1, 2$ or 3 . Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include $(f_a + f_b)$ and $(f_a - f_b)$, while the third order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$.

The ISL26712/10/08 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves, while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

Aperture Delay

This is the amount of time from the leading edge of the sampling clock until the ADC actually takes the sample.

Aperture Jitter

This is the sample-to-sample variation in the effective point in time at which the actual sample is taken.

Full Power Bandwidth

The full power bandwidth of an ADC is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

Common-Mode Rejection Ratio (CMRR)

The common-mode rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f , to the power of a $250\text{mV}_{\text{P-P}}$ sine wave applied to the common-mode voltage of $\text{AIN}+$ and $\text{AIN}-$ of frequency f_s shown in Equation 3:

$$\text{CMRR}(\text{dB}) = 10\log(\text{Pfl}/\text{Pfs}) \quad (\text{EQ. 3})$$

Pfl is the power at frequency f in the ADC output; Pfs is the power at frequency f_s in the ADC output.

Integral Nonlinearity (INL)

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero-Code Error

This is the deviation of the midscale code transition (111...111 to 000...000) from the ideal $\text{AIN}+ - \text{AIN}-$ (i.e., 0 LSB).

Positive Gain Error

This is the deviation of the last code transition (011...110 to 011...111) from the ideal $\text{AIN}+ - \text{AIN}-$ (i.e., $+\text{REF} - 1$ LSB), after the zero code error has been adjusted out.

Negative Gain Error

This is the deviation of the first code transition (100...000 to 100...001) from the ideal $\text{AIN}+ - \text{AIN}-$ (i.e., $-\text{REF} + 1$ LSB), after the zero code error has been adjusted out.

Track and Hold Acquisition Time

The track and hold acquisition time is the minimum time required for the track and hold amplifier to remain in track mode for its output to reach and settle to within 0.5 LSB of the applied input signal.

Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency, f , to ADC VDD supply of frequency f_s . The frequency of this input varies from 1kHz to 1MHz as shown by Equation 4.

$$\text{PSRR}(\text{dB}) = 10\log(\text{Pf}/\text{Pfs}) \quad (\text{EQ. 4})$$

Pf is the power at frequency f in the ADC output; Pfs is the power at frequency f_s in the ADC output.

Application Hints

Grounding and Layout

The printed circuit board that houses the ISL26712/10/08 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. A minimum etch technique is generally best for ground planes since it gives the best shielding. Digital and analog ground planes should be joined in only one place, and the connection should be a star ground point established as close to the GND pin on the ISL26712/10/08 as possible. Avoid running digital lines under the device, as this will couple noise onto the die. The analog ground plane should be allowed to run under the ISL26712/10/08 to avoid noise coupling.

The power supply lines to the device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed-through the board. A microstrip technique is by far the best but is not always possible with a double-sided board.

In this technique, the component side of the board is dedicated to ground planes, while signals are placed on the solder side.

Good decoupling is also important. All analog supplies should be decoupled with μF tantalum capacitors in parallel with $0.1\mu\text{F}$ capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 14, 2012	FN7999.0	Initial Release.
May 30, 2012	FN7999.1	Page 3, Ordering Information: removed "Coming Soon" from all SOT 23 parts.
June 20, 2012	FN7999.2	Updated Figure 25, "IDEAL TRANSFER CHARACTERISTICS," on page 13. Updated Table 1 on page 17.
August 22, 2012	FN7999.3	Bolded applicable MIN MAX specs in "Electrical Specifications" and "Timing Specifications" tables.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL26712, ISL26710, ISL26708](http://www.intersil.com/products)

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: <http://rel.intersil.com/reports/search.php>

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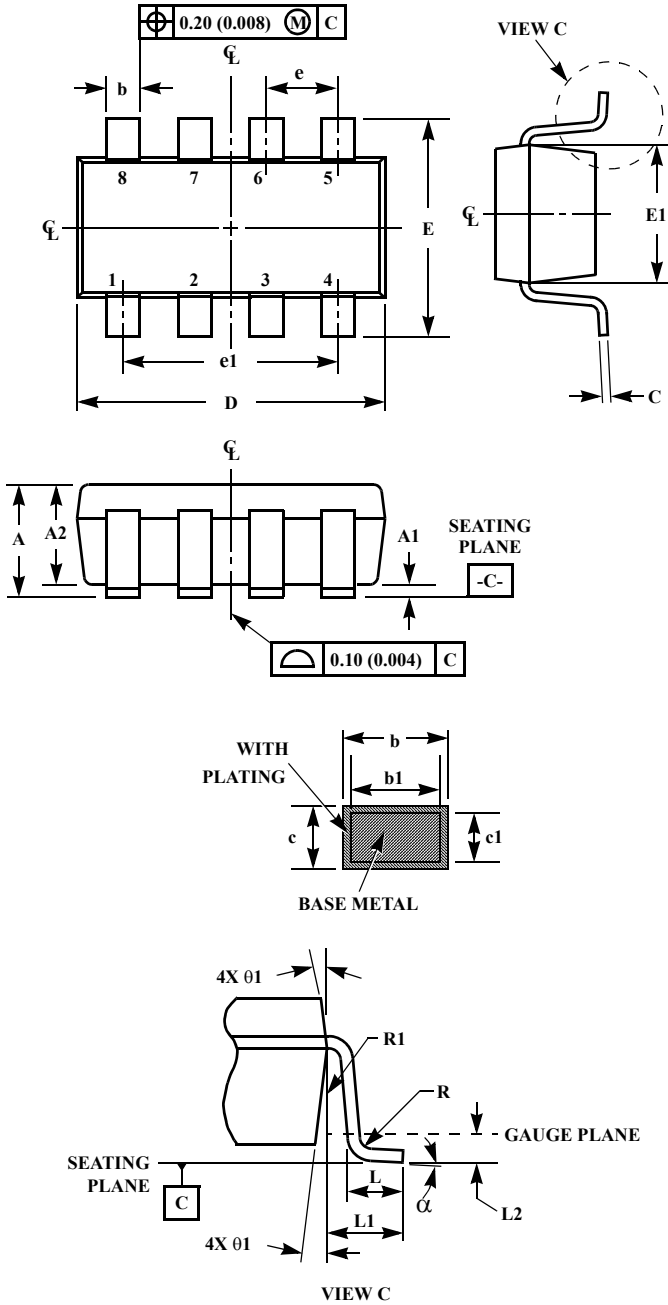
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Small Outline Transistor Plastic Packages (SOT23-8)

P8.064

8 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.036	0.057	0.90	1.45	-
A1	0.000	0.0059	0.00	0.15	-
A2	0.036	0.051	0.90	1.30	-
b	0.009	0.015	0.22	0.38	-
b1	0.009	0.013	0.22	0.33	-
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.008	0.08	0.20	6
D	0.111	0.118	2.80	3.00	3
E	0.103	0.118	2.60	3.00	-
E1	0.060	0.067	1.50	1.70	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0768 Ref		1.95 Ref		-
L	0.014	0.022	0.35	0.55	4
L1	0.024 Ref.		0.60 Ref.		-
L2	0.010 Ref.		0.25 Ref.		-
N	8		8		5
R	0.004	-	0.10	-	-
R1	0.004	0.010	0.10	0.25	-
α	0°	8°	0°	8°	-

Rev. 2 9/03

NOTES:

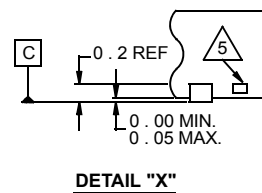
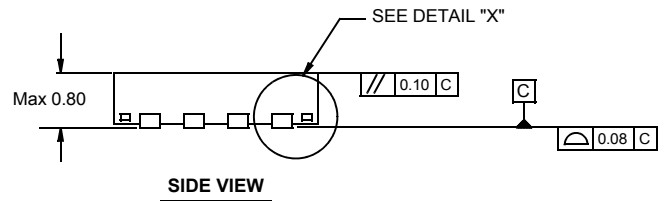
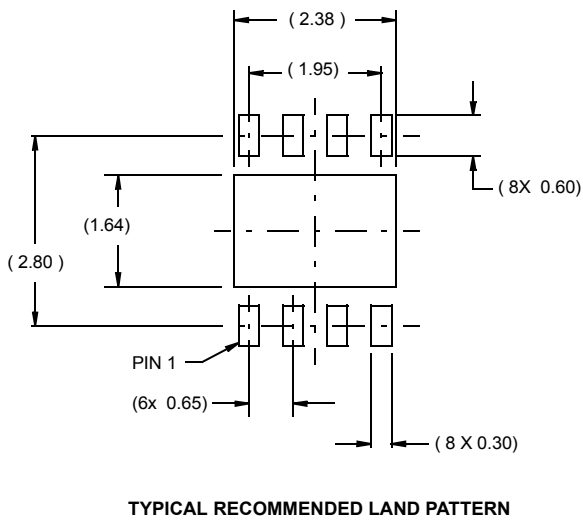
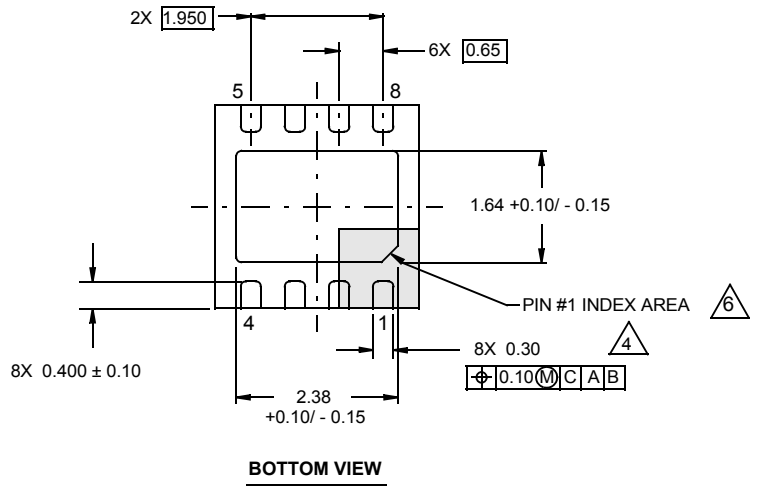
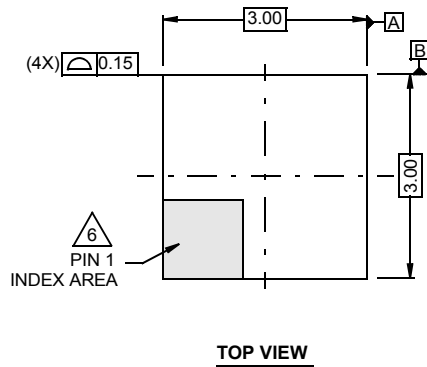
1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC M0178BA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. "N" is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

Package Outline Drawing

L8.3x3I

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

Rev 1 6/09



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.