ISL29124

Digital Red, Green and Blue Color Light Sensor with IR Blocking Filter

FN8454
Rev 2.00
January 13, 2015

The ISL29124 is a low power, high sensitivity, Red, Green, and Blue color light sensor (RGB) with an I^2C (SMBus compatible) interface. Its state-of-the-art photodiode array provides an accurate RGB spectral response and excellent light source to light source variation (LS2LS). The ISL29124 is designed to reject IR in light sources allowing the device to operate in environments from sunlight to dark rooms. The integrating ADC rejects 50Hz and 60Hz flicker caused by artificial light sources. A selectable range allows the user to optimize sensitivity suitable for the specific application. In normal operation mode the device consumes 56µA, which reduces to 0.5µA in power-down mode. The device operates on supplies (VDD) from 2.25V to 3.63V, I^2C supply from 1.7V to 3.63V, and operating temperature over the -40°C to +85°C ambient temperature range.

Features

- 56µA operating current, 0.5µA shutdown current
- Selectable range (via I^2C)
- I^2C (SMBus compatible) output
- ADC resolution 16 bits
- Two optical sensitivity ranges
  - Range 0 = 5.7 mlux to 375 lux
  - Range 1 = 0.152 lux to 10,000 lux
- Operating power supply 2.25V to 3.63V
- I^2C power supply 1.7V to 3.63V
- 4 Ld Optical COB (2.00x1.25mm) package

Applications

- Smart phone, PDA, GPS, tablet PCs, LCD-TVs, digital picture frames, digital cameras
- Dynamic display color balancing
- Printer color enhancement
- Industrial/commercial LED lighting color management
- Ambient light color detection/correction
- OLED display aging compensation

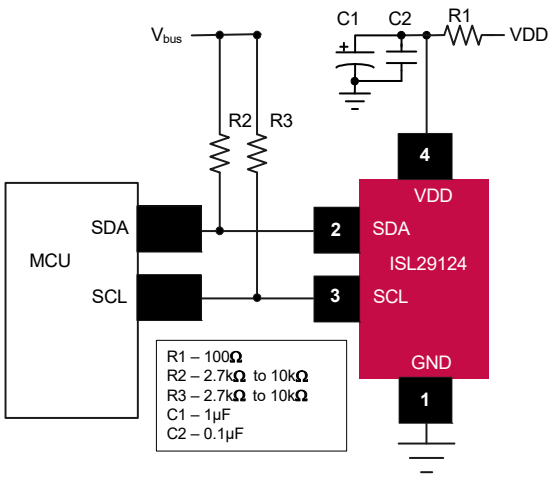


FIGURE 1. TYPICAL APPLICATION DIAGRAM

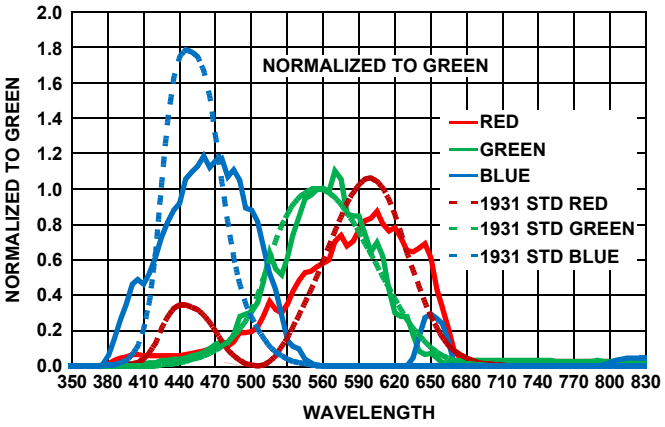
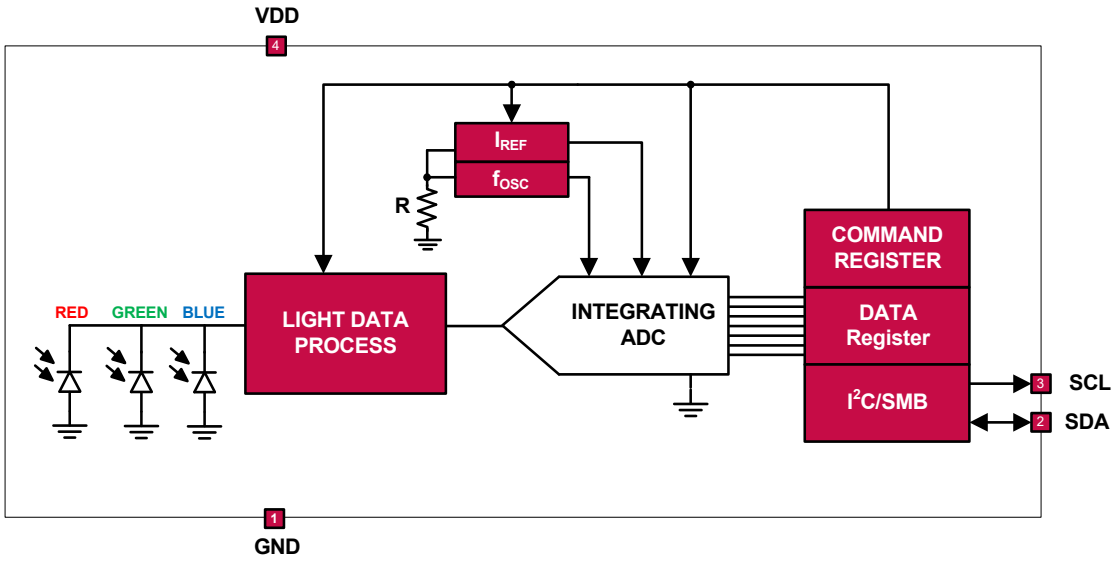


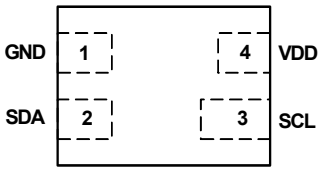
FIGURE 2. NORMALIZED SPECTRAL RESPONSE FOR RED, GREEN, AND BLUE SENSING

Block Diagram



Pin Configuration

ISL29124
(4 LD COB)
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	GND	Ground pin
2	SDA	I^2C serial data
3	SCL	I^2C serial clock
4	VDD	Power supply

Ordering Information

PART NUMBER (Notes 1, 2, 3)	TEMP RANGE (°C)	PACKAGE TAPE & REEL (Pb-free)	PKG. DWG. #
ISL29124IROZ-T7	-40 to +85	4 Ld COB	L4.2.00x1.25
ISL29124IROZ-EVALZ	Evaluation Board		

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For more information on MSL please see tech brief TB477.

Absolute Maximum Ratings

VDD to GND ..... +4.0V
I^2C Bus (SCL, SDA) Pin Voltage (Note 5) ..... -0.2V to 4.0V
I^2C Bus (SCL, SDA) Pin Current (Note 5) ..... <10mA
Input Voltage Slew Rate (Max) 0.1V/µs
ESD Ratings
Human Body Model (Tested per JESD22-A114E) 1500V

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W)
4 Ld COB Package (Note 4) 305
Maximum Junction Temperature (TJ_{MAX}) ..... +90°C
Storage Temperature Range ..... -40°C to +100°C
Operating Temperature ..... -40°C to +85°C
Pb-Free Reflow Profile (*) ..... see TB477
*Peak temperature during solder reflow +235°C max

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board. See Tech Brief TB379.
5. SDA current sinking capability are guaranteed by design.

Electrical Specifications

V_{DD} = 3.0V, T_A = +25°C, 16-bit ADC operation, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{DD}	Power Supply Range		2.25		3.63	V
I_{DD}	Supply Current			56	85	µA
I_{DD1}	Supply Current When Standby	Software disabled		29	37	µA
I_{DD2}	Supply Current When Powered Down	Software disabled		0.5	1.45	µA
V_{I2C}	Supply Voltage Range for I^2C Interface		1.7		3.63	V
t_{INT}	ADC Integration/Conversion Time	16-bit ADC data		101		ms
f_{I2C}	I^2C Clock Rate Range			500		kHz
D_{Dark}	Count Output When Dark	Lux = 0 lux, Range = 0 (375 lux)		1	5	Counts
CCT	Corrected Color Temperature Accuracy	Illuminant A is at 300 lux (See Note 11 and "References" on page 15 about CIE 1931, Planckian locus and standard illuminants)		±5		%
D_{FS}	Full Scale ADC Code	ADC 16 bits			65535	Counts
	Fullscale on Range 0 (Note 7)	Green = 565nm		18		$\mu W/cm^2$
		Red = 620nm		20		$\mu W/cm^2$
		Blue = 485nm		30		$\mu W/cm^2$

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
7. 565nm Green, 620nm Red LED, 485nm Blue in white LED is used in production test.

I^2C Interface Specifications V_{DD} = 3.0V, T_A = +25°C, 16-bit ADC operation, unless otherwise specified.

SYMBOL	PARAMETER (Note 9)	CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
V_{IL}	SDA and SCL Input Buffer LOW Voltage				0.55	V
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		1.25			V
V_{Hys} (Note 8)	SDA and SCL Input Buffer Hysteresis			0.05xVDD		V
V_{OL} (Note 8)	SDA Output Buffer LOW Voltage (open-drain), Sinking 4mA		0		0.4	V
C_{PIN} (Note 8)	SDA and SCL Pin Capacitance	T_A = +25°C, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V			10	pF
f_{SCL}	SCL Frequency				500	kHz
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid				900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission		1300			ns
t_{LOW}	SCL LOW Time		1300			ns
t_{HIGH}	SCL HIGH Time		600			ns
$t_{SU:STA}$	START Condition Setup Time		600			ns
$t_{HD:STA}$	START Condition Hold Time		600			ns
$t_{SU:DAT}$	Input Data Setup Time		100			ns
$t_{HD:DAT}$	Input Data Hold Time		30			ns
$t_{SU:STO}$	STOP Condition Setup Time		600			ns
$t_{HD:STHD:ST}$	STOP Condition Hold Time		600			ns
$t_{HD:ST}$	Output Data Hold Time		0			ns
$t_{HD:ST}$ (Note 8)	SDA and SCL Rise Time		20+0.1xCb			ns
$t_{HD:ST}$ (Note 8)	SDA and SCL Fall Time		20+0.1xCb			ns
Cb (Note 8)	Capacitive Loading of SDA or SCL	Total on-chip and off-chip			400	pF
R_{PU} (Note 8)	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For C_b = 400pF, max is about 2kΩ ~ 2.5kΩ. For C_b = 40pF, max is about 15kΩ ~ 20kΩ (Note 10)	1			kΩ

NOTES:

8. Limits should be considered typical and are not production tested.
9. These are I^2C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.
10. C_b is the capacitance of the bus in pF.

SDA vs SCL Timing

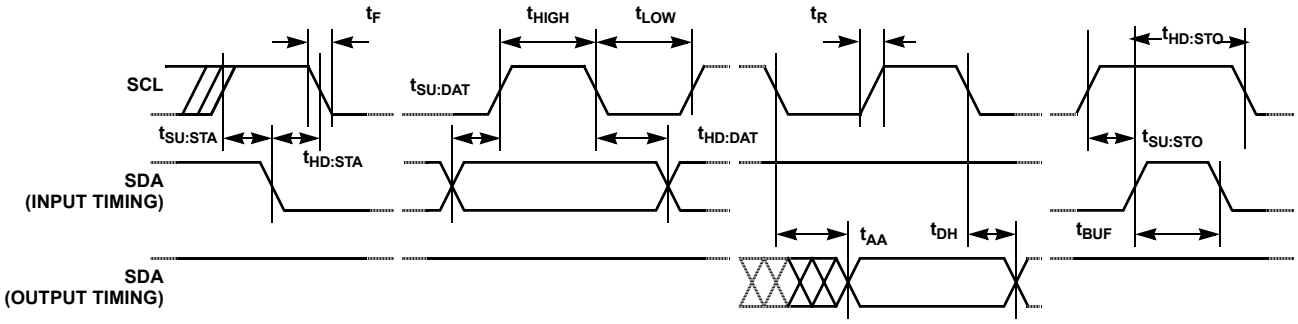


FIGURE 3. I^2C BUS TIMING

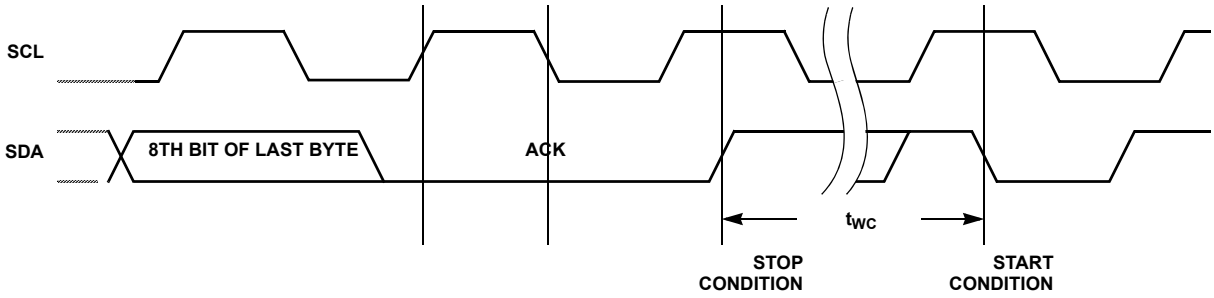


FIGURE 4. I^2C WRITE CYCLE TIMING

Typical Performance Curves

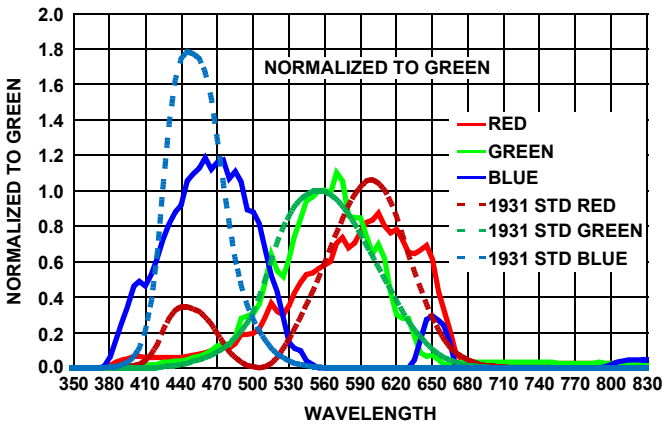


FIGURE 5. NORMALIZED SPECTRAL RESPONSE FOR AMBIENT LIGHT SENSING

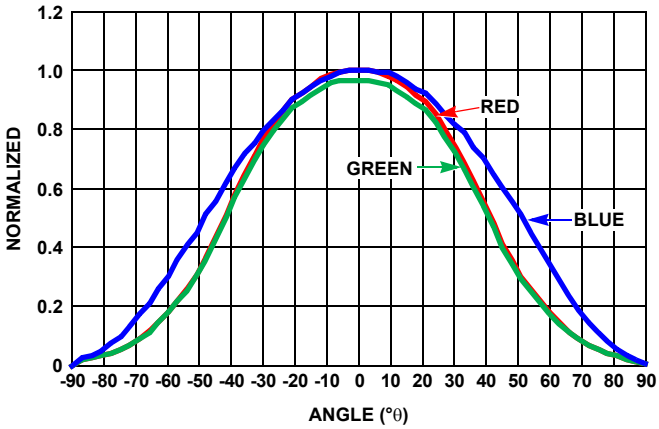


FIGURE 6. RADIATION PATTERN

Principles of Operation

Photodiodes and ADC

The ISL29124 contains three photodiode arrays, which convert light into current. The spectral response for RED, GREEN, and BLUE color ambient intensity sensing is as shown in Figure 2. After light is converted to current during the light to signal process, the current output is converted to a digital count by an on-chip Analog-to-Digital Converter (ADC). The ADC converter resolution is selectable from 12 or 16 bits. The ADC conversion time is inversely proportional to the ADC resolution.

The ADC converter uses an integrating architecture. This conversion method is ideal for converting small signals in the presence of a periodic noise. A 100ms integration time (16-bit mode) for instance, rejects 50Hz and 60Hz power line as well as fluorescent flicker noise.

The ADC integration time is determined by an internal oscillator and the n-bit (n = 12, 16) counter inside the ADC. A good balancing act of integration time and resolution depends on the application for optimum system performance.

The ADC provides two programmable ranges to dynamically accommodate different lighting conditions. For dim conditions, the ADC can be configured at its high sensitivity (low optical) range. For bright conditions, the ADC can be configured at its low sensitivity (higher optical) range. Note that the effective optical sensitivity of the ISL29124 in terms of counts/µW/cm^2 is directly proportional to the ADC integration time.

Power-On Reset

The Power-On Reset (POR) circuitry protects the internal logic against powering up in the incorrect state. The ISL29124 will power-up into Standby mode after VDD exceeds the POR trigger level and will power-down into Reset mode when VDD drops below the POR trigger level. This bidirectional POR feature protects the device against ‘brownout’ failure following a temporary loss of power.

The POR is an important feature because it prevents the ISL29124 from starting to operate with insufficient power supply voltage. The ISL29124 prevents communication to its registers and reduces the likelihood of data corruption on power-up.

Serial Interface

The ISL29124 supports the Inter-Integrated Circuit (I^{2}C) bus data transmission protocol. The I^{2}C bus is a two-wire serial bidirectional interface consisting of SCL (clock) and SDA (data). Both the wires are connected to the device supply via pull-up resistors. The I^{2}C protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The transmitting device pulls down the SDA line to transmit a “0” and releases it to transmit a “1”. The master always initiates the data transfer, only when the bus is not busy, and provides the clock for both transmit and receive operations. The ISL29124 operates as a slave device in all applications. The serial communication over the I^{2}C interface is conducted by sending the most significant bit (MSB) of each byte of data first.

Start Condition

During data transfer, the SDA line must remain stable while the SCL line is HIGH. All I^{2}C interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH (refer to Figure 9). The ISL29124 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (refer to Figure 9). A START condition is ignored during the power-up sequence.

Stop Condition

All I^{2}C interface operations must be terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA while SCL is HIGH (refer to Figure 9). A STOP condition at the end of a read/write operation places the device in its standby mode. If a stop is issued in the middle of a Data byte, or before 1 full Data byte and ACK is sent, then the serial communication of ISL29124 resets itself without performing the Read/Write. The contents of the register array are not affected.

Acknowledge

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device releases the SDA bus after transmitting 8-bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (refer to Figure 9). The ISL29124 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again, after successful receipt of an Address Byte. The ISL29124 also responds with an ACK after receiving a Data byte of a write operation. The master must respond with an ACK after receiving a Data byte of a read operation.

Device Addressing

Following a START condition, the master must output a Device Address byte. The 7 MSBs of the Device Address byte are known as the device identifier. The device identifier bits of ISL29124 are internally hard-wired as “1000100”. The LSB of the Device Address byte is defined as read or write (R/$\overline{W}$) bit. When this R/$\overline{W}$ bit is a “1”, a read operation is selected and when “0”, a write operation is selected (refer to Figure 7). The master generates a START condition followed by Device Address byte 1000100x (x as R/$\overline{W}$) and the ISL29124 compares it with the internal device identifier. Upon a correct comparison, the device outputs an acknowledge (LOW) on the SDA line (refer to Figure 9).

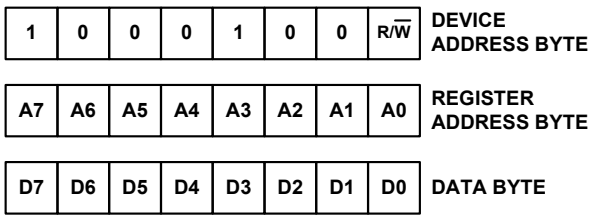


FIGURE 7. DEVICE ADDRESS, REGISTER ADDRESS, AND DATA BYTE

Write Operation

BYTE WRITE

In a byte write operation, the ISL29124 requires the Device Address byte, Register Address byte, and the Data byte. The master starts the communication with a START condition. Upon receipt of the Device Address byte, Register Address byte, and the Data byte, the ISL29124 responds with an acknowledge (ACK). Following the ISL29124 data acknowledge response, the master terminates the transfer by generating a STOP condition. The ISL29124 then begins an internal write cycle of the data to the volatile memory. During the internal write cycle, the device inputs are disabled and the SDA line is in a high impedance state, so the device will not respond to any requests from the master (refer to Figure 8).

BURST WRITE

The ISL29124 has a burst write operation, which allows the master to write multiple consecutive bytes from a specific address location. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first Data byte is transferred, the master can write to the whole register array. After the receipt of each byte, the ISL29124 responds with an acknowledge, and the address is internally incremented by one. The address pointer remains at the last address byte written. When the counter reaches the end of the register address list, it “rolls over” and goes back to the first Register Address.

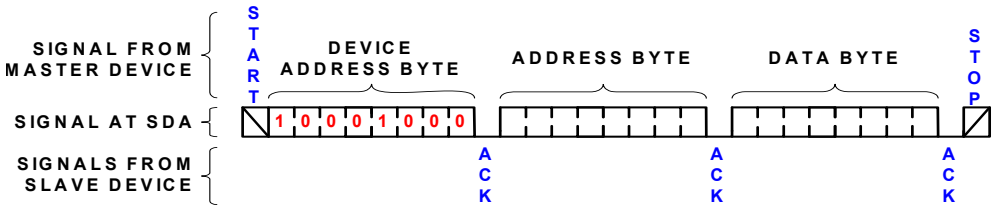


FIGURE 8. BYTE WRITE SEQUENCE

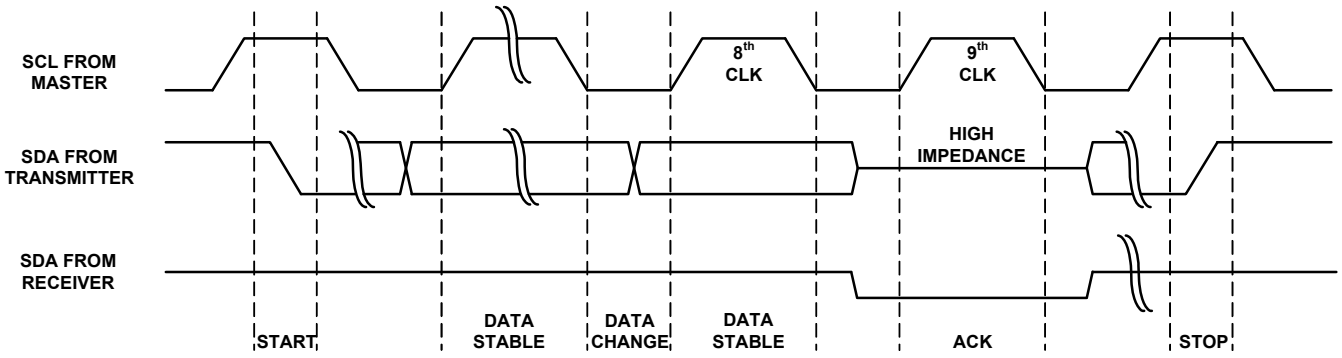


FIGURE 9. START, DATA STABLE, ACKNOWLEDGE, AND STOP CONDITION

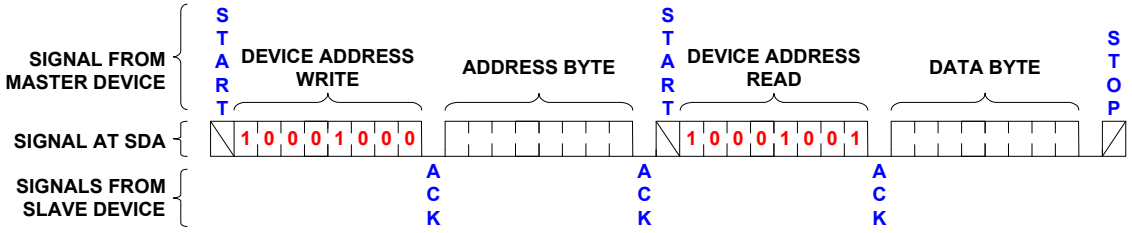


FIGURE 10. BYTE ADDRESS READ SEQUENCE

Read Operation

ISL29124 has two basic read operations: Byte Read and Burst Read.

BYTE READ

Byte read operations allows the master to access any register location in the ISL29124. The Byte read operation is a two step process. The master issues the START condition and the Device Address byte with the R/$\overline{W}$ bit set to “0”, receives an acknowledge, then issues the Register Address byte. After acknowledging receipt of the register address byte, the master immediately issues another START condition and the Device Address byte with the R/$\overline{W}$ bit set to “1”. This is followed by an acknowledge from the device and then by the 8-bit data word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 10.

BURST READ

Burst read operation is identical to the Byte Read operation. After the first Data byte is transmitted, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge but issuing a STOP condition (refer to Figure 11).

For more information about the I^{2}C standard, please consult the Phillips™ I^{2}C specification documents.

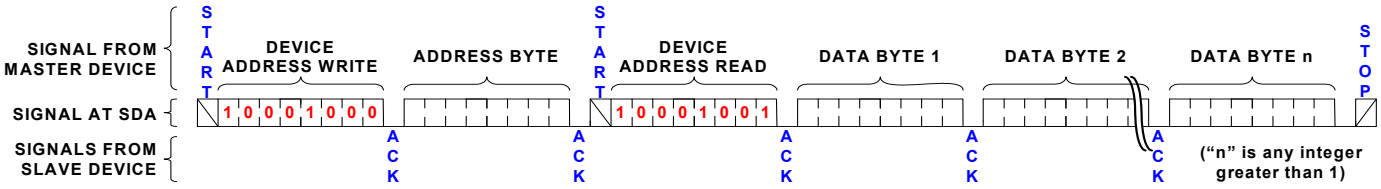


FIGURE 11. BURST READ SEQUENCE

TABLE 1. REGISTER MAP

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
Device ID	0	0x00	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	0x7D	RO
Device Reset			ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	NA	WO
Configuration - 1	1	0x01	RESERVED			BITS	RNG	MODE[2]	MODE[1]	MODE[0]	0x00	RW
Configuration - 2	2	0x02	IRCOM	RESERVED	ALSCC[5]	ALSCC[4]	ALSCC[3]	ALSCC[2]	ALSCC[1]	ALSCC[0]	0x00	RW
Reserved Register	3	0x03	RESERVED								0x00	RW
Reserved Register	4	0x04	RESERVED								0x00	RW
Reserved Register	5	0x05	RESERVED								0x00	RW
Reserved Register	6	0x06	RESERVED								0xFF	RW
Reserved Register	7	0x07	RESERVED								0xFF	RW
Status Flags	8	0x08	RESERVED		GRBCF[1]	GRBCF[0]	RESERVED	BOUTF	CONVENF	RESERVED	0x04	RO
Green Data - Low Byte	9	0x09	GREEN[7]	GREEN[6]	GREEN[5]	GREEN[4]	GREEN[3]	GREEN[2]	GREEN[1]	GREEN[0]	0x00	RW
Green Data - High Byte	10	0x0A	GREEN[15]	GREEN[14]	GREEN[13]	GREEN[12]	GREEN[11]	GREEN[10]	GREEN[9]	GREEN[8]	0x00	RW
Red Data - Low Byte	11	0x0B	RED[7]	RED[6]	RED[5]	RED[4]	RED[3]	RED[2]	RED[1]	RED[0]	0x00	RW
Red Data - High Byte	12	0x0C	RED[15]	RED[14]	RED[13]	RED[12]	RED[11]	RED[10]	RED[9]	RED[8]	0x00	RW
Blue Data - Low Byte	13	0x0D	BLUE[7]	BLUE[6]	BLUE[5]	BLUE[4]	BLUE[3]	BLUE[2]	BLUE[1]	BLUE[0]	0x00	RW
Blue Data - High Byte	14	0x0E	BLUE[15]	BLUE[14]	BLUE[13]	BLUE[12]	BLUE[11]	BLUE[10]	BLUE[9]	BLUE[8]	0x00	RW

Register Description

Following are detailed descriptions of the control registers related to the operation of the ISL29124 ambient light sensor device. These registers are accessed by the I^2C serial interface. For details on the I^2C interface, refer to “Serial Interface” on page 6.

All the features of the device are controlled by the registers. The ADC data can also be read. The following sections explain the details of each register bit. All RESERVED bits are Intersil used bits ONLY. The value of the reserved bit can change without any notice.

Device Register (Address: 0x00)

TABLE 2. DEVICE ID REGISTER ADDRESS

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
Device ID	0	0x00	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	0x7D	RO
Device Reset			ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	NA	WO

Register 0x00 performs two functions. If Reg 0x00 is in READ ONLY mode then it will be a Device ID. By default, the device ID is 0x7D in hex. Write 46h to register 0x00 in the WRITE ONLY, the device will reset all registers to their default states.

Configuration-1 Register (Address: 0x01)

TABLE 3. CONFIGURATION-1

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
Configuration-1	1	0x01	RESERVED BITS			BITS	RNG	MODE[2]	MODE[1]	MODE[0]	0x00	RW

RGB Operating Modes [B2:B0]

This device has various RGB operating modes. These modes are selected by setting B2:B0 bits in Table 4. The device powers up on a disable mode. All operating modes are in continuous ADC conversion. The following bits are used to enable the operating mode.

TABLE 4. OPERATION MODES

B2:B0	OPERATION
000	Power Down (ADC conversion)
001	GREEN Only
010	RED Only
011	BLUE Only
100	Stand by (No ADC conversion)
101	GREEN/RED/BLUE
110	GREEN/RED
111	GREEN/BLUE

RGB Data Sensing Range [B3]

The Full Scale RGB Range has two selectable ranges at bit 3. Each range has a maximum allowable lux value. B3 = 0 has the highest sensitivity at 16 bits resolution.

TABLE 5. SENSING RANGES

B3	RANGE
0	375 lux
1	10,000 lux

ADC Resolution [B4]

ADC's resolution and the number of clock cycles per conversion is determined by this bit in Table 6. Changing the resolution of the ADC, changes the number of clock cycles of the ADC which in turn changes the integration time. Integration time is the period the ADC samples the photodiode current signal for a measurement.

TABLE 6. ADC RESOLUTIONS

B4	RESOLUTION
0	16 bits
1	12 bits

Configuration-2 Register (Address: 0x02)

TABLE 7. CONFIGURATION-2

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
Configuration-2	2	0x02	IR-COM	RESERVED	ALSCC[5]	ALSCC[4]	ALSCC[3]	ALSCC[2]	ALSCC[1]	ALSCC[0]	0x00	RW

ACTIVE INFRARED (IR) COMPENSATION

The device is designed for operation under dark glass cover, which significantly attenuates visible light and pass the infrared light without much attenuation. The device has an on-chip passive optical filter designed to block (reject) most of the incident Infrared. In addition, the device provides a programmable active IR compensation, which allows fine tuning of residual infrared components from the output that allows optimizing the measurement variation between differing IR-content light sources. B7 is “IR Comp Offset” and B[5:0] is “IR Comp Adjust”, which provide a means for adjusting IR compensation. B7 = ‘0’ + B[5:0] is the effective IR compensation from 0 to 63 codes and B7 set to ‘1’ + B[5:0] (the effective IR compensation) is from 106 to 169. Table 8 shows light-weight for each IR compensation bit and Figure 12 is a typical system measure for both IR Comp Adjust and IR Comp Offset. For more details about the IR compensation, see IR compensation in “Applications Information” on page 13.

It is recommended to set BF at register 0x02 to max out the IR compensation value. It makes the High range reach more than 10,000lux.

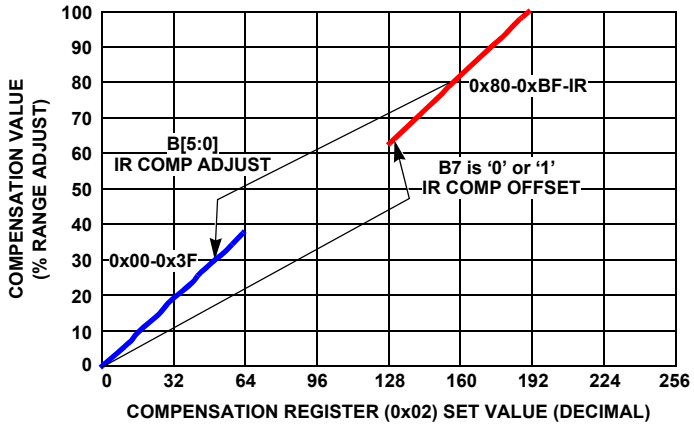


FIGURE 12. IR COMPENSATION SET

TABLE 8.

B7	B6	B5	B4	B3	B2	B1	B0	LIGHT-WEIGHT
IR-COM	RESERVED	ALSCC[5]	ALSCC[4]	ALSCC[3]	ALSCC[2]	ALSCC[1]	ALSCC[0]	
106		32	16	8	4	2	1	Codes

NOTES:

11. An illuminant is intended to represent typical, domestic, tungsten-filament lighting. Its CCT is about 2856K.
12. D series of illuminants are constructed to represent natural daylight. D65 is used in lab to represent as noon light to test. Its CCT is 6504K.
13. F series of illuminants represent various types of fluorescent lighting. F2 is cool white fluorescent using in lab to test. Its CCT is 4230K.

Status Flag Register (Address: 0x08)

TABLE 9. STATUS FLAG REGISTER

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
Status Flag	8	0x08	RESERVED	RESERVED	RGBCF[1]	RGBCF[0]	RESERVED	BOUTF	CONVENF	RESERVED	0x04	RO

CONVENF [B1]

This is the status bit of conversion. The bit is set to logic high when the conversion has been completed, and set to logic low when the conversion has not been completed (see Table 10).

TABLE 10. CONVERSION FLAG

B1	OPERATION
0	Still Convert or Cleared
1	Conversion Completed

BOUTF [B2]

Bit2 on register address 0x08 is a status bit for brownout condition (BOUT). The default value of this bit is HIGH, BOUT = 1, during the initial power-up. This indicates the device may have possibly gone through a brownout condition. Therefore, the status bit should be reset to LOW (BOUT = 0) by an I^2C write command during the initial configuration of the device. The default register value is 0x04 at power-on (see Table 11).

TABLE 11. BROWNOUT FLAG

B2	OPERATION
0	No Brownout
1	Power-down or Brownout occurred

RGBCF [B5:B4]

B[5:4] are flag bits which display that either Red or Green or Blue is under a conversion process (see Table 12).

TABLE 12. CONVERSION FLAG

B5:4	RGB UNDER CONVERSION
00	No Operation
01	GREEN
10	RED
11	BLUE

ISL29124 Data Register (Address: 0x09, 0x0A, 0xB, 0xC, 0xD and 0xE)

TABLE 13. CONFIGURATION-3

NAME	REGISTER ADDRESS		REGISTER BITS								DEFAULT	ACCESS
	DEC	HEX	B7	B6	B5	B4	B3	B2	B1	B0		
Green Data - Low Byte	9	0x09	GREEN[7]	GREEN[6]	GREEN[5]	GREEN[4]	GREEN[3]	GREEN[2]	GREEN[1]	GREEN[0]	0x00	RW
Green Data - High Byte	10	0x0A	GREEN[15]	GREEN[14]	GREEN[13]	GREEN[12]	GREEN[11]	GREEN[10]	GREEN[9]	GREEN[8]	0x00	RW
Red Data - Low Byte	11	0x0B	RED[7]	RED[6]	RED[5]	RED[4]	RED[3]	RED[2]	RED[1]	RED[0]	0x00	RW
Red Data - High Byte	12	0x0C	RED[15]	RED[14]	RED[13]	RED[12]	RED[11]	RED[10]	RED[9]	RED[8]	0x00	RW
Blue Data - Low Byte	13	0x0D	BLUE[7]	BLUE[6]	BLUE[5]	BLUE[4]	BLUE[3]	BLUE[2]	BLUE[1]	BLUE[0]	0x00	RW
Blue Data - High Byte	14	0x0E	BLUE[15]	BLUE[14]	BLUE[13]	BLUE[12]	BLUE[11]	BLUE[10]	BLUE[9]	BLUE[8]	0x00	RW

The ISL29124 has two 8-bit read-only registers to hold the higher and lower byte of the ADC value. The lower byte and higher bytes are accessed at address respectively. For 16-bit resolution, the data is from D0 to D15; for 12-bit resolution, the data is from D0 to D11. The registers are refreshed after every conversion cycle. The default register value is 0x00 at power-on. Because all of the registers are double buffered, the data is always valid on the data registers.

Applications Information

Figure 13 shows a plot of the 1931 standard normalized spectral response of various types of light sources for reference.

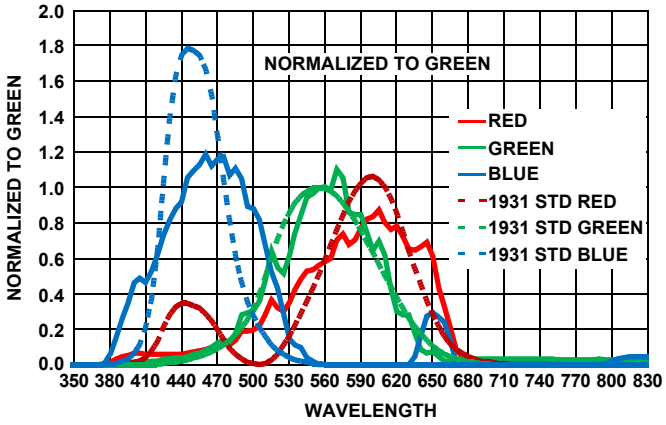


FIGURE 13. 1931 STANDARD NORMALIZED SPECTRAL RESPONSE OF LIGHT SOURCES

System Compensation and RGB to XYZ Transform (Chroma Meter)

The accuracy of the RGB sensor is extremely sensitive to the opto-mechanical design of the system in which it resides. The compensation setting and calculation of RGB to XYZ transform should be characterized within that environment with as many standard illuminants as possible. A minimal recommended set would include A, F2 and D65 illuminants (see Notes 11, 12, 13 on page 11 and “References” on page 15 about IEC 1931, Planckian locus and standard illuminants). The two most important opto-mechnical features are FOV (field of view FWHM) and optical filters as example of tinted cell phone glass through which the sensor will detect the ambient lighting. With the combination of the FOV and a large sample for the filter (30x30mm) it is possible to determine the best compensation and XYZ transform coefficients. It is also possible to project the accuracy of the measurement system.

RGB → XYZ TRANSFORM

Once the proper compensation setting is determined, measure the RGB values of the various illuminants at this value. Calculate the RGB to XYZ transform coefficients based on the measured result against appropriate Chroma Meter Standard (using x and y values).

$$\begin{bmatrix} X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} C_{XR} & C_{XG} & C_{XB} \\ C_{YR} & C_{YG} & C_{YB} \\ C_{ZR} & C_{ZG} & C_{ZB} \end{bmatrix} \times \begin{bmatrix} R \\ G \\ B \end{bmatrix} \quad \text{(EQ. 1)}$$

X, Y, and Z are in the IEC system which specifies the color and brightness of a particular homogeneous visual stimulus.

R, G, and B are digital output from the sensor.

Cs are coefficients. These coefficients will be changed respectively depending on the system setup.

COMPENSATION

The compensation adjustment is used to balance the various illuminants of interest (A, F2 and D65 recommended) such that the value measured at the same power level (measured with a Lux meter) is the closed value. Since the compensation adjustment is piecewise linear, the proper setting can be determined by extrapolating from a pair of measurements and calculating the closest intersection of the sources of interest.

The Configuration register (Reg 0x02[7:0]) allows coarse tuning B7 and fine tuning (B[5:0] of the residual infrared component from the ALS output.

The recommended procedure for determining ALS IR compensation is as follows:

- Illuminate the ISL29124 based design configuration with a no IR F2 light source. Record the ALS measurement and the Lux level.
- Illuminate the device with A, and D65 with heavy IR and the F2 light sources. Take an ALS measurement and Lux level measurement.
- It really depends on the system setup in order to adjust the Configuration register (Reg 0x02, B7 and B[5:0]) to compensate for the IR contribution.
- Repeat previous steps until the IR light source contribution to the ALS measurement is under 10% assuming there is no change in Lux level due to IR light source.

Figure 14 example shows how to calculate the compensation for varying levels of infrared components such as A, F2 and D65 (see Notes 11, 12 and 13). With compensation adjustment from 0% to 100%, the crossing point is the IR compensation value, which makes tighter variation of varying level of infrared components. This setup system is a sensor without IR tinted glass and illuminates with 3 different light sources. Since it is not under IR tinted glass, then reg0x2 setups like b7 = ‘0’ and B[5:0] is at about 25% compensation adjust (%/range), which means about 40 codes.

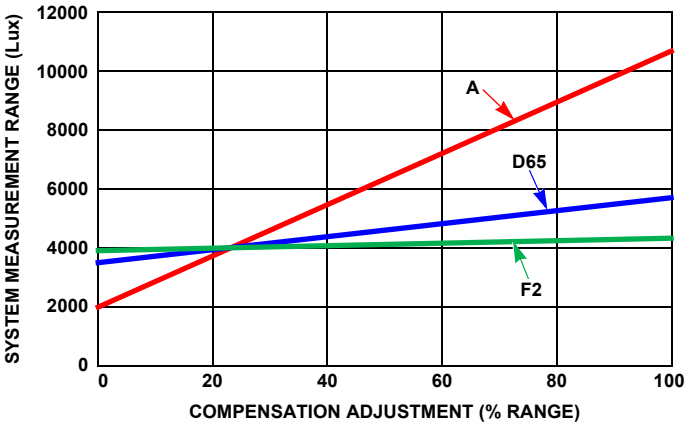


FIGURE 14. IR COMPENSATION VALUE

Calculating Lux

Y-coordinate is Ev measured in lux. The data can be converted to lux by using an equation. There are two different data sensing ranges (375 lux and 10,000 lux) and also two different resolution selections (16 bits and 12 bits) on this device. Equation 2 is dependent on both of these parameters.

$$Ev = Y = (C_{YR} x Red + C_{YG} x Green + C_{YB} x Blue) x Range \quad \text{(EQ. 2)}$$

Noise Rejection

Electrical AC power worldwide is distributed at either 50Hz or 60Hz. Artificial light sources vary in intensity at the AC power frequencies. The undesired interference frequencies are infused on the electrical signals. This variation is one of the main sources of noise for the light sensors. Integrating type ADC's have excellent noise-rejection characteristics for periodic noise sources whose frequency is an integer multiple of the conversion rate. By setting the sensor's integration time to an integer multiple of periodic noise signal, the performance of an ambient light sensor can be improved greatly in the presence of noise. In order to reject the AC noise, the integration time of the sensor must be adjusted to match the AC noise cycle. For instance, a 60Hz AC unwanted signal's sum from 0ms to k*16.66ms ($k = 1,2...k_i$) is zero. Similarly, setting the device's integration time to be an integer multiple of the periodic noise signal greatly improves the light sensor's output signal in the presence of noise.

Digital Inputs and Termination

The ISL29124 digital inputs are guaranteed to CMOS levels. The internal register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the lines driving the clock and the digital inputs are 50Ω lines, then 50Ω termination resistors should be placed as close to the sensor inputs as possible, connected to the digital ground plane (if separate grounds are used).

Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, take the total variation, (V_{HIGH} - V_{LOW}), and divide by the temperature extremes of measurement (T_{HIGH} - T_{LOW}). The result is divided by the nominal reference voltage (at T = +25°C) and multiplied by 10^6 to yield ppm/°C. This is the "Box" method for specifying temperature coefficient.

Layout and Board Mounting Considerations

Suggested PCB Footprint

It is important that users check TB477 "Surface Mount Assembly Guidelines for Optical Chip On Board (COB) Package" before starting COB product board mounting.

Board Mounting

For applications requiring the light measurement, the board mounting location should be reviewed. The device uses an Optical Chip On Board (COB) package, which subjects the die to mild stresses when the printed circuit (PC) board is heated and cooled, which slightly changes the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location.

Layout

The ISL29124 is relatively insensitive to layout. Like other I^2C devices, it is intended to provide excellent performance even in significantly noisy environments. There are only a few considerations that will ensure best performance.

Route the supply and I^2C traces as far as possible from all sources of noise. Use two power-supply decoupling capacitors (1µF and 0.1µF) placed close to the device.

Soldering

Convection heating is recommended for reflow soldering; direct-infrared heating is not recommended. The plastic COB package does not require a custom reflow soldering profile, and is qualified to +260°C. A standard reflow soldering profile with a +260°C maximum is recommended.

Typical Circuit

A typical application for the ISL29124 is shown in Figure 15. The ISL29124's I^2C address is internally hard-wired as 1000100. The device can be tied onto a system's I^2C bus together with other I^2C compliant devices.

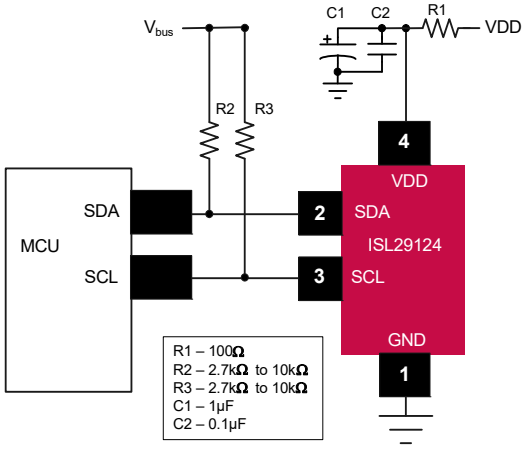


FIGURE 15. ISL29124 TYPICAL CIRCUIT

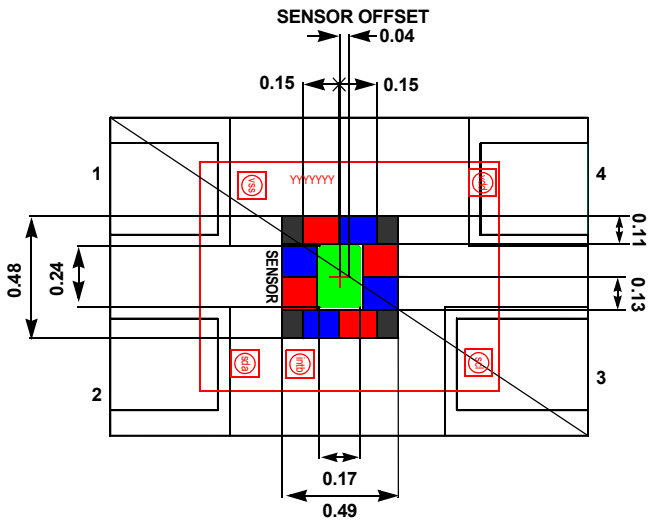


FIGURE 16. 4 LD ODFN SENSOR LOCATION OUTLINE

References

[1] Standard illuminants

[2] Planckian locus approximation

[3] CIE 1931 2°, XYZ CMFs modified by Judd (1951) and Vos (1978)

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
January 13, 2015	FN8454.2	Updated paragraph under “RGB Data Sensing Range [B3]” on page 10.
February 19, 2014	FN8454.1	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

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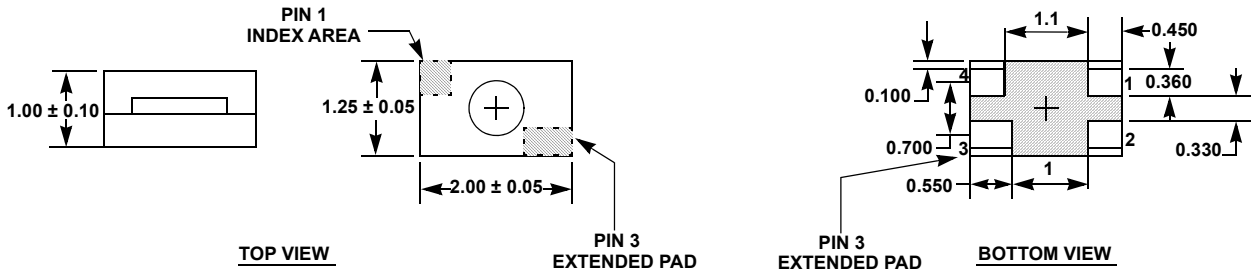
Reliability reports are also available from our website at www.intersil.com/support

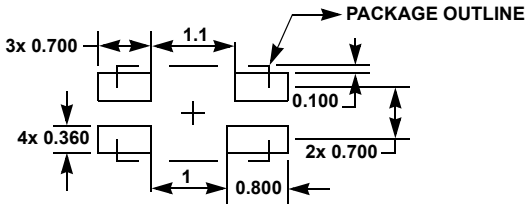
Package Outline Drawing

L4.2.00x1.25

4 LD OPTICAL CHIP ON BOARD PACKAGE (COB)

Rev 3, 2/14





TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Pin 1 is diagonal to extended Pad Pin 3 on bottom surface.